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Enhancement Mode Ga_2O_3 Field Effect Transistor with Local Thinning Channel Layer

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Abstract: $\beta-Ga_2O_3$ field−effect transistors (FETs) were fabricated with and without local thinning to change the threshold voltage. A 220 nm Ga_2O_3 layer was mechanically exfoliated from a Cr−doped gallium oxide single crystal. Approximately 45 nm Ga_2O_3 was etched by inductively coupled plasma to form the local thinning. The threshold voltage of the device with etched local thinning increased from −3 V to +7 V compared to the unetched device. The effect of the local thinning was analyzed by device simulation, confirming that the local thinning structure is an effective method to enable enhancement−mode Ga_2O_3 FETs.

Keywords: Ga_2O_3; field−effect transistors; enhancement−mode; local thinning

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1. Introduction

$\beta-Ga_2O_3$ has attracted significant attention attributing to its ultra−wide bandgap, high breakdown electric field (~8 MV cm^{-1}), and excellent chemical stability [1–5]. In addition, the Baliga's figure of merit of Ga_2O_3 is approximately 3200, which is three times higher than that of GaN and eight times higher than that of SiC [1,6]. This shows that Ga_2O_3 has great potential as a future power electronics material. Epitaxial $\beta-Ga_2O_3$ layers have been grown by many techniques including metal−organic chemical vapor deposition, molecular beam epitaxy, and pulsed laser deposition [7,8]. Ga_2O_3−based field−effect transistors [9–11], metal−semiconductor field−effect transistors [6,12], and Schottky barrier diodes [13–16] have demonstrated potential as next−generation high−power electronic devices. In particular, Ga_2O_3−based FETs have shown high current densities [17,18], high voltage breakdown [19], low ohmic contact resistance [20], and early prospects for modulation doping [21] and integration [22].

Since $\beta-Ga_2O_3$ bulk crystal monoclinic structures have large lattice constant differences between the a, b, and c axes, they can be used to prepare single−crystalline nanolayer flakes by the mechanical exfoliation method [23]. Mechanically exfoliated $\beta-Ga_2O_3$ nanolayer flakes are strain−free and have flat surfaces with high crystallinity. Gallium oxide doped with Si [24], Sn [25] and Ge [26] can achieve n−type films. However, an n−type Ga_2O_3 FET is a depletion−mode device with a negative threshold voltage (V_{th}); with the lack of effective p−type doping, enhancement−mode (e−mode) operation has been limited. Enhancement−mode devices are preferred to mitigate the off−state power dissipation and for safe high−voltage operations in practical power applications [27].

Even so, there have been many reports on e−mode $\beta-Ga_2O_3$ FETs in recent years. Chabak et al. [28] fabricated Sn−doped Ga_2O_3 wrap−gate fin−array field−effect transistors (finFETs) with a threshold voltage between 0 and +1 V. Zongyang Hu et al. [29] fabricated an enhancement−mode Ga_2O_3 vertical power metal–insulator field−effect transistors with fin−shaped channels. Yuanjie Lv et al. [27] fabricated Ga_2O_3 metal−oxide−semiconductor field−effect transistors with gate recess depths of 110 nm and 220 nm, respectively. Additionally, upon increasing the recess depth, the threshold voltage increased to +3 V. Kamimura et al. [30] fabricated enhancement−mode devices using N−Si co−doping technology. Zhaoqing Feng et al. [31] achieved an enhancement−mode Ga_2O_3 metal−oxide semiconductor field−effect transistor by incorporating a laminated ferroelectric charge storage gate structure. Janghyuk Kim et al. [6] demonstrated the realization of an E−mode quasi−two−dimensional Ga_2O_3 FET with a novel graphene gate architecture via a van der Waals heterojunction. Xunxun Wang et al. [32] fabricated SnO/Ga_2O_3 p−n heterojunctions in the back channel, achieving enhancement−mode operation.

Herein, bottom−gate (BG) Ga_2O_3 FETs can be easily fabricated with a local thinning channel layer based on high−quality Ga_2O_3 layers with a thickness of 220 nm, exfoliated from Cr−doped Ga_2O_3 single crystals [33]. Before the experiment, the effects of local thinning on the device were thoroughly analyzed based on Technical Computer−Aided Design (TCAD) simulation. The simulation results show that the local thinning can achieve larger output current compared to the overall thinning. Moreover, the threshold voltage shifted in the positive direction by about 4 V for every 50 nm increase in the locally thinned thickness. It can be known from the simulation results that the threshold voltage of the device can be adjusted by changing the thickness of Ga_2O_3. Therefore, by preparing a bottom gate structure transistor, we etch on the top of the gallium oxide, and change the thickness of the Ga_2O_3 layer to achieve the purpose of enhancement mode. The transistor realized by the bottom gate device does not need the preparation process of preparing the trench gate, which greatly simplifies the preparation process. An enhancement−mode Ga_2O_3 FET was made with local thinning depth of 45 nm, exhibiting a high threshold voltage of +7 V and a saturation current of 0.34 μA.

2. Materials and Methods

In this study, unintentionally doped bulk β−Ga_2O_3 crystals were used. The carrier concentration of the crystal is approximately 1×10^{17} cm^{-3}. The arrangement of atoms in the monoclinic system β−Ga_2O_3 allows a facile exfoliate into thin flakes in the (100) direction, which has a larger lattice constant than other directions [9,34]. The device process flow is shown in Figure 1. First, nano−scale thickness Ga_2O_3 flakes were prepared by repeated mechanical exfoliation from the bulk Ga_2O_3 crystals. Then, Ga_2O_3 flakes were transferred to a p−type silicon wafer, with a 100 nm thickness thermally grown SiO_2. For the Ga_2O_3 flakes to have better contact with the Si substrate and reduced amount of contaminants, the substrate was pretreated by oxygen plasma (ProCleanerTM, Harrick Plasma, Ithaca, NY, USA) for 3 min prior to the transfer. The source and drain electrodes were defined by Ti/Au (20 nm/80 nm) using an electron−beam evaporation technique on both ends of the Ga_2O_3 flakes. The source and drain contacts improved by inductively coupled plasma etching before electrode deposition with the power, chamber pressure, gas flow, and etching time of 150 W, 20 mTorr, BCl_3/Ar (15 sccm/5 sccm) and 2 min, respectively. Finally, dry etching was performed using a BCl_3/Ar plasma with a photolithography mask used to form the recess. The power, chamber pressure, gas flow, and etching time was 350 W, 20 mTorr, BCl_3/Ar (15 sccm/5 sccm) and 3.5 min, respectively [35]. After etching, a Ga_2O_3 local thinning structure device was formed as shown in Figure 1f. The channel length and width are 12 μm and 1.1 μm, respectively.

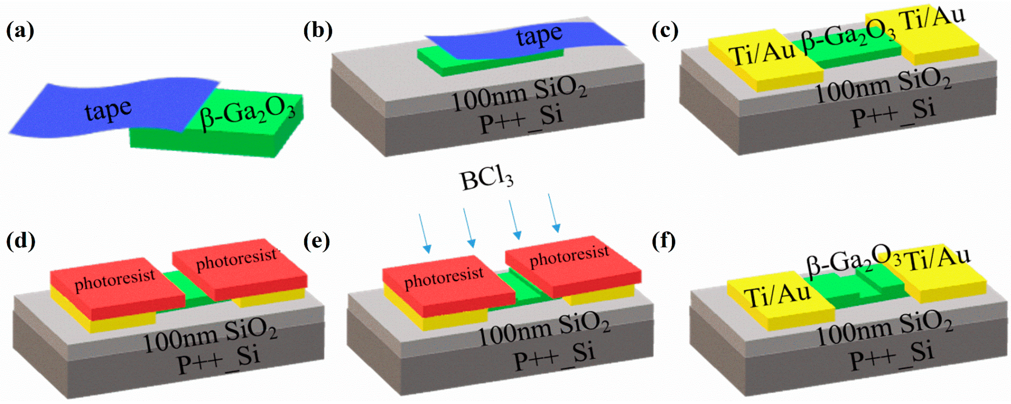

Figure 1. Schematic of the exfoliated $\beta-Ga_2O_3$−flake−based enhancement−mode FET fabrication process: (**a**) Nano−scale thickness $\beta-Ga_2O_3$ flakes were prepared by repeated mechanical exfoliation from the bulk Ga_2O_3 crystals, (**b**) $\beta-Ga_2O_3$ flakes were transferred to a p−type silicon wafer, (**c**) the schematic structure of the fabricated $\beta-Ga_2O_3$ flake FET, (**d**) the etched position of the local thinning after the FET device was subjected to a photolithography process, (**e**) etching to form the local thinning and (**f**) the schematic structure of the $\beta-Ga_2O_3$ flake FET with the local thinning.

The fabricated devices were characterized by scanning electron microscopy (SEM, FEI Nano 450, Hillsboro, OR, USA), atomic force microscopy (AFM, Benyuan CSPM5500, Guangzhou, China), and their electrical characteristics were measured using a source/measurement unit semiconductor parameter analyzer (Keysight B2902A, Santa Rosa, CA, USA) at room temperature.

3. Results

TCAD provides an efficient way to understand the properties of the device. Up to now, many related works have been reported on the TCAD simulation of Ga_2O_3 transistors [36–38]. Due to the non−convergence of the bottom gate model, we used a similar structure for the top gate to analyze the effect of the local thinning on the threshold voltage. Here, the effect of gate recess on the Ga_2O_3 FET with a doping concentration of 10^{17} cm^{-3} was investigated by modeling prior to device fabrication. In the model, the channel layer had a 200 nm thick Ga_2O_3 film and a gate dielectric layer of 100 nm SiO_2. Figure 2 shows the simulation schematics with overall thinning of 50 nm (a) and local thinning of 50 nm (b), respectively. As shown in Figure 2c, comparing the output characteristic curves of the overall thinning and the local thinning, the current of the overall thinning is significantly smaller than that of the local thinning, but the transfer curves show that the threshold voltage of the overall thinning and the local thinning hardly changes, as shown in Figure 2d. This result indicates that local thinning can effectively prevent the current reduction caused by thinning Ga_2O_3 film.

Figure 3a,b shows the simulated structure of Ga_2O_3 FET without and with local thinning, respectively. To directly compare the V_{th} shift by increasing the locally thinned thickness, we set the thinning thickness to increase from 0 to 150 nm. Figure 3c shows the variation of the output current of Ga_2O_3 FETs with different thinning thicknesses. Obviously, with the increase in the local thinning depth, the output current gradually decreases. In addition, the thickness of the local thinning increases by 50 nm, and the threshold voltage is shifted in the positive direction by about 4 V, as shown in Figure 3d.

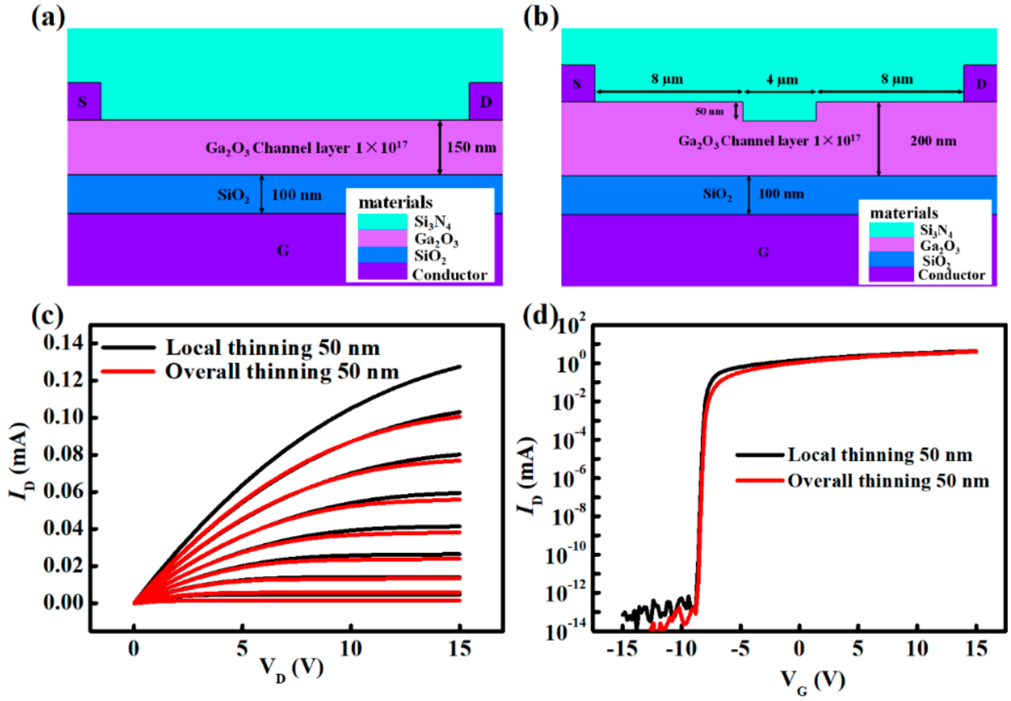

Figure 2. Schematic diagram of the simulation of the overall thinning of 50 nm (**a**) and the local thinning of 50 nm (**b**), output characteristic curves (**c**) and transfer characteristic curves (**d**) of overall thinning 50 nm and local thinning 50 nm.

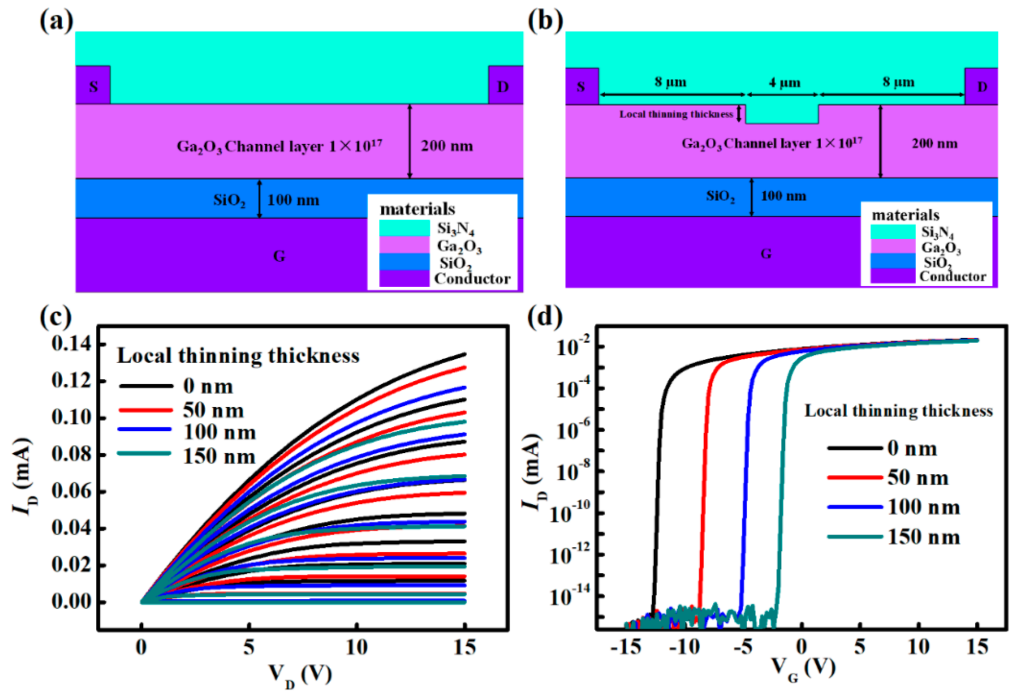

Figure 3. Schematic diagram of the simulation structure of bottom−gate Ga_2O_3 FET without (**a**) and with (**b**) local thinning, output characteristic curves (**c**) and transfer characteristic curves (**d**) of diiferent local thinning thickness.

Based on the simulation results, $\beta-Ga_2O_3$ thin−film FET devices were prepared. Figure 4a and b show the SEM images of the $\beta-Ga_2O_3$ flake fabricated into a FET structure with a Ti/Au electrode and a FET device with local thinning, respectively. Figure 4c shows the local thinning depth is 45 nm and the bulk $\beta-Ga_2O_3$ crystal peeled off into a sheet with a thickness of approximately 220 nm, as revealed by the atomic force microscopy image, as shown in Figure 4d.

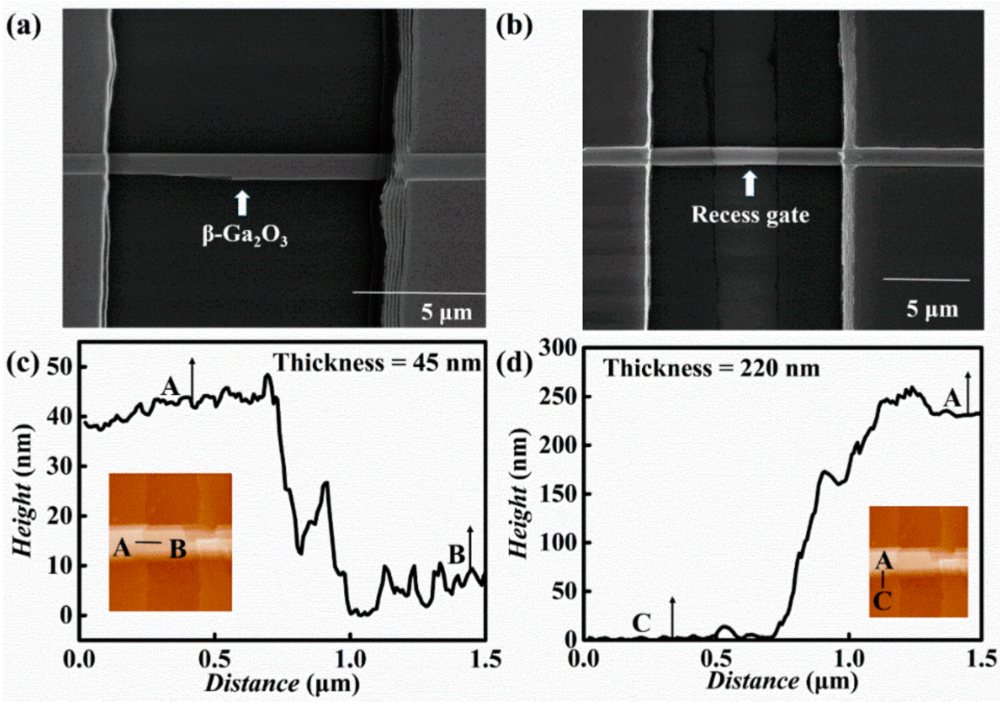

Figure 4. (**a**) SEM image of a β−Ga_2O_3 thin film made of a FET structure using a Ti/Au electrode, (**b**) SEM image of the local thinning of a Ga_2O_3 FET, (**c**) AFM height distribution of the local thinning and the Ga_2O_3 (**d**).

The output characteristics of the β−Ga_2O_3 FET with and without the local thinning structure were measured using a semiconductor characterization system at room temperature. In the measurements, the drain−source voltage ranges from 0 V to 10 V. The fabricated Ga_2O_3 FETs exhibited good saturation and pinch−off characteristics. As shown in Figure 5a and b, a linear increase in I_D at low V_D, and saturation at high V_D, represent effective gate modulation in an n−type channel. A maximum drain current (I_{Dmax}) of 0.4 μA was obtained at the V_G of +5 V in the device before etching, while the I_{Dmax} was just 0.34 μA at the V_G of +12 V after etching, mainly because the etched oxide channel forms the local thinning. The local thinning structure also results in a low drain current. The transfer characteristics of the Ga_2O_3 FETs before and after etching were also measured. During the measurement, the device drain bias was set to +10 V. As shown in Figure 5c, the device before etching has a threshold voltage of −3 V, and after etching, the threshold voltage reaches +7 V, as shown in Figure 5d. This change is from a depletion mode to an enhanced field−effect transistor, mainly because the formation of a 45 nm local thinning structure after etching decreases the thickness of the channel layer, resulting in an earlier depletion pinch−off of the device during operation. Overall, the result is that V_{th} shifts from negative values in D−mode to positive values in E−mode by reducing the thickness of Ga_2O_3 [39]. The forward threshold voltage forms a normally on FET device. Comparing the off−state drain current before and after etching, the leakage current after etching is approximately 6×10^{-11}, which is larger than that of 8×10^{-12} before etching, showing that dry etching damages the n−type Ga_2O_3 layer to some extent. Before the etching, the on/off current ratio of the device reaches 1×10^5, because of the relatively low off−state current. After the etching, the on/off current ratio reduced to 2.2×10^4, because of the rising leakage current.

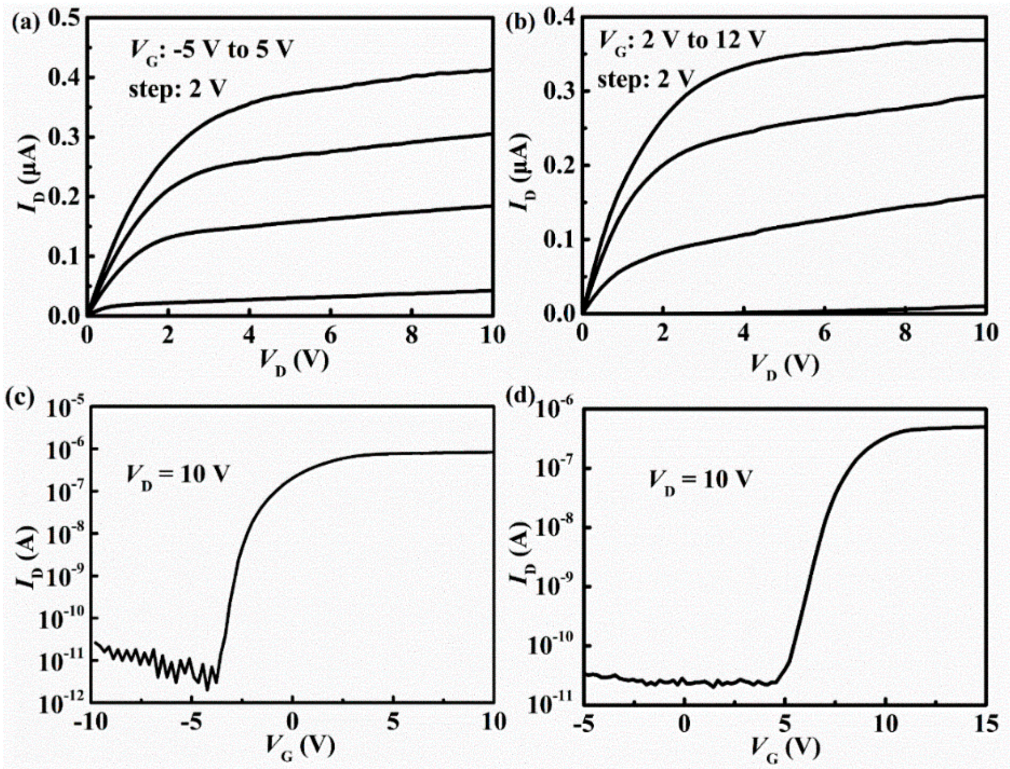

Figure 5. (**a**) Output characteristic curve with various V_G before and after (**b**) etching of $\beta-Ga_2O_3$ FET, the transfer curve in log scale before (**c**) and after (**d**) etching.

4. Conclusions

In summary, Ga_2O_3 FETs were fabricated with and without the local thinning based on high−quality quasi−two−dimensional single−crystalline $\beta-Ga_2O_3$ flakes exfoliated from a bulk single crystal. The effect of the local thinning structure was investigated by device simulations. The simulation results show that the local thinning can achieve larger output current compared to the overall thinning. In addition, the threshold voltage shifted in the positive direction by about 4 V for every 50 nm increase in the locally thinned thickness. The fabricated Ga_2O_3 FETs have good saturation and pinch−off characteristics. In the device with a doping concentration of 10^{17} cm^{-3}, the device before etching has a threshold voltage of −3 V, and after etching, the threshold voltage reaches +7 V. By optimizing the device processing, the performance of Ga_2O_3 FET may be further improved.

Author Contributions: M.X. and Q.X. conceived and designed the experiments; L.G., Q.C. and S.W. performed the experimental work and analyzed the data under the supervision of A.S., X.T., Z.J. and W.M.; writing—original draft preparation, L.G. All authors have read and agreed to the published version of the manuscript.

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