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Board Level Drop Test for Evaluating the Reliability of High-Strength Sn–Bi Composite Solder Pastes with Thermosetting Epoxy

Lu Liu, Songbai Xue *, Ruiyang Ni and Peng Zhang

College of Materials Science and Technology, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China; luciana.liu@nuaa.edu.cn (L.L.); niruiyang@nuaa.edu.cn (R.N.); mstzhangpeng@nuaa.edu.cn (P.Z.)

* Correspondence: xuesb@nuaa.edu.cn

Abstract: The Sn–Bi solder paste is commonly used in electronic assembly and packaging, but its brittleness causes poor reliability in shock environments. In this study, the mechanical reliability of Sn–Bi solder paste and Sn–Bi composite solder paste with thermosetting epoxy (TSEP Sn–Bi) was investigated with the board level drop test. The crack characterizations of solder joints were evaluated using a stereomicroscope after the dye and pull test. The microstructure characterization and failure types of solder joints were analyzed by a scanning electron microscope (SEM), and an energy dispersive spectrometer (EDS) was employed to investigate the initial phase identification and elemental analysis. Compared with Sn–Bi solder paste, the results show that the TSEP Sn–Bi solder pastes reduced the proportion of the complete failure and partial failure of the solder joints during the drop test. The microstructure observation of the crack path showed that the Sn–Bi/TSEP Sn–Bi solder joints were reinforced through the cured epoxy resin. The number of drops of the Sn–Bi/TSEP Sn–Bi-x (x = 3, 5, 7) solder joints had 1.55, 2.57, and over 3.00 times that of Sn–Bi/Sn–Bi solder joints after the board level drop test.

Keywords: board level drop test; composite solder paste; crack characterization; mechanical reliability

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1. Introduction

Recently, with the miniaturization of electronic products, the reliability of solder joints has greatly concerned semiconductor and electronic product manufacturers [1–3]. Sn–Ag–Cu solders with good mechanical property and reliability are widely used in surface-mount technology (SMT) [4–6]. However, due to the complexity of electronic assembly and packaging, the production process needs multiple reflow soldering, which requires solders with different melting temperatures [7,8]. In addition, the Sn–Ag–Cu solders cannot apply to temperature-sensitive devices that require a low-temperature soldering process, and the difference of the coefficients of thermal expansion (CTE) of the substrates and chips easily causes a warpage under the high reflow temperature [9,10].

Low-temperature soldering can reduce warpage caused by thermal stress, improve product reliability, and reduce nearly 40% of the CO_2 emissions and production costs [11,12]. In recent years, low-temperature lead-free solders have attracted much attention, in which the SnBi eutectic solder alloy is the most widely used in low-temperature soldering connections for device-level packaging and system-level packaging [13]. The Sn–Bi solder has good wettability and mechanical properties, and the melting point is 139 °C. However, the brittleness of the Bi phase results in poor plasticity of the solder, and the solder joints have poor mechanical reliability [14,15].

Previous studies showed that the addition of a third element (such as Ag/Cu/Ni/Sb) or nanoparticles to Sn–Bi eutectic alloys could improve mechanical properties and reliabilities [14,16,17]. Park et al. investigated the effect of 85 °C/1000 h aging on the reliability of a

Sn-58Bi solder joint with different content of Ag-decorated multi-walled carbon nanotubes (Ag-MWCNTs). After aging for 1000 h, it was observed that the addition of Ag-MWCNTs at 0.05 wt.% had a higher bonding strength, whereas the addition of Ag-MWCNTs at over 0.3 wt.% decreased the mechanical and thermal properties of solder joints [18]. Myung et al. investigated the mechanical and electrical properties of Sn-58Bi, Sn-57.6Bi-0.4Ag, and Sn-57Bi-1Ag solder joints. It was reported that the Sn-57Bi-1Ag and Sn-57.6Bi-0.4Ag solder joints had higher shear strength than Sn-58Bi solder joints after aging for 1000 h and that the IMC thickness increased slower than Sn-58Bi solder joints [19]. Although many studies demonstrated that the addition of the third element or nanoparticles to Sn–Bi eutectic alloy benefitted the properties of solder joints, the complexity of the material's preparation process and the problem of cost increase were needed to be considered. To overcome these issues, the Sn–Bi composite solder paste with thermosetting epoxy (TSEP Sn–Bi) was mentioned to prepare the high-performance joint in our previous studies [20,21]. After the thermal cycling test and temperature and humidity test, the TSEP Sn-Bi solder joints demonstrated better mechanical characteristics. The addition of the epoxy system could provide good protection for the solder joints, and reduce fatigue damage from environmental influence [22].

The failure of solder joints is influenced not only by the temperature and humidity environment changes in the electronic devices but also by dust, stress, shock, and vibration. The board level drop test, which is based on the mechanical shock test (refer to the standards of JEDEC JESD 22-B110 and JESD22-B111A), is an essential method for determining the mechanical reliability of solder joints [23–25]. Previous studies have focused on the mechanical reliability of Sn–Ag–Cu solder joints due to their wide use in SMT. When Zhang et al. studied the board level drop reliability and the failure location of Sn–Ag–Cu solder joints, the results indicated that the solder joint failure occurred most frequently at the four corners of the IC package, and cracks occurred at the interface between IMC and the Ni pad [26]. Gu et al. investigated the board level drop/vibration reliability of Sn-3.0Ag-0.5Cu solder joints after thermal/isothermal cycling and analyzed the failure modes and mechanisms of Sn-3.0Ag-0.5Cu solder joints under different loading conditions [27]. However, due to the brittleness of Sn–Bi solder joints, there have been only a few investigations of Sn–Bi solder in a board level drop test. The demand for low-temperature soldering has propelled the wide use of Sn–Bi solders into SMT over the last five years. Fu et al. proposed a method for improving printed circuit board (PCB) warpage and mechanical reliability by soldering Sn–Ag–Cu solder with Sn–Bi solder paste at a peak reflow temperature below 200 °C [12]. Ren et al. studied the board level drop reliability of hybrid Sn–Ag–Cu/Sn–Bi–X solder joints, and the Sn–Ag–Cu/Sn-49Bi-1Ag solder joints had the best drop reliability for assembling [28]. In this study, a hybrid solder joint of Sn–Bi and TSEP Sn–Bi was prepared and investigated.

The main objective of this study was to evaluate the mechanical reliability performance of solder joints with a eutectic Sn–Bi solder paste and TSEP Sn–Bi solder pastes in a board level drop test.

2. Materials and Methods

2.1. Preparation of Test Specimen

The Chip side was designed as a FR4 PCB with dimensions of 23 mm × 23 mm × 1.6 mm and 8 × 8 arrays of Cu substrates. The PCB side was designed as a FR4 PCB with dimensions of 77 mm × 77 mm × 1.6 mm and 64 Cu substrates interconnected with Chip sides. According to the standard of JESD22-B111A, in order to ensure a total symmetric design for the board, the PCB layout for each of these four components was identical, as shown in Figure 1, and each solder joint was connected by a daisy chain. The copper pads on the PCB side and chip side were designed with a 0.60 mm diameter and a 35 µm thickness, and the surface treatment method of the copper pad was organic solderability preservatives (OSP).

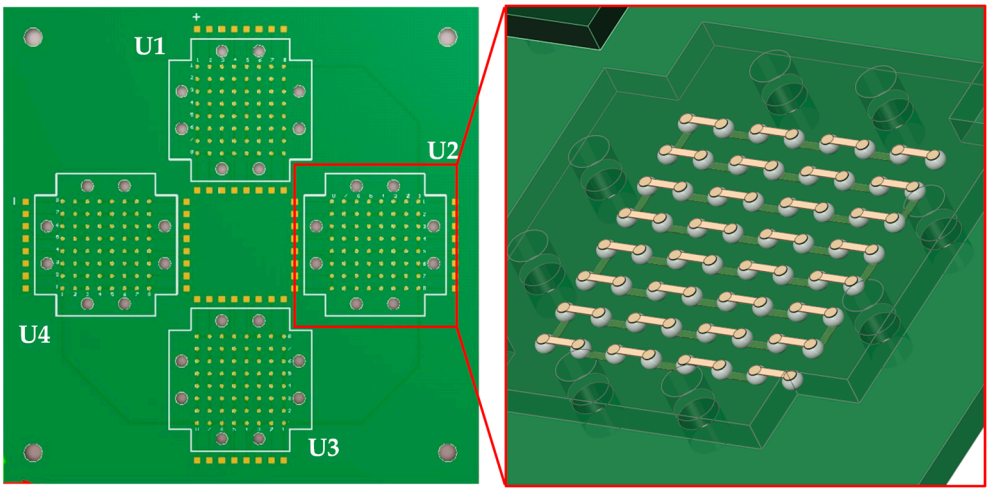

Figure 1. The design of test board and layout.

Four types of solder pastes were used in this study. The eutectic Sn–Bi solder paste was used to print on the Chip side and PCB side, forming the Sn–Bi/Sn–Bi solder joint. The Sn–Bi composite solder paste with thermosetting epoxy with different proportions (3 wt.%, 5 wt.%, and 7 wt.%) (TSEP Sn–Bi-x, x = 3, 5, 7) was used to print on the PCB side, forming the hybrid Sn–Bi/TSEP Sn–Bi-3, Sn–Bi/TSEP Sn–Bi-5, and Sn–Bi/TSEP Sn–Bi-y solder joints. The TSEP Sn–Bi solder paste was prepared using Sn–Bi solder powder (particle size 25–45μm), flux, and epoxy system, and the epoxy resin system consisted of thermosetting epoxy resin and a curing agent, which can be seen in previous studies regarding the preparation of TSEP Sn–Bi solder paste [20,22]. Figure 2 illustrates a two-part schematic diagram of the drop test specimen's preparation process. The first step was to print the eutectic Sn–Bi solder pastes to Cu substrates and form a Sn–Bi solder joint on the chip side after the reflow soldering process. Each of the stencil apertures on the chip side was 150 μm thick and 1.6 mm in diameter. To enable the solder paste to constitute solder joints after the reflow soldering process, the stencil apertures were designed to be larger than the Cu lands. The second step was to complete the assembly of the test specimen by printing the eutectic Sn–Bi solder paste or TSEP Sn–Bi-x solder paste to Cu lands on the PCB side, where the stencil holes were 150 μm thick and 0.8 mm in diameter. Using the hybrid rework system (Kurtz Ersa, Kreuzwertheim, Bavaria Germany, HR 600/2), the chip sides were assembled to the PCB sides and then implemented a connection.

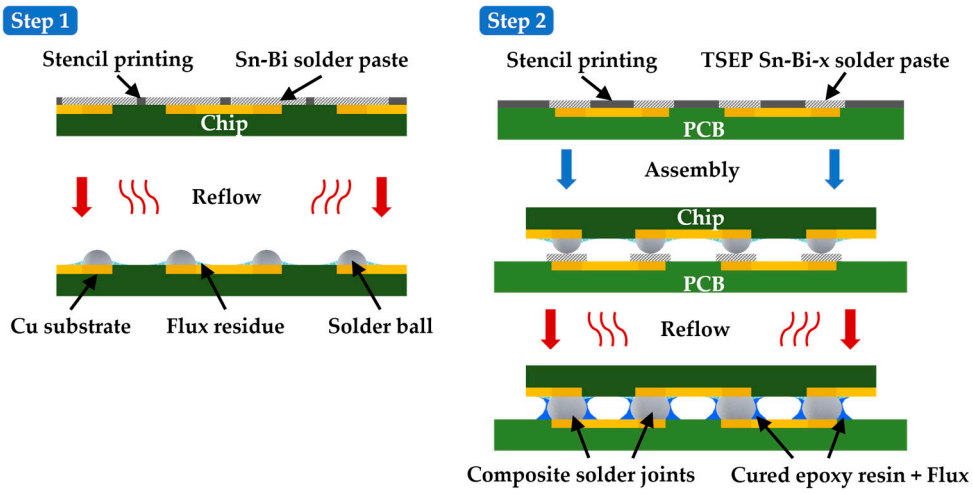

Figure 2. Schematic diagram of the drop test specimen preparation process.

In the previous study, the epoxy resin system curing reaction of TSEP Sn–Bi-x solder pastes was analyzed with a differential scanning calorimeter (DSC). The results showed that the peak temperature of the epoxy resin system was 151.4 °C, and the curing reaction was completed close to 200 °C [22]. An optimized reflow profile was applied to the solder TSEP Sn–Bi-x solder pastes, while the original reflow profile was used to solder the Sn–Bi solder paste in order to allow the epoxy resin system to complete the curing reaction [20,22]. The reflow profiles of the Sn–Bi solder paste and TSEP Sn–Bi solder pastes are shown in Figure 3.

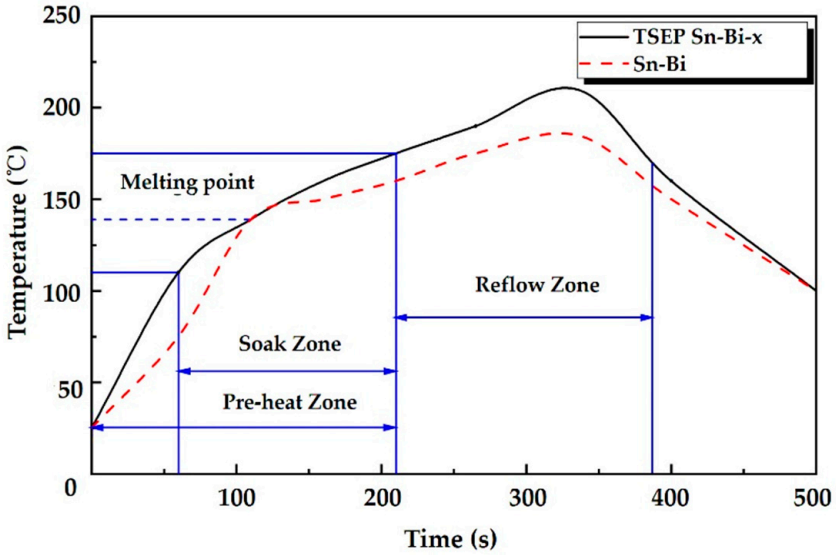

Figure 3. Reflow profile of the Sn–Bi solder paste and TSEP Sn–Bi-x solder pastes [20,22].

2.2. Experimental Procedures

2.2.1. Board Level Drop Test

Figure 4 shows the schematic configuration of the drop test apparatus. A high-acceleration shock tester (King Design Industrial, New Taipei City, Taiwan China, DP-1200-18) was used to evaluate the mechanical reliability of the Sn–Bi/Sn–Bi solder joints and hybrid Sn–Bi/TSEP Sn–Bi-x solder joints at the same condition. The specimen (with the chip side facing down) was mounted on the base plate, where the four corners was fastened with a single-pass copper stud with thread size of M2.5, bolt length of 25 mm, and thread length of 6 mm. A torque wrench was used to fasten the single-pass copper studs, with the tightening torque setting at 0.18 N. The table was raised to a prescriptive height and then released freely to impact the striking surface once the drop test was accomplished. The repeated up and down bending of the PCB during the drop impact process has been identified as the primary cause of solder joint failure in many investigations. In this study, the parameters were set as follows: the acceleration peak was 1500 G, the pulse duration was 0.5 ms, and the equivalent drop height was 112 cm. The failure criterion was defined as the case in which the digital multimeter detected an open circuit between the positive and negative terminals of the PCB. Five specimens of each solder paste were selected for testing, and the number of drops after failure was recorded to take the average value.

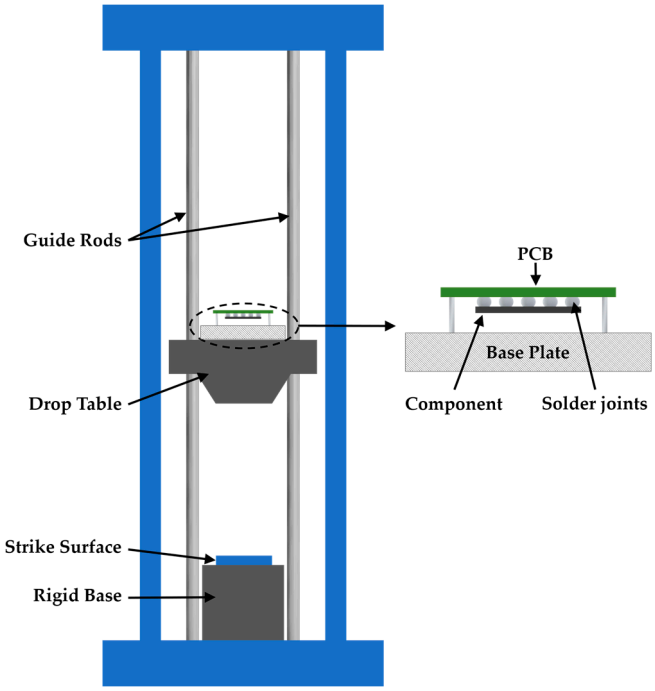

Figure 4. Schematic configuration of the drop test apparatus.

2.2.2. Microstructural Characterization and Failure Analysis

A dye and pull test was used to analyze the crack characterizations of the four kinds of solder joints after the board level drop test. According to the standard IPC TM-650 2.4.53 "Dye and Pull Test Method (Formerly Known as Dye and Pry)", the specimens were submerged in red dye and then subjected to alternating vacuum to force the dye into any cracked interfaces. After that, the specimens were put in an oven and allowed to dry at 60 °C for 15 min, and then the pull test was used to separate the interconnected surfaces. Both the PCB sides and chip sides of the interconnecting surface were inspected for any traces of dye using the stereomicroscope. The red color penetrated any cracks that had formed before being submerged, and the specimens were prepared for cross-sectional analyses after the board level drop test. The microstructure characterization and failure types of solder joints were analyzed by a scanning electron microscope (SEM, Hitachi, Tokyo, Japan, S3400N Type II), and an energy-dispersive spectrometer (EDS) was employed to investigate the initial phase identification and elemental analysis.

3. Results and Discussion

3.1. Drop Test Results

The connectivity of the circuit was detected after each drop impact process, and the failure criterion was defined as an open circuit that corresponded to 100% of the solder joint cracks. There were five specimens of each solder paste selected, and the number of drops was recorded. Figure 5 shows the drop test results for Sn–Bi and TSEP Sn–Bi-x (x = 3, 5, 7) solder pastes after the board level drop test. The Sn–Bi/Sn–Bi solder joints failed when the drop number was 1163. The Sn–Bi/TSEP Sn–Bi-x solder joints (x = 3, 5) failed when the number of drops were 1807 and 3004, which were 1.55 and 2.57 times that of the Sn–Bi solder joints, respectively. In addition, the Sn–Bi/TSEP Sn–Bi-7 solder joints did not fail after 3500 drops, over 3.00 times as many as the Sn–Bi/Sn–Bi solder joints. The results demonstrated that under the same testing conditions, the number of drops were increased with the addition of the epoxy resin system. Solder joints prepared with TSEP Sn–Bi-x solder pastes had higher reliability under impact drop conditions than Sn–Bi solder joints did.

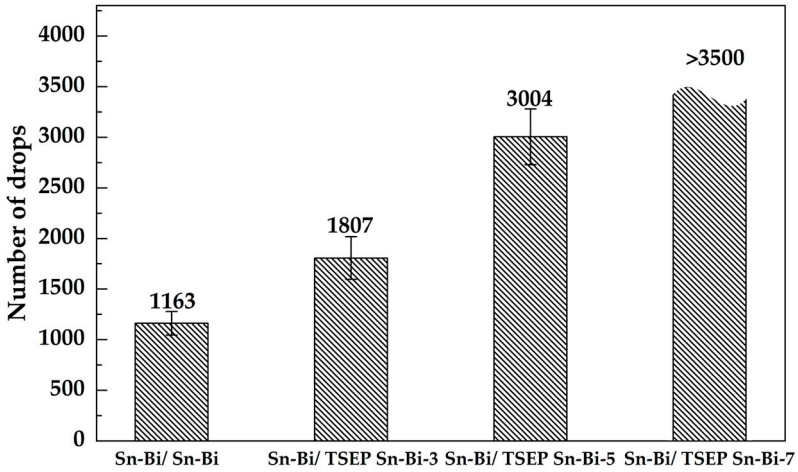

Figure 5. Drop test results for Sn–Bi/Sn–Bi and Sn–Bi/TSEP Sn–Bi-x solder joints after the board level drop test.

3.2. Crack Characterization of Sn–Bi/Sn–Bi Solder Joints and Sn–Bi/TSEP Sn–Bi-x Solder Joints

After the board level drop test, the digital multimeter detected an open circuit between the positive and negative terminals of the PCBs. It indicated that there were over 50% disconnected failures inside the solder joints. At the same time, the resistance was increased continually during the real-time monitoring of circuit resistance changes, indicating that there were some cracks and crack growth in the solder joints during the drop test. The dye and pull test was used to analyze the position and cause of internal defects in the solder joints, by observing the pads and solder joints of the lifted circuit board that had been stained red.

There were 4 pics of chips on each specimen, and a digital multimeter was used to measure the conduction of each chip. The U3 of Sn–Bi/Sn–Bi, U1 of Sn–Bi/TSEP Sn–Bi-3, U4 of Sn–Bi/TSEP Sn–Bi-5, and U3 of Sn–Bi/TSEP Sn–Bi-7 were chosen for the dye and pull test, and they were tested via open circuit.

The solder joints were observed by a stereoscopic microscope, and the crack characterizations of the Sn–Bi/Sn–Bi solder joints and Sn–Bi/TSEP Sn–Bi-x solder joints after the dye and pull test were shown in Figure 6. There were four solder joints chosen from each specimen, which were framed with blue wire in Figure 7. The PCB sides and chip sides of solder joints after the dye and pull test were shown to observe and analyze the crack characterization of the solder joints. The principle of the dye and pull test was to use the liquid's penetration characteristics, which could penetrate all solder gaps. If the solder joints were stained red in the place that had been soldered, that was the crack's position.

There are several types of crack modes in Figure 6, such as complete crack, partial crack, PCB crack, and no penetration crack. In complete crack mode, the whole fracture was dyed red, indicating that there was nearly 100% failure of the solder joints in the drop test. The no-penetration crack mode had a bright crack surface, which was formed during the pull test after the dye and pull test. The fracture of partial crack mode consisted of red and bright colors; there was still a connection between the chip side and the PCB side. In addition to the three crack modes above, another crack mode was the PCB crack, where cracks occurred primarily between the PCB matrix and the Cu substrate. These were generally accompanied by partial cracks in the solder joints. However, the solder matrix was still soldered with Cu substrate, which was not defined as a failure of the solder joints.

The distribution of failed solder joints in the four specimens above that were stained red were counted as shown in Figure 7. The nearly 100% failed solder joints were set as Type A and marked with red color, the partial failure of solder joints were set as Type B and marked with the red grid line, and the solder joints with no penetration were set as Type C and marked with white. Among the solder joints tested by the Sn–Bi/Sn–Bi solder joints in Figure 7a, 18.75% of the solder joints failed completely as Type A, and 15.63% of the solder

joints were likely to fail as Type B. Solder joints both near the outside of the PCB and inside the PCB had more dyed areas; in particular, the four corners of solder joints more easily failed. There was a less dyed area of the solder joints at center area of solder joint array, meaning that the maximum stress was primarily distributed on the outside corners of the solder joints.

Figure 7b–d show the fracture distribution maps of Sn–Bi/TSEP Sn–Bi-x (x = 3, 5, 7) solder joints. Among the solder joints, 9.37%, 6.25%, and 0% of solder joints were nearly 100% failure (Type A). The amounts of partial failure (Type B) of the solder joints were 7.81%, 7.81%, and 4.68%. The distribution of failed solder joints was similar to the Sn–Bi solder joints. However, compared with the distribution of failed solder joints of the Sn–Bi specimen, the quantity of failed solder joints decreased with the increase of the epoxy resin system addition, meaning that the TSEP Sn–Bi solder pastes could not only improve the reliability of solder joints but also reduce the proportion of the complete failure and partial failure of solder joints.

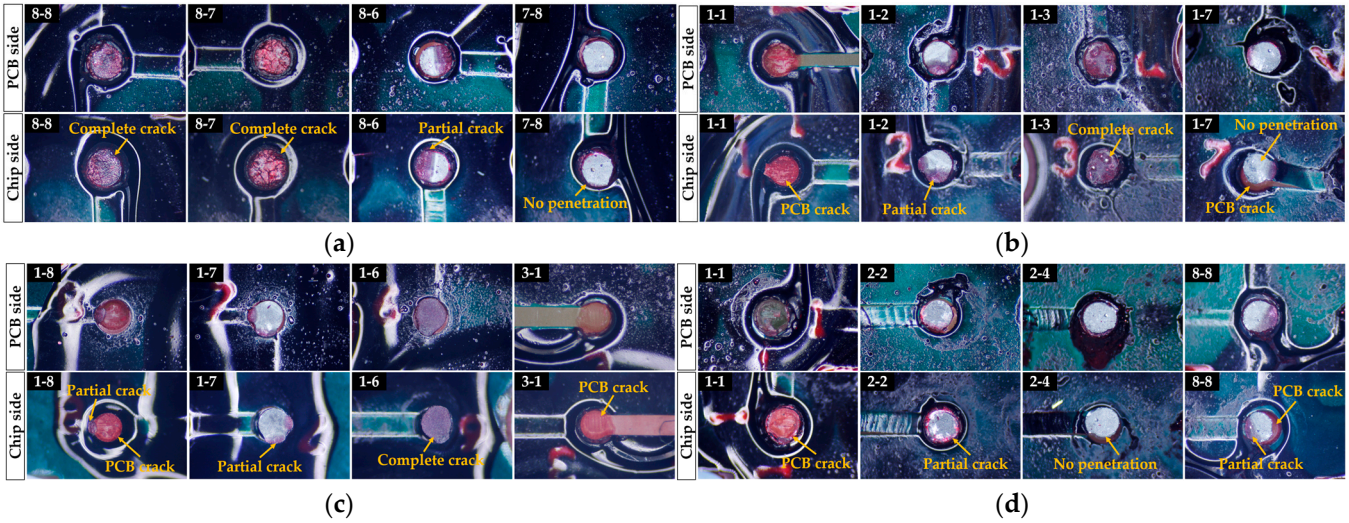

Figure 6. The crack modes of the Sn–Bi/Sn–Bi solder joints and Sn–Bi/TSEP Sn–Bi-x solder joints after the dye and pull test. (**a**) Sn–Bi/Sn–Bi. (**b**) Sn–Bi/TSEP Sn–Bi-3. (**c**) Sn–Bi/TSEP Sn–Bi-5. (**d**) Sn–Bi/TSEP Sn–Bi-7.

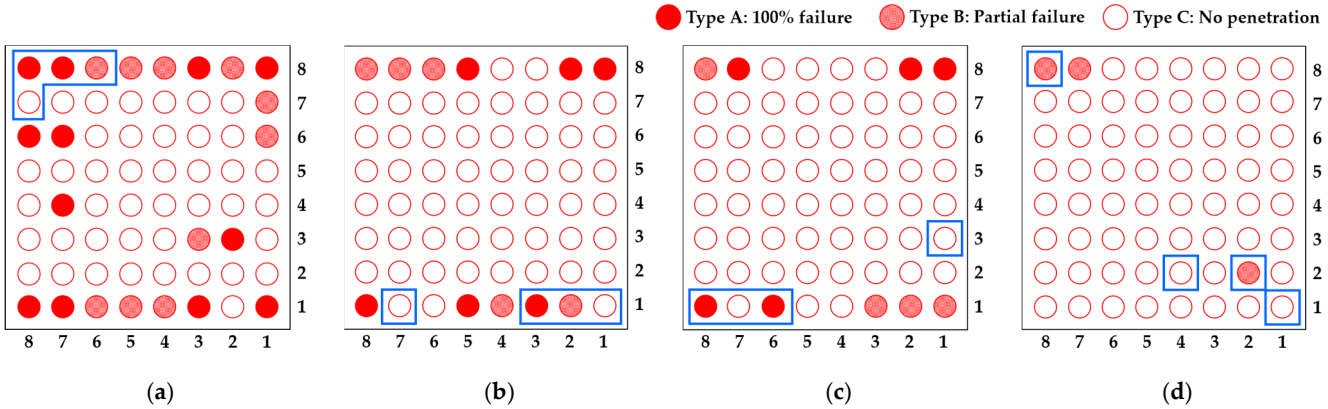

Figure 7. The fracture distribution maps of Sn–Bi/Sn–Bi solder joints and Sn–Bi/TSEP Sn–Bi-x solder joints after a board level drop test. (**a**) Sn–Bi/Sn–Bi U3. (**b**) Sn–Bi/TSEP Sn–Bi-3 U1. (**c**) Sn–Bi/TSEP Sn–Bi-5 U4. (**d**) Sn–Bi/TSEP Sn–Bi-7 U3.

3.3. Fracture Behavior of Sn–Bi/Sn–Bi Solder Joints and Sn–Bi/TSEP Sn–Bi-x Solder Joints

Previous studies summarized several possible crack modes of failed solder joints during the board level drop test [29,30]. Combined with the fracture modes of the solder

joint in this study, the seven types of possible crack paths were predicted in Figure 8. In the board level drop test, an open circuit was detected from the specimens, which indicated that a complete crack occurred in the solder joints. When the electrical resistance measured by the detector showed a significant increase, this indicated circuit defects and that a partial solder joint cracked. The complete cracks and partial cracks were primarily located between the intermetallic compound (IMC) and solder interface (Type 3 and Type 4 in Figure 8), between the Cu substrate and IMC (Type 2 and Type 5 in Figure 8), or at the solder matrix fracture (Type 7 in Figure 8), which could cause the circuit defects. In addition, when the copper-clad plate (CCL) pad matrix could no longer endure the drop impact, some cracks formed between the Cu substrate and PCB matrix (Type 1 and Type 6 in Figure 8), which might not cause the solder joint failure temporarily.

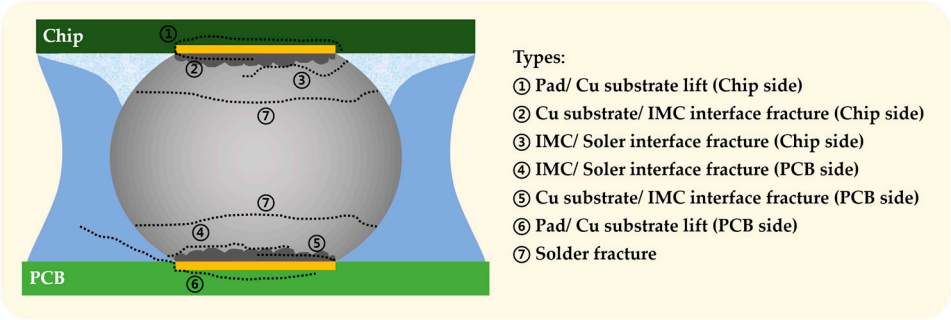

Figure 8. The possible crack path of solder joints from the board level drop test.

The microstructure of failed solder joints was observed through SEM and EDS to compare the failure modes between the Sn–Bi/Sn–Bi solder joints and Sn–Bi/TSEP Sn–Bi-x solder joints. Figure 9 shows the cross-section microstructure of solder joints after the board level drop test, and Figure 10 shows the enlarged images of cracks area in Figure 9, which are marked in orange lines in Figure 9. As shown in Figure 9a, the Sn–Bi solder was completely separated from the Cu substrate on the chip side, and a partial crack formed on the PCB side. The complete crack fracture of the Sn–Bi/Sn–Bi solder joint was a mixed fracture, and the crack path was along the boundary of the IMC layer and solder (type 4), as shown in Figure 10a. Due to a higher plastic strain between the PCB and solder matrix, this type of crack was more likely to occur at the corner edges of the components.

Figure 9b shows a partial crack mode of the Sn–Bi/Sn–Bi solder joint, and there was an obvious deformation of the Cu substrate on the PCB side. The PCB had a greatly flexural deflection under the 1500 G drop impact load, and the cracks were caused by stress concentrations. The crack initiation was more likely to occur at the solder/Cu substrate/PCB point of intersection due to the different elasticity modulus of the materials. In addition, the IMC layer was relatively thin after the reflow soldering, which is shown in Figure 10b; the cracks propagated mainly along the edges of the Sn–Bi solder and the IMC layer (type 4). There was also a crack mode located on the substrate Cu/PCB matrix (type 6). Although the formation of this crack mode did not result in an open circuit in the short term, it ultimately resulted in the propagation of crack in the solder joints, eventually leading to failure. The primary reason for cracks in this mode could be a poor substrate quality due to the PCB's manufacturing process. The stress was concentrated at the intersection of solder/Cu substrate/PCB, which was the second reason for cracks. The intersection became more vulnerable to cracks, the solder hardness increased, and at a given strain level, more stress was transmitted to the interface of the PCB pad, leading to the crack initiation and propagation into the bulk of the PCB. Furthermore, the PCB temperature difference before and after the reflow soldering increases resulted in a more mismatched CTE of the horizontal plane between the PCB and the solder joint, as well as increased stress on the solder joints.

Compared to the crack modes of the Sn–Bi/Sn–Bi solder joints, the Cu substrates were not deformed in Sn–Bi/TSEP Sn–Bi-x solder joints. As shown in Figure 10c–f, the orange dotted lines were used to mark the uncleaned flux residues and cured epoxy resin after soldering, which covered and wrapped around the solder joints. However, there were only no-cleaning flux residues covered around the Sn–Bi/Sn–Bi solder joints. The cured epoxy resin acted like an adhesive and provided mechanical resistance to the solder joints, which could reduce the warpage deformation of the PCB substrate during the repetitive drop impact. Combined with the results of the board level drop test, we discovered that with more epoxy resin system added, the protective layer was thicker, and the solder joints became much more reliable.

The microstructure of the Sn–Bi/TSEP Sn–Bi-x solder joint crack paths is shown in Figure 10. The microstructure near the crack was analyzed. The EDS analysis showed that the Bi-phase was observed in white color according to Spectrum A, and the Sn-phase was observed in gray color. Spectrum B of Figure 10e shows the IMC layer was Cu_6Sn_5. Figure 10c,d show the microstructure and crack path of Sn–Bi/TSEP Sn–Bi-3. The crack path of Figure 10c was mainly located along the solder matrix, and the crack path of Figure 10d was extended between the IMC layer and the solder interface (type 4). The crack path of Sn–Bi/TSEP Sn–Bi-5 is shown in Figure 10e, where the crack initiated from the solder matrix and expanded along with the solder interface and IMC layer. Mapping C of Figure 10f indicated that the crack path of Sn–Bi/TSEP Sn–Bi-7 solder joints also expanded between the IMC layer and the solder interface (type 4), which was similar to the Sn–Bi/TSEP Sn–Bi-3 and Sn–Bi/TSEP Sn–Bi-5.

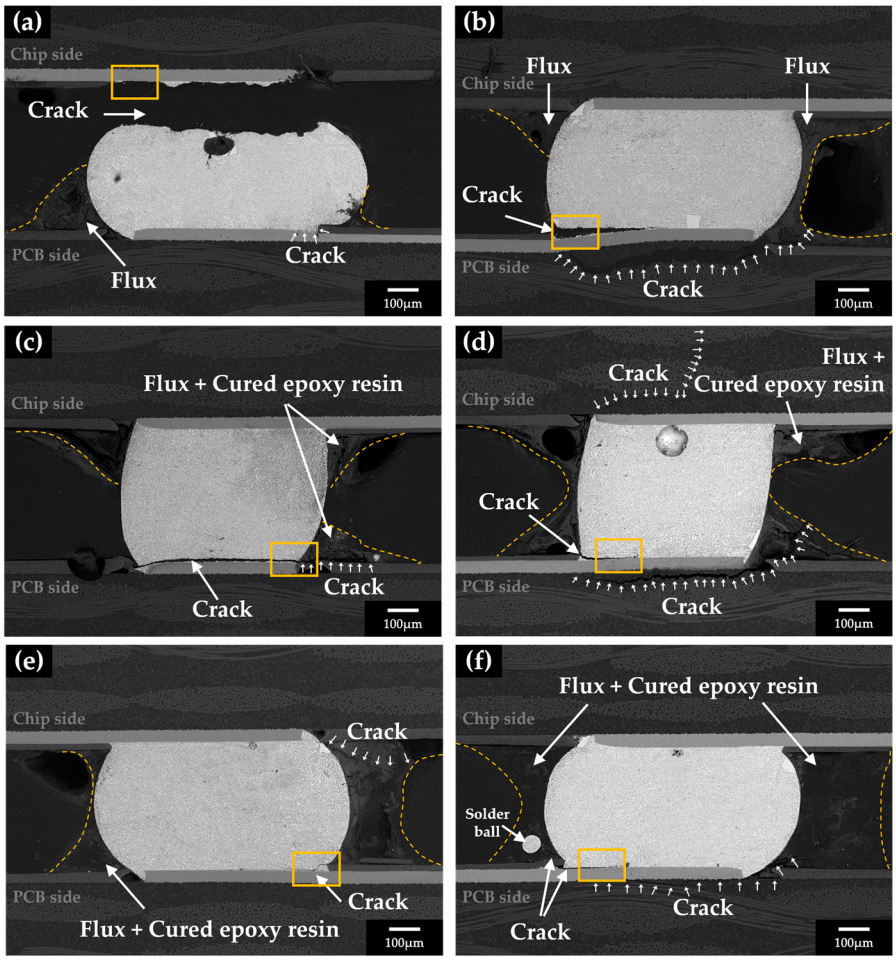

Figure 9. The typical failures of solder joints after the board level drop test: (**a**,**b**) Sn–Bi/Sn–Bi, (**c**,**d**) Sn–Bi/TSEP Sn–Bi-3, (**e**) Sn–Bi/TSEP Sn–Bi-5, (**f**) Sn–Bi/TSEP Sn–Bi-7.

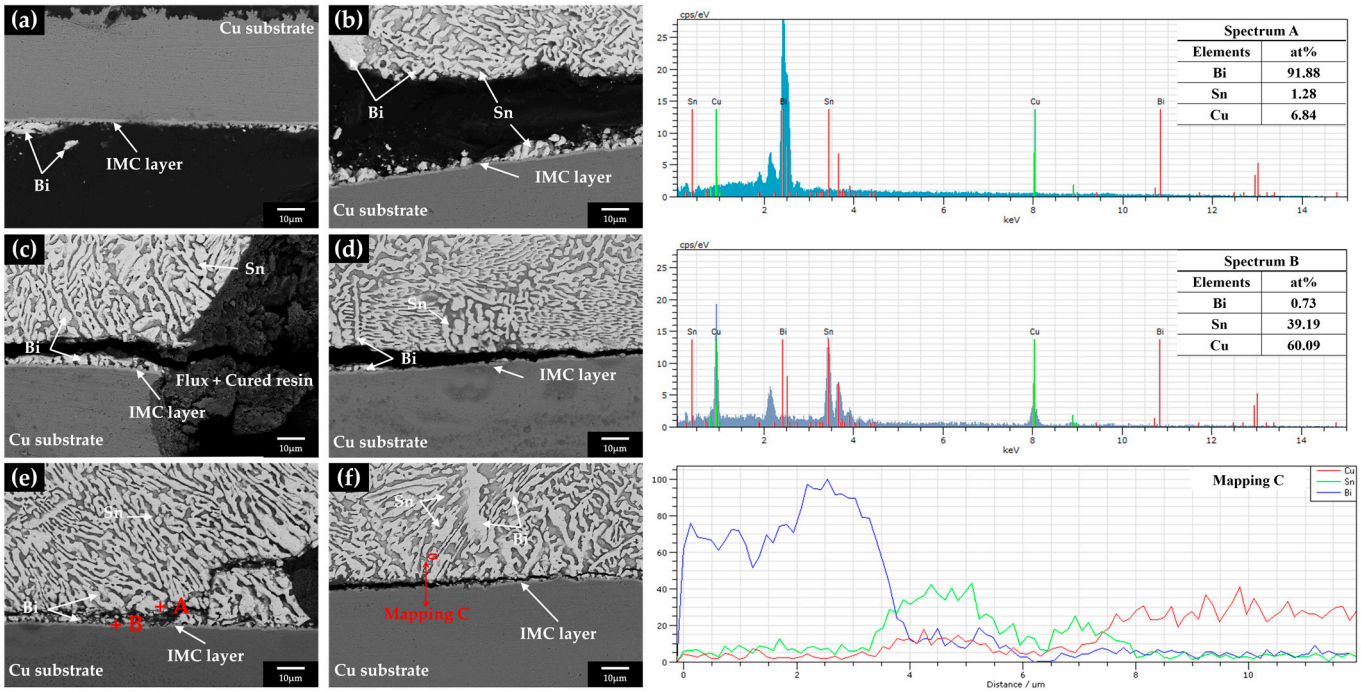

Figure 10. The SEM and EDS cross-section microstructure of solder joint crack paths: (**a**,**b**) Sn–Bi/Sn–Bi, (**c**,**d**) Sn–Bi/TSEP Sn–Bi-3, (**e**) Sn–Bi/TSEP Sn–Bi-5, (**f**) Sn–Bi/TSEP Sn–Bi-7.

During the drop test, the bending deformation of the PCB produced tensile and compressive stress on the solder joints at the corners of the specimens. In addition, the strains in the non-perpendicular planes subjected the solder joints to shear stress. Under the continuous reciprocal bending of the PCB, the crack gradually initiated and propagated, resulting in the complete failure of the solder joints. The stress produced by bending was dispersed and released under the protection of the cured epoxy resin, thereby increasing the fatigue resistance and mechanical strength of the solder joints and improving product reliability. Furthermore, a solder ball was observed in the solder joints of Sn–Bi/TSEP Sn–Bi-7, as shown in Figure 9f. The solder ball was embedded in the flux and cured epoxy resin, which did not violate minimum electrical clearance. According to the standard IPC A610G "Acceptability of Electronic Assemblies", it is acceptable when the diameter of the solder ball is no more than 0.13 mm. However, the increase in the amount of epoxy resin system added would increase the proportion of the flux. During the reflow soldering, the more epoxy resin system in the flux, the better the liquidity. As the temperature increased, the flux flowed preferentially, and it dispersed part of the unmelted solder alloy powder. When the temperature rose to the melting temperature of the Sn–Bi alloy, the dispersed solder alloy powder could not fuse with the solder to rely on surface tension, which formed as a solder ball.

4. Conclusions

In this study, the effects of the epoxy resin system addition on the mechanical and reliability of the Sn–Bi solder joints were investigated with the board level drop test.

The overall results indicated that the addition of epoxy resin system increased the mechanical reliability of solder joints. Sn–Bi/TSEP Sn–Bi-3 and Sn–Bi/TSEP Sn–Bi-5 solder joints failed at 1807 and 3004 drops after the board level drop test, which were 1.55 and 2.57 times that of the Sn–Bi/Sn–Bi solder joints, respectively. The Sn–Bi/TSEP Sn–Bi-7 solder joints had not failed after 3500 drops. It was observed that in the dye and pull test, the number of cracked solder joints decreased with the addition of the epoxy resin system content in Sn–Bi solder paste. In the Sn–Bi/Sn–Bi solder joint, 18.75% of solder joints had 100% failure, and 15.63% of the solder joints had a partial failure. The 100%

failure decreased to 9.37%, 6.25%, and 0%, and the partial failure decreased to 7.81%, 7.81%, and 4.68% after reinforcement with 3 wt.%, 5 wt.%, and 7 wt.% epoxy resin system in the Sn–Bi solder joints, respectively.

The microstructure of the Sn–Bi/Sn–Bi solder joints and Sn–Bi/TSEP Sn–Bi-x (x = 3, 5, 7) solder joints showed the cracks were commonly initiated at the solder/Cu substrate/PCB point of intersection, and the cracks propagated along the edges of the Sn–Bi solder and the IMC layer. However, compared with the Sn–Bi/TSEP Sn–Bi-x (x = 3, 5, 7) solder joints, the copper substrates of the Sn–Bi/Sn–Bi solder joints were deformed obviously and failed earlier. The cured epoxy resin was covered and wrapped around the solder joints, which acted as an adhesive, provided mechanical resistance to the solder joints, dispersed, and released the stress produced by bending to reduce the warpage deformation of the PCB substrate during the repetitive drop impact. The more epoxy resin system that was in the flux, the better the affection was.

Therefore, compared with the Sn–Bi solder paste, the TSEP Sn–Bi-x (x = 3, 5, 7) solder pastes extended the service life of the solder joints and improved mechanical reliability. The TSEP Sn–Bi-7 solder paste had a better performance than the TSEP Sn–Bi-3 and TSEP Sn–Bi-5, but the solder pastes with higher epoxy resin system content needed a special application environment.

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