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Investigation of the Temperature Dependence of Volt-Ampere Characteristics of a Thin-Film Si_3N_4 Memristor

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Abstract: The compatibility of memristor materials with advanced complementary metal-oxide-semiconductor (CMOS) technology is a key factor for microelectronics element base manufacturing. Therefore, we continued studying previously fabricated CMOS-compatible $Ni/Si_3N_4/SiO_2/p+$-Si samples. We approximated volt-ampere characteristics (VAC) at different temperatures using the general form of the spatial charge-limiting current (SCLC) equation assuming exponential and Gaussian trap distribution within the band gap of Si_3N_4. Our approximation demonstrated better experimental data matching compared to previous work, where the approximation was based on the uniform trap distribution law. Further, we performed another additional sample measurement set of the samples to evaluate the parameters of the low-resistance state (LRS) variations at different temperatures. Analysis of these measurements allowed us to estimate the temperatures at which the samples will retain LRS for 10 years.

Keywords: memristor; silicon nitride; trap distribution; retention

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1. Introduction

Modern and widely used computing devices are based on von Neumann architectures. They have a fundamental rate limitation for data transfer between dynamic random-access memory (DRAM) and the central processing unit (CPU) or its coprocessors. The CPU and memory are mostly fabricated using the CMOS process, which is the basis of the entire microelectronics industry. To eliminate this limitation related to external DRAM, new approaches propose to relocate computations from the entire CPU directly into the memory array in order to eliminate extra data pass. The most advanced of them are in-memory computing architectures, where input data are loaded, transformed, and stored in the same memory array. Such architectures use a non-volatile ultra-high-speed element base built on new principles—ReRAM (Resistive RAM), FRAM (Ferroelectric RAM), PCRAM (Phase change RAM), and others [1,2].

The memristor is considered one of the most efficient devices for in-memory computing. It was predicted by Leon Chua in 1971 [3] and was first implemented by Hewlett Packard in 2008 [4]. It typically consists of top and bottom electrodes separated by a dielectric. In a modern interpretation [5,6], the memristive effect refers to cyclic and reversible transitions between a high-resistance state (HRS) and a LRS. Such transitions occur under the influence of both a short voltage pulse and a smooth voltage change from one range boundary to another.

Limitations of memristors are caused by the complexity of simultaneously obtaining minimum acceptable values for all consumer parameters, including stability of the resistive state in time (retention), the durability of the number of switches (endurance), bit depth,

and accuracy of their setting (plasticity), and parameters of pulse duration and amplitude during reading/writing [7,8].

Various physical effects can explain retention in memristors. When an electric field is applied to a dielectric, positive and negative charges shift. One of the mechanisms for the accumulation of such charges is various impurities. Depending on the dielectric material, its band gap may contain a set of energy levels where the charge carriers are trapped. Such trapping is due to the presence of impurities in a particular dielectric material. The further from the bottom of the conduction level the trapped carriers are, the higher activation energy is necessary for their release. Traps with energy levels located more than 1 eV below the bottom of the conduction zone are considered deep traps [9].

Therefore, impurities with deep energy levels significantly affect the concentration of trapped charge carriers, hence the operational characteristics of the memristor. These include the VAC and the HRS or LRS retention times. Determining the parameters of captured charge carriers' distribution of energy levels allows for estimating their actual concentration. Thus, the characterization of impurities with deep energy levels is a necessary technological task.

Since the beginning of the 20th century, scientists have been developing and studying various models of the charge transfer mechanism for dielectrics, and then for memristors [5,10–14]. Some of the prominent models are the Frenkel model, the Schottky model, the Hill–Adachi model, the Makram–Ebeid and Lanno models, the Nasyrov–Gritsenko model, the SCLC model, and others.

In our work, we further studied the behavior of a sandwich structure with Ni as the top electrode and a bilayer dielectric of Si_3N_4 and SiO_2 placed on a p-type silicon substrate. This structure was designed as a part of the study [13]. In [15], co-authors of this paper investigated the endurance of such structures and estimated it to be in the range of 5000–7000 resistive switching.

We noticed that in [13] some of the structural parameters obtained from the electrical response model are inconsistent. Therefore, we reviewed the electrical response model considering different trap distribution laws in the band gap. Then, we evaluated the stability of the resistive state over time. We reviewed the previously described electrical response model for $Ni/Si_3N_4/SiO_2/p+$-Si structure and proposed a new approximation model using the SCLC equation with the Gaussian distribution of traps.

The contributions of this work are as follows:

- We reviewed the previously described electrical response model for $Ni/Si_3N_4/SiO_2/p+$-Si structure and proposed a new approximation model using the SCLC equation with a Gaussian distribution of trap states;
- Using the mean absolute percentage error (MAPE) algorithm, we showed that the new approximation model provides a better experimental data fit;
- We calculated and analyzed the Gaussian distribution of trap states at different temperatures for the LRS and HRS of the studied structure;
- We measured memristor resistance over time at different elevated operating temperatures and evaluated conditions for 10-year LRS retention.

The paper content is organized as below. The Section 2 briefly provides the related research on the SCLC model, laws of distribution of trap states, and operation-specific memristors. The Section 3 includes a brief description of the fabricated structure. Then, the parameters of the SCLC model and expressions for the exponential and Gaussian law of trap distribution in the band gap were provided. To estimate the retention time of the LRS, Arrhenius's law was chosen, and the temperature-dependent LRS resistance variation with time was determined. The Section 4 includes the approximation of VAC with consideration of the exponential and Gaussian law of trap distribution in the LRS and HRS of the memristor. An estimation of temperature conditions for LRS retention over 10 years was conducted as well. Finally, the Section 5 summarizes our research and includes an idea for further investigation.

2. Related Work

Its state retention capability makes the memristor an important element in hardware computing. On the one hand, a memristor can function as a memory cell. In this case, HRS and LRS are interpreted as logical 0 and 1. The transition processes from HRS to LRS and vice versa (*SET* and *RESET*) are called resistive switching.

On the other hand, the memristor limits the current flowing through it. In this case, the memristor serves as the electrical counterpart of the synaptic weight in calculating the output of the artificial neural network. Preserving the resistive state allows applying memristors in crossbars to simulate synaptic weights. After weighing the input voltage at the memristor, the current is summed with similar ones from parallel circuits in a crossbar column. By Ohm's and Kirchhoff's laws, a matrix multiplication may be performed directly in the neural network [16–18].

In order to build a model that predicts memristor behavior we examined the electrical characteristics of fabricated memristive structures and tried to match them with mathematical descriptions. Such mathematical models are applied to analyze the performance of a memristor. If the memristor meets the requirements, this mathematical model is used in computer-aided design (CAD) software for circuit development.

However, before analyzing the memristor function mathematically, it is necessary to determine the physical principles of its operation. There are currently two main hypotheses about mechanisms responsible for resistive switching in memristors. The diffusion of active electrode ions or oxygen vacancies in the dielectric explains the filamentary mechanism in the LRS state. During the transition to HRS, the filament is reversibly destroyed by thermal effects. In the non-filament mechanism, the conductive channel is implemented through localized states in the dielectric. One version of this mechanism is the filling (trapping) and emptying (detrapping) of trap centers (Figure 1) [19,20].

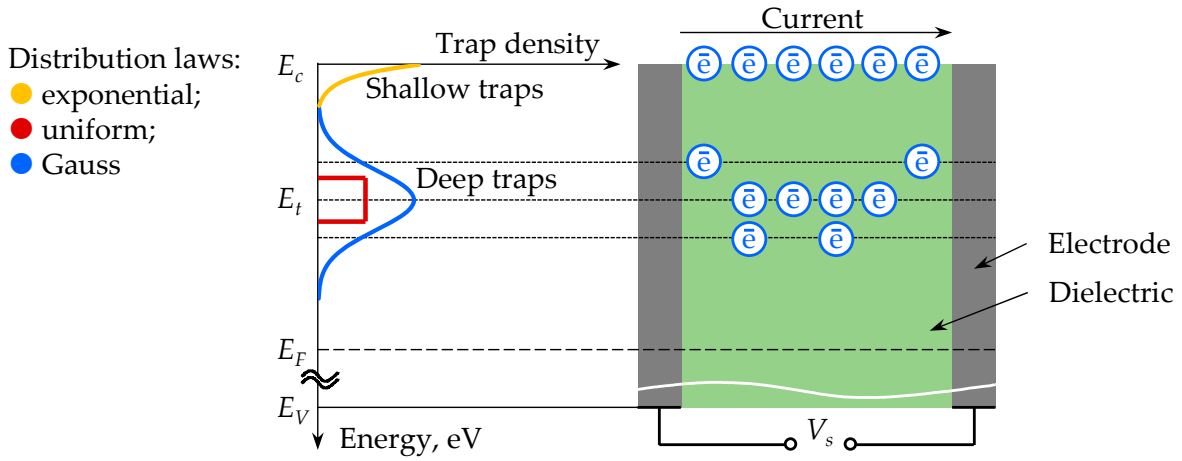

Figure 1. A simplified diagram to explain electron trapping. E_c—the bottom of the conduction band; E_t—activation energy of deep traps; E_F—Fermi level; E_V—the top of the valence band. V_S is the voltage applied to the electrodes of the structure. The energy range between EC and EV is called the band gap (E_g). The energy levels for shallow traps as well as hole trapping are not shown.

Traps are impurities and structural defects that capture charge carriers during charge transfer [21]. The charge carriers are electrons and holes. Figure 1 shows a combined and simplified representation of the energy diagram and structure of an electrode-dielectric-electrode memristor. Electrons provide the electric current when voltage is applied to the memristor. Their energy level is equal to the conduction energy E_C, which we take as the zero point of reference.

Traps in a dielectric can be located at different energy levels. The so-called activation energy is the minimum required to release a carrier from the trap into the conduction zone. Traps are considered deep traps if the activation energy is greater than 1 eV; otherwise, they

are called shallow traps. Since the traps are located at several adjacent energy levels, the distribution of the traps over the levels can be described by the known distribution laws.

For example, the shallow traps may be mostly located near the E_c level, with their number at each successive energy level decreasing according to an exponential distribution law. Therefore, both the capture and release of charge carriers by such traps require less energy than in the case of deep traps. Deep trap levels can be distributed across energy levels around the central value of E_t according to a Gaussian law or an exponential law [19]. Releasing charge carriers from deep traps requires more activation energy than releasing them from shallow traps. Therefore, to improve the retention of resistive states, materials with the highest concentration of deep traps should be selected.

Dielectric materials contain very few free charge carriers. The conductivity of such materials is managed by the injection of free carriers. Excess charge carriers create a space charge that affects the current flow through the dielectric. This current is called the space charge limited current (SCLC). Mott and Gurney were the first to derive the SCLC model for trap-free dielectrics. Later, various authors enhanced the SCLC model to account for traps present in dielectric materials. When traps are occupied with the injected carriers, as expected, the current density is lower than in the trap-free case. The shape of VAC varies depending on the trap state distribution in the band gap [22,23].

The CMOS process is the basis of modern microelectronic manufacturing [24]. Therefore, it is important to use compatible materials in memristor development [25,26]. Silicon oxide SiO_2 and silicon nitride Si_3N_4 are dielectrics widely used in this technology [9].

The electronic structure of these dielectrics has similar well-studied memristive properties that allow the materials to be applied as memristive functional layers. Silicon oxide has a low trap concentration, whereas silicon nitride has a high level of electron and hole trap concentration ($\approx 10^{19}$ cm^{-3}) [17]. The trap energy in Si_3N_4 is concentrated in the range of 1 . . . 1.5 eV and is shifted to the conduction zone [9]. Deep traps in the dielectric layer of Si_3N_4-based memristors provide an information storage time of about 10 years at a temperature of 358,15 K (85 °C) [17].

Numerous papers [18,27–29] describe various applications of SiO_2, Si_3N_4, and non-stoichiometric SiNx for memristor fabrication. In some cases, SiO_2 was not used, and silicon nitride thicknesses ranged from about 30 nm in thick films up to about 5 nm in thin film samples. To achieve resistive switching in thick film devices, it is necessary to use bipolar voltage with an amplitude of about ±20 V. Such voltage is not applicable in practice; however, the obtained results are easily scalable to the case of thin films. In addition, the performance of memristors depending on different top electrode materials has been extensively investigated [5,13,27,30].

The analysis of memristive devices allows us to distinguish the following states [6]: the virgin (pristine) state, LRS, and HRS after fabrication. In some cases, an intermediate state between LRS and HRS was also observed [5,6]. With the application of voltage, the state of the memristor changes. The irreversible transition from the virgin (pristine) state to LRS or HRS is called the electroforming or forming process. VAC is used to represent these processes [15,31], using the decimal logarithm of the absolute value of the current.

There are three basic types of resistive switching [1]: unipolar, bipolar, and threshold. In the case of unipolar switching, the VAC is symmetrical concerning the polarity of the applied voltage, so set and reset can occur at the same polarity. The forming voltage is usually higher than the LRS and HRS junction voltages. After forming, the memristor switches to the LRS state. The threshold switching memristor also has a symmetrical VAC, but the LRS is only maintained when the bias voltage is applied. In bipolar switching memristors, the waveform is asymmetrical to the applied voltage, so a bipolar voltage is required. After forming, a bipolar switching memristor can switch to either LRS or HRS [6]. The maximum device current is limited to prevent irreversible dielectric breakdown.

Memristors made in the form of metal-insulator-metal (MIM) structures can be integrated directly into the multilayer metallization system, such as HfO_2-based memristors [32]. Memristors can be built on metal-insulator-semiconductor (MIS) structures as

well. The implementation of a monocrystalline semiconductor layer in a multilayer metallization structure of an integrated circuit is unlikely. Therefore, memristors of this type are fabricated on semiconductor substrates. Arrays of such memristors can either be fabricated as a part of the processor itself or formed on a silicon interposer for 2.5D integration or on a separate silicon substrate for subsequent 3D integration. [33].

3. Materials and Methods

3.1. Fabrication of the Ni/Si_3N_4/SiO_2/p+-Si Structure

The Ni/Si_3N_4/SiO_2/p+-Si structure considered in this paper was presented earlier in the article [13] (Figure 2). With the consent of all authors, we used their data for further analysis and samples for additional measurements. Below is the summary of the structure fabrication process.

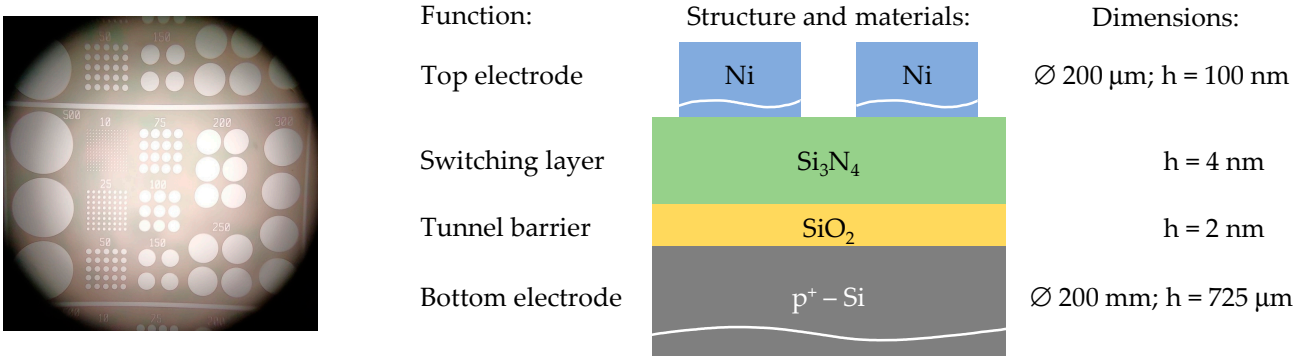

Figure 2. Photo of the manufactured samples and their sketches.

A silicon p-type substrate with a resistivity of 0.005 Ohm·cm was used. Then, a 2 nm thick SiO_2 layer was formed by thermal oxidation. Next, a 4 nm thick Si_3N_4 film was formed by low-pressure chemical vapor deposition (LPCVD) with a mixture of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) in a ratio of 1:3 and at 700 °C.

A highly doped p+-type layer was formed in a silicon substrate. First, ion implantation with heavy boron difluoride BF_2^+ ions with an energy of 40 keV and a dose of 8×10^{14} cm^{-2} through the previously obtained dielectric layers was performed. Then, the impurity was activated by rapid thermal anneal performed at 1030 °C. Finally, the top Ni electrodes were deposited using a thermal evaporator through a shadow mask.

3.2. The SCLC Model and Laws of Trap Distribution for the VAC Approximation

In [13], one of the co-authors of this paper used the Cascade Summit 12000B-AP probe station (Cascade Microtech, Beaverton, OR, USA) and Agilent B1500A semiconductor analyzer (Keysight Technologies, Santa Rosa, CA, USA) and then obtained the following results for the investigated structure:

- The absence of the need for a forming operation;
- Reproducible bipolar switching (Figure 3a);
- VACs measurement at temperatures of 298.15 K, 348.15 K, and 398.15 K (Figure 3b);
- VAC approximation using the SCLC model with uniform distribution of traps [10] described by following Equations (1)–(4);
- Structure parameters obtained from the approximation, including the effective radius of 100 µm in HRS and 46 nm in LRS.

$$I_{Uni} = I_{Ohm} + I_{SCLC} = Se\mu n\frac{U}{d} + S\frac{9}{8}\mu\varepsilon\varepsilon_0\theta\frac{U^2}{d^3}, \quad (1)$$

$$n = \frac{2N_d}{1+\sqrt{1+\frac{4gN_d}{N_c}exp\left(\frac{E_a}{kT}\right)}}, \quad (2)$$

$$N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2}, \tag{3}$$

$$\theta = \frac{1}{1 + \frac{N_t}{N_c} exp\left(\frac{W_t}{kT}\right)}, \tag{4}$$

where I_{Ohm} is the ohmic current, I_{SCLC} is the *SCLC* current, S is the area involved in charge transfer, e is the charge of an electron, μ is the electron mobility, U is the applied voltage, d is the dielectric thickness, ε is the static dielectric constant, ε_0 is the vacuum permittivity, n is the free electron concentration inside the dielectric layer, N_d is the concentration of donors, g is the degeneracy coefficient, E_a is the donor activation energy, k is Boltzmann's constant, T is temperature, m^* is the effective mass of the electron, h is Planck's constant, θ is the free charge carrier fraction of all injected carriers (free and trapped), N_t is the trap concentration, N_c is the effective density of states, and W_t is the trap energy.

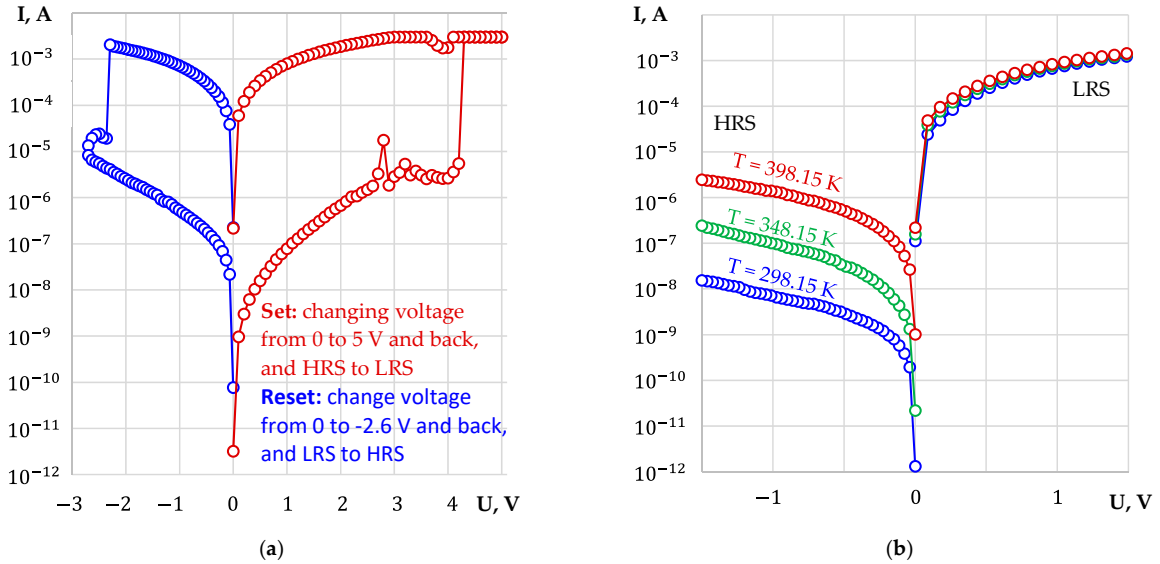

Figure 3. VACs of memristors: (**a**) VAC of one of the switching cycles at room temperature; (**b**) VACs at three temperatures for HRS and LRS.

The current is determined by current density multiplied by the effective area in charge transfer S. The effective area of a circular shape is characterized by its effective radius. Reducing the effective radius leads to a resistance increase. The effective radius in the HRS must be smaller than in the LRS. The results in [13] are not consistent with this statement. Therefore, we had to refine the approximation model by considering the exponential and Gaussian distribution of traps for the SCLC model [14,34].

We multiplied the area involved in the charge transfer by the current density from [22] to obtain the current value (5). It is possible to obtain the distribution parameters for the exponential and Gaussian laws after calculating the parameter l using Formulas (6) and (7).

$$I_{Gau,Exp} = Se^{(1-l)}\mu N_c \left(\frac{2l+1}{l+1}\right)^{l+1} \left(\frac{l\varepsilon\varepsilon_0}{(l+1)N_t}\right)^{l} \frac{U^{(l+1)}}{d^{(2l+1)}}, \tag{5}$$

$$l_{Exp} = \frac{T_c}{T}, \tag{6}$$

$$l_{Gau} = \sqrt{\frac{2\pi}{16}}\frac{\sigma_t}{kT}, \tag{7}$$

where l—is the parameter that is equal to l_{Exp} in the case of exponential distribution and l_{Gau} in the case of Gaussian distribution, T_c—is a temperature parameter that characterizes the exponential trap distribution, the so-called "Characteristic Temperature of Trap Distri-

bution", and σ_t—is the standard deviation of the Gaussian distribution. This Equation (5) at $l = 1$ looks like I_{SCLC} in (1) for the uniform law, but uses the multiplier N_c / N_t instead of θ.

In [5], it is determined that in the case of high voltages for HRS and the exponential law of the trap distribution, the current I is presented by the sum of Equations (1) and (5). At that, N_c is applied instead of N_t in the denominator of Equation (5).

In Section 4.1, we approximated the VAC branches in Figure 3b using expression (5) by adjusting the effective radius and the parameter l, which determines the slope angle of the approximated VAC. Then, using MAPE, we selected the more accurate version of the approximation from those calculated by expression (1) and expression (5).

3.3. Determining the State Retention Time for LRS

There are various methods for estimating the storage time of the resistive states that do not require significant time expenditure. A common and well-proven method [35] uses the Arrhenius Equation (8), which involves testing the sample at elevated temperatures.

$$t \propto exp\left(\frac{E_a}{kT}\right) \tag{8}$$

Here, the time t is proportional to the exponent of the activation energy E_a of the processes in the resistive-switching memory devices, k is the Boltzmann constant, and T is the device temperature.

A common way to assess retention is to heat the structure to a high temperature (up to 730 K, for example), which it can withstand, for example, for a day or more [36]. Resistance is measured for the duration of high-temperature exposure until the point of structural failure. The next sample is then tested at a temperature that was changed by a certain amount. The result is a family of resistance versus time plots, each plot at a particular constant temperature.

We performed similar measurements at 563.15 K, 543.15 K, and 532.15 K (Figure 4). However, instead of waiting for the sample to fail, we noted time points at which the resistance of the sample increased by 5% and 10% of the readings at the initial moment. In Figure 4, the initial and increased resistance values R_0 are shown by the green dashed lines. The six points of intersection of the resistance vs. time plots with these lines are marked by squares indicating the corresponding time. In Section 4.2, we used the six points in Figure 4 and Arrhenius equation to assess the LRS retention over 10 years.

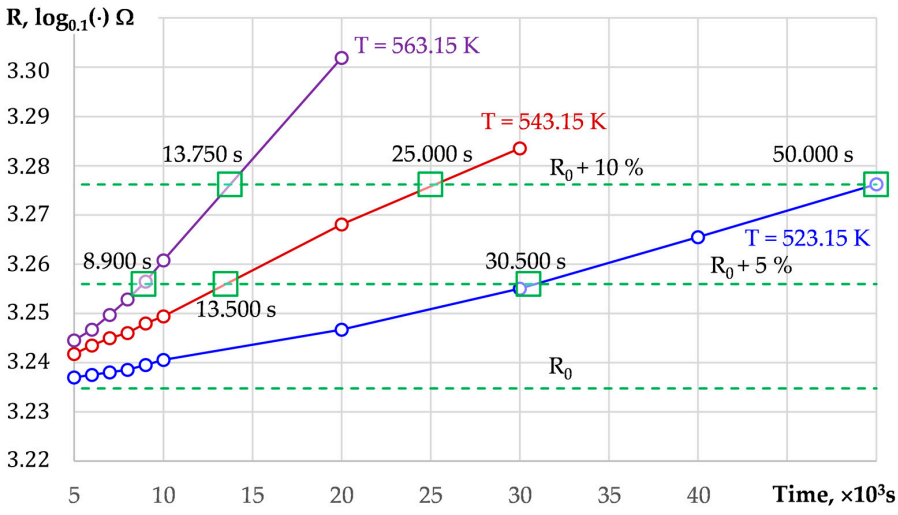

Figure 4. The time dependence of resistance at LRS and high temperatures.

4. Results and Discussion

4.1. Approximation of the VACs with the SCLC Model in the Case of Exponential and Gaussian Laws of Trap Distributions

Let us consider applying expression (5) to approximate the VAC in the case of a circular section $S = \pi r^2$, where r is the effective radius of the conductive zone between the top and bottom electrodes. The rest of the parameters for the calculation are taken from [13]: $d = 4$ nm; $\varepsilon = 7$; $m^* = 0.5 \cdot m_e$, where m_e is electron mass; $\mu_{HRS} = 2.5 \cdot 10^{-4}$ cm^2/(V·s); $\mu_{LRS} = 1 \cdot 10^{-4}$ cm^2/(V·s); $E_{aHRS} = 1.456 \cdot 10^{-19}$ J; $E_{aLRS} = 0.064 \cdot 10^{-19}$ J; $W_t = 0.8 \cdot 10^{-19}$ J; $g = 2$; $N_{dHRS} = 1 \cdot 10^{25}$ m^{-3}; $N_{dLRS} = 7 \cdot 10^{25}$ m^{-3}; $N_t = 5 \cdot 10^{24}$ m^{-3}.

We used the simplex search method [37] to obtain the closest fit of the VAC to the experimental data. In [5], it was stated that the VAC can be approximated by the sum of expressions (1) and (5). We performed such calculations. For HRS the obtained three terms have orders of 10^{-31}, 10^{-13}, and 10^{-6}, respectively. The first two terms are negligible and may be omitted. For the LRS, the approximation function with the three terms does not fit the experimental VAC. In this case, even at $l = 0$, the graph does not rotate by an angle sufficient to fit the VAC. Therefore, we used expression (5) without taking into account expression (1) to approximate the VAC.

Using the MAPE algorithm [38], we calculated the errors of our approximation for expression (5) $\text{MAPE}_{\text{Gau,Exp}}$ and the approximation from [13] for expression (1) MAPE_{Uni} (Table 1). For all six VACs, the approximation error of $\text{MAPE}_{\text{Gau,Exp}}$ is at least 53 % less than MAPE_{Uni}, and therefore our approximation is more accurate.

Table 1. Values of calculated parameters for $I_{Gau,Exp}$ and comparison of approximation accuracy with I_{Uni}.

Resistance State	**HRS**			**LRS**		
***T*, K**	**298.15**	**348.15**	**398.15**	**298.15**	**348.15**	**398.15**
parameter l	0.1996	0.4587	0.2837	0.4652	0.3158	0.2485
effective radius r nm	0.15	0.40	1.54	58.09	63.34	63.24
$\text{MAPE}_{\text{Gau,Exp}}$, $\times 10^4$	54	56	41	61	63	59
MAPE_{Uni}, $\times 10^4$	115	220	101	341	257	248
Improvement of $\text{MAPE}_{\text{Gau,Exp}}$ compared to MAPE_{Uni}, %	53	75	59	82	75	76

Note that in HRS the effective radius r at different temperatures is around 1 nm, while in LRS the parameter r is about 60 nm. As noted above, the effective radius for HRS must be smaller than the LRS. From this point of view, our values are adequate. Our value of the effective radius for LRS is in agreement with the value from [13]. The effective radius value of 100 μm obtained in [13] for HRS should be replaced by our value of 1 nm.

Further calculation of the distribution law parameters can be performed using expressions (9) and (10) [39,40] calculated as T_c and σ_t (Table 1).

$$D_{tGau}(E) = \frac{N_t}{\sqrt{2\pi\sigma_t}} exp\left[-\frac{[E-(E_c-E_t)]^2}{2\sigma_t^2}\right], \quad (9)$$

$$D_{tExp}(E) = \frac{N_t}{kT_c} exp\left[-\frac{(E_c-E)}{kT_c}\right], \quad (10)$$

where D_{tGau}, D_{tExp} are the Gaussian and exponential distributions of trap states, E is the considered energy, E_c is the energy of the conduction band, and E_t is the center of trap distribution.

Figure 5 shows the Gaussian distribution of trap states at different temperatures for LRS and HRS according to (9). With increasing temperature, the parameter reflecting the slope of the VAC decreases (Table 1). Thus, according to Ohm's law, the resistance of our structure decreases with increasing temperature. Consequently, the maximum of the

Gaussian distribution of trap states grows (Figure 5a), and trap states tend to occupy energy levels as close to the level as possible.

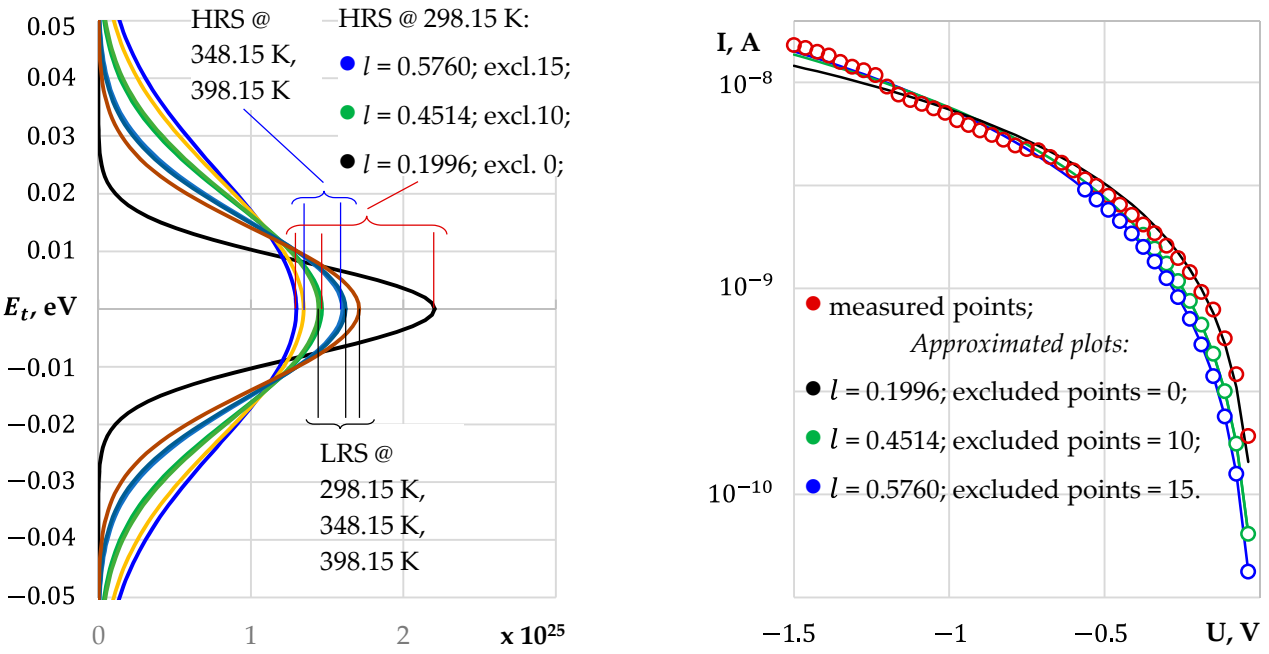

Figure 5. Gaussian distribution of trap states at different temperatures for LRS and HRS. For LRS, an increase in temperature leads to an increase in the maximum of the probability density function (**a**). For HRS, this temperature dependence is expected but not present. The black plot maximum for 298.15 K exceeds the yellow plot maximum for 348.15 K. Examining the approximation plot (black) and the experimental plot (red dots), we see the need to rotate the VAC clockwise (**b**). Excluding the first 10 experimental data points in the low-voltage region gives green plots in (**b**,**a**) with $l = 0.4514$. Excluding the first 15 experimental data points gives $l = 0.5760$. This results in a reduction in the distribution maximum to the acceptable value (blue plots in (**a**,**b**)). The reason for this effect is explained in the text.

Therefore, as the temperature increases, the maximum of the Gaussian distribution of trap states in the HRS state should also increase similarly to the LRS. Figure 5a shows that this dependence holds for temperatures 348.15 K and 398.15 K. The maximum for 298.15 K should have a smaller value than the maximum for 348.15 K, but it is almost two times greater than expected.

To find the cause, we considered the approximation plot (Figure 5b). Red circles represent the experimental data; a solid black curve represents the approximation with $l = 0.1996$ (Table 1). Increasing the slope of the approximation VAC will reduce the discrepancy with the experimental data. Comparing the red and black curves, we can assume that the slope of the approximated VAR is smaller than the slope of the experimental VAC in the range $-1.5 \ldots -1.0$ V. Obviously, the limiting factor is the experimental data points in the low voltage region.

The exclusion of 15 experimental points gives $l = 0.5760$ and increases the slope of the VAC for 298.15 K. Thus, the maximum for this temperature (blue curve in Figure 5a) is now smaller than the maximum for 348.15 K. The plot shows the growth of the maxima for HRS with increasing temperature, which is consistent with the similar dependence for LRS.

The need to exclude the low voltage experimental data points at 298.15 K is justified as follows. Of all the six branches of the VAC (Figure 3b), this branch belongs to the region of highest resistance, especially in the low voltage range of 0 . . . −0.5 V. The discrepancy between the experimental values and the approximation could be interpreted by the presence of transient resistance at low voltage levels and low (room) temperature for HRS. The resistance in LRS is significantly lower (difference in effective conductor area radius 0.15 and ~60 nm) than in HRS, so the effect of transient resistance at the same temperature and voltage does not affect the final VAC.

The exclusion of points from the low voltage range of the experimental VAC for HRS at 298.15 K allowed us to obtain refined parameters of the sample: VAC slope parameter $l = 0.5760$, effective radius $r = 0.11$. These updated values should be used instead of those given above for HRS at 298.15 K in Table 1.

Figure 5a shows the probability density distribution in the case of the exponential law for six cases according to Table 2. It follows from the expression (10) that the maximum of the distribution function is at the energy level of the conduction band E_c. This means that in our case the exponential law applies to shallow traps.

Table 2. Parameters for the Gaussian and exponential laws.

Resistance State	**HRS**			**LRS**		
***T*, K**	**298.15**	**348.15**	**398.15**	**298.15**	**348.15**	**398.15**
Distribution maximum $D_{tGau}(E)$, $\times 10^{25}$	1.298	1.346	1.601	1.444	1.622	1.710
σ_t for the Gaussian law	0.0236	0.0220	0.0155	0.0191	0.0151	0.0136
Distribution maximum $D_{tExp}(E)$, $\times 10^{30}$	9.964	9.265	6.554	8.048	6.380	5.741
T_c for the exponential law	171.73	159.68	112.95	138.71	109.95	98.94

However, as mentioned in the Section 2 of this paper, the trap energy in Si_3N_4 is concentrated in the 1 . . . 1.5 eV energy range and is shifted towards the conduction band. Therefore, in our case, the distribution of deep traps is described by a Gaussian law, as shown in Figure 5b.

4.2. Estimation of Temperature Conditions That Allow 10-Year Retention of LRS

In Section 3.3 we obtained six data points from the resistance vs. time plot, where the resistance of a room temperature memristor increases by 5% or 10% when the sample is heated to 563.15 K, 543.15 K, and 532.15 K. Applying a natural logarithm to the Arrhenius Equation (5), these points are plotted on the $\ln(t)$ vs. $1/kT$ plot (Figure 6). Further, we used linear regression to extrapolate two dependencies for R_0 + 5 % and R_0 + 10 % and obtain the values of temperature corresponding to t = 10 years. The linear regression parameters are as follows:

- A slope factor of 0.8197 with an offset of −7.3716 (approximation reliability value R^2 = 0.9995) for a 5 % change in resistance;
- A slope factor of 0.7845 with an offset of −7.1326 (approximation reliability value R^2 = 0.9735) for 10% change.

The regressions yield two temperature values, 373.15 K and 386.15 K. These are the temperatures at which it will take 10 years for the resistance to change by 5% and 10%. The 5% and 10% variation in resistance does not affect the ability to distinguish between memristor resistance states. Therefore, we estimated the retention of the memristor to be at least 10 years if it operates at temperatures that do not exceed 386.15 K. These results are consistent with retention parameters of similar Si_3N_4-based structures [17].

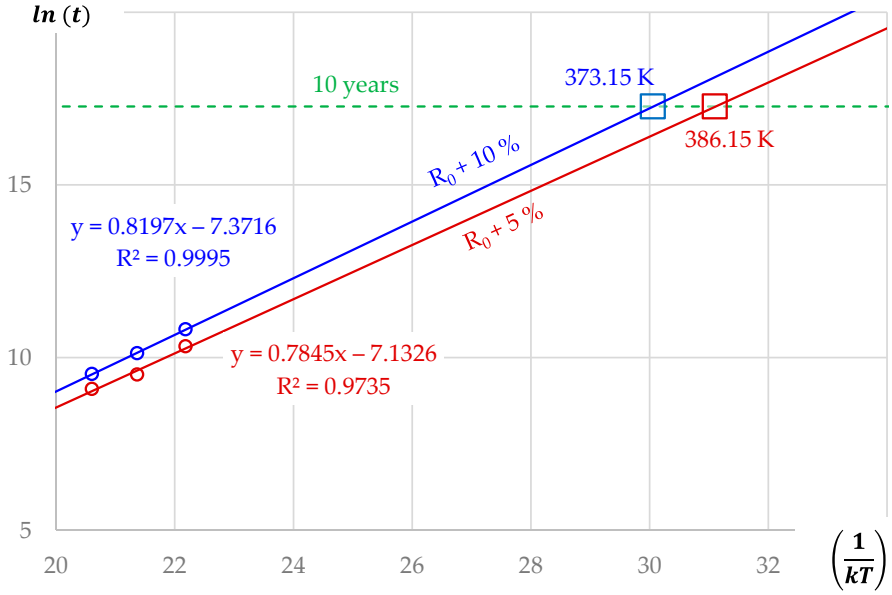

Figure 6. Estimation of temperature conditions that allow 10-year retention of LRS.

5. Conclusions

Studying our fabricated memristor samples with $Ni/Si_3N_4/SiO_2/p+$-Si structure, we determined that using the Gaussian distribution of trap states in the SCLC model provides a better experimental data fit and adequate structure parameters. We refined our earlier results and demonstrated up to 53% better MAPE results for VAC current approximation. The approximation results allowed us to establish the effective conductive radius at different temperatures at 1 and 60 nm for HRS and LRS correspondingly. Further, we took additional measurements and studied the change in LRS with time at high temperatures in the 523.15 . . . 563.15 K range. We estimate that in 10 years the resistance in LRS would change by 5% at 373.15 K (100 °C) and by 10% at 386.15 K (113 °C).

As mentioned in related work, preserving the resistive state allows applying memristors in crossbars to simulate synaptic weights. The retention value of memristors we studied is comparable to the life cycle of a processor. The endurance is 5000–7000 resistive switching times, which is suitable for applications with a limited number of synaptic weight changes during the life cycle. Such memristors can be used in a simple processor to detect an activation phrase in speech because this phrase is not usually changing. Further work may lie in finding ways of integrating the memristors into the crossbar and interfacing with the CMOS control circuitry.

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