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The Impact of Hysteresis Effect on Device Characteristic and Reliability for Various Fin-Widths Tri-Gate $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric FinFET

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Abstract: In this study, we developed a facilitated ferroelectric high-k/metal-gate n-type FinFET based on $Hf_{0.5}Zr_{0.5}O_2$. We investigated the impact of the hysteresis effect on device characteristics of various fin-widths and the degradation induced by stress on the ferroelectric FinFET (Fe-FinFET). We clarified the electrical characteristics of the device and conducted related reliability inspections. For the Fe-FinFET, the hysteresis behavior of the $Hf_{0.5}Zr_{0.5}O_2$-based gate stack in the Si-fin body is apparent, especially at narrower fin-widths, which affects device performance and reliability under voltage stress. The gate ferroelectric film is worsened after voltage stress with higher impact ionization, resulting in hysteresis degradation and serious induced device performance degradation. It is suggested that the hysteresis degradation is caused by both a shift in polarization of the gate ferroelectric film and generation of interface traps after high-energy carrier stress, which was confirmed by crystal structure inspection.

Keywords: FinFET; ferroelectric; hysteresis; reliability

Citation: Zhang, W.-Q.; Wu, P.-T.; Lin, Y.-H.; Yang, Y.-L. The Impact of Hysteresis Effect on Device Characteristic and Reliability for Various Fin-Widths Tri-Gate $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric FinFET. *Crystals* **2023**, *13*, 628. https://doi.org/10.3390/cryst13040628

Academic Editor: Artem Pronin

Received: 16 March 2023
Revised: 1 April 2023
Accepted: 3 April 2023
Published: 6 April 2023

1. Introduction

Since the negative capacitance property of $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based ferroelectric materials was proposed in 2008 [1], ferroelectric field-effect transistors (Fe-FETs) have been extensively researched and come to be considered to be highly viable options for low-power-consumption logic devices with low-operating voltage requirements. The reason Fe-FETs are able to overcome physical limitations is due to the negative capacitance property of the ferroelectric layer, which can display a subthreshold swing (SS) of less than 60 mV/decade through dipole switching and arrangement [2–6]. In comparison to conventional MOSFETs, a lower threshold voltage (V_{TH}) can be achieved for Fe-FETs with an ultrasteep SS, which leads to a reduction in the applied voltage (V_{DD}) for a given gate overdrive voltage ($V_G - V_{TH}$) [7–9].

In order to meet performance requirements and address the limitations of planar bulk transistors when scaling down to sizes below 22 nm, the semiconductor industry has developed new technologies such as the fin field-effect transistor (FinFET) [10]. The FinFET is considered the most promising candidate for replacing traditional planar bulk devices beyond the 22 nm technology node, owing to their excellent performance in reducing leakage current and improving short channel behavior [11,12]. The primary difference in geometry between a planar MOSFET and a FinFET is that the FinFET device has a non-planar 3D structure. The Si-bulk fin can be covered on three sides by a high-k/metal gate, while the fin-width can be made very thin to minimize the device's short channel effect. Tri-gate FinFET devices have been developed using different gate stacks, such as Poly-Si/SiON or high-k/metal gate, on bulk-Si substrate [13–15]. However, in order to further improve their performance, alternative materials and designs are being explored.

Ferroelectric FinFETs (Fe-FinFETs) are an emerging type of transistor that combines the unique properties of ferroelectric materials with the high performance of FinFETs. Fe-FinFETs have been shown to exhibit improved device performance, such as faster switching speeds and reduced power consumption, compared to conventional FinFETs. Among these, Fe-FinFET is a promising option for upcoming applications due to its unique ferroelectric properties [16,17].

A comprehensive understanding of reliability physics is a crucial requirement for the successful commercialization of this promising technology. Hot carrier injection (HCI), which is a well-known reliability issue in modern MOSFET technology, is of great interest due to its important role in device reliability. HCI occurs when high-energy electrons or holes are injected into the gate oxide of a transistor, which can lead to changes in the device's electrical characteristics over time. Recent studies have shown that HCI can accelerate the degradation of gate oxide in FinFETs, leading to a further reduction in device performance and reliability [18,19]. It is even more severe in FinFETs due to the higher probability of carrier capture in the tri-gate structure and the higher density of available Si-H bonds at (110) fin sidewalls. Except HCI, positive biasing temperature instability (PBTI) is also another reliability issue for FinFET devices. PBTI-induced high electric field effects can result in gate oxide degradation and alter the threshold voltage and subthreshold swing (SS) of the device. [20]. Both HCI and PBTI will affect the Si/interfacial layer (IL) interface of Fe-FinFET devices. The quality of the interface between Si and IL is a crucial factor that impacts the hysteresis phenomenon and device performance of Fe-FinFETs [21]. However, the effect of hysteresis on the reliability characteristics for Fe-FinFETs remains understudied, and there is little research on the relationship between hysteresis and the reliability of Fe-FinFETs.

In this work, the impact of hysteresis on voltage stress-induced device degradation for n-type Fe-FinFETs was investigated. Our findings suggest that the degradation of Fe-FinFETs due to voltage stress-induced device degradation will be more severe because of the deterioration of the hysteresis of the gate ferroelectric film under hot carrier stress, particularly in devices with narrower fin-widths. The primary cause of hysteresis degradation is attributed to the degradation of the Si/IL interface. Furthermore, we observed that after voltage stress with higher impact ionization, which mainly occurs in narrower Si-fin channels, the gate ferroelectric film undergoes severe carrier ion bombardment, resulting in changes in the crystal structure with high hysteresis.

2. Materials and Methods

N-type tri-gate FinFETs were fabricated on SOI wafer with a film thickness of 20 nm. Si film was etched at first to form the Si-fin for oxidation and etch steps. The silicon film was etched to form thin silicon fins with widths from 20 nm to 400 nm and channel lengths from 20 nm to 40 nm, as shown in Figure 1a. B ions were implanted into the Si-fins to form p-well regions for N-type tri-gate FETs. The gates were formed using a replacement metal gate (RMG) process with gate length scaling down to 20 nm. The gate stack shown in Figure 1b includes a 0.6 nm interfacial layer of SiO_2 grown by thermal oxidation, a ferroelectric layer deposited by ALD at 250 °C and 5 nm $Hf_{0.5}Zr_{0.5}O_2$ followed by TaN and TiN stack metal film deposition as the gate electrode. The gate insulator effective oxide thickness (EOT) was 1.0 nm. A nickel self-aligned silicidation approach was implemented to reduce the contact resistance between the metal and silicon, followed by a standard tungsten-plug filling process and copper metallization as an interconnection backend. The real fabricated Fe-FinFET structure has a thin (5 nm) ferroelectric layer formed uniformly around Si-fin with a fin-width of 20~400 nm. The electrical characteristics of devices, hot carrier stress and negative/positive biasing-induced instability were evaluated using an Agilent B-1500A semiconductor analyzer. Stress conditions of V_{GS} = 2.3~2.7 V and V_{DS} = 0~2.7 V were utilized in this work.

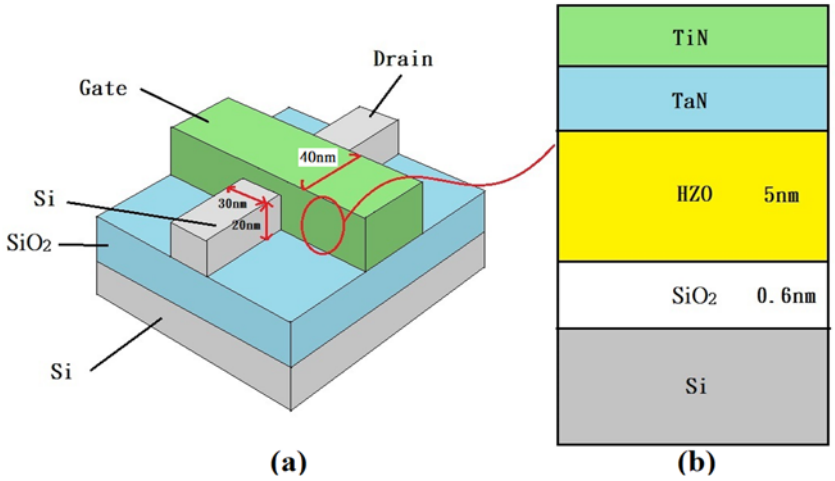

Figure 1. (**a**) Schematic diagram of tri-gate ferroelectric FinFET structure, and (**b**) the related gate stack picture of this fabricated ferroelectric FinFET.

3. Results

Figure 2 shows (a) I_D-V_G characteristics and (b) transconductance for various fin-widths of n-type Fe-FinFET. Better subthreshold swing but lower drive current could be observed for the narrower fin-width Fe-FinFET. Based on our observations, it was found that decreasing the fin-width of the Fe-FinFETs resulted in an improvement of the subthreshold swing, while simultaneously causing a reduction in the drive current. The obtained result implies that the subthreshold behavior of Fe-FinFETs can be managed by reducing the fin-width. Nevertheless, the reduction in the effective channel width resulted in a corresponding decrease in the drive capability. When the gate voltage sweep is performed from negative to positive, the measured I_D-V_G curve is referred to as forward (FWD) sweep. Conversely, the sweep from positive to negative is referred to as reverse (RVS) sweep. In this work, the hysteresis value is defined as $V_{TH,RVS}$-$V_{TH,FWD}$. A positive hysteresis value indicates that the device exhibits clockwise hysteresis, which is suggested to be caused by electron trapping from the channel. Conversely, a negative hysteresis value indicates counterclockwise hysteresis, which is attributed to the ferroelectric response [22]. Furthermore, it was observed that the devices with narrower fin-width exhibited a larger hysteresis window, indicating a higher density of interface traps.

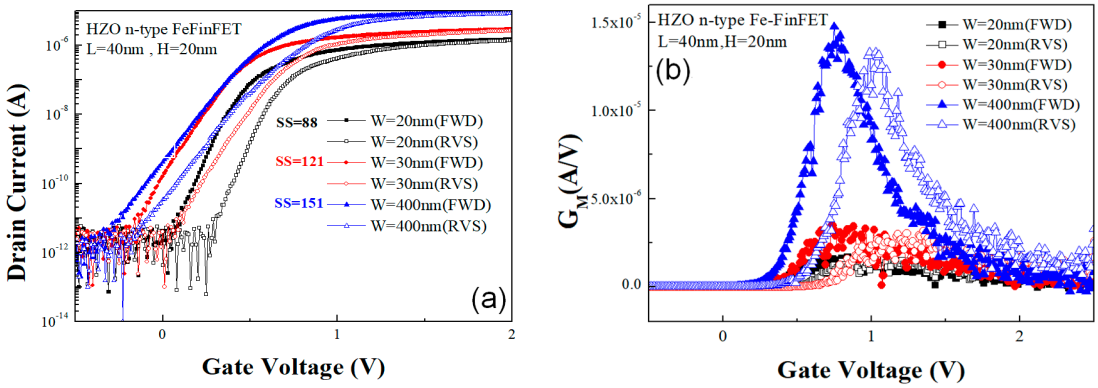

Figure 2. (**a**) I_D-V_G characteristics and (**b**) transconductance for various fin-widths of n-type Fe-FinFET.

To assess the impact of hot carrier injection-induced stress on Fe-FinFETs, the devices were subjected to a stress condition with $V_G = V_D = 2.3$ V for a duration of 5000 s. Figure 3a,b illustrate the I_D-V_G characteristics and transconductance, respectively, both pre- and post-HCI stress. Following hot carrier stress, the device with a narrower fin-width demonstrated the most severe subthreshold and transconductance degradation. Conversely, we noted that

the narrower fin-width Fe-FinFET displayed a more pronounced V_{TH} shift compared to its larger fin-width counterpart, which suggests an increase in the gate ferroelectric hysteresis as the fin-width decreased. It is suggested that a narrower Fe-FinFET results in more significant carrier ion bombardment to the gate ferroelectric film, leading to an increase in the hysteresis effect of the ferroelectric film and ultimately degrading its driving capability. During hot carrier stress, the strongest impact ionization occurs on a narrower fin-width Fe-FinFET, causing interface state generation and resulting in severe SS degradation. In fact, the most significant degradation was observed in 20 nm fin-width devices. Furthermore, this stress-induced device degradation is worsened in narrow fin-width Fe-FinFET due to the more serious gate ferroelectric hysteresis.

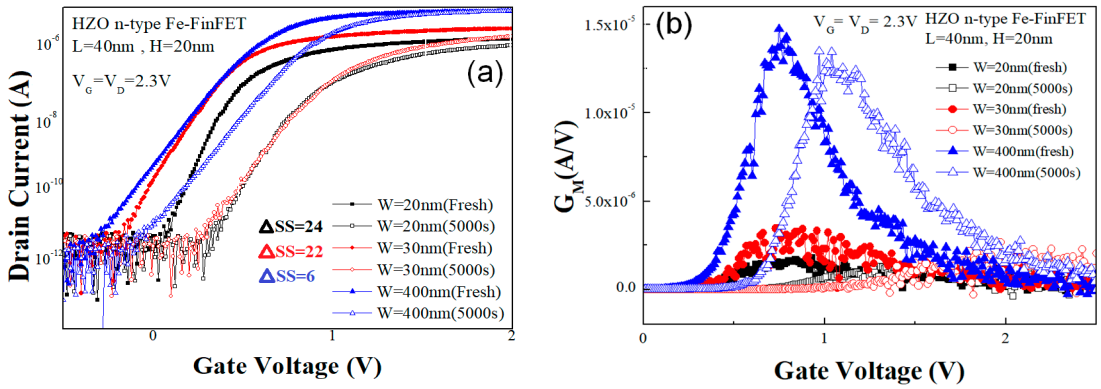

Figure 3. Hot-carrier-induced (**a**) I_D-V_G characteristics and (**b**) transconductance degradations for various fin-widths of n−type Fe-FinFET.

The impact of hot carrier stress on the subthreshold swing and hysteresis of n-type Fe-FinFETs with varying fin-widths was investigated, as depicted in Figure 4. As shown in Figure 4a, the results revealed that as the fin-width decreased, the SS degraded more severely. Specifically, the degradation rates of SS after 5000 s of hot carrier stress for devices with fin-widths of 20 nm, 30 nm and 400 nm were 27%, 18% and 3%, respectively. Interestingly, this device degradation was found to be correlated with the hysteresis behavior of the gate ferroelectric material, as illustrated in Figure 4b. It could be found that higher hysteresis happened in a narrower fin-width device. The most severe hysteresis degradation of 40% happened on a 20 nm fin-width n-type Fe-FinFET after hot carrier stress for 5000 s, in comparison with 30% and 20% hysteresis degradation, which happened on 30 nm and 400 nm, respectively. Serious hysteresis degradation was caused by impact ionization during hot carrier stress, meaning the device's gate stack control was also decayed, further resulting in serious device degradation.

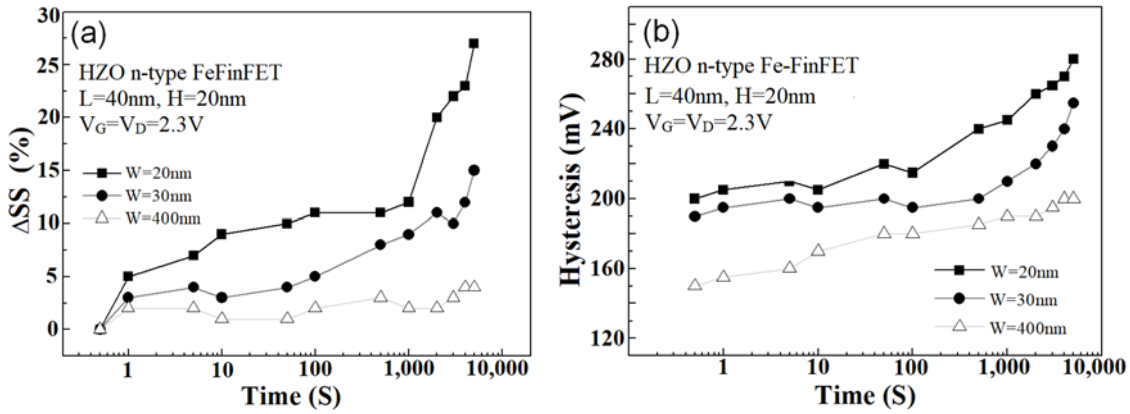

Figure 4. Hot-carrier-induced (**a**) subthreshold swing and (**b**) hysteresis degradations for various fin-widths of n-type Fe-FinFET.

In order to investigate the dependence of the device's instability on the hysteresis of the gate ferroelectric film, various voltage stress conditions of V_D = 0, 2.5 and 2.7 V while V_G = 2.7 V were applied to Fe-FinFETs. Devices with fin-widths of 30 nm were utilized in this work. Subthreshold swing degradation for n-type Fe-FinFET under various stress conditions is shown in Figure 5a. It can be observed that the SS degradation increases with the increase in V_D, and it is not obvious when V_D = 0 V. Figure 5b shows the spread of experimental data for SS degradation versus hysteresis deviation. It could be found that most SS degradation was related to stress-induced hysteresis deviation of the gate ferroelectric. At a stress level where both the V_D and V_G were set to 2.7 V, a more significant degradation in the SS could be observed. Additionally, there was a greater deviation in hysteresis under this stress condition. During the application of positive bias temperature instability (PBTI) stress, where V_D was set to 0 V, there were minimal variations observed in both SS and hysteresis. This was because hot carrier stress caused higher impact ionization, leading to increased interface defects and deterioration of the gate ferroelectric film's hysteresis. Based on the content provided, it appears that there is a correlation between SS degradation and hysteresis deviation, but the relationship is not entirely positive. This suggests that as SS degradation increases, hysteresis deviation may not always increase in a linear fashion. This implies that hysteresis deviation is not solely caused by interface traps and that another mechanism, which is important to identify, may also contribute to this phenomenon.

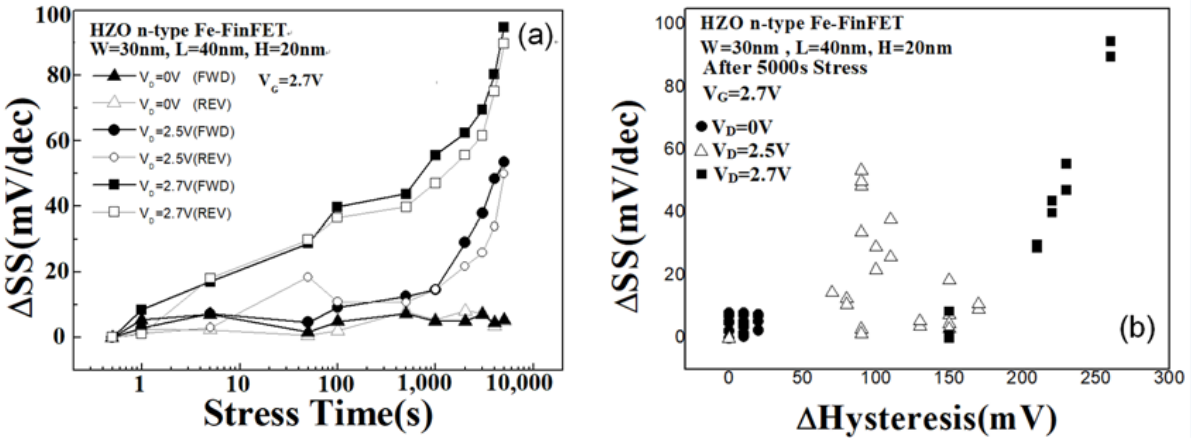

Figure 5. Subthreshold swing degradation (**a**) versus stress time and (**b**) versus hysteresis deviation after various voltage stresses for n-type Fe-FinFET.

In order to investigate the correlation between the gate ferroelectric film and the performance of Fe-FinFET, cross-sectional high-resolution transmission electron microscopy (HRTEM) was performed before and after hot carrier stress, as shown in Figure 6. Prior to hot carrier stress, the HZO-based ferroelectric film exhibited a pure polycrystalline structure (Figure 6a). However, after hot carrier stress, it was observed that the ferroelectric film underwent a transformation to a partially amorphous crystal structure (Figure 6b). Moreover, the Si/IL interface on Fe-FinFET changed from an apparent amorphous/single-crystal Si/IL interface (Figure 6a) to a blurry amorphous/single-crystal Si/IL interface after hot carrier stress (Figure 6b). This change in the Si/IL interface state was found to correspond to device degradation. Furthermore, it is possible that the hysteresis of the gate ferroelectric film may worsen due to the change in the crystal structure of the ferroelectric film after hot carrier stress.

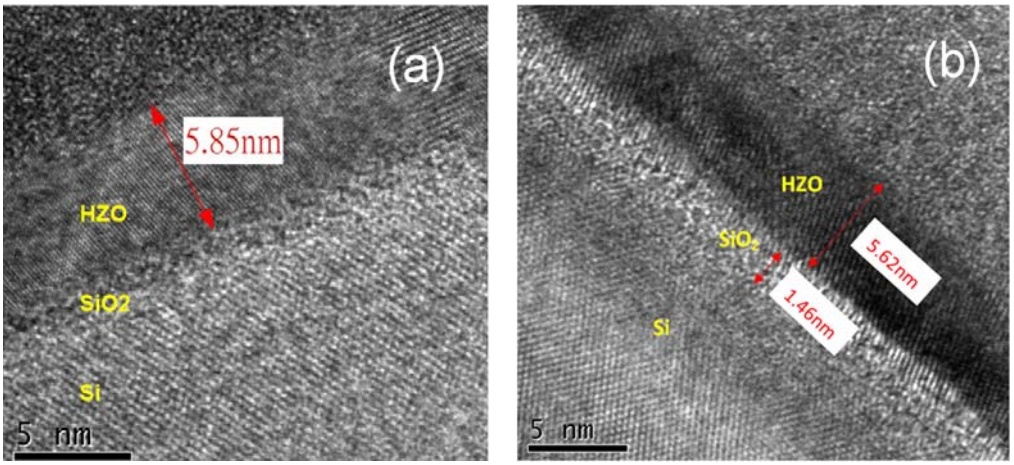

Figure 6. HRTEM of gate stack for Fe-FinFET (**a**) before and (**b**) after hot carrier stress.

In Figure 7, the selected area electron diffraction (SAED) pattern of a gate ferroelectric film for Fe-FinFET is shown before and after hot carrier stress. The SAED image reveals that voltage stress with electrical charging can decay the hysteresis of this ferroelectric FinFET, leading to a change in the crystal properties of the gate ferroelectric film. The main cause of hysteresis degradation is the shift of polarization [23] in the gate ferroelectric film after high-energy carrier stress. This shift in polarization induces a change in the crystal structure of the ferroelectric film from an orthonormal structure with lower hysteresis to an orthogonal structure with higher hysteresis. When subjected to voltage stress, especially in the Si-fin channel where higher impact ionization occurs, the gate ferroelectric film undergoes serious carrier ion bombardment, resulting in further changes to the crystal structure and causing high hysteresis.

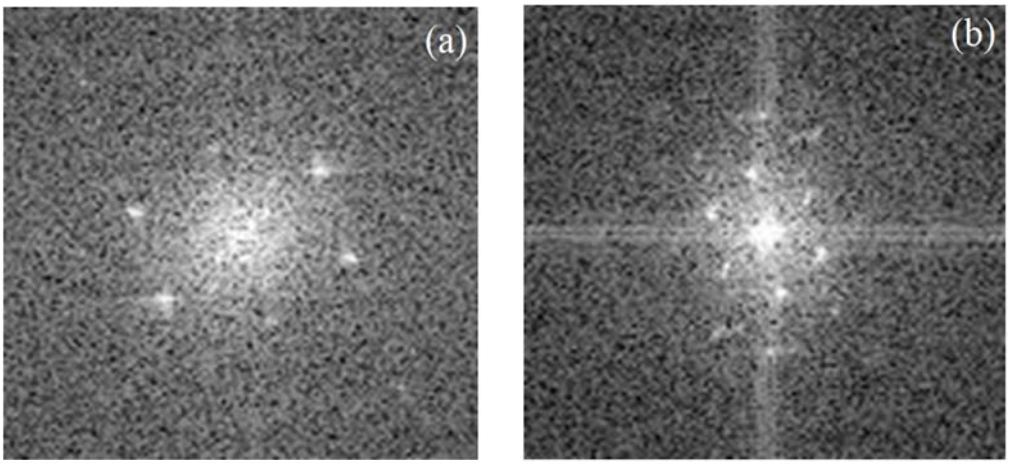

Figure 7. The selected area electron diffraction (SAED) for Fe-FinFET (**a**) before and (**b**) after hot carrier stress.

4. Conclusions

The degradation of Ferroelectric FinFETs under different stress conditions and fin-widths, including SS degradation and hysteresis deviation, were investigated in this work. The Fe-FinFET device exhibits superior performance with narrower fins; however, it is more susceptible to device degradation under hot carrier and bias stress. From HRTEM images, the damaged Si/IL interface after hot carrier stress could be observed. As a result of voltage stress, the hysteresis of the gate ferroelectric film deteriorated, causing a transformation in its crystal properties from an orthonormal structure with lower hysteresis to an orthogonal structure with higher hysteresis. The findings suggest that during hot carrier stress, Fe-FinFET not only harms the Si/IL interface but also alters the structure

of the gate ferroelectric film. SS degradation, which is linked to hysteresis deviation, is notable after HCI stress.

Author Contributions: Methodology, W.-Q.Z. and Y.-L.Y.; experiments, P.-T.W. and Y.-H.L.; writing, W.-Q.Z.; funding acquisition, Y.-L.Y.; supervision, W.-Q.Z. and Y.-L.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This work was financially supported by the National Science and Technology Council in Taiwan (contract MOST 111-2221-E-017-011).

Data Availability Statement: Not applicable.

Acknowledgments: The authors would like to thank the staff of the Taiwan Semiconductor Research Institute (TSRI) for their commendable support.

Conflicts of Interest: The authors declare no conflict of interest.

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