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Communication

Efficient Activation and High Mobility of Ion-Implanted Silicon for Next-Generation GaN Devices

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Abstract: Selective area doping via ion implantation is crucial to the implementation of most modern devices and the provision of reasonable device design latitude for optimization. Herein, we report highly effective silicon ion implant activation in GaN via Symmetrical Multicycle Rapid Thermal Annealing (SMRTA) at peak temperatures of 1450 to 1530 °C, producing a mobility of up to 137 cm^2/Vs at 300K with a 57% activation efficiency for a 300 nm thick 1×10^{19} cm^{-3} box implant profile. Doping activation efficiency and mobility improved alongside peak annealing temperature, while the deleterious degradation of the as-grown material electrical properties was only evident at the highest temperatures. This demonstrates efficient dopant activation while simultaneously maintaining low levels of unintentional doping and thus a high blocking voltage potential of the drift layers for high-voltage, high-power devices. Furthermore, efficient activation with high mobility has been achieved with GaN on sapphire, which is known for having relatively high defect densities but also for offering significant commercial potential due to the availability of cheap, large-area, and robust substrates for devices.

Keywords: GaN; doping; ion implantation; ion implantation activation; annealing; SMRTA; symmetrical multicycle rapid thermal annealing

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1. Introduction

Gallium nitride materials and devices are critical to current and future communications and power electronics. The anticipated demand for faster data communication, power conversion devices for electromobility, and a myriad of additional applications has driven significant interest in obtaining efficient GaN devices with traditional topologies owing to their intrinsic potential with respect to their high breakdown fields, switching speed, power density, and efficiency [1–7]. These topologies inherently require spatially defined doping regimes, which are best implemented via ion implantation and annealing, the current industrial standard. While the material properties of GaN show great potential, this material's inherent high-temperature instability precludes long anneals at standard-pressure, resulting in limited device topologies and necessitating novel solutions for spatially confined doping. To date, this has primarily been achieved via confined epitaxy or regrowth and etch methods. Inherently, these solutions introduce interfacial challenges resulting in reduced capabilities compared to a monolithic growth process [8].

The difficulty in achieving ion implant activation stems from the limited annealing temperatures available, namely, ca. 1000 °C, for long periods before decomposition. To achieve effective atomic mobility in order to remove implant-induced damage and activate dopants, temperatures must typically exceed 1300–1400 °C as this is ~2/3 of the melting point of GaN at 2200 °C. At these temperatures, GaN will decompose to its constituent elements without an excess nitrogen vapor pressure of several GPa [9], which is often termed ultra-high-pressure annealing (UHPA) [10–12]. This basic stabilization method proves effective when used with implanted devices and architectures tested on small samples [13–15];

however, when scaled up to the wafer scale, processing remains challenging or impossible depending on the temperature and pressure regime. While the limited activation of dopants, including devices, via rapid thermal-annealing (RTA) topologies in conjunction with capping moieties has been demonstrated previously [16–18], there is a dearth of data showing low compensation, high mobility, and high efficiency. Specifically, concerning silicon implant activation, demonstrations as early as 1995 exhibited low mobility and n-type conductivity [19], while improvements in the following decade made by various groups [20–23] demonstrated activation efficiencies/mobilities of up to 68%/~100 cm^2/Vs at a 1×10^{15} cm^{-2} dose [21] and ~60%/240 cm^2/Vs and 15%/112 cm^2/Vs at 5×10^{17} and 1×10^{19} cm^{-3} donor concentrations, respectively [23].

In this study, we present the activation of a silicon ion implanted into GaN on sapphire, leading to results exceeding previously reported values while simultaneously maintaining the low doping of the adjacent, in-implanted regions via symmetric multicycle rapid thermal annealing (SMRTA). Such a process has shown previous success with respect to activating implanted Mg for p-type films [24–27], reducing contact resistance with an Si implant [28], and maintaining or improving undoped film quality [29,30].

2. Materials and Methods

Unintentionally doped GaN was grown 2.2 µm thick on c-plane sapphire using a 25 nm AlN buffer layer. The growth temperature of the GaN was 1020 °C at a pressure of 200 Torr and a growth rate of 2.2 µm/h [31]. The GaN film was etched with 10 µm wide trenches approximately 1.5 µm deep via Ar/Cl RIE to isolate measurement structures and imprint sample identification markings. Samples were then coated with 30 nm of PECVD SiN_x at 600 °C for protection during ion implantation and subsequently patterned using standard photolithography processes, utilizing 3 µm of photoresist to locally block the implant to produce Van derPauw structures and linear and circular transmission line measurements (TLMs). Silicon was implanted at 7 degrees and room temperature using energies ranging from 15 to 360 keV, as previously reported [32], to approximate a 1×10^{19} cm^{-3} box profile that was ~335 nm deep (at 5×10^{18} cm^{-3} concentration) with a surface concentration of 5×10^{19} cm^{-3} and thus facilitate electrical contact (as shown in Figure 1a). The implant total dose was 5×10^{14} cm^{-2}, of which 4.24×10^{14} cm^{-2} was expected to reside in the GaN according to SRIM calculations, with the rest having remained in the implant cap. Previous SIMS measurements have shown very good agreement between SRIM and as-implanted dopant profiles. After implantation, samples were cleaned in heated Piranha solution and then concentrated HF solution to remove photoresist and implant cap. After cleaning, wafers were coated with a 200 nm PECVD SiN_x anneal cap (n~1.99 via ellipsometry), diced into coupons, and annealed under various SMRTA conditions. Figure 1b shows the central region of sample 2A after dicing, and Figure 1c shows the same area after annealing at a peak temperature of 1500 °C. After annealing, the cap was removed in HF immediately before the electron beam evaporation of standard Ti/Al/Ni/Au contacts and measured as deposited.

Annealing and activation of implanted dopants were achieved via SMRTA consisting of a degree of moderate nitrogen overpressure of ~35 bar, the cap described above, and a three-step annealing process. The first step consisted of heating for a 30 min period at ~980 °C, wherein the GaN was thermodynamically stable, which was followed by 20 metastable high-temperature pulses separated by 60 s, and finally an additional 30 min period at 980 °C. Such a three-step process has been shown to be beneficial from a structural perspective [33]. Figure 2a shows a time–temperature profile of the high-temperature pulses for the nominal 1530 °C annealing phase. Each individual pulse remained above 1000 °C for less than 8 s and achieved up to 330 K/s heating and cooling rates, thereby highlighting the transient nature of this annealing process. Figure 2b shows a comparison of the average temperature pulses for the three peak temperatures, highlighting the similar ramp rates and timescale while presenting differing peak absolute temperatures from 1450–1530 °C. Figure 2c shows a plot of the cumulative time at a given temperature on semi-log scales

achieved for these annealing schemes for comparative purposes. An additional sample was annealed at 980 °C for 80 min as a baseline; however, it was too resistive to measure.

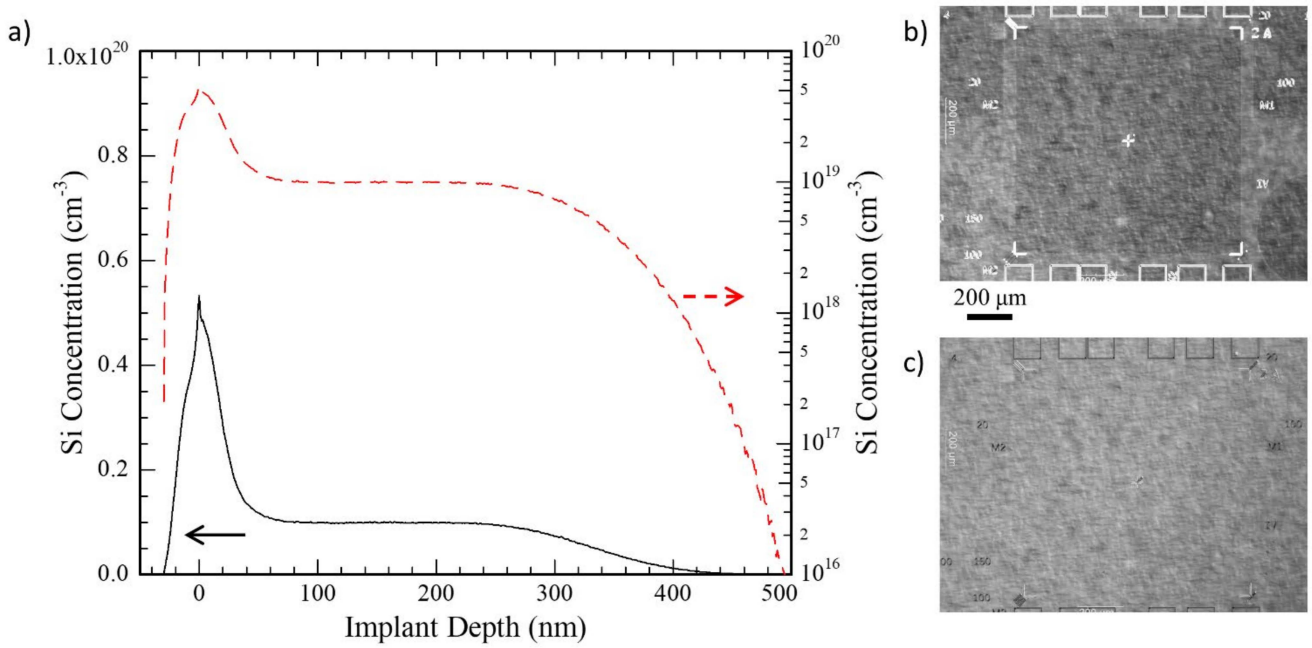

Figure 1. (**a**) SRIM calculation of dopant profile in GaN with 30 nm SiN_x cap, where 0 nm denotes SiN_x:GaN interface on linear (solid black line) and log (dashed red line). (**b**) Nomarski image after implantation, wherein damage is visible as darkened regions, and (**c**) Nomarski image after annealing showing damage recovery and unchanged surface.

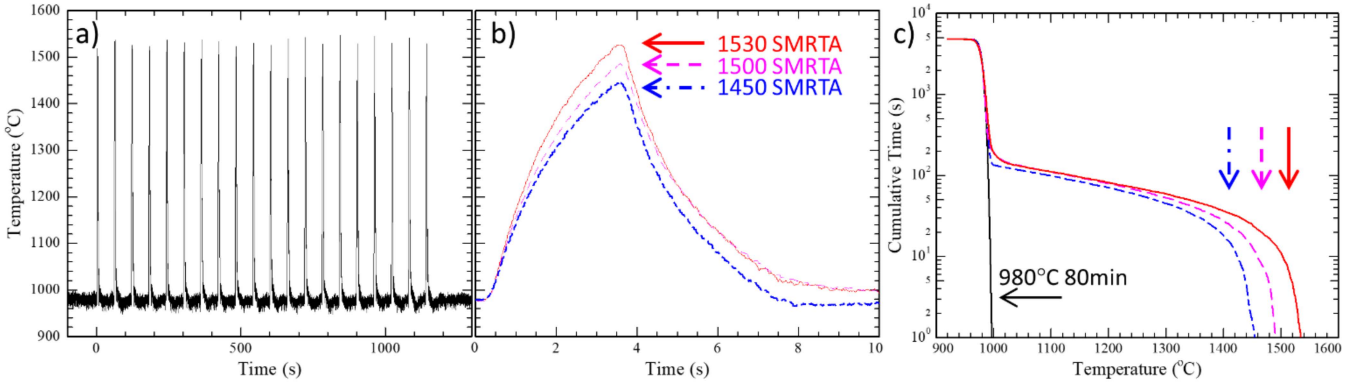

Figure 2. (**a**) Observed temperature profile of SMRTA pulses during 1530 °C anneal. To ensure a greater focus on pulses, preceding and subsequent static annealing steps at ~980 °C are not shown. (**b**) Average of all 20 pulses for each SMRTA annea and (**c**) cumulative time duration at or above the indicated temperature for each SMRTA anneal and an 80 min anneal at 980 °C.

Contact and GaN sheet resistance was first characterized via linear TLMs with pad separations ranging from 4 to 80 µm using a Keithly 4200SCS SMU. Figure 3a shows ohmic contacts of TLM pads, while Figure 3b shows the well-behaved nature of contacts in the implanted region after the 1500 °C SMRTA. Hall effect was measured on a Lakeshore Cryotronics system with M90 Fast Hall across ±0.95 T field at 300 K. Contacts were determined to be ohmic as deposited, with specific contact resistances of 1.6 to 6.6 × 10^{-5} Ω-cm^2, and TLM-extracted sheet resistances exhibited good agreement with measurements of Van der Pauw structures during AC Hall effect testing. No contact-alloying anneal was utilized and no trend was observed in contact resistance as a function of the SMRTA peak temperature.

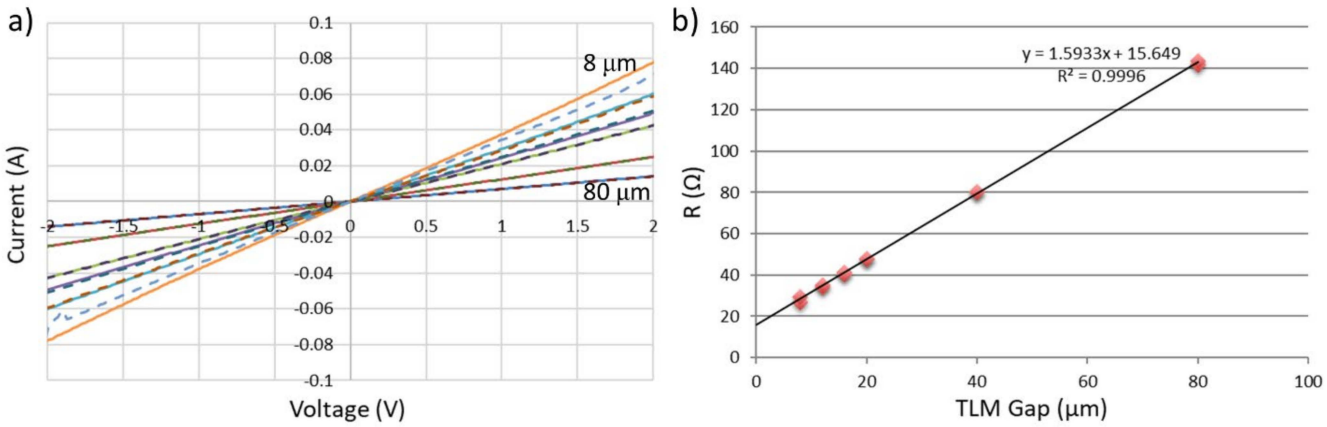

Figure 3. TLM results with (**a**) increasing gap showing linear contacts under all conditions (dashed and solid lines are adjacent test structures) and (**b**) exhibiting linearity across all gaps, showing GaN acting as typical resistor after 1500 °C SMRTA, for which R_s ~160 Ω/□ and $R_{C,sp}$ ~4 × 10^{-4} Ω-cm^2 were observed.

3. Results

Hall effect data were acquired at room temperature with the sheet resistance measured at zero field and at each field point to improve statistics and verify that the probes did not shift. The magnetoresistive effects observed were small compared to all other variations due to probe contact. Due to asymmetries in layout or contacts, the hall voltage was found to have a small offset (typically < 0.1 µV). This offset was circumvented by determining the sheet carrier density directly from dV_H/dB and then mobility from the sheet resistance and sheet density. Consequently, the resultant values were consistent and uniform across multiple Hall structures on a single sample. Figure 4a shows the resultant sheet carrier density and mobility for the implanted regions, for which both quantities are shown to improve alongside an increasing annealing temperature up to 1500 °C, yielding 2.4 × 10^{14} cm^{-2} and 137 cm^2/Vs. Above 1500 °C, a marked degradation of the UID film and excess activation beyond the implant dose were noted. Figure 4b shows the effective activation efficiency obtained by dividing the sheet carrier density by the implant dose (4.24 × 10^{14} cm^{-2}), showing a value of 57% after the 1500 °C SMRTA and 156% after the 1530 °C SMRTA, further exemplifying the degradation after annealing at 1530 °C. Judging by the activation efficiency at 1500 °C and the intended 1 × 10^{19} cm^{-3} box implant profile, the majority of the box should have a carrier density near ~6 × 10^{18} cm^{-3}. Given the degree of mobility under this condition, this suggests a compensation ratio of ~0.45 [34], which is in reasonable agreement with unity minus the observed sheet activation efficiency. In comparison, the SIMS data of similar as-grown films indicate an unintentional impurity inclusion of [Si] < 1 × 10^{16} and [C]~[O] = 5 × 10^{16} cm^{-3}. The significant increase in mobility and activation efficiency relative to the previously reported results further confirms the resultant high quality of the annealed material and the low level of compensation developed, indicating the effectiveness of SMRTA over traditional RTA-style anneals. This effectiveness likely stems from the higher temperatures and long durations enabled via the SMRTA process, which result in reduced residual defect concentrations; however, the specific mechanisms and limiting defect species require further investigation.

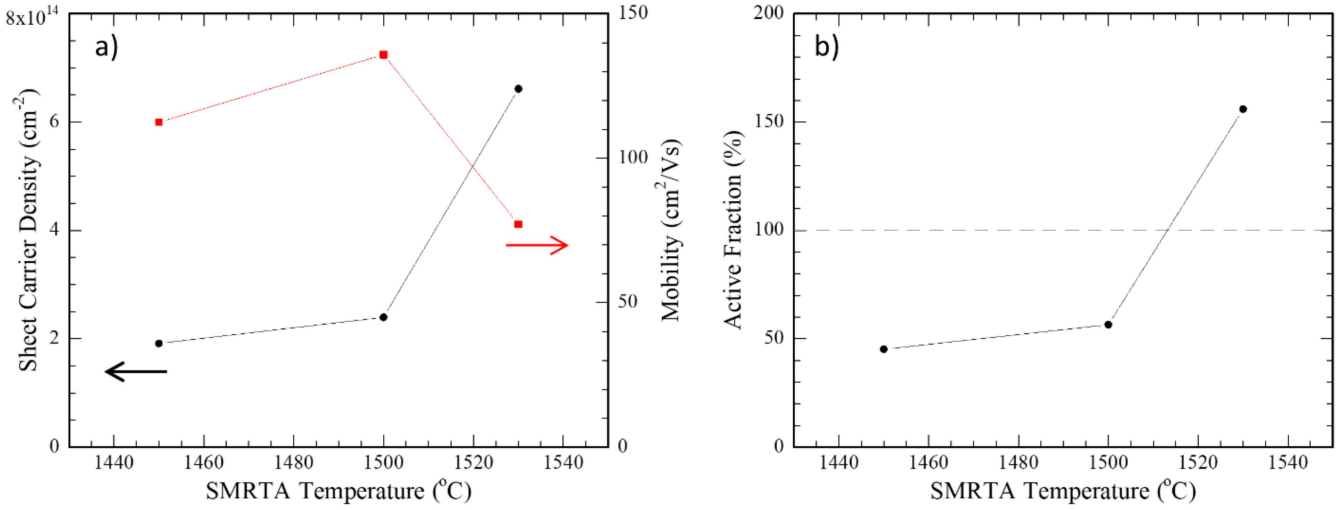

Figure 4. (**a**) Implanted GaN sheet carrier density (black circles, left axis) and mobility (red squares, right axis) and (**b**) resultant activation efficiency as a function of peak annealing temperature.

While improved mobility and activation efficiency are useful for devices, care must be taken to ensure that there are no significant alterations to unintentionally doped or resistive films, which must hold large fields when implemented in devices. Figure 5 shows the measured sheet carrier density and implied volumetric carrier density in the in-implanted Van derPauw structures immediately adjacent to the implanted structures. While the carrier density increases from the low 15 s to the mid 17 s, we note that carrier densities of $1-2 \times 10^{16}$ cm^{-3} (condition after 1500 °C SMRTA) are sufficient for 1.5 kV class devices and have separately been fabricated in-house on bulk GaN [35], yielding 1.3 kV PiN diodes. This demonstrates the compatibility of these implant and annealing processes for the fabrication of future two-terminal (e.g., JBS and MPS diodes) or three-terminal (e.g., VDMOS, CAVET, etc.) devices with traditional device topologies, while further optimization of the anneal conditions can produce improved UID and implant performance.

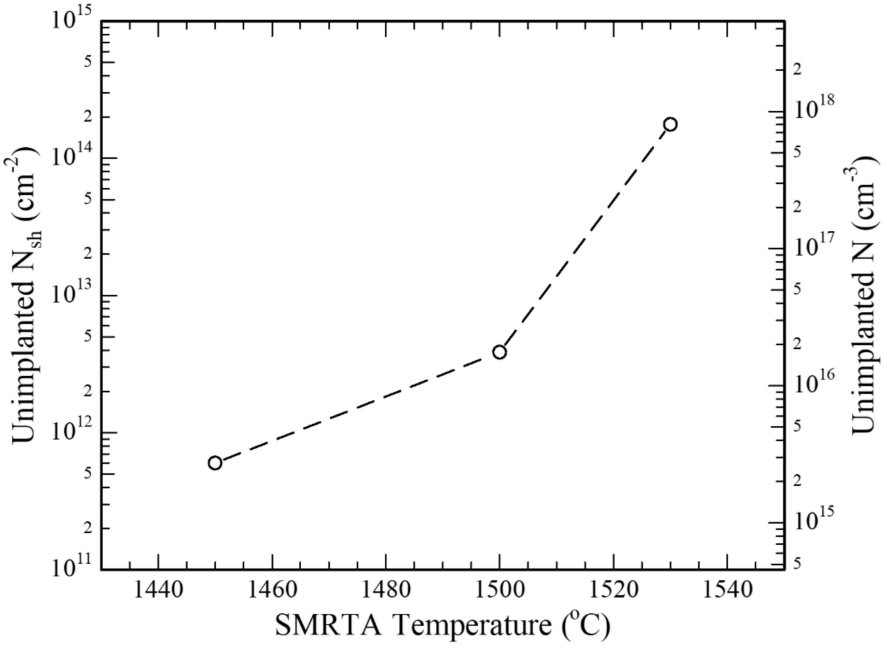

Figure 5. Un-implanted, unintentionally doped GaN carrier concentration (sheet—left axis; volumetric—right axis) after SMRTA annealing as a function of peak annealing temperature.

4. Conclusions

The initial testing of a silicon ion implanted into GaN on sapphire has shown a peak in mobility at 137 cm^2/Vs with 57% activation efficiency after the a 1500 °C peak temperature SMRTA resulting in an estimated 45% compensation ratio. Above this temperature, significant degradation was observed. Unimplanted regions that were directly adjacent showed resultant carrier densities of 1.8×10^{16}, which is sufficient for ~1.5 kV class devices under these conditions despite the lack of optimization of annealing temperature or pulse structure, co-implantation for vacancy reduction, or implant condition effects, suggesting that readily accessible improvements are possible and thus applicable to higher-voltage devices. Furthermore, the demonstration of effective, selective area, n-type implant activation for a 1.5 kV class material on commercially scalable and inexpensive GaN on sapphire provides a facile route toward rapid integration for future GaN devices.

Author Contributions: A.G.J. was responsible for the project's coordination, material processing and annealing, data acquisition, and analysis and was the lead writer of the manuscript. B.N.F. was responsible for project management, inception, funding, and the annealing procedure's conception. J.A.S. was responsible for data acquisition and material processing. M.J.T. was responsible for guidance and mentoring, J.K.H. grew the GaN films. K.D.H. and T.J.A. were responsible for project management. All authors contributed equally to this work and manuscript. All authors have read and agreed to the published version of the manuscript.

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