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A Novel Low On–State Resistance Si/4H–SiC Heterojunction VDMOS with Electron Tunneling Layer Based on a Discussion of the Hetero–Transfer Mechanism

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Abstract: In this study, we propose a novel silicon (Si)/silicon carbide (4H–SiC) heterojunction vertical double–diffused MOSFET with an electron tunneling layer (ETL) (HT–VDMOS), which improves the specific on–state resistance (R_{ON}), and examine the hetero–transfer mechanism by simulation. In this structure, the high channel mobility and high breakdown voltage (BV) are obtained simultaneously with the Si channel and the SiC drift region. The heavy doping ETL on the 4H–SiC side of the heterointerface leads to a low heterointerface resistance (R_H), while the R_H in H–VDMOS is extremely high due to the high heterointerface barrier. The higher carrier concentration of the 4H–SiC surface can significantly reduce the width of the heterointerface barrier, which is demonstrated by the comparison of the conductor energy bands of the proposed HT–VDMOS and the general Si/SiC heterojunction VDMOS (H–VDMOS), and the electron tunneling effect is significantly enhanced, leading to a higher tunneling current. As a result, a significantly improved trade–off between R_{ON} and BV is achieved. With similar BV values (approximately 1525 V), the R_{ON} of the HT–VDMOS is 88% and 65.75% lower than that of H–VDMOS and the conventional SiC VDMOS, respectively.

Keywords: Silicon carbide (4H–SiC); heterojunction; vertical double–diffused MOSFET (VDMOS); on–state resistance

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1. Introduction

Silicon carbide (4H–SiC) MOSFET shows excellent performance in the applications of high power, high frequency and high temperature owing to the prominent material characteristics of 4H–SiC [1]. As a unipolar device, 4H–SiC MOSFET possesses a faster switching speed than the Si IGBT while achieving a much higher breakdown voltage compared with the Si MOSFET [2,3]. The critical electric field of SiC is almost 10 times that of Si, resulting in a much thinner thickness of the drift region of the SiC MOSFET with the same withstanding voltage, namely, a much lower drift resistance. However, the low channel mobility caused by the high SiC/SiO_2 interface state density which is introduced in the gate oxide fabricated processes is the most important limit for the development of SiC MOSFET [4]. Channel resistance is the major component of the specific on–state resistance (R_{ON}) of SiC MOSFET. Moreover, the poor–quality gate oxide of SiC MOSFET leads to some stability issues, such as threshold voltage (V_{TH}) shift [5]. Therefore, research into the suppression of the SiC/SiO_2 interface states and improving the gate oxide quality are pivotal to the SiC MOSFET.

In the past two decades, studies have been carried out on the SiC/SiO_2 interface, and many process optimization method have been used to decrease the density of the interface state in SiC/SiO_2 [6–9]. Nevertheless, the channel mobility of SiC MOSFET is still much lower than that of Si MOSFET (above 50% of the bulk mobility of 1360 cm^2/Vs) [10]. Attempts to address the channel mobility issue in SiC MOSFET need further research and

experiments. As the Si channel has higher mobility, the Si/SiC heterojunction vertical double–diffused MOSFET (VDMOS) device, which combines the high mobility of the Si channel and the high critical electronic field of the SiC drift region, was proposed by L. Chen et al. [11]. Baoxing Duan et al. proposed a Si/SiC heterojunction VDMOS with breakdown point transfer technology to improve the reverse stability of the device [12]. The Si/SiC heterojunction structure has great potential in vertical power devices, especially in power MOSFETs. However, the transfer mechanisms of the Si/SiC heterojunction are not clear, and the forward characteristics of the Si/SiC heterojunction VDMOS can be further optimized.

In this paper, a novel Si/4H–SiC heterojunction VDMOS with an electron tunnel layer (ETL) (HT–VDMOS) is proposed. On the 4H–SiC side of the heterointerface in the JFET region of the proposed structure, a thin heavy doping layer, which we call ETL, is introduced to increase the tunneling current of the heterojunction at on–state. The heterojunction transfer mechanism analysis indicates that the higher doping concentration of the 4H–SiC surface can dramatically decrease the heterointerface resistance (R_H) due to the much narrower heterointerface barrier, namely, the greatly higher tunnel current. Consequently, a significantly lower R_{ON} is achieved by the HT–VDMOS compared with the general Si/4H–SiC heterojunction VDMOS (H–VDMOS) and the conventional SiC VDMOS (C–VDMOS). In addition, the results of the simulation indicate that the heterointerface states benefit the R_{ON} but increase the gate charge (Q_G) and gate–to–drain charge (Q_{GD}) of the HT–VDMOS.

2. Device Structure and Transfer Mechanism

2.1. HT–VDMOS Device Structure

The structures of the HT–VDMOS, H–VDMOS and C–VDMOS are shown in Figure 1. Both heterojunction devices take advantage of the high channel mobility of Si and the high withstanding voltage of 4H–SiC. The ETL on the SiC side of the heterojunction of the JFET region in the HT–VDMOS can significantly enhance the electron tunnel current of the heterojunction, and this results in a lower R_{ON}. As the ETL has a negative effect on the electric field in the gate oxide and the Si PN junction, the lower width of the JFET (W_{JFET}) region is required for the HT–VDMOS. W_{JFET} values of 2 μm, 3 μm and 3 μm were chosen for the HT–VDMOS, H–VDMOS and C–VDMOS, respectively, while the doping concentration, thickness and length of the ETL in HT–VDMOS were optimized to be 5×10^{17} cm^{-3}, 0.07 μm and 1 μm, respectively. The thickness of the Si layer in HT–VDMOS and H–VDMOS was 0.1 μm. The doping concentration of the channels of the HT–VDMOS, H–VDMOS and C–VDMOS was set to 9.2×10^{16} cm^{-3}, 9.2×10^{16} cm^{-3} and 1.7×10^{16} cm^{-3}, respectively. The channel mobility of the C–VDMOS was set to 20 cm^2/Vs.

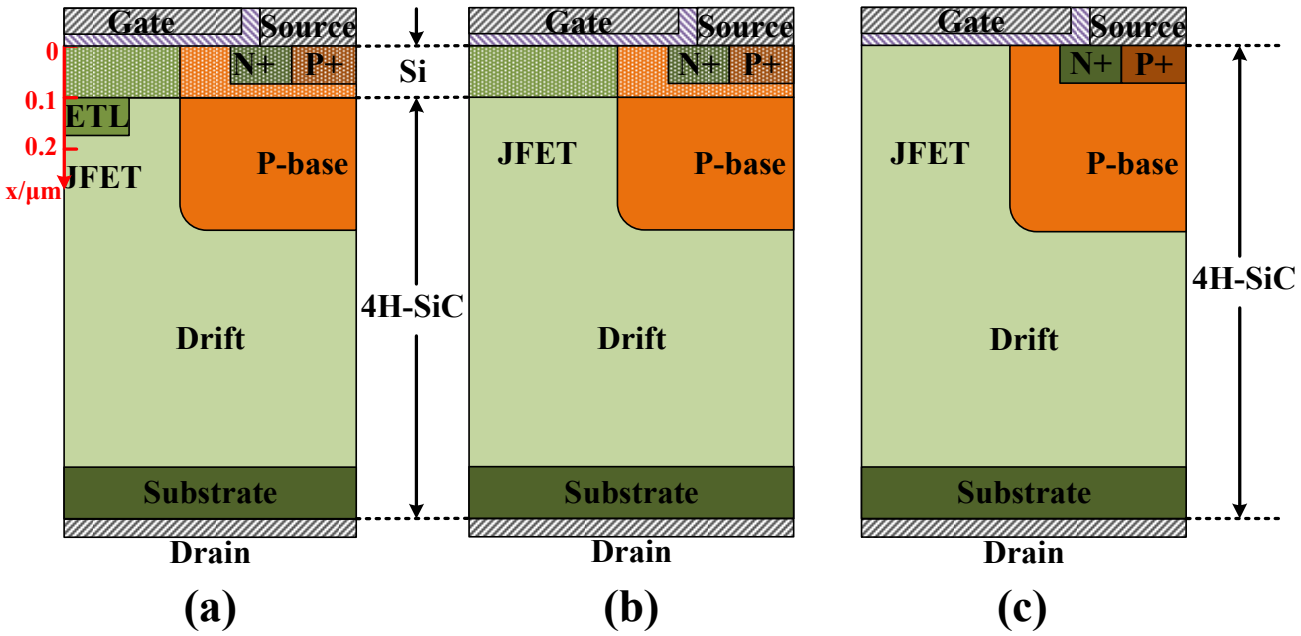


Figure 1. Schematic illustration of the device structures: (**a**) HT–VDMOS; (**b**) H–VDMOS; (**c**) C–VDMOS.

2.2. Heterojunction Transfer Mechanism

Owing to the different band gap and electron affinity between Si and 4H–SiC, a band offset occurs in the heterointerface, as shown in Figure 2a, and a high interface barrier similar to the Schottky contact leads to a high R_H when setting a positive bias on the 4H–SiC side (drain electrode). As a result, the R_{ON} of the heterojunction device without the ETL is significantly increased due to the large value of the R_H. In an attempt to reduce the R_H, the ETL structure was introduced into the novel HT–VDMOS. As the energy band of the heterojunction with the ETL on the SiC side shows in Figure 2b, a higher doping concentration decreases the energy level in the ETL and a lower width of the barrier in the heterointerface is obtained.

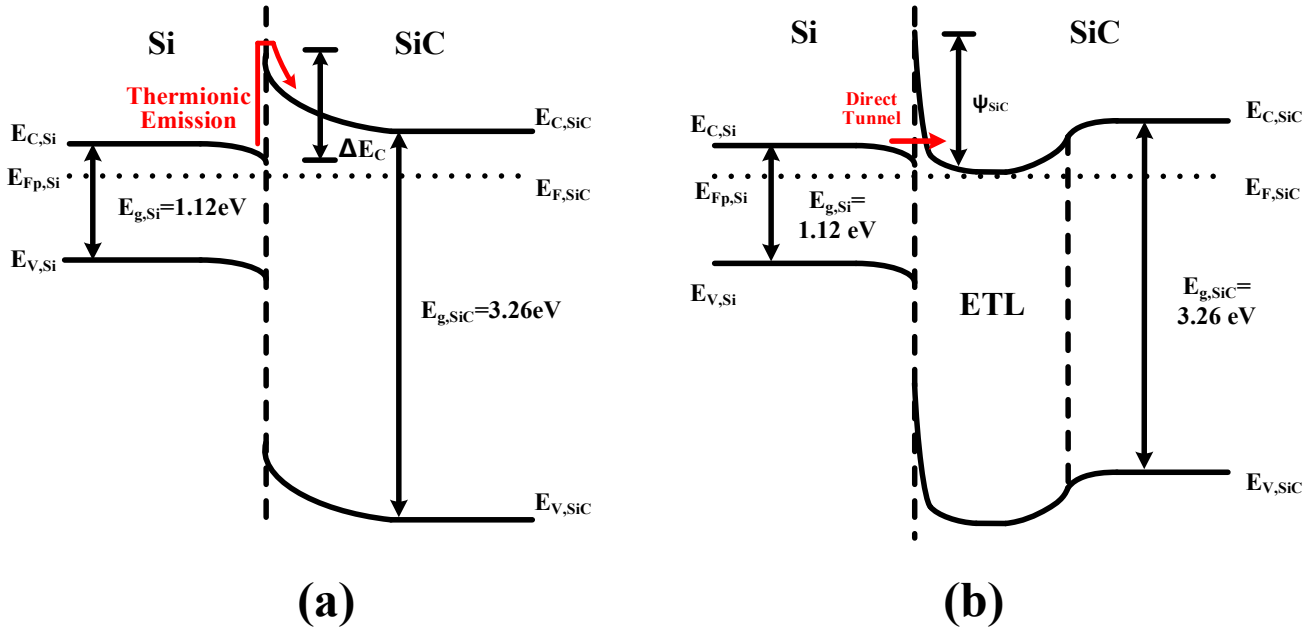


Figure 2. Energy band schematics of the Si/SiC heterojunctions in (**a**) H–VDMOS and (**b**) HT–VDMOS.

There are two transport modes for electrons in the heterojunction: the thermionic emission mode and the direct tunneling mode. In the thermionic emission mode shown in Figure 1a, the electrons require enough energy to cross the high heterointerface barrier, resulting in a low current and a high R_H. When the electrons transfer by direct tunneling, the tunneling probability (P_T) is determined by the tunneling distance (D_T). Based on the Wentzel–Kramers–Brillouin approximation, the relation between P_T and D_T for the triangular barrier can be evaluated by the following formula:

$$P_T \approx \exp\left(-\frac{4\sqrt{2m^*\psi_b}}{3h}D_T\right) \quad (1)$$

where m^* is the effective mass, ψ_b is the triangular barrier height and h is the Planck constant. P_T is the exponential positive correlated with D_T, and the direct tunneling becomes the main transfer mode when the width of the barrier reduces to a small value, as shown in Figure 2b. In this condition, the heterojunction exhibits ohmic behavior, and a large tunneling current can be obtained. Referring to the current of the ohmic contact, the direct tunneling current of the heterojunction (I_{HT}) in the HT–VDMOS can be analyzed by the following formula:

$$I_{HT} \propto \frac{V_{DS}}{\exp\left\{\frac{4\pi}{h}\sqrt{m_n^*\varepsilon_r\varepsilon_0}\left(\frac{\psi_{SiC}}{\sqrt{n_{ETL}}}\right)\right\}} \quad (2)$$

where m_n^* is the electron effective mass, $\varepsilon_r\varepsilon_0$ is the permittivity of 4H–SiC, ψ_{SiC} is the heterointerface barrier height and n_{ETL} is the concentration of electrons in the ETL. Since the ψ_{SiC} shows a weak correlation with the doping concentration of ETL (N_{ETL}) and I_{HT} is strongly and positively correlated to the n_{ETL}, a higher N_{ETL} can lead to a higher I_{HT}. Therefore, the *ETL* structure can significantly decrease the R_{ON} of the HT–VDMOS due to the much lower R_H.

The simulation results demonstrate the analysis of the electron transfer mechanism of the heterojunction. Figure 3a shows the simulation results for the conductor energy band (E_C) with different N_{ETL} values. The E_C drops on the 4H–SiC side of the heterointerface (in the ETL) with when N_{ETL} increases, leading to the decrease in the width of the heterointerface barrier. As the N_{ETL} increases to 5×10^{17} cm^{-3}, a narrow heterointerface barrier, through which the electrons can easily tunnel, is obtained at the heterojunction in the HT–VDMOS, and both a high tunneling current and a low R_H are achieved.

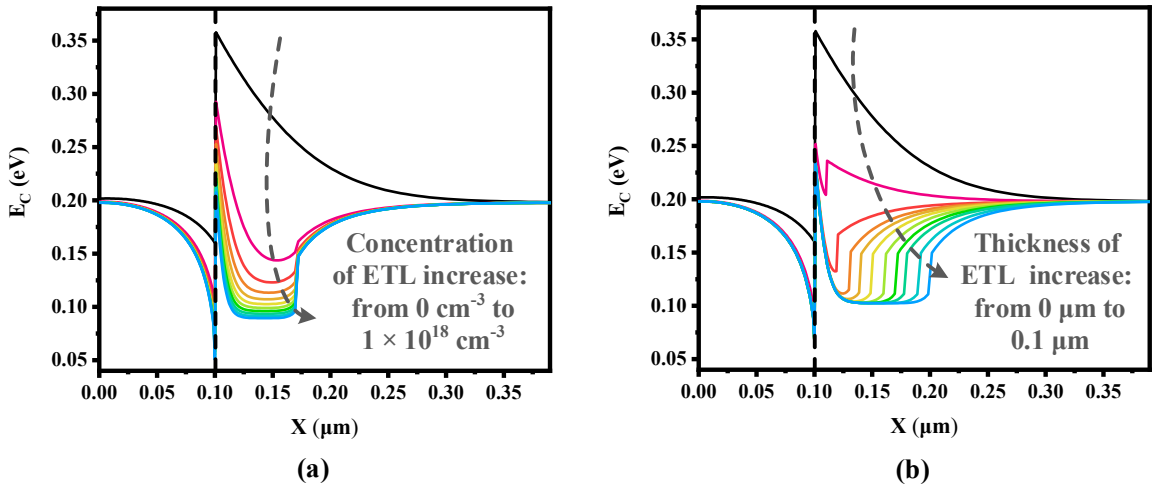


Figure 3. (**a**) Simulation results for the E_C of the heterojunction with different N_{ETL} values at T_{ETL} = 0.1 μm. In the direction of the arrow, N_{ETL} is 0, 1×10^{17}, 2×10^{17}, 3×10^{17}, 4×10^{17}, 5×10^{17}, 6×10^{17}, 7×10^{17}, 8×10^{17}, 9×10^{17}, and 1×10^{18} cm^{-3}, respectively. (**b**) Simulation results for the EC of the heterojunction with different T_{ETL} values at $N_{ETL} = 5 \times 10^{17}$ cm^{-3}. In the direction of the arrow, T_{ETL} is 0, 0.01, 0.02, 0.03, 0.04, 0.05, 0.06, 0.07, 0.08, 0.09 and 0.1 μm, respectively. The region corresponding to the X axes is indicated in Figure 1.

The influence of the thickness of the ETL (T_{ETL}) on the E_C of the heterojunction according to the simulation is shown in Figure 3b. The T_{ETL} should not be excessively small, as with a much thinner ETL, the energy band on the SiC side cannot drop enough to form the narrow heterointerface barrier for the electron tunneling.

2.3. Heterointerface Charge Analysis

To date, two technologies, heteroepitaxy growth and wafer bonding, can be utilized to realize the Si/SiC heterojunction devices [13–17]. Both technologies will generate dislocations and defects at the heterointerface owing to the 19.3% lattice mismatch value between the Si and SiC. This heterointerface state can affect the heterojunction on the I–V and C–V characteristics [18,19]. The current of the heterojunction can be increased by the interface states, which we consider to be caused by the trap–assisted tunneling shown in Figure 4. In the barrier, electrons can tunnel into the defect energy level provided by the heterointerface states before their transfer to the SiC, and a lower electron D_T and a higher tunneling current are obtained.

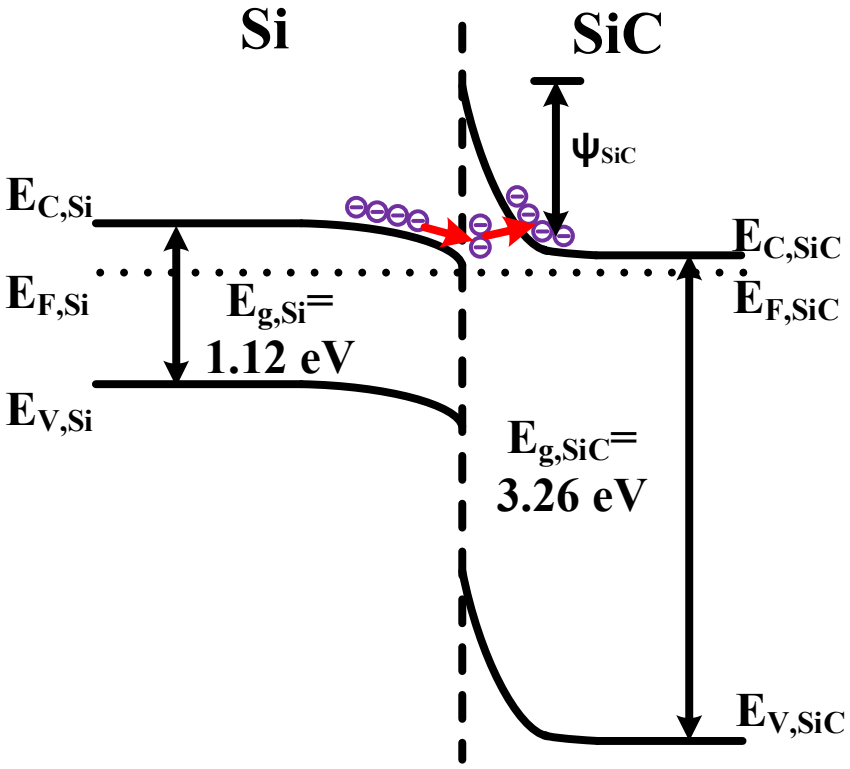


Figure 4. Energy band schematics of the Si/SiC heterojunctions and the trap–assisted tunneling effect.

Some studies have utilized the donor–type heterointerface charges (electrons) to investigate the effect of heterointerface dislocations by simulation [20,21]. Similar to trap–assisted tunneling, the donor–type heterointerface charges can reduce the D_T for electrons and lead to a significant increase in the forward current of the HT–VDMOS. The heterointerface charge defaults to the donor type in the rest of this paper.

3. Device Simulation and Discussion

3.1. Simulation Models and Mobility Parameters

The following physics models were utilized in the TCAD simulation: cvt, analytic, conmob, fldmob, srh, incomplete, bgn, auger, fermi, optr and hei. The cvt, analytic, conmob and fldmob models are correlated to the mobility parameters. The parameters for the mobility of Si are set to be the default of the Silvaco, and the core parameters of the channel–

carrier mobility of 4H–SiC are listed in Table 1. We increased the surface roughness factor of the 4H–SiC and the channel–carrier mobility was reduced to 20 cm^2/Vs. In contrast, the channel–carrier mobility of Si was 500 cm^2/Vs, according to the simulation.

Table 1. Simulation Parameters of the mobility of 4H–SiC.

Parameters	Value	Unit	Parameters	Value	Unit	Parameters	Value	Unit	Parameters	Value	Unit
bn.cvt	4.776×10^7	cm^2/Vs	en.cvt	1	–	mun	947	cm^2/Vs	vsatn	2×10^7	cm/s
cn.cvt	4.431×10^5	cm^2/Vs	feln.cvt	1×10^{70}	cm^2/Vs	tmun	2	–	betan	2	–
taun.cvt	0.0284	–	kn.cvt	2	–	mup	124	cm^2/Vs	vsatp	1.2×10^7	cm/s
dn.cvt	0.3333	–	deln.cvt	7.3×10^{12}	cm^2/Vs	tmup	2	–	betap	1	–

3.2. Optimization of Structure Characteristics

The ETL structure can significantly improve the forward performance of the HT–VDMOS, but this also results in reverse stability issues, such as the increasing electric field at the gate oxide and the PN junction in Si layer. In order to ensure the ability of the withstand voltage of the HT–VDMOS, a detailed study of the structure optimization was carried out via the TCAD Silvaco to achieve a low R_{ON} and high reverse reliability simultaneously for the proposed device.

We studied the influences of four important structure characteristics of the HT–VDMOS on the R_{ON}, the maximum electric field of the gate oxide ($E_{OX–M}$) and the electric field at the Si PN junction (E_{Si}). The influence of N_{ETL} and T_{ETL} on the R_{ON}, $E_{OX–M}$ and E_{Si} is shown in Figure 5a,b. In agreement with the analysis of the E_C, as the N_{ETL} and T_{ETL} values increase, the R_{ON} decreases while the $E_{OX–M}$ and E_{Si} values increase. When the N_{ETL} and T_{ETL} decrease to small values, the R_{ON} of the HT–VDMOS increases rapidly due to the failure of the electron tunneling. The variation of the $E_{OX–M}$ is more obvious than that of the E_{Si} under the effect of the N_{ETL} and T_{ETL}, and the E_{Si} never exceeds the critical electric field of Si. Thus, considering the trade–off between the R_{ON} and $E_{OX–M}$, the N_{ETL} value of 5×10^{17} cm^{-3} and the T_{ETL} value of 0.07 μm were chosen as the optimized values for the HT–VDMOS.

The length of the ETL (L_{ETL}) also remarkably affects the device characteristics, as shown in Figure 5c. The influence on the $E_{OX–M}$ is weak, but the larger L_{TEL} will significantly increase the E_{Si}. Furthermore, the improvement in the R_{ON} is less dramatic with larger values of the L_{ETL}. Therefore, the optimized value of the L_{TEL} in the HT–VDMOS was chosen to be 1 μm.

The last structure characteristic we studied was the W_{JFET}, and the simulation results are shown in Figure 5d. Since the introduction of the ETL leads to a higher doping concentration of the JFET region, a lower W_{JFET} is required for the HT–VDMOS than the C–VDMOS. The W_{JFET} shows the significant influence on the $E_{OX–M}$, and the R_{ON} is also increased with the reduction of the W_{JFET} owing to the larger resistance of the JFET region (R_J). Synthesizing the effects of the W_{JFET} on the $E_{OX–M}$ and R_{ON}, we chose a final W_{JFET} value of 2 μm for the HT–VDMOS.

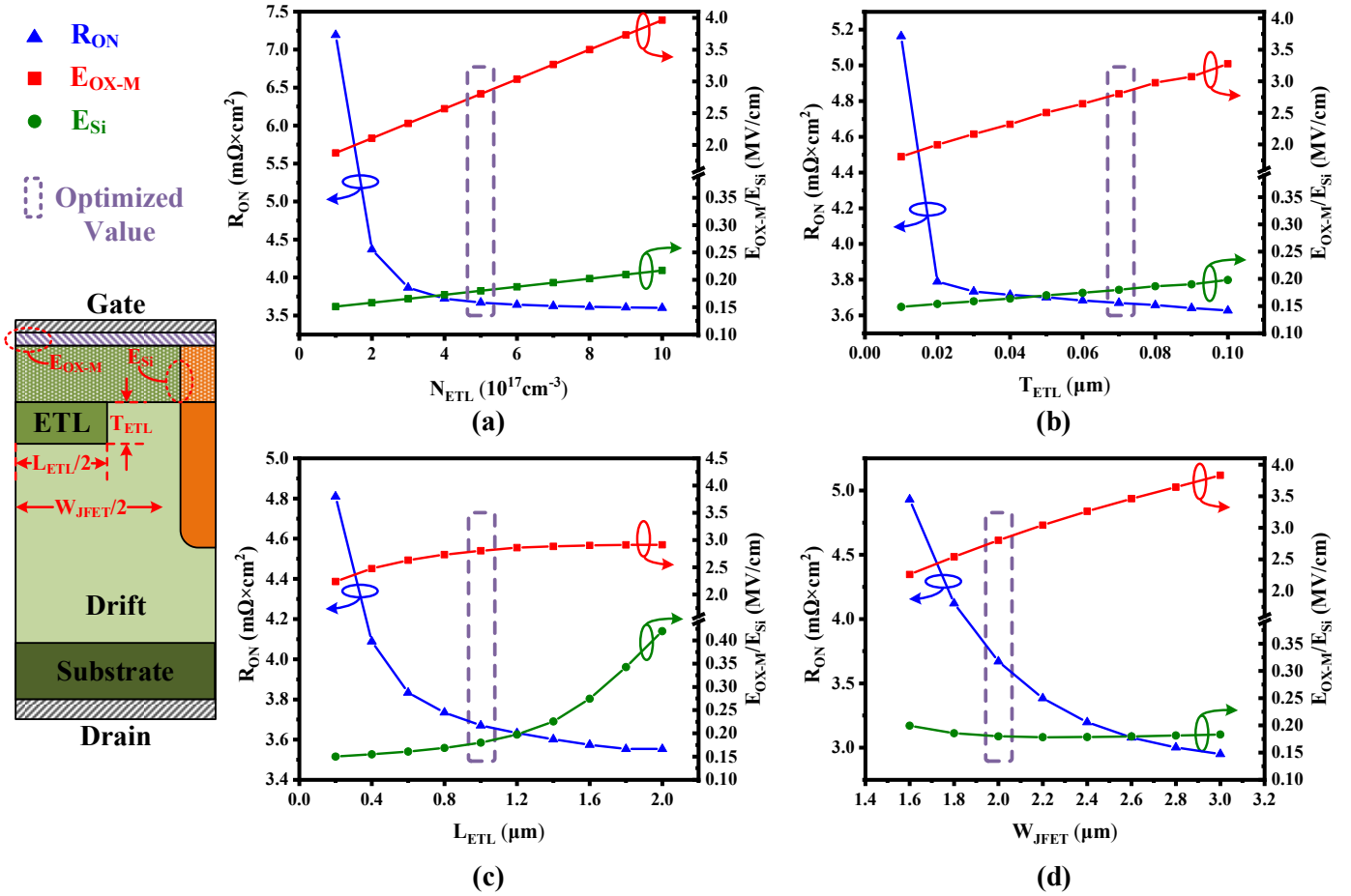


Figure 5. The trade–offs among the R_{ON}, $E_{OX–M}$ and E_{Si} with the variation of (**a**) N_{ETL}, (**b**) T_{ETL}, (**c**) L_{ETL} and (**d**) W_{JFET}. $N_{ETL} = 5 \times 10^{17}$ cm^{-3}, $T_{ETL} = 0.07$ μm, the $L_{ETL} = 1$ μm and $W_{JFET} = 2$μm are chosen as the optimized values. In each graph, the optimized values of the other three are utilized.

3.3. Comparison of Device Performances

Among the HT–VDMOS, H–VDMOS and C–VDMOS devices, the proposed HT–VDMOS achieves the lowest R_{ON} due to the lower channel resistance and R_H, as shown in Figure 6. The HT–VDMOS and H–VDMOS have a much lower R_{CH} than the C–VDMOS, owing to the high channel mobility, while R_H value of the C–VDMOS is zero. The R_H, which is extremely high in the H–VDMOS, can be greatly reduced by the ETL structure in the proposed HT–VDMOS. In spite of the narrower JFET region of the HT–VDMOS leading to a higher R_{JFET}, the increased values of the JFET resistance (R_{JFET}) and R_H are significantly lower than the decreased value of the R_{CH} compared with the C–VDMOS, resulting in the lowest R_{ON} for the HT–VDMOS among these three structures. On the contrary, the H–VDMOS shows a poor forward current ability due to the extremely high R_H.

The breakdown voltage of the HT–VDMOS is slightly higher than those of the H–VDMOS and C–VDMOS. As discussed before, the $E_{OX–M}$ and E_{Si} are limited below the safety values, and the breakdown point of the HT–VDMOS is the P + N junction in the 4H–SiC region. Thus, the BV of the VDMOS devices is determined by the electric field of the edge of the P–well region. According to the curvature effect, the lower W_{JFET} in the HT–VDMOS leads to a large curvature and results in the weakened concentration of the electric field, namely, a higher BV.

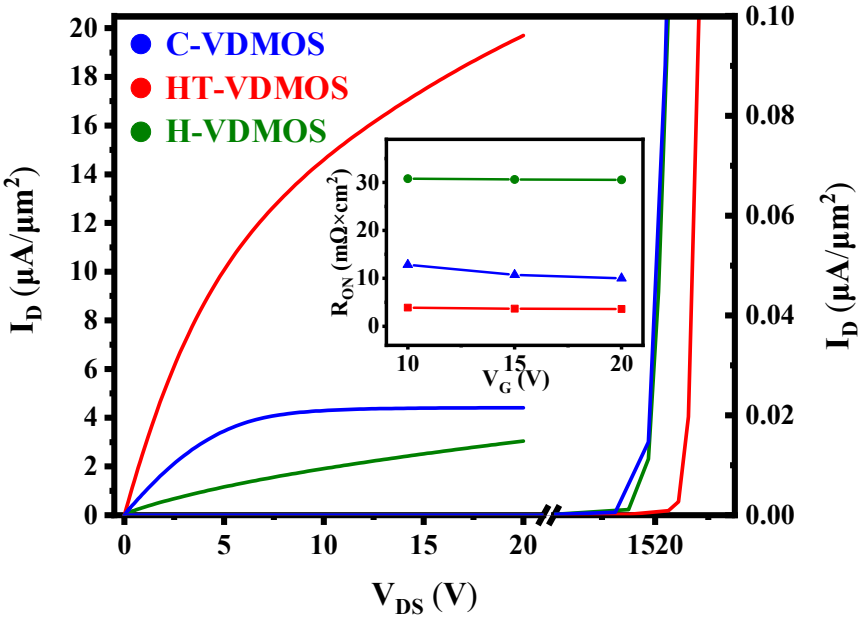


Figure 6. The output I–V curves with V_G values of 10 V, 15 V and 20 V and the reverse characteristics of the HT–VDMOS, H–VDMOS and C–VDMOS. The inset graph shows the variation of the R_{ON} of these three devices with the different V_G values.

The HT–VDMOS possesses the lowest miller capacitance (C_{rss}) among these three devices at V_D = 400 V, while the C_{rss} of the H–VDMOS is the highest, as shown in Figure 7. The C_{rss} of the VDMOS device is determined by the barrier capacitance in the JFET and drift regions (C_B) and the gate oxide capacitance (C_{OX}). At the condition of high V_D voltage bias, the C_{OX} is the major component of the C_{rss}, and the lower W_{JFET} of the HT–VDMOS leads to a lower C_{rss} than the other two devices. The permittivity of the Si layer in the HT–VDMOS and H–VDMOS is higher than the 4H–SiC, resulting in a higher C_B in the JFET region than in the C–VDMOS. Therefore, the C_{rss} of the H–VDMOS is highest at V_D = 400 V.

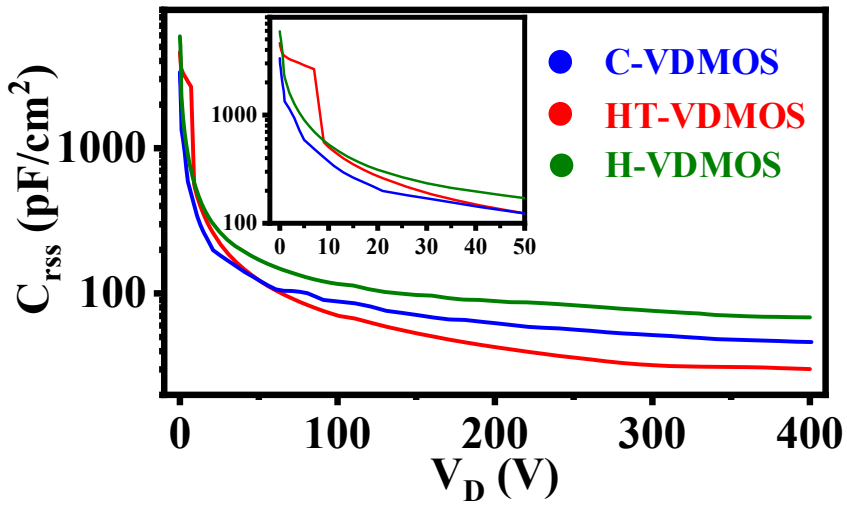


Figure 7. Simulation results of the C_{rss}–V_D curves with the test frequency value of 1 MHz.

At the condition of low V_D voltage bias, the C_B rapidly increases with the decrease of the V_D and becomes the main part of the C_{rss}. As a higher C_B is obtained for the HT–VDMOS and H–VDMOS due to the higher permittivity of the Si layer, the C_{rss} of the C–VDMOS is the lowest at this condition. The ETL also leads to a higher C_B owing

to the narrower width of the barrier region caused by the higher doping concentration. Consequently, an abnormal increase occurs in the C_{rss}–V_D curve of the HT–VDMOS with a V_D value from 1 V to 9 V.

Figure 8 shows the gate charge tests of HT–VDMOS, H–VDMOS and C–VDMOS devices. The HT–VDMOS and C–VDMOS obtain a similar Q_G, which is lower than that of the H–VDMOS. The Q_{GD} of the HT–VDMOS is the lowest among the three devices, which is attributed to the lowest C_{rss} at a high voltage bias condition. Relatively, the Q_{GD} of the H–VDMOS is higher than that of the HT–VDMOS and C–VDMOS. The higher gate platform voltage (V_{GP}) of the C–VDMOS is caused by the higher V_{TH} and the lower μ_{CH}. The V_{GP} can be expressed by the following formula:

$$V_{GP} = V_{TH} + \sqrt{\frac{J_{ON} W_{Cell} L_{CH}}{2\mu_{CH} C_{OX}}} \quad (3)$$

where J_{ON} is the on–state current density, W_{Cell} is the cell width, L_{CH} is the length of the channel and μ_{CH} is the channel mobility. The comparison of the main characteristics of the HT–VDMOS, H–VDMOS and C–VDMOS is listed in Table 2.

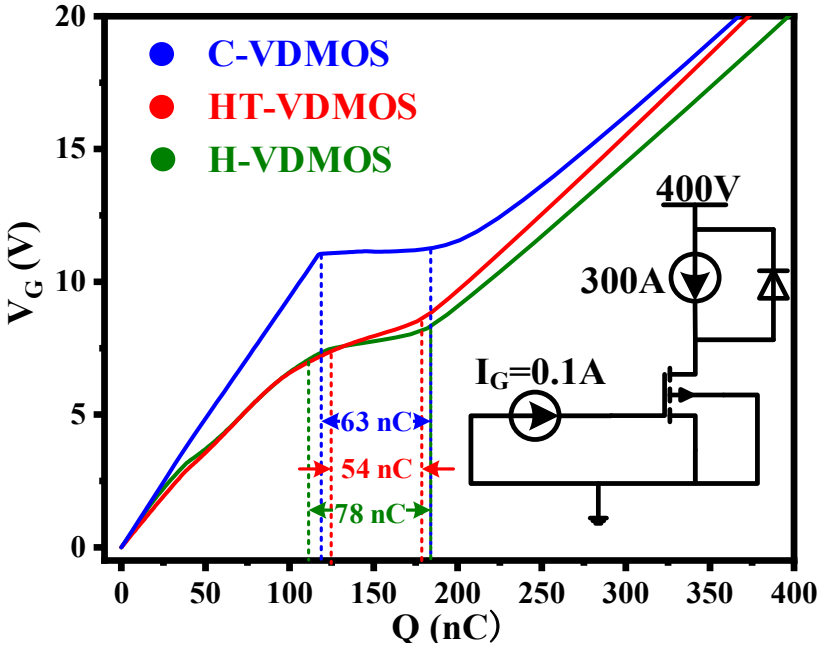


Figure 8. Gate charge tests with the test circuit shown in the inset. The area of each device was set to 1 cm^2. Q_{GD} values of 54 nC/cm^2, 78 nC/cm^2 and 63 nC/cm^2 and Q_G values of 371 nC/cm^2, 408 nC/cm^2 and 365 nC/cm^2 were obtained for the HT–VDMOS, H–VDMOS and C–VDMOS devices, respectively.

Table 2. Characteristics of HT–VDMOS and C–VDMOS.

Parameters	HT−VDMOS	H−VDMOS	C−VDMOS	Conditions	Unit
Breakdown voltage, BV	1529	1522	1522	I_D = 0.1 μA/μm^2	V
	3.88	30.76	12.83	V_G = 10 V, V_D = 1 V	mΩ × cm^2
On–state resistance, R_{ON}	3.67	30.62	10.72	V_G = 15 V, V_D = 1 V	mΩ × cm^2
	3.60	30.54	9.99	V_G = 20 V, V_D = 1 V	mΩ × cm^2
Miller capacitance, C_{rss}	30	68	46	F = 1 MHz, V = 400 V	pF/cm^2
Gate–drain charge, Q_{GD}	54	78	63	V_D = 400 V, I_D = 300 A	nC/cm^2
Gate charge, Q_G	371	408	365	V_D = 400 V, I_D = 300 A	nC/cm^2

3.4. Analysis and Discussion of R_{ON}

The R_{ON} of the VDMOS device consists of five components: the source resistance R_S, R_{CH}, R_H, the R_{JFET}, and the drain resistance R_{ND}, as shown in Figure 9a. According to the analysis of the components shown in Figure 9b, the major differences in the total R_{ON} originate from the R_{CH}, R_H and R_{JFET}, which has been discussed previously. With the increasing V_G, the R_{CH} of these two structures both significantly decrease due to the higher channel carrier density. However, the proportion of the R_{CH} in the R_{ON} of the HT–VDMOS is low, and the variation of R_{CH} caused by V_G is not obvious for the R_{ON}. On the contrary, as the proportion of the R_{CH} in the R_{ON} is much higher for the C–VDMOS due to the poor channel mobility, the reduction in R_{ON} caused by the increasing V_G is much more significant, although the increase in the channel carrier density of the C–VDMOS with the increasing V_G is slower than that of the HT–VDMOS owing to the higher width of band gap of SiC.

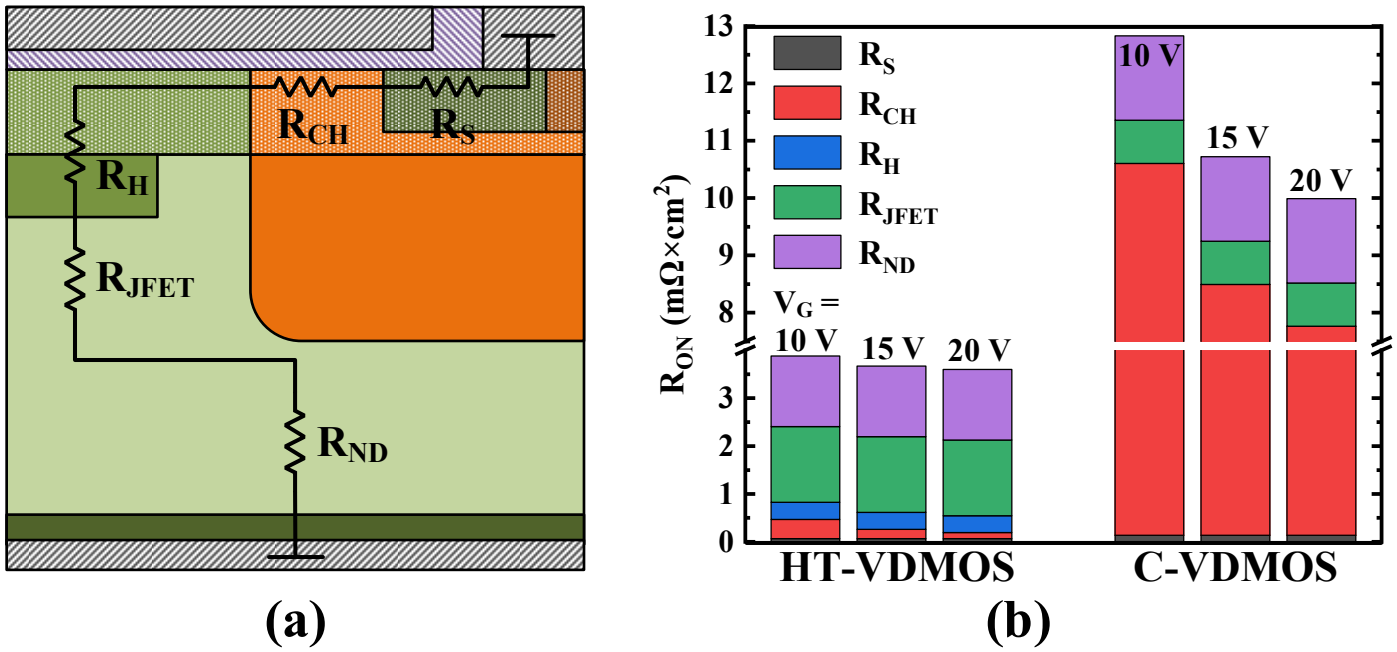


Figure 9. (**a**) Components of the R_{ON} corresponding to the geometrical positions in the structure. (**b**) Values of the components of the R_{ON} of the HT–VDMOS and C–VDMOS under different V_G values.

The influence of the charge density in the gate oxide (Q_{OX}) on the R_{ON} of these two structures is similar to that of the V_G, as shown in Figure 10a. During the practical work of VDMOS, a few charges will enter the gate oxide, leading to a threshold voltage shift after long–term work. Thus, the different values of Q_{OX} can also affect the channel carrier density, resulting in a similar variation in the R_{ON} of these two structures compared with the V_G.

The heterojunction can be fabricated by wafer bonding or deposition. If the Si deposition process was utilized, the Si film may not be monocrystalline, and the R_{ON} of the HT–VDMOS will be different when the Si film is polycrystalline due to the variation of the μ_{CH}. Therefore, the influence of the μ_{CH} of the HT–VDMOS on the R_{ON} was studied, as shown in Figure 10b. The R_{ON} of the HT–VDMOS decreases with degeneration of the μ_{CH} and the decrease becomes rapid when the μ_{CH} of HT–VDMOS is lower than 150 cm^2/Vs. Nevertheless, the proposed HT–VDMOS can achieve a lower R_{ON} than the C–VDMOS, as long as the μ_{CH} of the HT–VDMOS is higher than 69.8 cm^2/Vs.

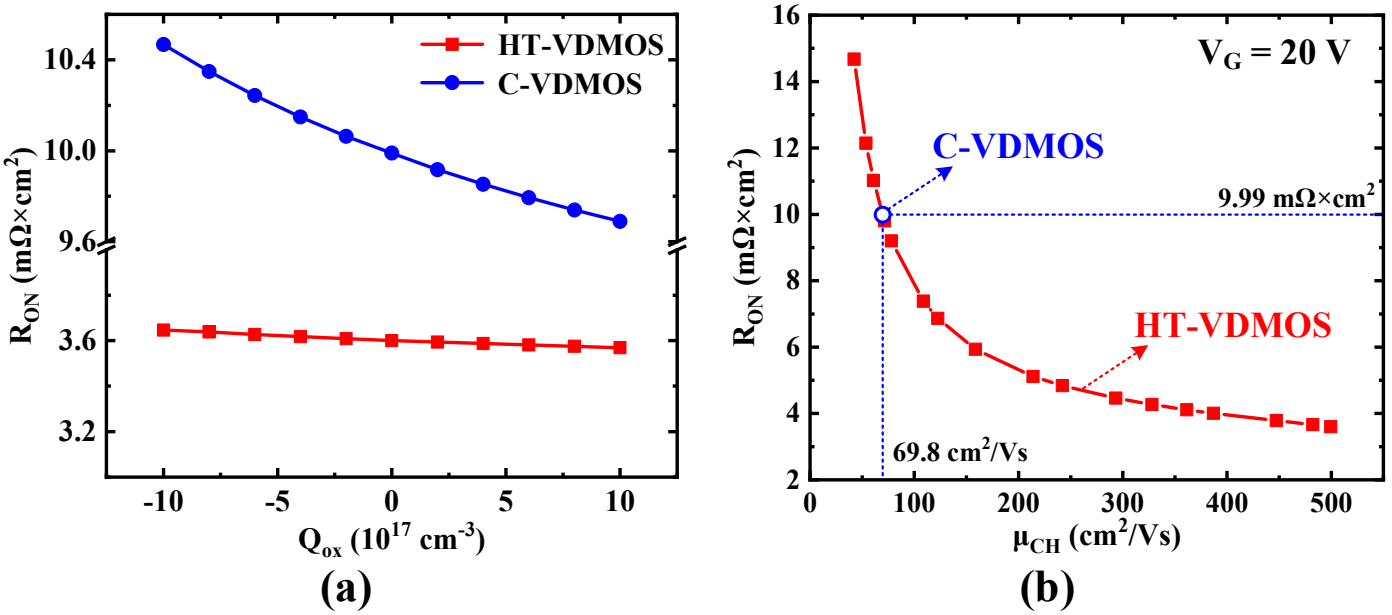
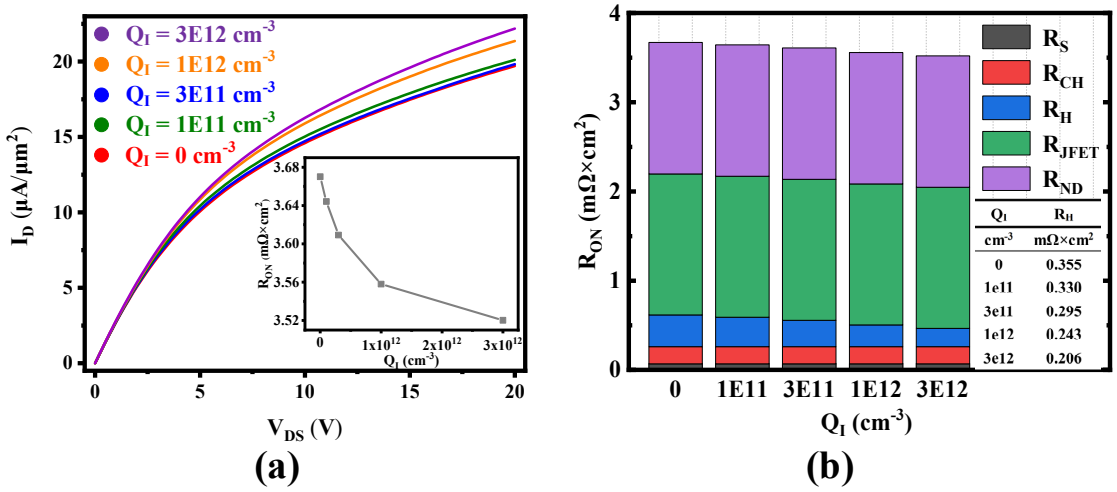


Figure 10. (**a**) The influence of the Q_{OX} value on the R_{ON} of the HT–VDMOS and C–VDMOS. (**b**) The influence of the μ_{CH} value on the R_{ON} of the HT–VDMOS.

3.5. Influence of Heterointerface Charges

The influence of the heterointerface charge density (Q_I) on the output I–V characteristic and R_{ON} of the HT–VDMOS is shown in Figure 11. The forward current of the HT–VDMOS is enhanced with increasing Q_I, which is caused by the trap–assisted tunneling. The R_{ON} values of 3.67 mΩ × cm^2, 3.64 mΩ × cm^2, 3.61 mΩ × cm^2, 3.59 mΩ × cm^2 and 3.52 mΩ × cm^2 were obtained for the HT–VDMOS for Q_I = 0, 1 × 10^{11} cm^{-3}, 3 × 10^{11} cm^{-3}, 1 × 10^{12} cm^{-3} and 3 × 10^{12} cm^{-3}, respectively. The analysis of the components of the R_{ON} of HT–VDMOS with different Q_I values, shown in Figure 11b, demonstrated that trap–assisted tunneling can reduce the R_H, resulting in a lower R_{ON}. As the proportion of the R_H in R_{ON} is also low, the variation of R_{ON} is slight, and the reduction of the R_{ON} caused by the heterointerface charges becomes slow when the Q_I values become larger, as shown in the inset graph in Figure 11a. These results indicate that the R_H of the HT–VDMOS is becomes lower as a minor component of a R_{ON} with a high Q_I.



Q_I cm^{-3}	R_H mΩ×cm^2
0	0.355
1e11	0.330
3e11	0.295
1e12	0.243
3e12	0.206

Figure 11. (**a**) Output I–V characteristic curves of the HT–VDMOS for different Q_I values. The inset graph shows the corresponding R_{ON} values. (**b**) Values of the components of the R_{ON} of the HT–VDMOS with different Q_I values. The V_G is set to 15 V.

The Q_G and Q_{GD} of the HT–VDMOS increase with increasing Q_I, as shown in Figure 12. The heterointerface charges lead to a higher C_{rss} due to the narrower width of the barrier in the JFET region, and this causes extra charges for the gate charges, resulting in a higher Q_{GD} and Q_G in the HT–VDMOS. Q_{GD} values of 54 nC, 57 nC, 60 nC, 69 nC and 85 nC and Q_G values of 371 nC, 369 nC, 368 nC, 379 nC and 401 nC were obtained for the HT–VDMOS for Q_I = 0, 1×10^{11} cm^{-3}, 3×10^{11} cm^{-3}, 1×10^{12} cm^{-3} and 3×10^{12} cm^{-3}, respectively.

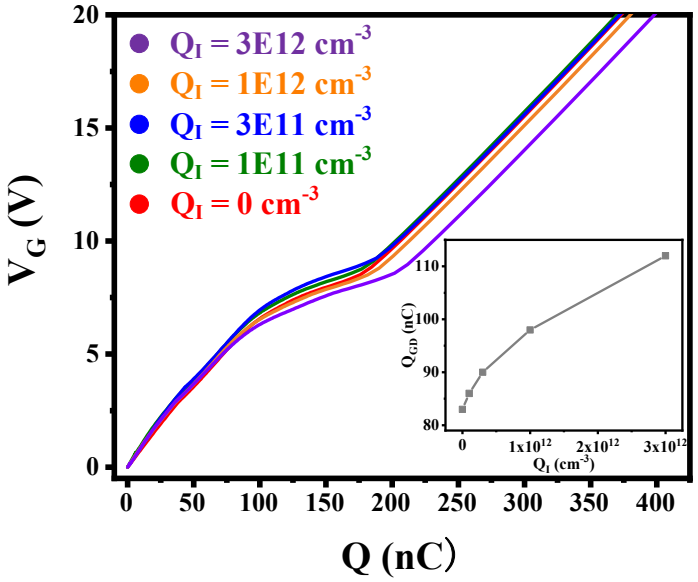


Figure 12. Gate charge tests of the HT–VDMOS for different Q_I values. The area of each device was set to 1 cm^2. The inset graph shows the corresponding Q_{GD} values.

4. Conclusions

A novel HT–VDMOS structure, which features an introduced ETL and a low R_{ON}, is proposed, and we discuss its hetero–transfer mechanism based on device simulation studies. The HT–VDMOS possesses the advantages of Si and 4H–SiC, namely, high channel mobility and high critical electric field, respectively. The heavily doped ETL on the 4H–SiC side of the heterointerface in the JFET region can greatly reduce the R_H caused by the high barrier in the heterointerface due to the direct tunneling effect. With a high doping concentration, the energy band level on the 4H–SiC side of the heterointerface can be decreased, and a significantly narrower interface barrier is formed. Thus, the electrons on the Si side can easily transfer to 4H–SiC by direct tunneling, and a lower R_H is achieved. Our study of the influence of the heterointerface charges indicates that the heterointerface charges can enhance the forward current of the HT–VDMOS but leads to a degeneration of gate charge characteristics. Consequently, the R_{ON} of the HT–VDMOS is decreased by 88% and 65.8% compared with the H–VDMOS and C–VDMOS, respectively.

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