

Transistor-Based Synaptic Devices for Neuromorphic Computing

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Abstract: Currently, neuromorphic computing is regarded as the most efficient way to solve the von Neumann bottleneck. Transistor-based devices have been considered suitable for emulating synaptic functions in neuromorphic computing due to their synergistic control capabilities on synaptic weight changes. Various low-dimensional inorganic materials such as silicon nanomembranes, carbon nanotubes, nanoscale metal oxides, and two-dimensional materials are employed to fabricate transistor-based synaptic devices. Although these transistor-based synaptic devices have progressed in terms of mimicking synaptic functions, their application in neuromorphic computing is still in its early stage. In this review, transistor-based synaptic devices are analyzed by categorizing them into different working mechanisms, and the device fabrication processes and synaptic properties are discussed. Future efforts that could be beneficial to the development of transistor-based synaptic devices in neuromorphic computing are proposed.

Keywords: transistor; synaptic device; neuromorphic computing



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1. Introduction

The von Neumann computer plays important roles in artificial intelligence and data computing [1], and it is believed to be one of the most noteworthy electronic devices so far. However, von Neumann computing needs substantial data transmission between processors and memory units in the system, which may cause high energy consumption and a time delay effect. Moreover, the von Neumann computer can only perform prespecified programs and cannot execute unstructured and real-time problems [2]. By contrast, the human brain can implement high-speed information processing parallelly with low energy consumption and excellent fault-tolerance capabilities [3,4]. It can be considered an efficient and perfect biological computing system. Therefore, neuromorphic computing, i.e., brain-like computing, is regarded as the most efficient way to the von Neumann bottleneck.

The human brain is a complex neuronal network that is composed of approximately 10^{13} neurons and 10^{15} synapses [5,6]. An image of a human brain synapse structure, including the presynaptic and postsynaptic terminals and a synaptic cleft, is shown in Figure 1a. In the synapse, action potentials are usually triggered after information has been perceived. Once the action potential spreads toward the axon terminal, the synaptic cleft aids the secretion of neurotransmitters (chemical signals) and their transmission to the dendrites of postsynaptic neurons [7]. After excitatory/inhibitory neurotransmitters are released, excitatory postsynaptic currents (EPSCs)/inhibitory postsynaptic currents (IPSCs) are formed and can then be improved or weakened depending on the external signals' rate and strength. This occurrence is known as biological synaptic plasticity, which is crucial to the processing of external information for the human neural network [8]. The plasticity may include EPSCs/IPSCs, short-term potentiation/depression (STP/STD), long-term

potentiation/depression (LTP/LTD), spike-time-dependent plasticity (STDP), as well as spike-rate-dependent plasticity (SRDP) based on various processed information conditions [9–11]. STP/STD is the temporary enhancement/inhibition of neural connections [12], while LTP/LTD is synaptic plasticity with long-memory retention. As shown in Figure 1b, STDP evolution depends on the order and interval of the external stimulus arriving at the synaptic terminals [13], and it is widely regarded as a basic learning mechanism for the brain. SRDP describes synaptic plasticity based on external pulses with different frequencies. This kind of plasticity plays major roles in cognitive behavior for the human brain [13–17].

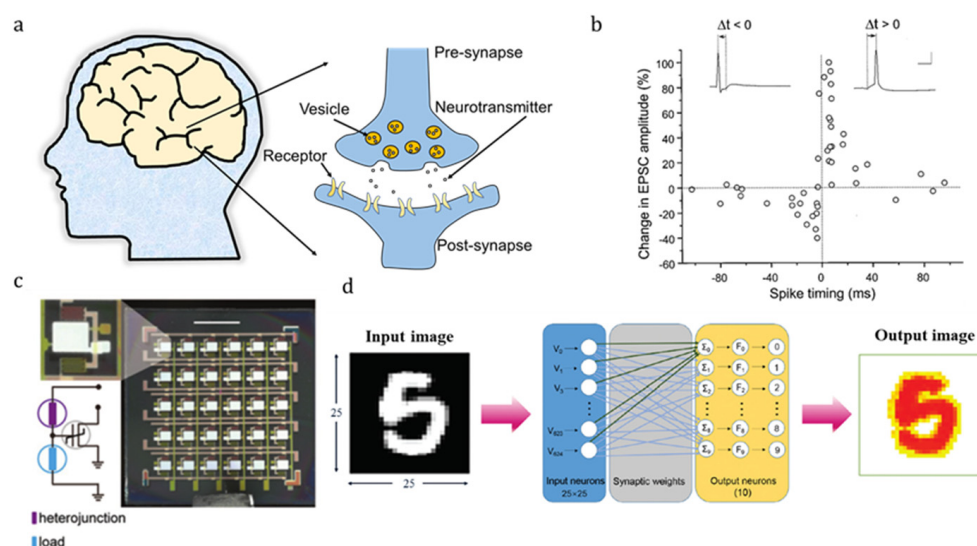


Figure 1. (a) Schematics of the human brain and a synapse structure. (b) Spike-time-dependent plasticity (STDP) function in the human brain neural network. Reproduced with permission from Ref. [13]; Copyright 1998 Society for Neuroscience. (c) A 5×6 neuromorphic computing array system. Reproduced with permission from Ref. [18]; Copyright 2018 WILEY-VCH. (d) System-level Modified National Institute of Science and Technology (MNIST) pattern recognition. Reproduced with permission from Ref. [19]; Copyright 2021 Royal Society of Chemistry.

In principle, neuromorphic computing for learning and processing information utilizes various plasticity behaviors in the human brain neural network [20,21]. It is therefore an essential prerequisite to fabricate hardware array devices that can mimic these synaptic functions for the construction of artificial neural networks (Figure 1c) [18]. A transistor is a multiterminal electronic device that has been investigated substantially [22–25]. It can be used for information detection and some memristive systems [26–28], indicating the possible application of transistors as synaptic devices in neuromorphic computing. Transistor-based synaptic devices have the advantage of synergistic control capabilities arising from their multigate characteristics [29], and they are expected to mimic synaptic plasticity with a considerable dynamic range and superior linearity [30]. Given that the dimensional scaling of the devices has followed Moore’s law for decades, synaptic transistors are also improving in terms of size [31]. A high-quality synaptic transistor with a nanoscale size can be fabricated [32–34], benefiting from the developed complementary metal oxide semiconductor (CMOS) technology. These characteristics assure the fabrication of synaptic devices with high density and the mimicking of synaptic functions with high performance. An artificial neural network based on a transistor array synaptic system can be used for pattern recognition through specific training [19,35–37], which is demonstrated in Figure 1d. This network contains 625 input neurons and 10 output neurons, with complete connection through 625×10 synapse weights on the basis of a hard array architecture. Pattern recognition for Modified National Institute of Standard and Technology (MNIST) was successfully achieved on the basis of this computing system. Various low-dimensional inor-

organic materials such as silicon nanomembranes, carbon nanotubes, nanoscale metal oxides, and two-dimensional materials have demonstrated special electronic properties [38,39]. Researchers have substantially investigated these synaptic transistors based on these low-dimensional materials for the realization of this kind of similar task in recent years [40], and these transistors have demonstrated excellent potentials for neuromorphic computing. However, synaptic properties still need to be improved on the basis of their application requirements. Herein, the fabrication methods, working mechanisms, and properties of these transistor-based synaptic devices are discussed in the current work. Perspectives for future development are also analyzed.

2. Different Working Mechanisms of Synaptic Transistor Devices

2.1. Capture and Release of Carriers

In consideration of distinct bandgap offsets in semiconductor devices [41], the heterojunctions formed in these devices can be classified into type-I, type-II, and type-III. A built-in electric field in a typical type-II heterojunction causes the generated electrons and holes to move in opposite directions through the interface; then, the conductivity of the devices can be regulated on the basis of the carrier distribution and trapping effects. This mechanism can be used for mimicking synaptic functions in synaptic transistor devices.

Yin et al. fabricated a hybrid synaptic transistor device based on organo-lead halide perovskite (MAPbI₃) and a silicon nanomembrane (Si NM) [42]. Its schematic is demonstrated in Figure 2a. Si-on-insulator (SOI) wafers (purchased from Soitec) were used as the substrate in the device; the Si NM was used as the channel; and the perovskite thin film was used as the light absorption layer, which was obtained through a spinning-coating (SC) method. The patterned Au electrodes were then prepared via thermal evaporation (TE) through a shadow mask, which was used to achieve a channel size of 25 μm (length) × 500 μm (width). TE deposition is a common method to form metal electrodes, while the SC method has the advantages of simple operation and low cost. These methods are widely used in the preparation of synaptic devices [43–45].

The working mechanism of this device can be described through energy band alignment, as demonstrated in Figure 2b,c. A type-II heterojunction is formed at the interface of Si NM and MAPbI₃. Photogenerated electrons and holes are formed in MAPbI₃ in response to an optical pulse. The photogenerated holes are effectively moved into the Si NM under the driving of the built-in electric field between Si NM and MAPbI₃. The recombination of photogenerated holes and electrons must overcome the barrier between Si NM and MAPbI₃. Therefore, the concentration of holes in Si NM could further increase in response to consecutive external optical pulses, and it contributes to the conductance enhancement of the synaptic transistor, as shown in Figure 2d. Therefore, the device can successfully mimic synaptic functions of EPSC and STP-to-LTP transition, under optical stimulation. Furthermore, the Fermi level shifted toward the valence band maximum in Si NM when the device worked at a negative gate voltage. This negative gate voltage caused the energy band of Si NM to curve seriously at the Si-NM/MAPbI₃ interface, heightening the built-in electric field between Si NM and MAPbI₃. Consequently, the trapping capability increased, which is more beneficial for the device to mimic LTP with a high dynamic range. The energy consumption of this synaptic transistor is ~1 pJ at $V_D = 0.01$ V with a spike width of 200 ms, the energy consumption of which is 900 times smaller than conventional CMOS technology and approximated biological synaptic events [46,47]. However, such energy consumption must be further reduced to meet the requirements of neuromorphic computing. Synaptic devices on the basis of the hybrid structure of lead perovskites and other materials, such as organic semiconductors and metal oxides, have also been reported, and they successfully mimicked various synaptic functions and promoted the development of photosynapse transistors [43,44].

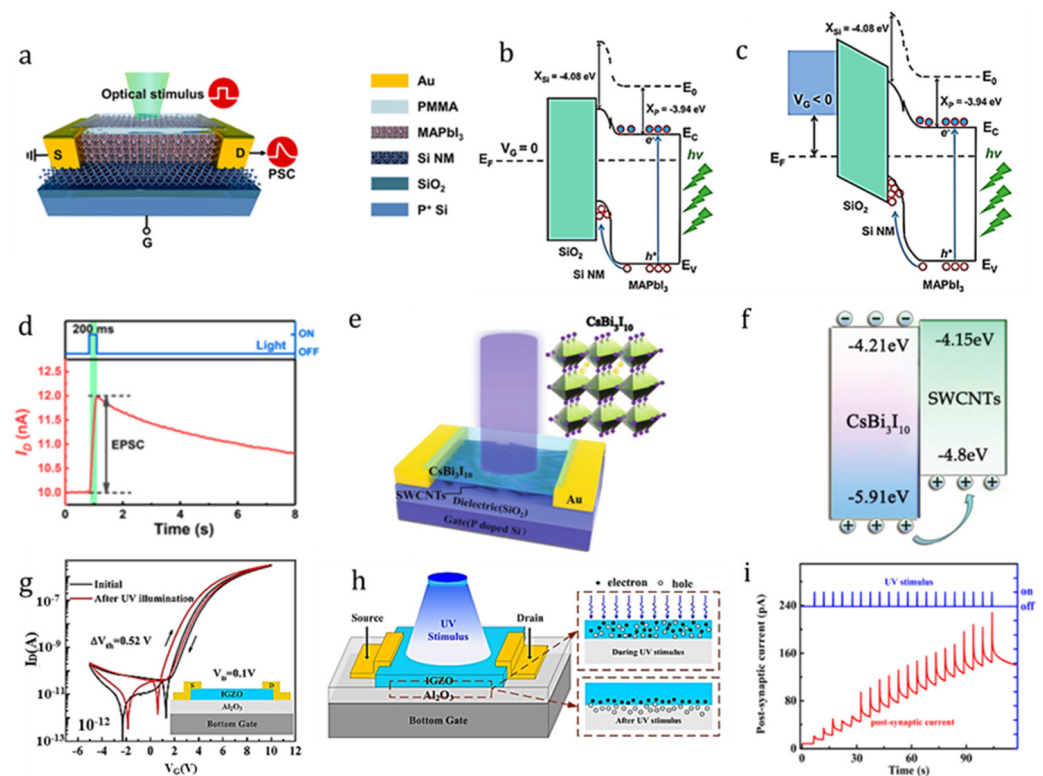


Figure 2. (a) Three-terminal synaptic device based on MAPbI₃ and silicon membrane. Band structure diagram of the (b) synaptic device at $V_G = 0$ and (c) $V_G < 0$. (d) EPSC response of the devices in response to an optical spike. Reproduced with permission from Ref. [42]; Copyright 2020 American Chemical Society. (e) Synaptic transistor based on the CsBi₃I₁₀/single-walled carbon nanotube (SWCNT) hybrid film. (f) Band diagram of the hybrid structure based on CsBi₃I₁₀ and SWCNTs. Reproduced with permission from Ref. [48]; Copyright 2019 WILEY-VCH. (g) Synaptic transistor and its transfer curves at initial state (black) and after ultraviolet (UV)-light illumination (red). (h) Carrier distribution in the device during and after UV-light illumination. (i) Postsynaptic current response of the device stimulated by consecutive UV-light pulses. Adapted with permission from Ref. [49]; Copyright 2018 Applied Physics Letters.

However, these lead perovskites are toxic and harmful to the environment [50–54]. Compared with traditional lead perovskite materials, lead-free perovskite materials have low toxicity and broad application prospects, which have attracted people’s attention [55–59]. Liu et al. fabricated a lead-free perovskite transistor based on CsBi₃I₁₀ and single-walled carbon nanotubes (SWCNTs), as seen in Figure 2e [48]. CsBi₃I₁₀ was used as the light absorption layer, and an SWCNT was used as the channel. Silicon wafer with a thermally grown SiO₂ on its surface was used as the substrate. SWCNT film was obtained by drop-casting (DC) its precursor solution onto the substrate. The CsBi₃I₁₀ thin film was prepared on the SWCNT using the SC technique. The TE technique was employed to grow Au electrodes on the SWCNT layer through a shadow mask. Based on a mechanism similar to the work of Pi et al. [42], the lead-free CsBi₃I₁₀/SWCNTs hybrid transistors can mimic synaptic functions, such as EPSC, PPF, and STP-to-LTP transition [60,61]. In addition, synaptic transistors utilizing bulk heterojunctions have been reported. For example, indacenodithiophene-co-benzothiadiazole (IDTBT) and [6,6]-phenyl-C61-butyric acid methyl ester (PCBM) materials were hybridized to prepare optoelectronic synaptic transistors via the SC method [19]. As a result of the formed bulk heterojunctions in this device, the synaptic behavior of EPSC/IPSC, PPF/PPD, and LTP/LTD was successfully mimicked.

Defects, including various atom vacancies and various dangling bands of nanocrystals, are common in materials that could trap carriers [62–64]. These defects contribute to carrier trapping and regulation of the conductivity in synaptic transistors. For example, a transistor synaptic device was developed by Li et al. on the basis of the structure of indium gallium zinc oxide (IGZO)/aluminum oxide (Al_2O_3) [49]. The schematic of this device structure and its transfer curves are demonstrated in Figure 2g. Through atomic layer deposition (ALD), a 30 nm thick Al_2O_3 film was obtained on the Si substrate. Meanwhile, a 50 nm IGZO thin layer was formed on the Al_2O_3 film via radio frequency magnetron sputtering (RFMS). A $20\ \mu\text{m}$ (length) \times $40\ \mu\text{m}$ (width) channel pattern was obtained through lithography and wet etching techniques. Then, the Au/Ti electrodes were deposited on the basis of this pattern through the electron beam evaporation (EBE) method in the transistor device. The transfer curves of the devices before and after ultraviolet (UV)-light illumination are demonstrated in Figure 2h. Following UV-light illumination, the transfer curve shifts to the left, indicating a drop in the device's threshold voltage (V_{th}). This decrease is attributed to the photogenerated holes that were captured by the oxygen vacancies in the Al_2O_3 films and/or the IGZO/ Al_2O_3 interface (Figure 2h). Based on this vacancy-trapping effect, postsynaptic currents of the device increased in response to the consecutive UV-light pulse (Figure 2i). Various synaptic functions, such as PPF and LTP, could be mimicked in this structure. Many synaptic devices have been investigated substantially and shown to mimic synaptic functions based on similar mechanisms [65–68]. It should be mentioned that charge-trap-flash-based synaptic transistors were successfully fabricated based on a silicon nitride film as the charge-trapping layer and a silicon film as the channel layer in transistor devices [69,70]. Some oxide materials were employed to be the dielectric layers in these devices. Defects in the silicon nitride layer are utilized as the carrier-trapping centers. This type-based synaptic devices have the advantages of nonvolatile memory, high reliability, and low variation properties, exhibiting the greatest commercialization application potentials for neuromorphic computing. This demonstrates that introducing defect states via special material selection and structure design in synaptic devices would help to trap the carriers and mimic synaptic functions. In addition, some works about synaptic transistors based on the ionization and deionization of oxygen vacancies have been reported and are discussed below [71,72].

2.2. Ionization and Neutralization of Oxygen Vacancies

Oxygen vacancies (V_o) are abundant in oxide semiconductors. The ionization and neutralization of V_o play critical roles for persistent photoconductivity (PPC) behavior. V_o could trap electrons; thus, when the oxide semiconductor materials are subjected to light with a photon energy greater than the energy gap from the neutral to ionized states, the ionization of V_o produces excess charges, which contribute to an increase in the conductivity of the oxide semiconductor. The reduction in conductivity through neutralization may take a long time because of the barrier to the neutralization of the ionized V_o [73,74]. Therefore, mimicking different synaptic activities can be achieved on the basis of the PPC effect in nanoscale metal-oxide-based transistor synaptic devices [75–77].

For example, Duan et al. demonstrated a synaptic device based on a nanoscale oxide semiconductor InGaCdO (IGCO) film, as shown in Figure 3a [78]. The radio frequency sputtering technique was employed to prepare the IGCO film on the SiO_2/Si substrate. The EBE technique was used to obtain the Ti/Au source/drain electrodes through a shadow mask. The obtained device, whose transfer curves are shown in Figure 3c, was $600\ \mu\text{m}$ in length and $800\ \mu\text{m}$ in width. The curves of the device revealed that its mobility values for the linear and saturation field regions are as large as 106 and $89.9\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$, respectively. These mobility values suggest that IGCO-based transistor synaptic devices have high optical response properties since the response and its mobility are positively related. In response to external optical spikes, the electrons can be directly excited when the photon energy is greater than the energy gap of V_o (left part of Figure 3b). Afterward, it is neutralized by overcoming its barrier after eliminating the optical spikes. When the photon energy is

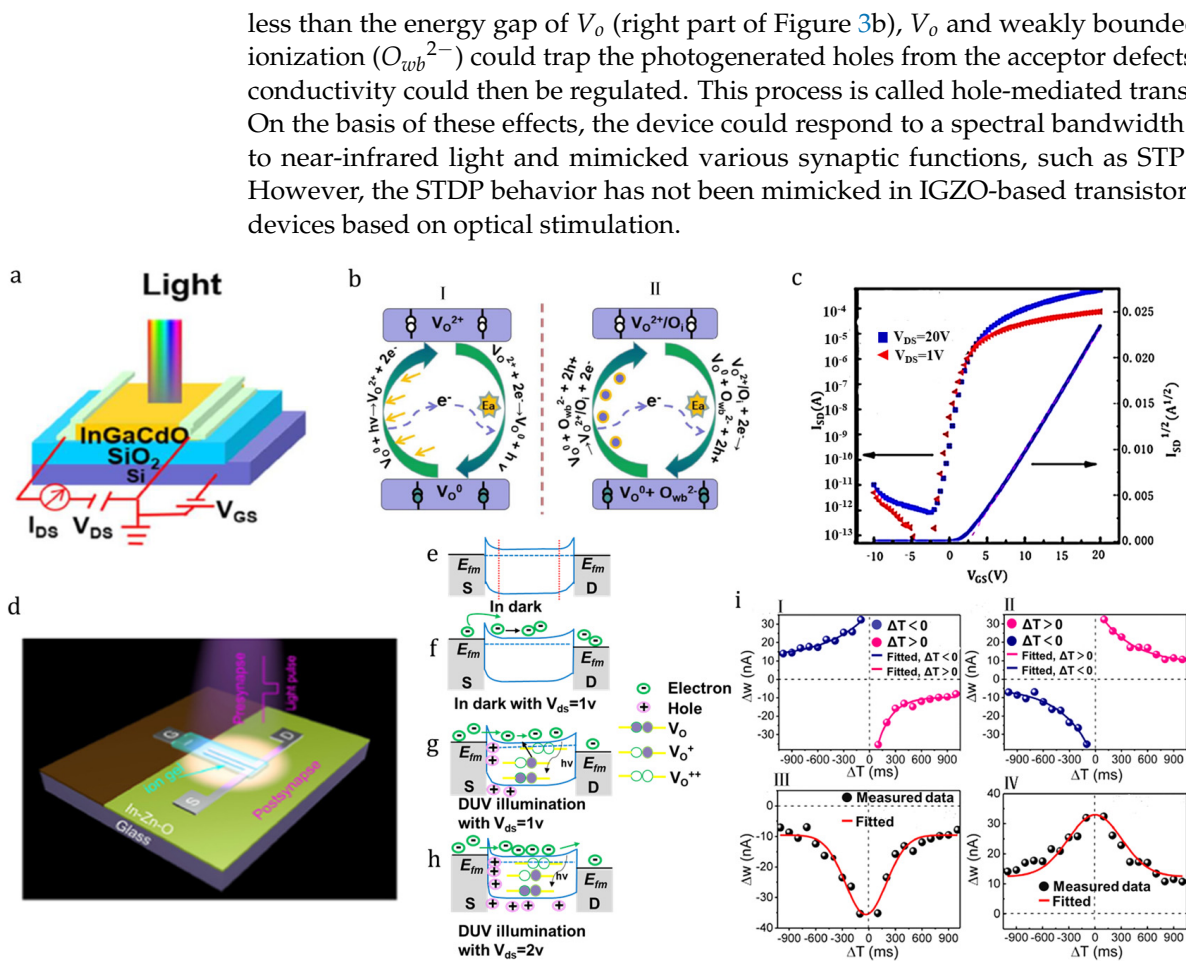


Figure 3. (a) Synaptic transistor based on IGZO. (b) Cyclic processes of ionization and neutralization for oxygen vacancies by (I) direct light-excited transitions and (II) hole-mediated transitions. (c) Transfer curves of this IGZO-based transistor device at $V_{ds} = 1$ (red) and 20 V (blue), respectively. Adapted with permission from Ref. [78]; Copyright 2020 WILEY-VCH. (d) Schematic of the InZnO phototransistor synaptic device. (e) Energy band diagram illustration of the Al/InZnO/Al device with $V_{ds} = 0$ V at $V_{gs} = -1$ V in a dark environment. Energy band diagram of the device with (f) $V_{ds} = 1$ V at $V_{gs} = -1$ V in a dark environment, (g) $V_{ds} = 1$ V at $V_{gs} = -1$ V under DUV illumination, and (h) $V_{ds} = 2$ V at $V_{gs} = -1$ V under DUV illumination. (i) Asymmetric and symmetric Hebbian learning STDP rule for the phototransistor synaptic device. Adapted with permission from Ref. [80]; Copyright 2018 Applied Physics Letters.

Interestingly, Wang et al. reported an oxide semiconductor InZnO phototransistor (Figure 3d), which can mimic STDP based on photoelectric synergy effects [80]. The InZnO layer was prepared on glass substrates through the SC method. The TE technique was used to deposit patterned Al electrodes on the InZnO layer through a shadow mask. A device with a channel size of 1600 μm (width) \times 80 μm (length) was obtained. The ion-gel dielectric as the gate terminal in the device was prepared on the InZnO layer based on the razor blade and transfer techniques using tweezers. The conductivity can be regulated through the gate terminal. A large photoresponse effect can be observed in the device when it is exposed to 275 nm of deep-ultraviolet (DUV) light. Synaptic functionalities, including EPSC, PPF, and photoelectric potentiation–depression functions, were successfully mimicked in the device based on its PPC and electrical erasing effects. Meanwhile, synaptic weights may be regulated by the synergistic actions of postsynaptic voltage spikes and presynaptic DUV light, thus achieving STDP. The working mechanism is explained in Figure 3e–h, which demonstrate the energy band of the InZnO–Al contact

in the device under dark or illuminated conditions. Specifically, Figure 3e shows the energy band alignment under dark conditions without V_{ds} and V_{gs} , indicating a symmetrical band structure. As shown in Figure 3f, the device used thermionic emission as the primary transport channel when it was biased at $V_{ds} = 1$ V for $V_{gs} = -1$ V. When the device was under DUV illumination (Figure 3g), electron–hole pairs were generated. Some holes were trapped by defect centers in the metal semiconductor interface region with the assistance of $V_{ds} = 1$ V, which resulted in a shrinking of the barrier width between Al and InZnO. When V_{ds} was increased to 2 V, additional photogenerated holes accumulated at the interface (Figure 3h), allowing increased electron injection due to the further narrowing of the barrier width. Therefore, the photogenerated carriers were modulated in the channel based on the synergism effects. Therefore, asymmetric STDP and symmetric STDP were obtained easily in response to external DUV optical and voltage pulses (Figure 3i (I–IV)), thus overcoming the biggest challenge for the realization of STDP learning rules in optoelectronic synaptic devices [81,82].

2.3. Ion-Gated Synaptic Transistors

Ions exist in the electrolyte dielectric layer of ion-gated transistors (IGTs), and these ions can be effectively utilized to modulate the channel conductivity in response to external spikes [83,84]. When a weak voltage (V_G) is applied to the gate terminal, positive or negative charges can accumulate at the interface of the electrolyte and semiconductor in the devices. These positive/negative charges include electrons and holes in the semiconductor materials and cations and anions in the electrolyte [85]. This accumulation at the interface regulates the channel conductance of the IGT; this phenomenon is called the electric double layer (EDL) effect. After the removal of the gate voltage, these charges can return to the initial state within a short time. STP can be mimicked in ion-gated synaptic transistors on the basis of this effect [86]. When a large voltage is applied to the gate electrode, the ions in the electrolyte can be inserted into the channel, leading to a phase transition change and resistivity switching [87], which can still be maintained for a long period even after the gate voltage is removed. This process is called the electrochemical doping effect, and LTP can be mimicked on the basis of this property in synaptic transistors [88].

A nanoscale tungsten–oxide (WO_3) thin-film transistor synaptic device (Figure 4a) was demonstrated by Yang et al. using the EDL and electrochemical doping mechanisms [89]. The 30 nm WO_3 thin film was used as the conductive channel, and it was grown on a $LaAlO_3$ substrate via pulsed laser deposition (PLD). Photolithography and argon–ion etching methods were used to form a channel pattern, which was employed to prepare a Cr adhesion layer (3 nm) and a Au layer (100 nm) through TE on the channel layer as electrodes. Subsequently, an ionic liquid DEME-TFSI was dropped onto the $500\ \mu\text{m}$ (length) \times $50\ \mu\text{m}$ (width) channel to complete the device. Figure 4b illustrates how $DEME^+$ ($TFSI^-$) ions in the ionic liquid (IL) accumulated at the IL/channel interface with a positive V_G that was less than the threshold value of the hydrolysis reaction (V_T). Once V_G was removed, the $DEME^+$ ($TFSI^-$) ions in the IL relaxed and merged within a short period. On the basis of this EDL effect, STP can be mimicked in the device. As shown in Figure 4c, the water molecules contaminated in the IL can be separated into protons and hydroxyls if V_G is larger than V_T . Even when V_G is eliminated, a stable H_xWO_3 phase is formed due to the proton-intercalation-induced change in valence from W^{6+} to W^{5+} . This method allows the device to mimic synaptic functions, such as EPSC, STDP, and STP-to-LTP transition. Many synaptic devices have been studied for neuromorphic computing based on these EDL and electrochemical doping mechanisms [90–95].

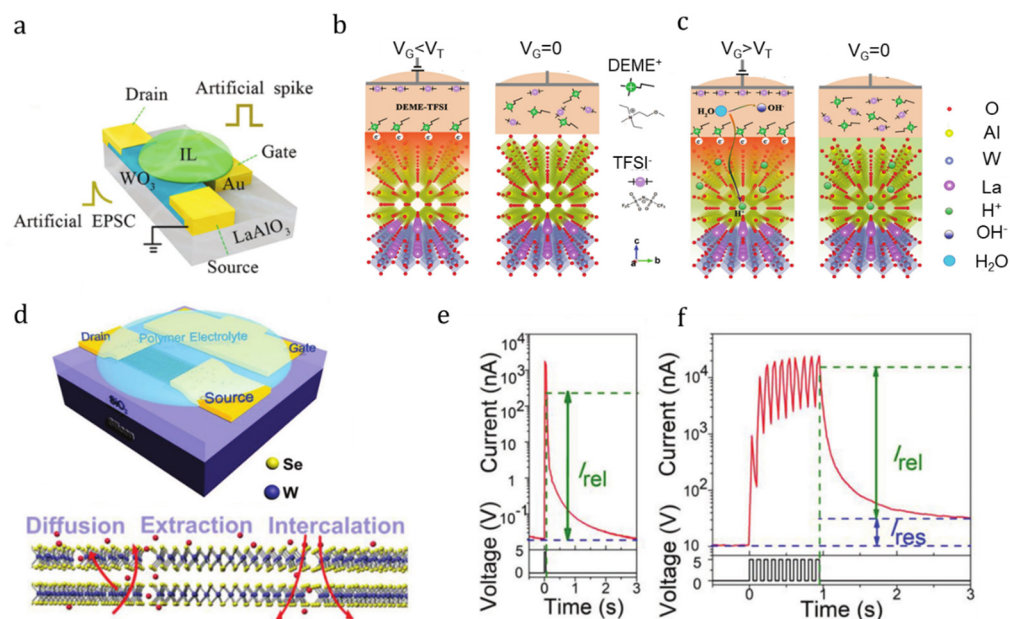


Figure 4. (a) Ion-gated WO_3 synaptic transistor device. (b) Ion dynamics at $V_G < V_T$ and $V_G = 0$ V for the ion-gated synaptic device. (c) Proton and hydroxyl dynamics at $V_G > V_T$ and $V_G = 0$ V for the ion-gated synaptic device. Adapted with permission from Ref. [89]; Copyright 2018 WILEY-VCH. (d) Ion-gated WSe_2 -based synaptic transistor and its working mechanism. (e) Current response of the device stimulated by a single 5 V pulse. (f) Current response of the device stimulated by consecutive 5 V pulses. Reproduced with permission from Ref. [96]; Copyright 2018 Wiley-VCH.

Synaptic transistors based on two-dimensional (2D) materials have also been investigated on the basis of these mechanisms. Using 2D α -phase molybdenum oxide (α - MoO_3) as the channel and an ionic liquid 1-ethyl-3-methylimidazolium bis-(trifluoromethanesulfonyl)-imide as the gate terminal, Yang et al. established a synaptic transistor [97]. A 2D α - MoO_3 was obtained using mechanical exfoliation and transfer techniques while the ionic liquid gate was prepared via the drip method. The TE process was employed to obtain Cr/Au (5 nm/60 nm) electrodes. This liquid might function as both the gate dielectric layer and a water electrolysis cell that provides protons and hydroxyls for the device, similar to the work of Jin et al. [89]. Therefore, this device can mimic the synaptic functions of EPSC, LTP, and LTD based on the same mechanism, with an energy consumption of 9.6 pJ per spike. Meanwhile, Zhu et al. demonstrated an ion-gated synaptic transistor based on the hybrid structure of a polymer electrolyte (LiClO_4 dissolved in polyethylene oxide) and WSe_2 (Figure 4d) [96]. The WSe_2 layer was obtained utilizing the ME and transfer methods. This layer was used as the channel in the device. The electrodes were prepared via EBE and then patterned via electron beam lithography. The polymer electrolyte layer was prepared through a DC method. Various behaviors, such as EPSC and STP, are mimicked on the basis of the same mechanism (Figure 4e,f). As a result of the small size advantage of the 2D WSe_2 materials, the energy consumption is approximately 30 fJ per spike. This energy consumption is similar to that of biological synapses in terms of magnitude, demonstrating great application potential in neuromorphic computing [7]. However, these synaptic transistors suffer from large-scale integration challenges due to the fluidity of their ionic liquid electrolytes. Subsequently, Yang et al. demonstrated an all-solid-state, environment-independent synaptic transistor with α - MoO_3 nanosheets as the channel [45]. In this device, Li ion-based solid dielectric materials were used as the gate terminal. This device can mimic synaptic functions, such as EPSC and LTP/LTD, on the basis of a similar mechanism. This solid dielectric avoids the fluidity drawback of liquid dielectrics, assuring that the all-solid-state transistor synaptic device exhibits excellent cycle-to-cycle and device-to-device variations (<12%), thereby promoting the development of ion-gated synaptic transistors in neuromorphic computing.

2.4. Ferroelectric Polarization

Recently, ferroelectric field effect transistors (FeFETs) have been investigated substantially as next-generation computing devices because they can exhibit excellent memory performances as synaptic devices [98]. Under external electrical stimulation, the polarized states are formed by separating the positive and negative charges in the ferroelectric materials; these states can regulate the conductivity of the materials [99,100]. After the removal of the applied electric field, the polarized states do not disappear instantaneously, indicating excellent memory properties. This characteristic leads to a superior multidomain polarization switching ability for ferroelectric materials; hence, ferroelectric multilevel channel conductance can be reached in FeFET devices [101–103]. These ferroelectric materials have then been used as a channel in FeFET-based synaptic devices [104–107]. For example, Tang et al. fabricated a ferroelectric synaptic transistor based on α -indium selenide (α -In₂Se₃) (Figure 5a) [108]. In₂Se₃ nanosheets were used as the channels and were obtained using a conventional Scotch tape-based exfoliation method and the transfer technique. The EBE technique was used to prepare the Ti/Pd metal electrodes on the In₂Se₃ layer through the mask. When a negative voltage was applied to the gate electrode of the resulting FeFET device, the positive charges were drawn to the lower surface of the In₂Se₃ layer, and the negative charges were repelled to the upper surface, as demonstrated in Figure 5b. This phenomenon is called out-of-plane (OOP) polarization. Meanwhile, in-plane (IP) polarization pointing from left to right could be formed if external voltage is applied in the source–drain electrodes, as illustrated in Figure 5c. The OOP and IP polarizations in α -In₂Se₃ materials can be coupled, and would cooperate to regulate the conductivity of the material [109–111]. This influence is reflected in Figure 5d,e, which demonstrate that I_{ds} can be regulated in response to external negative/positive gate spikes. When the gate voltage was removed, the ferroelectric polarization did not immediately relax back to its original state; thus, conductivity could be maintained for a while. Conductivity could be enhanced if a second gate voltage spike is introduced in this case. Based on these characteristics, this device could successfully implement the mimicking of synaptic functions such as EPSC, PPF, STP-to-LTP transition, and LTD. However, the dynamic range in this device was relatively small. Subsequently, Tang et al. substituted SiO₂ for HfO₂ as the gate dielectric in α -In₂Se₃-based synaptic transistors [112]. HfO₂ is a kind of high-k ferroelectric material, and a dynamic range of 158 was reached in the device based on this dielectric material.

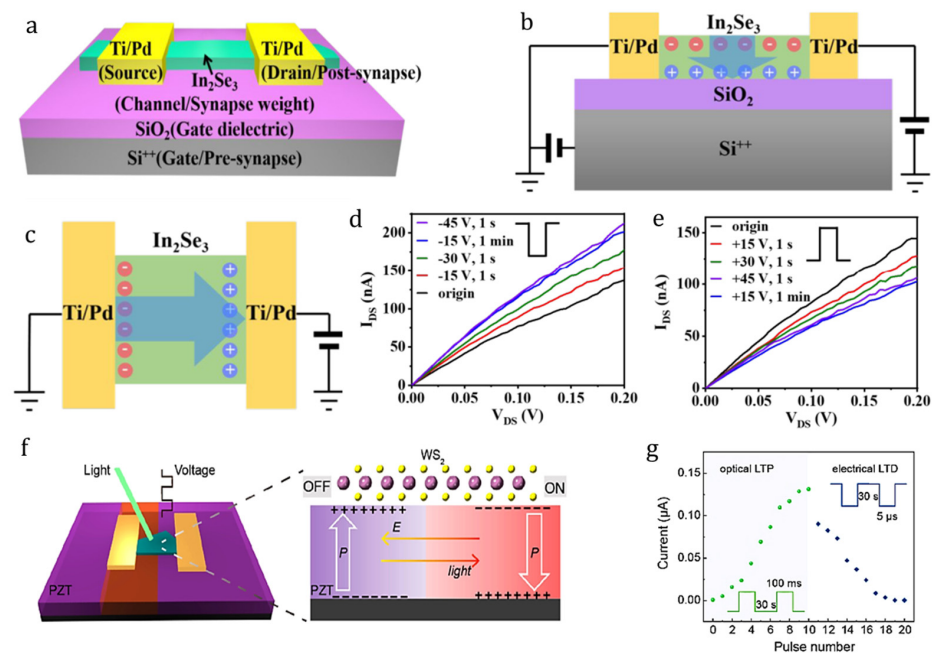


Figure 5. (a) Three-terminal In₂Se₃ synaptic transistor. (b) Ferroelectric polarization caused by the negative gate voltage in the out-of-plane (OOP) direction. (c) In-plane (IP) polarization induced

by the source–drain voltage. (d) $I_{DS}-V_{DS}$ curves measured at negative gate voltages. (e) $I_{DS}-V_{DS}$ curves measured at positive gate voltages. Reproduced with permission from Ref. [108]; Copyright 2020 American Chemical Society. (f) Optoelectronic synaptic device on the basis of WS_2 /PZT hybrid structure and its physical properties. (g) Optical potentiation and electrical depression synaptic behaviors of the device. Adapted with permission from Ref. [113]; Copyright 2020 American Chemical Society.

Ferroelectric materials can act as a dielectric layer in synaptic transistors [114–118]. Based on the characteristics of switchable polarization, a ferroelectric thin film as the gate dielectric can regulate the charge distribution and transport in the channel [119–121]. For example, Luo et al. fabricated a synaptic transistor on the basis of a bilayer structure of 2D semiconductor materials, WS_2 and ferroelectric $PbZr_{0.2}Ti_{0.8}O_3$ (PZT) thin film, as shown in Figure 5f [113]. The PZT thin films were fabricated on the $SrRuO_3$ -layer-buffered $SrTiO_3$ substrates via the PLD technique. WS_2 flakes were prepared onto the PZT films based on the Scotch tape-based ME and transfer techniques. Given the excellent optical absorption properties of the WS_2 film, its multilevel channel conductance values regulated with the aid of the permanent polarization PZT layer can be reached after applying optical pulses, as shown in Figure 5g. Interestingly, the conductance states of this WS_2 /PZT device can be erased by applying electrical pulses from the gate. Hence, the WS_2 /PZT transistors can respond to optical and electrical stimulus to mimic synaptic functions, such as EPSC, PPF, STP, LTP, and LTD. Numerous works on synaptic transistors based on PZT as gate terminals have been reported [122,123]. However, PZT is toxic owing to its lead content, which may limit its application. Jerry et al. prepared a synaptic transistor based on a lead-free ferroelectric material $Hf_{0.5}Zr_{0.5}O_2$ (HZO), which was used as the ferroelectric dielectric layer in the device [124]. HZO was first prepared via the ALD technique and its multiple ferroelectric domains were formed after annealing at 600 °C. Appropriate gate voltage pulses can partially polarize the multiple ferroelectric domains of HZO, which then regulate the conductance of the channel. STDP was then successfully mimicked in HZO-based synaptic transistors based on its excellent polarization properties.

To realize the applications of these transistor-based synapses in neuromorphic computing, a neural network system based on synaptic transistors is needed. Currently, system integration of array synaptic transistor devices with various logic circuits based on NAND, AND, as well as NOR gates has been implemented for constructing the neural network system [125–129]. These synaptic transistors mainly conduct the computing based on the mechanisms of carrier trapping, ion-gated effects, and ferroelectric polarization. These constructed systems have comparable long-term-memory properties. The ferroelectric-based synaptic system exhibits the lowest switching voltages; the ion-gated synaptic system has the largest dynamic range update property among the three array networks. However, the synaptic parameters for these systems such as device size, energy consumption, and synaptic linearity still need to be further optimized.

3. Perspectives

The development of transistor synaptic devices has promoted the realization of brain-like computing. These devices have been fabricated on the basis of different materials, such as Si NMs, carbon nanotubes, nanoscale metal oxides, 2D materials, perovskite materials, and ferroelectric materials [130–132]. These materials have demonstrated great physical properties and are used as channel layers and active materials. They are mainly prepared using physical deposition methods (e.g., sputtering, evaporation techniques, PLD) and chemical methods (e.g., ALD, SC, and DC). Some 2D materials are mainly obtained through ME and transfer techniques. Meanwhile, lithography, etching, and masking methods are used to prepare nano/microscale patterned electrodes for these devices. PLD and ALD can grow high-quality thin films; there is a high-speed film deposition advantage for the magnetron sputtering technique; the cost is low for the SC method; and lithography and etching methods are necessary for obtaining nanoscale array systems.

These methods demonstrate great application potential in preparing high-quality synaptic transistor devices that could mimic some basic biological synaptic plasticity functions, such as STP, LTP, LTD, SRDP, and STDP. Some progress in their synaptic properties has been achieved in these devices, benefiting from the excellent physical properties of these low-dimensional materials. However, the synaptic properties, including the dynamic range, linearity, size, energy consumption, and mimicking of inhibitory plasticity functions, still need to be improved for most devices. To clearly illustrate the synaptic properties, key synaptic parameters for these devices based on various mechanisms are demonstrated in Table 1.

Table 1. Property parameters of various synaptic transistors based on various mechanisms. SC, RFMS, TE, EBE, PLD, ALD, DC, and ME refer to spin coating, radio frequency magnetron sputtering, thermal evaporation, electron beam evaporation, pulse laser depositing, atomic layer deposition, drop casting, and mechanical exfoliation, respectively. S is the area magnitude of the devices; E indicates the energy consumption magnitude of the devices.

Mechanisms	Fabrication Processes	S (μm^2)	E (pJ)	Dynamic Range	Linearity	Ref.
Capture and release of carriers	SC/RFMS/TE/EBE/ALD	$\sim 10^2 \sim 10^4$	$\sim 10^{-4} \sim 10^2$	$\sim 2 \sim 11$	Poor for $\sim 55\%$	[42–45,48,49,56,65–67,133]
Ionization and neutralization	SC/RFMS/TE/EBE/DC	$\sim 10^3 \sim 10^5$	$\sim 10^{-2} \sim 10^1$	$\sim 1.5 \sim 45$	Poor for $\sim 86\%$	[76–82]
Ion-gated effects	SC/TE/EBE/ALD/DC/ME/PLD	$\sim 10^4 \sim 10^5$	$\sim 10^{-2} \sim 10^2$	$\sim 1.1 \sim 7$	Poor for $\sim 71\%$	[89,90,92,94–97,134]
Ferroelectric polarization	SC/EBE/ALD/ME/PLD	$\sim 10^1 \sim 10^4$	$\sim 10^{-2} \sim 10^2$	$\sim 1.3 \sim 158$	Poor for $\sim 44\%$	[108,112–116,122–124]

The dynamic range, referring to the ratio of high-to-low current values, should be at least 100 when working as a biological synapse device [135]. Currently, the dynamic ranges for most devices are below 10 [136–138], indicating that they are still far from meeting application requirements. The synaptic currents for most devices exhibit nonlinear response properties, which are not conducive to information processing in brain-like computing [139]. The response properties should be as linear as possible with the number of pulses. So far, the size of most synaptic transistor devices is still at the micrometer scale [140–142], which is not beneficial for device integration and energy conservation [143]. Nanoscale synaptic transistor devices with a high integration density are required for the system's application. However, this application is limited to their energy consumption because they consume magnitudes of picojoules for most single synaptic transistor devices. Furthermore, most synaptic devices hardly mimic inhibitory synaptic plasticity due to the decay time limitation of the response current. The lack of mimicking inhibitory synaptic plasticity strongly hinders their application in pattern recognition. Currently, all characteristic times of the synaptic current response are on the order of 0.1–1 s for most reported transistor synaptic devices. It is clear that this level of performance cannot yet compete with biological neurons.

The above problems in these devices are highly related to the photo-, electric-, or dual-driven response properties, which are mainly determined by the type of material utilized in the devices. To overcome these challenges, various means have been employed to address the barriers. A diagram of potential avenues based on these challenges and their expected achievements is clearly seen in Figure 6. In principle, excellent photo-, electric-, or dual-driven response properties for devices with strong carrier-trapping capabilities are required for synaptic devices. Based on these specific conditions, low-dimensional hybrid functional materials must be developed by regulating the composition, phases, and defects to improve their response and trapping properties. Moreover, an appropriate device design must be able to improve these properties. For example, bilayer hybrids of superior photon-response materials, such as perovskite and high-mobility channels (e.g., 2D materials in

the transistor), are conducive to carrier separation and resistivity change. The ability to capture charge carriers in the device can be promoted by introducing a silicon nitride film with excellent trapping capabilities or an ion-migration-blocking layer, which promotes the mimicking of inhibitory synaptic functions. However, clarifying memory mechanisms for different material structures and device designs is still needed, which leaves room for further research efforts in the areas of theoretical and experimental methods. This may provide ideas for designing suitable low-energy defect centers so that magnitudes for the synaptic response and decay behaviors can be achieved at the microsecond and millisecond, respectively. This would assure the operation of a neural network with high efficiency. Deep energy defect centers may be introduced through the device structure design based on some specific active materials for ferroelectric and ion-gated effects and silicon nitride materials for carrier-trapping effects in these devices. These efforts would promote the achievement of nonvolatile analogues in these devices. In addition, high-quality thin film preparation is needed because it is beneficial for the preparation of nanoscale synaptic sizes with good uniformity. The preparation of advanced nanoscale synaptic transistor devices relies on specific fabrication processes to reach improved compatibility. Hence, further studies must develop suitable preparation techniques for fabricating these devices. For example, the various processes discussed above may be cross-referenced.

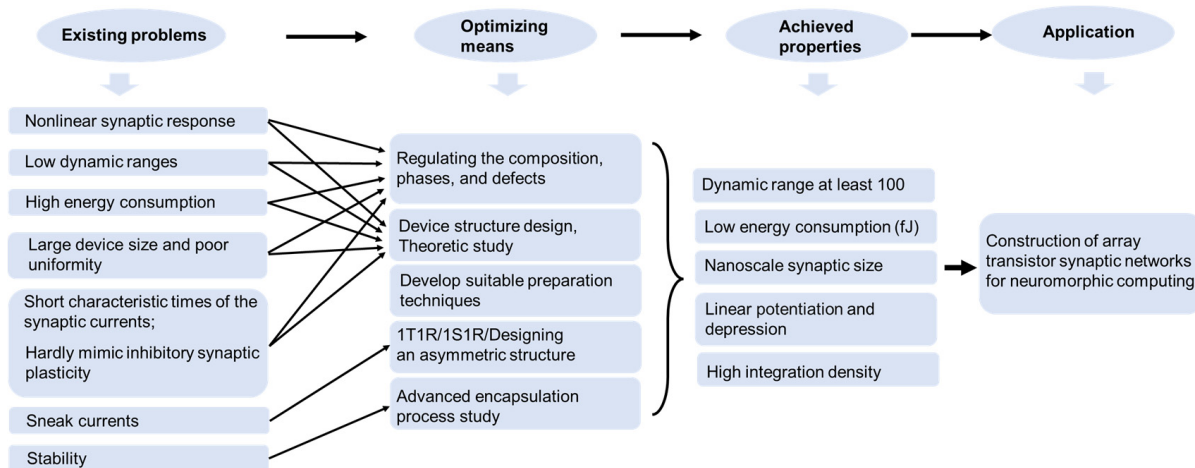


Figure 6. A diagram demonstrating the challenges, methods, and achieved properties for transistor synaptic devices and neuromorphic computing systems.

Sneak currents may exist in synaptic transistor array systems and influence system recognition. Except for the methods of 1T1R or 1S1R (a transistor or a selector connected in series with a memristor) technology, designing an asymmetric structure through changing electrodes and regulating doping in the channel may restrain the sneak currents in the systems, thereby promoting the application of synaptic transistors in neuromorphic computing. Stability properties are significant for device application. Si NMs, nanoscale metal oxide-based semiconductors, and ferroelectric materials have the advantages of excellent water/oxygen-resistant properties and efforts should be made to improve their synaptic properties for neuromorphic computing. Furthermore, a hardware transistor neuromorphic network is basically an array system, which calls for studies of advanced encapsulation processes for its final application. These endeavors would significantly promote the development of transistor synapses for future computing.

4. Conclusions

This study reviewed the working mechanisms and synaptic behaviors of transistor-based synaptic devices on the basis of various low-dimensional materials. Various preparation processes that are used to obtain these synaptic devices were also analyzed. Various important synaptic functions including STP/STD, LTP/LTD, SRDP, and STDP, were mim-

icked on the basis of the different mechanisms in these transistor-based synaptic devices. However, some efforts are still needed to improve synaptic properties, such as dynamic range, linearity, energy consumption, device size, and trapping abilities, and eventually fulfill their requirements for use as synaptic devices for neuromorphic computing. Further studies must be conducted from the perspective of material and device structure design, device manufacturing processes, and theoretical research. For example, silicon nitride materials, due to their excellent carrying capturing capabilities and commercialization application potentials, could be considered as trapping centers for designing perovskite and other optoelectronic material-based synaptic transistors. The simple and low-cost SC preparation method should be optimized for obtaining high-quality perovskite and other films. The design of the trapping energy level could be implemented from theoretical research to satisfy the decay time requirements of the devices. These schemes are expected to contribute substantially to the large-scale development of transistor-based synaptic devices in neuromorphic computing.

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