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Molecular Dynamics Simulation of Nanoscale Abrasive Wear of Polycrystalline Silicon

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Abstract: In this work, molecular dynamics simulations of the nanoscratching of polycrystalline and singlecrystalline silicon substrates using a single-crystal diamond tool are conducted to investigate the grain size effect on the nanoscale wear process of polycrystalline silicon. We find that for a constant indentation depth, both the average normal force and friction force are much larger for single-crystalline silicon compared to polycrystalline silicon. It is also found that, for the polycrystalline substrates, both the average normal force and friction force increase with increasing grain size. However, the friction coefficient decreases with increasing grain size, and is the smallest for single-crystalline silicon. We also find that the quantity of wear atoms increases nonlinearly with the average normal load, inconsistent with Archard's law. The quantity of wear atoms is smaller for polycrystalline substrates with a larger average grain size. The grain size effect in the nanoscale wear can be attributed to the fact that grain boundaries contribute to the plastic deformation of polycrystalline silicon.

Keywords: molecular dynamics; nanoscale wear; polycrystalline silicon

1. Introduction

Silicon has been the material most commonly used in microelectromechanical systems (MEMS). However, high wear has been one of the major barriers to the development and commercialization of silicon-based MEMS [1–3]. Therefore, in the past decades, great efforts have been made to study the wear mechanisms of silicon. Most of the previous studies analyzed the wear process based on the classic Archard's law [4], which describes the worn volume as proportional to both the applied load and the sliding distance. However, recent studies have shown that the nanoscale wear processes cannot be fully described by Archard's wear law [5–7]. For example, the wear rate is typically not constant for the nanoscale wear of single-crystal silicon tips [5–10]. In particular, the recently proposed atom-by-atom wear mechanism was used to explain the wear of single-crystal silicon tips sliding on a polymer surface [5] and a diamond surface [7]. In addition, Alsem et al. studied the sliding wear mechanisms using polycrystalline silicon friction MEMS specimens [11,12]. Bhushan et al. carried out nanoscratching tests on silicon (100), specifically doped and undoped polysilicon at normal loads ranging from 20 to 100 μ N [13,14]. They found that the scratch depth for silicon (100) was smaller than that for the undoped polysilicon. Chung et al. also performed experiments to evaluate the wear coefficients of silicon (100), silicon oxide, silicon nitride, and polysilicon under 100 µN normal load. They found that the average wear coefficient of silicon (100) was smaller than that of polysilicon [15].

In addition to experimental investigations, molecular dynamics (MD) simulations have also been used to explore the nanoscale deformation and wear mechanisms of silicon [16–22]. Zhang et al. found scratching induced amorphous phase transformation in single-crystal silicon [16]. Nanoscale abrasive wear on single-crystal silicon has been studied using large-scale MD [17]. In addition, MD simulations have been carried out to investigate the nanoscale cutting of single-crystal silicon, and amorphous phase transformation has been observed [18,19]. Chrobak et al. found that the plasticity of bulk silicon is dominated by phase transformations, whereas that of silicon nanoparticles is dislocation-driven [20]. Recently, Goel et al. found that phase transformation is the primary plastic deformation mechanism in the nanoindentation deformation process of polycrystalline silicon using MD simulation and experimentation [21]. Goel et al. also investigated the cutting process of polycrystalline silicon using MD [22].

Overall, so far, most of the studies in the literature have focused on the mechanical and wear behaviors of single-crystal silicon, although some work has been done to study the deformation and wear process of polycrystalline silicon [13–15,21,22]. In addition, it is well-known that grain refinement is a promising way of improving the friction- and wear-resistance of metals [23,24]. However, to our best knowledge, at present, a study that investigates how the grain size affects the friction and wear behaviors of polycrystalline silicon is still lacking, even though polycrystalline silicon is extensively used in most real-world applications (e.g., solar cell substrates). This study is intended to fill this gap. As MD simulation can capture atomic details of the wear process, MD simulation has been a powerful tool to study the mechanisms of nanoscale wear [25]. Therefore, in this work, MD simulations of the nanoscratching process of single-crystal and polycrystalline silicon using a diamond tool are performed to explore the effects of grain size on the wear behaviors of polycrystalline silicon.

2. Simulation Details

In this work, MD simulations were carried out using the large-scale atomic/molecular massively parallel simulator (LAMMPS) [26]. We analyzed the simulation results using OVITO [27]. The simulation model consisted of a hemispherical rigid single-crystal diamond tool and a silicon substrate (Figure 1). The hemispherical diamond tool created from perfect diamond atomic lattices had a radius of 5 nm. The single-crystal silicon substrate had the three crystal orientations of *x*-[100], *y*-[010], and *z*-[001]. The scratching was conducted on the (001) surface along the [-100] direction. To address the effect of grain size on the wear, polycrystalline silicon substrates with average grain size ranging from 2 to 5 nm were generated by Voronoi tessellation code [21,22,28]. Dimensions of single-crystalline silicon and polycrystalline silicon with different average grain sizes are listed in Table 1.

Average Grain Size (nm)	Length (nm)	Width (nm)	Height (nm)	Number of Atoms
Single crystal	35.9	17.9	8.0	261,360
2	36.6	18.3	8.2	259,880
3	36.4	18.2	8.2	259,812
4	36.3	18.2	8.2	259,582
5	36.2	18.1	8.2	259,634

Table 1. Dimensions of single-crystalline silicon and polycrystalline silicon with different average grain sizes.

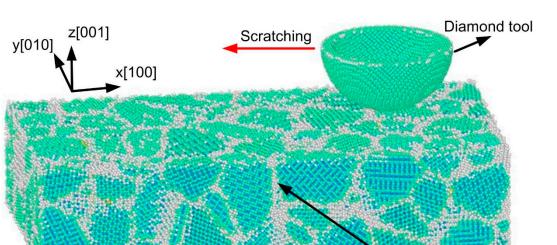


Figure 1. Molecular dynamics (MD) simulation model of the wear of polycrystalline silicon.

The silicon substrates were divided into three different areas: boundary atoms, thermostat atoms, and Newtonian atoms. Atoms in the bottom 0.5-nm region of substrate were kept fixed in space as boundary atoms. Atoms in the 1-nm-thick region of substrate adjacent to the boundary atoms were thermostat atoms. The thermostat atoms were kept at a constant temperature of 300 K using a velocity scaling method [29] to mimic the heat dissipation in real wear processes. The velocity scaling method obtains the desired target temperature by rescaling the velocities of thermostat atoms with the same factor α (equal to the square root of the ratio of target temperature to the temperature of thermostat atoms) [29]. The remaining substrate atoms were Newtonian atoms that moved freely according to interatomic forces. The equations of motion were integrated with a velocity-Verlet algorithm. The time step was 1 fs. Periodic boundary conditions were imposed in the *x* and *y* directions.

Interatomic forces between silicon atoms in the substrate were depicted by the Tersoff potential [30], which has been widely used to study the deformation behaviors of silicon [16–19,31]. The interactions between tool atoms were ignored since the tool was treated as a rigid body. The interaction between silicon and diamond tools was modeled by the widely used Morse potential [32]:

$$V(r) = D(e^{-2\alpha(r-r_0)} - 2e^{-\alpha(r-r_0)}),$$
(1)

Grain boundaries

where V(r) is a pair potential energy function; D is the cohesion energy; α is the elastic modulus; and r and r_0 are the instantaneous and equilibrium distance between two atoms, respectively. The cutoff radius of the Morse potential was 10.0 Å. The Morse potential parameters [17–19,31,33] were given as D = 0.435 eV, $\alpha = 4.6487$ Å⁻¹, and $r_0 = 1.9475$ Å.

In the simulations, the diamond tool was initially positioned above the silicon substrate surface. After the system was fully relaxed, the tool moved downward to the silicon substrate until a desired scratching depth was reached, and then scratched the surface along the negative *x* direction. Note that the indentation and scratching velocities reported in the references are on the order of 1–200 m/s for most MD simulations to save computational costs [33–39]. In this work, both the indentation velocity and scratching velocity were 100 m/s.

3. Results and Discussion

Figure 2 shows the typical deformation behavior of a polycrystalline silicon substrate for different scratching distances at the scratching depth of 2 nm. We observed bct5 phase with fivefold coordination and β -Si phase with sixfold coordination around the tool in the substrate during the nanoindentation and nanoscratching process. This clearly suggests the occurrence of a pressure-induced phase transformation. In addition, no pile-up was observed in the nanoindentation process. However,

we could see a ridge in the sides of the tool and pile-up in front of the tool in the scratching process (Figure 2b,c). Moreover, we observed some elastic recovery in the substrate behind the tool as the tool slid.

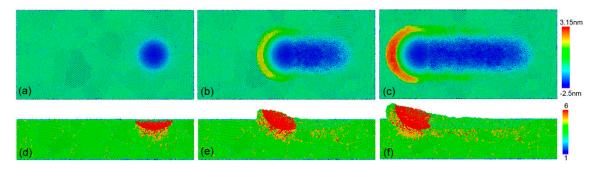


Figure 2. Deformation behavior of a polycrystalline silicon substrate with average grain size of 4 nm for the scratching distance of 0 nm (**a**,**d**); 10 nm (**b**,**e**); and 20 nm (**c**,**f**) at the scratching depth of 2 nm. In the figures (**a**–**c**), atoms are colored according to their heights in the *z* direction, while in the figures (**d**–**f**) atoms are colored according to the coordination number. (**a**–**c**) are top views and (**d**–**f**) are front views of the polycrystalline silicon.

To study the effect of grain size on the wear process of polycrystalline silicon, we firstly recorded the variations of friction force and normal force for polycrystalline silicon substrate and single-crystal silicon substrate in the wear process, as shown in Figure 3. The forces were calculated by summing the atomic forces of substrate atoms on the tool atoms. The friction force and normal force are defined as the forces parallel to the x direction and the z direction, respectively. Figure 3a, b shows the variation of the typical friction and normal force during the nanoscale wear of silicon substrates. It can be seen that at the initial stage, the friction force increased gradually while the normal force decreased. Then, both the friction force and normal force fluctuated around a constant value. This was mainly due to the change of contact area (number of contact atoms) during the scratching process. It is well known that the friction force and normal force are closely related to the transverse contact area (projected in the scratching direction) and normal contact area (projected in the normal direction), respectively. In the initial stage of scratching, the normal contact area decreased while the transverse contact area increased due to the pile-up in front of the tool. After that, the wear reached a steady stage. The fluctuation of forces during the wear process results mainly from the thermal motion of substrate atoms and plastic deformation. In order to gain deeper insights, we calculated the average friction force and average normal force for polycrystalline and single-crystalline silicon substrates (Figure 3c,d). The friction coefficient [40,41] defined as the ratio of the average friction force to average normal force was also obtained (Figure 3e,f). The average forces were calculated for the scratching distance from 5 to 20 nm where wear was in a steady state. It could be found that for a constant scratching depth, both the average normal force and the friction force were much larger for single-crystalline silicon compared to polycrystalline silicon, which is consistent with the experiments [13,14] and simulation results [22]. It was also found that for the polycrystalline substrates, both the average normal force and the friction force increased with increasing grain size. However, the friction coefficient decreased with increasing grain size, and was the smallest for single-crystalline silicon.

Note that for metals, the friction coefficient generally increases linearly with scratching depth, as predicted by Bowden and Tabor [42]. However, the friction coefficient for single-crystal silicon showed a rather complicated relationship with scratching depth, as shown in Figure 3f. The friction coefficient first decreased and then increased slightly with scratching depth. This was due to the fact that the friction force grew more slowly than the normal force as the scratching depth increased from 0.5 to 1 nm. Si et al. observed a similar tendency in the scratching of single-crystal silicon using MD simulations [43]. However, the friction force underwent a slightly faster increase than the normal force for scratching depths between 1 and 2.5 nm (Figure 3c,d).

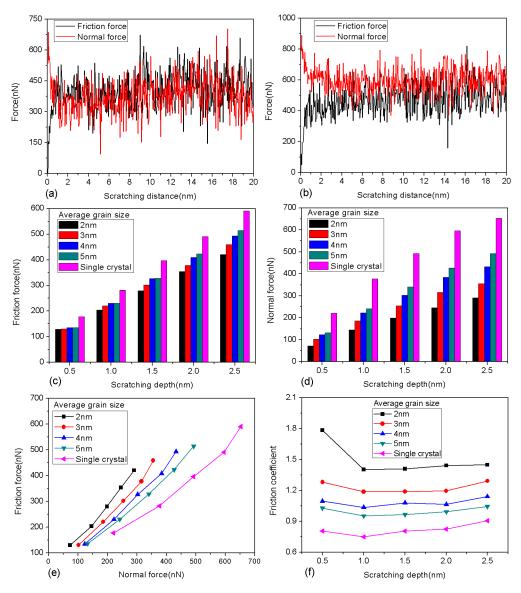


Figure 3. The friction force and normal force for polycrystalline silicon substrates and single-crystal silicon substrate. (**a**,**b**) The force–distance curves for the polysilicon substrate with an average grain size of 4 nm and single-crystal silicon substrate, respectively, at the scratching depth of 2 nm. (**c**,**d**) The variation of the average friction force and normal force for polycrystalline silicon substrates with different average grain sizes and single-crystal silicon substrate, respectively. (**e**) The value of average friction force as a function of normal load. (**f**) The friction coefficient of polycrystalline silicon substrates and single-crystal silicon substrate as a function of scratching depth.

To quantitatively describe how the wear of polycrystalline silicon depends on the grain size, we calculated the number of wear atoms during the wear process. In this work, the substrate atoms that moved on top of the original substrate surface were considered as wear atoms [44]. This is equivalent to the measurements of groove volume or groove depth [45] widely used in wear experiments [24,46]. The quantity of wear atoms was directly proportional to the scratching distance for all the silicon substrates and scratching depths (Figure 4). This is because the wear volume (i.e., total volume of wear atoms) was essentially equal the groove volume on the substrate surface [45]. Furthermore, we present the relation between the quantity of wear atoms and the average normal force for all the substrates in Figure 4f. We observed that the quantity of wear atoms increased nonlinearly with the average normal force, inconsistent with Archard's law [6–9,47]. This suggests that Archard's law is inadequate for describing nanoscale single-asperity wear of silicon substrate. In fact, Archard's law is

a purely empirical equation. Although Archard's law has been widely used at the macroscale, it has been proven that it fails to model the nanoscale wear mechanisms of silicon (e.g., the atom-by-atom wear process) [7–9]. Under the same normal load, the quantity of wear atoms was smaller for polycrystalline substrates with a larger average grain size for the normal loads studied. Moreover, under the same normal load, the quantity of wear atoms of single-crystalline silicon substrate was smaller than that of polycrystalline substrates, which is consistent with the wear experiments by atomic force microscopy [15].

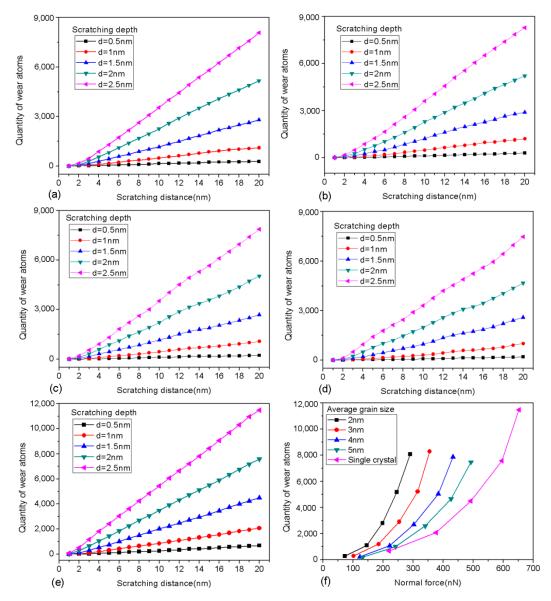


Figure 4. Data plots for the quantity of wear atoms. (**a**–**d**) The wear relations of polycrystalline silicon substrates with average grain sizes of 2 nm, 3 nm, 4 nm, and 5 nm, respectively. (**e**) The wear relation of single-crystal silicon substrate. (**f**) The quantity of wear atoms as a function of normal load for different silicon substrates.

To explore the underlying mechanisms behind the effect of grain size on the nanoscale wear of polycrystalline silicon, we analyzed the typical deformation behaviors of polycrystalline silicon (Figure 5). We employed OVITO to identify the diamond structure of silicon [22,24]. It was found that in the wear process, the occurrence of plastic deformation (amorphization) of polycrystalline silicon tended to be along the grain boundaries [21]. In addition, a previous simulation has shown that grain boundaries can reduce the critical stress of plastic deformation of silicon [22]. As a result,

plastic deformation takes place more easily for substrates with a smaller average grain size, since the number of grain boundaries is larger for polycrystalline silicon with a smaller grain size. Therefore, both the average friction force and the normal force decreased with the decrease of the average substrate grain size, as shown in Figure 3. This also explains why the quantity of wear atoms increased with the decrease of the average substrate grain size, as shown in Figure 4. Note that the grain size effect of silicon contradicts the Hall–Petch relation. This is because the Hall–Petch effect (grain-boundary strengthening effect) results from the dislocation–dislocation interactions. However, in our simulations of silicon, the main plastic deformation mechanism was not the generation and movement of dislocations.

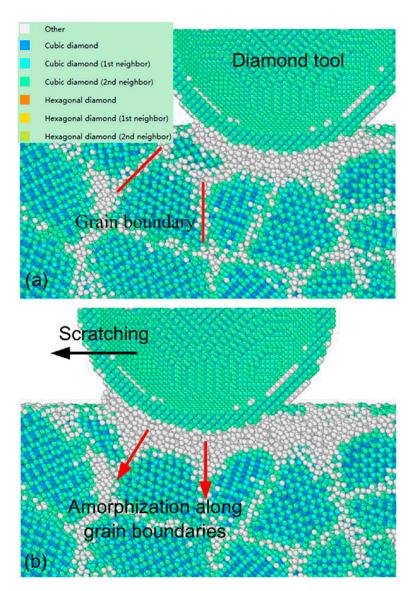


Figure 5. Deformation behavior of a polycrystalline silicon (**a**) and the amorphization of silicon along the grain boundary (**b**). Here the average substrate grain size is 4 nm. The scratching depth is 1 nm. Atoms are colored using theIdentify diamond structure module in OVITO.

4. Conclusions

In this work, MD simulations of the nanoscratching of polycrystalline and single-crystalline silicon substrates using a single-crystal diamond tool were performed to investigate the effect of grain size on the nanoscale wear process of polycrystalline silicon. It was found that for a constant scratching depth, both the average normal force and friction force were much larger for single-crystalline silicon

compared to polycrystalline silicon. Furthermore, for the polycrystalline substrates, both the average normal force and friction force increased with increasing grain size. However, the friction coefficient decreased with increasing grain size, and was the smallest for single-crystalline silicon. We also found that the quantity of wear atoms increased nonlinearly with the average normal force, inconsistent with Archard's law. In the wear process, the pressure-induced phase transformation took place around the tool. The fact that grain boundaries contribute to the occurrence of plastic deformation of polycrystalline silicon can explain the grain size effect in the nanoscale wear of polycrystalline silicon.

Author Contributions: P.Z. designed the simulation cases. P.Z. and H.Y. conducted the simulation. P.Z. wrote the paper. P.Z., R.L. and H.Y. discussed the results and revised the paper.

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Conflicts of Interest: The authors declare no conflict of interest.

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