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Monotype Organic Dual Threshold Voltage Using Different OTFT Geometries

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Abstract: It is well known that organic thin film transistor (OTFT) parameters can be shifted depending on the geometry of the device. In this work, we present two different transistor geometries, interdigitated and Corbino, which provide differences in the key parameters of devices such as threshold voltage (V_T), although they share the same materials and fabrication procedure. Furthermore, it is proven that Corbino geometries are good candidates for saturation-mode current driven devices, as they provide higher I_{ON}/I_{OFF} ratios. By taking advantage of these differences, circuit design can be improved and the proposed geometries are, therefore, particularly suited for the implementation of logic gates. The results demonstrate a high gain and low hysteresis organic monotype inverter circuit with full swing voltage at the output.

Keywords: OTFT; interdigitated; Corbino; dual-threshold inverter; modelling; simulation

1. Introduction

Organic thin film transistors (OTFTs), employing organic dielectric and semiconductor layers, show considerable competitive advantages over their inorganic counterparts, such as low cost, low temperature processing and light-weight [1,2]. Compared with the conventional silicon dioxide-based devices, OTFTs with polymer dielectrics and blends of small-molecule semiconductors are ideally compatible with flexible substrates and solution processes. Apparently, solution-processable materials are very attractive because they are compatible with spin-coating, drop casting and printing technologies at room temperature and under ambient conditions. Meanwhile, this capability has practical advantages when coupled with photolithographic processes as a patterning techniques enable high-resolution, smaller process variations [3] and high-throughput [4]. By virtue of their excellent solution processability together with promising large-area coverage, OTFTs are attractive candidates in diverse applications [5–10], such as flexible displays [10,11] and radio frequency identification (RFID) [12], among others. Research on organic circuits has addressed in the last decades the development of inverters [13,14], logic gates, shift registers [14,15] and amplifiers [16–18]. In the majority of the works reporting organic circuits, the most widespread technology is single-threshold voltage (V_T) p-type only [19]. Although the most favourable route to obtain robust organic circuitry involves using organic complementary technology, this requires the matching of the n-type material in device performance which has proved difficult for complex circuits from a technological point of view [20]. Recently, the more widespread technology used to address the robustness of the organic circuits has been dual-V_T using only p-type organic semiconductors (OSC). Over recent years, several approaches have been elaborated in order to tune the electrical parameter V_T. For that purpose, two main routes have been considered: using chemical reactions at the dielectric/OSC interface or by modifying the OTFT geometry. For the former route, some examples include local chemical-doping

of the channel [21], chemical modification of the channel interface through self-organizing polymer blending [22–24], and ultraviolet (UV) ozone and oxygen plasma treatments [25–27]. However, these chemical means present some drawbacks, such as the need for selective patterning of the reactive species/treatments or the fine control of the introduced charged states at the dielectric/OSC interface, which thus do not enable simple, large area processing. For the latter route related to OTFT geometry, good control over V_T was achieved by adding a double gate [28,29], enabling control and reversible shift over a wide range. However, this technology requires additional metal patterning by photolithography to vary the V_T through bottom and top electrodes substantially increasing the complexity of the devices and the circuits, as well as the number of layers and interconnections. Another approach to control V_T through the geometry is by means of the Corbino OTFT structure. Very few works have previously reported inorganic Corbino TFTs [30–33]. As OTFT based on small molecule OSC can present large diversity of crystal orientation and grain boundaries [34,35] and thus high V_T variability, Corbino OTFTs were developed to overcome this by having a circular channel making them more robust. In addition, Corbino shaped electrodes provide less overlaying areas in comparison with conventional interdigitated electrodes, which generates less parasitic capacitance, thus changing their electrical parameters compared with interdigitated electrodes. Other interesting features of Corbino OTFTs are the increment of the output resistance and the compatible fabrication with conventional interdigitated OTFTs without adding additional fabrication steps or chemical treatments. So far, Corbino TFTs have been uniquely employed as uniform current drivers in Active-Matrix Organic Light Emitting Diodes (AMOLED) to enhance the power efficiency [31,33].

Therefore, the ability to fabricate OTFTs using a fabrication methodology without involving chemical treatments with reproducible and uniform V_T is critical for practical circuit design. Improved circuit functionality is the main motivation for the present study, which considers both Corbino and interdigitated OTFT geometries as having dual-V_T behaviour. For the first time, dual-geometry allows innovative configuration of the logic gates presenting enhanced performance compared with single-geometry. Subsequently, dual-geometries were introduced and a substantial increase in gain and output voltage swing was achieved for inverters.

In addition, the efficient design of complex integrated circuits based on OTFTs requires preliminary characterization and modelling [36]. For this purpose, the development of accurate compact models is particularly appealing. In this paper, we first model and analyse the electrical characteristics and the performance parameters of the Corbino and interdigitated OTFTs possible in unipolar organic electronics using models based on the well-known Metal oxide field effect transistor (MOSFET) level 3.

2. Materials and Methods

The fabrication was carried out at the Centre for Process Innovation (CPI, Sedgefield, UK) using the Gen2 photolithography facilities. The Corbino and interdigitated OTFTs employ top gate bottom contact (TGBC) architecture in which the fabrication process begins with the spin-coating of the planarizing layer of a proprietary acrylate polymer (PCAF, from CPI) on carrier glass followed by a soft-bake, then a cross-linking process using UV light in a nitrogen environment, followed by hard-baking. Au (50 nm) were sputter coated and patterned using photolithography and wet etching to form drain and source electrodes. In order to increase the surface energy, the substrates were oxygen plasma-treated and then a self-assembled monolayer (SAM) of 3-fluoro-4-methoxythiophenol (Fluorochem, Glossop, United Kingdom) was deposited from a 10 mM solution in isopropanol and baked at 100 °C for 60 s. Afterwards, the OSC FlexOS^{TM} solution was spin-coated at 500 rpm for 10 s followed by 1000 rpm for 60 s and then a further bake at 100 °C for 60 s in order to obtain a 20 nm thick film. The OSC solution comprises a small molecule semiconductor and a high-k polymer semiconductor binder (Figure S1 in Supplementary Materials). The dielectric used in this work was Cytop CTL-809M (Asahi Glass, Tokyo, Japan) and it was diluted to 4.5% solids and spin-coated in order to obtain a 300 nm thick film and a gate capacitance of 6×10^{-9} F/cm^2. Au (50 nm) was thermally-evaporated, patterned using photolithography and wet etching. The gate-source/electrode overlapping area is

2.6×10^{-4} cm^2 and 1.4×10^{-5} cm^2 for Corbino and interdigitated devices, respectively. The unwanted areas of OSC and dielectric were patterned by oxygen reactive-ion etching plasma etching using the gate metal as a hard-mask. Subsequently, Polyvinyl alcohol (Sigma-Aldrich, Saint Quentin Fallavier, France) and SU-8 (MicroChem, Westborough, MA, United States of America) were deposited and patterned as a passivation layers. The metal interconnect layer (Au 50 nm) was sputtered and patterned to create electrical connections. Finally, the third protective passivation layer (SU-8, 450 nm thick) was deposited in a similar way to the first two passivation layers. All the layer thicknesses were measured through SEM images.

The devices were characterized with the requirements established for the model development, performing a wide range of values for the gate or drain voltage applying potential from −30 to 30 V. Using this procedure, experimental data on key parameters were successfully extracted. By fixing the polarization of the transistor with the same V_{GS} and V_{DS} the saturation region is assured, in our case −20 V, allowing implementation of the well-known extraction procedure for the saturation region of the transistors [37]. This procedure is based on plotting the square root of the drain current versus the gate voltage. In the polarization point of $V_{GS} = V_{DS}$, a straight line is plotted until the x-axis intercept where the threshold voltage value is extracted, see Figure S2B. The hole mobility was obtained dividing the slope value, in the polarization point of $V_{GS} = V_{DS}$, by the device total capacitance. Finally, the I_{ON}/I_{OFF} ratio was extracted from the ratio between the maximum current and the minimum current.

The dimensions of the Corbino devices were calculated as proposed in [38]. Defining R2 as the bigger radius and R1 the smaller one, the equivalent length of the device can be defined as:

$$L = (R2 - R1)$$

while the width of the transistor is determined with:

$$W = \frac{2 \cdot \pi}{\ln\left(\frac{R2}{R1}\right)} \cdot (R2 - R1)$$

The model implemented is based in MOSFET level 3 where some modifications had been implemented in order to fit the different transistors studied in this publication. Since the devices cannot be included in the under micrometre group, the effects of narrow width and short channel can be neglected, and the channel length modulation, λ, have to be considered, moreover the mobility degradation factor, θ, is included in terms of trapping in the channel. Finally, the bulk resistance has been implemented as, R_{BULK}, and added in all the stages of the compact model for keeping coherence between the different transistor behaviours. Additionally, the most common parameters such as the mobility, μ, the insulator capacitance, C_{INS}, the channel width, W, or the channel length, L, are included. The voltage and currents through the device are defined with the source, drain or gate terminals, having the difference between the first and the last defined terminals. The different regions and equations are introduced in the following equations:

For $V_{SG} < V_T$ in the cut-off region:

$$I_{SD} = R_{BULK} \cdot V_{SD}$$

$V_{SD} < V_{SG}$-V_T for the linear region:

$$I_{SD} = \frac{\mu \cdot C_{INS} \cdot \frac{W}{L} \cdot \left(V_{SG} - V_t - \frac{V_{SD}}{2}\right) \cdot V_{SD} \cdot (1 + \lambda \cdot V_{SD})}{1 + \theta \cdot (V_{GS} - V_t)} + R_{BULK} \cdot V_{SD}$$

$V_{SD} >= V_{SG}$-V_T when is in saturation region:

$$I_{SD} = \frac{\frac{1}{2} \cdot \mu \cdot C_{INS} \cdot \frac{W}{L} \cdot (V_{SG} - V_t)^2 \cdot (1 + \lambda \cdot V_{SD})}{1 + \theta \cdot (V_{GS} - V_t)} + R_{BULK} \cdot V_{SD}$$

The model has been extracted by using an in-house Matlab script that iterates with the equations and the experimental data of the transistors introducing a random stochastic value in a delimited range for an improved fitting in each device. These arbitrary values are initialized with the parameter extraction of the experimental data. Once the device is fitted with the MOSFET model, it is introduced in a Verilog—A module ready to be implemented in Virtuoso from Cadence (California, CA, United States of America).

All the electrical measurements were performed in ambient conditions and ambient light. The electrical characterization of the OTFTs was carried out using an Agilent B1500A Semiconductor Analyzer. The images were acquired using a light microscope DM4000 from Leica (Wetzlar, Germany).

3. Results

3.1. Interdigitated and Corbino OTFTs

For most of the basic research, the inverted/staggered and co-planar OTFT structures are the most commonly reported devices [39]. OTFTs can be implemented in different structures depending on the relative positions of the electrodes. Moreover, the electrodes in interdigitated configuration were predominantly adapted over the development of OTFT to account for the low conductivity of OSC. In this configuration, the source and drain electrodes are in a form of a comb, such that the finger of the drain comb is interdigitated with the fingers of the source comb providing larger current flow by increasing the channel width. Furthermore, it is worth mentioning that in the interdigitated geometry used in this work the gate layer totally overlies the source and drain electrodes. Figure 1Ai,Aii depicts the scheme and an optical image of the interdigitated electrodes fabricated in this work, respectively. The main advantage of this configuration is their efficiency concerning the ratio between the transistor surface and the transistor width [40]. However, such geometry is not entirely satisfactory in terms of performance since great efforts were made to enhance the alignment of OSC crystal perpendicularly along the Drain and Source (D/S) electrodes during the OSC deposition such as undergoing a nitrogen flow, temperature, and varying the solvent nature and ratio [41–43]. In order to overcome this limitation and for the sake of fabrication simplicity, OTFTs with circular channel, called Corbino OTFTs, are commonly proposed. The circular geometry experiences all orientations of the crystals providing less device variability. Although one intrinsic feature of Corbino geometry is a low gate-drain overlying area over their interdigitated geometry counterpart, in this work, the Corbino devices present an overlapped gate-source/drain capacitance of 2.6×10^{-4} cm^2 while the interdigitated devices present 1.4×10^{-5} cm^2. Figure 1Bi,Bii shows a cross-section and the optical image of interdigitated and Corbino geometries, respectively.

Interdigitated and Corbino OTFTs were electrically characterized with a W/L of 40 (W = 160 µm/L = 4 µm) and 34 (W = 680 µm/L = 20 µm), respectively. For a better understanding of the device performances according to the geometry, the transfer curves were compared by normalizing the drain current with the W/L ratio, called channel dimension (CD). Since the devices were fabricated simultaneously on the same substrate, they show the same layer thicknesses and characteristics, thus, the observed differences in the transfer-output electrical characteristics are solely attributed to OTFT geometry.

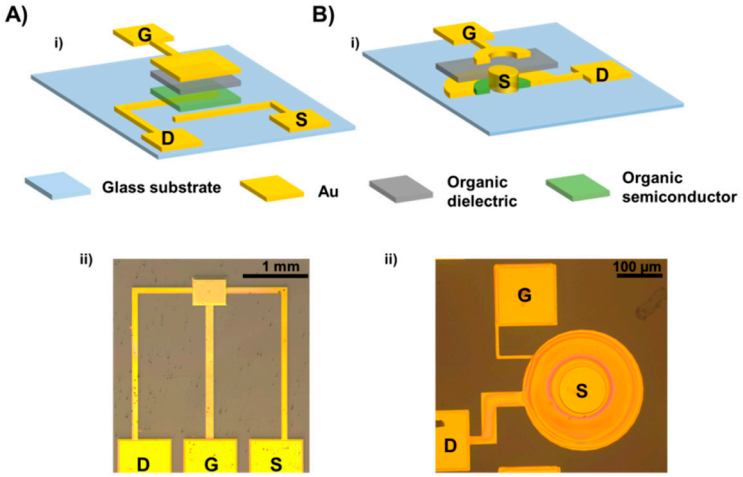


Figure 1. (**A**) (i) 3D scheme of the Interdigitated geometry and (ii) its optical image; (**B**) (i) 3D scheme of the Corbino geometry and (ii) its optical image. D, G and S refer to drain, gate and source electrodes, respectively.

The measured and simulated transfer and the output characteristics of the interdigitated and Corbino OTFTs are shown in Figure 2. As can be observed in Figure 2A, the model correctly predicts with high precision the transfer curves for both geometries. In addition, the simulated output curves fit well with the measurement by providing a smooth linear-to-saturation transition, as shown in Figure 2B. Thus, the used model can be widely applied to OTFTs with interdigitated and Corbino geometries serving as a practical and versatile tool for organic-based circuit development. Figure 2C,D show the measured output electrical characteristics for both geometries. The maximum drain current, named as I_{ON}, is significantly larger for Corbino devices than interdigitated devices, as can be observed in the zoom-in in Figure 2D, presenting values of 4.8 µA and 1.4 µA, respectively, for V_{DS} = −20 V and V_{GS}= −20 V. The same tendency is corroborated in the linear regime as can be seen in the transfer curve in Figure S3, where the higher current is attributed to the Corbino geometry. Despite the fact that effective carrier mobility is affected by the dimensions of the channel length, the Corbino OTFTs tends slightly to saturate. In contrast, the output drain current of interdigitated OTFTs showed a linear increase with V_{DS} and did not saturate. The unsaturated output characteristics in interdigitated devices were also clearly of larger channel length (see Figure S4 Supporting Information), thus, this phenomenon was not totally governed by short-channel effects. Indeed, the output characteristics of both geometries exhibited an obvious I_{DS} offset at V_{GS} = 0 V indicating an appreciable conduction, more pronounced in interdigitated OTFTs, due to a parasitic conduction path from the drain to the source. Due to this fact, the depletion mode current, which is called I_{OFF}, can be achieved by applying a positive voltage such that the conduction is suppressed. The depletion mode current in interdigitated geometry was reached by applying a V_{GS} = −20 V while in Corbino geometry the voltage applied was reduced to V_{GS} = −10 V, as can be compared in Figure 2C and the inset of Figure 2D. The I_{OFF} displayed are about one order of magnitude larger for interdigitated compared with Corbino devices, for V_{GS} = 0 V and V_{DS} = −20 V. In comparison with the Corbino devices reported previously [32], the circular devices developed in this work yielded similar output curves regardless the bias configuration, i.e., the inner-drain or outer-drain condition (see Figure S5, Supporting Information).

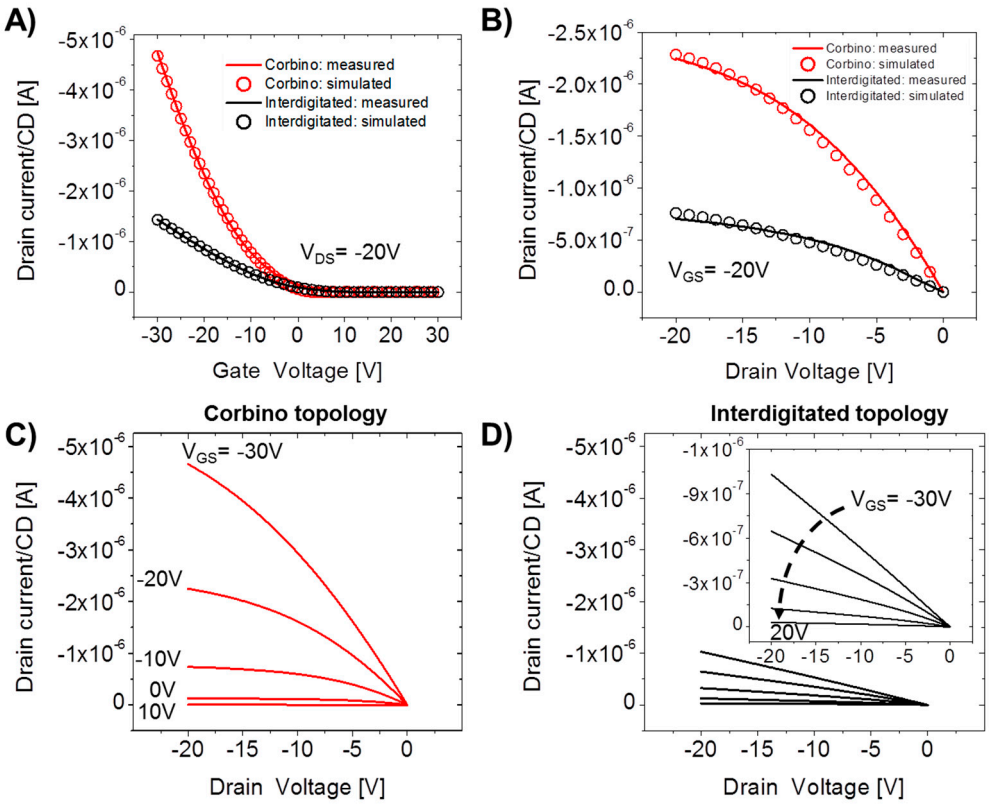


Figure 2. Experimental transfer (**A**) and output (**B**) characteristics for Corbino and interdigitated geometries normalized to Channel Dimension (CD) for V_{DS} = −20 V and V_{GS} = −20 V, respectively. The circular symbol refers to the theoretical transfer and output characteristics simulated by using a MOSFET level 3. (**C**) Experimental output characteristics of Corbino geometry devices. (**D**) Experimental output characteristics of interdigitated geometry devices where gate voltage (V_{GS}) were swept by −10 V from −30 V to 20 V. The output graph for interdigitated geometry is rescaled in the inset graph for better comparison. The channel length is 4 µm and 20 µm for interdigitated and the Corbino devices, respectively. Both have almost the same W/L ratio.

In order to gain insight into the electrical performance of both geometries, effective mobility, $V_{T,}$ and I_{ON}/I_{OFF} current ratio were investigated as a figure of merit of interdigitated and Corbino geometries as shown in Figure 3A–C, respectively. Notably, there is a big difference in the effective hole mobility between the devices with different geometries. This result is due to the Corbino geometry despite presenting higher channel length compared with interdigitated OTFTs. The extracted effective hole mobility for Corbino geometries is about 1.61 $cm^2/V{\cdot}s$, and for interdigitated devices is about 0.71 $cm^2/V{\cdot}s$. Clearly, the OTFTs with Corbino geometry performed V_T closer to 0 V in the 4–8 V range, whereas interdigitated geometry performed V_T ranging from 8 to 14 V. Despite showing different threshold voltage for each geometry, the turn on voltage is the same for both devices since they share the same materials and fabrication procedure. Turn-on voltage has been extracted from the maximum point of the derivative in the logarithmic scale of the transfer curve and this result is included in Figure S6. Corbino devices present less variability of V_{ON} values than the interdigitated geometry devices. Regarding this difference, both types have very similar values for the turn on voltage, which is linked to the materials of the devices. Both devices work in accumulation mode, a result in good agreement with the improvement of the effective hole mobility in Corbino devices, which makes the V_T nearer zero. Interestingly, in the Corbino OTFTs, the V_T and effective hole mobility possess uniformity in terms of electrical parameter dispersion, which indicates that circular channel geometry is more robust in delivering good performance over large areas despite the polycrystalline nature of the small-molecules. A large number of methods have been developed to reduce the OTFT's current variability induced by

random grain orientations of the organic semiconductor [44–46]. The semiconductor used in this work, FlexOS^{TM}, presents large crystal sizes in the range of tens of micrometres. As the grain structures have different grain orientations, the extreme grain-to-channel alignments were solved by a circular-shaped channel providing higher effective mobility and thus, lower V_T. The channel length is in the range of the grain domains: L = 4 µm and 20 µm for interdigitated and Corbino geometries, respectively. In order to measure the uniformity of the devices, the relative standard deviation (RSD), defined as the ratio of the standard deviation to the mean drain current, was used. In particular, our results show that the overall RSD in drain current for interdigitated OTFT and Corbino OTFT were found to be 65.18% and 12.4%, respectively. Apart from the reduction in variability, an enhanced effective mobility and threshold voltage were achieved for Corbino OTFTs. Other electrical parameters of the devices have been studied as can be seen in Figure 3C, where the I_{ON}/I_{OFF} ratio is degraded for interdigitated devices owing to the presence of parasitic current in the *OFF* state. The I_{ON}/I_{OFF} ratios for Corbino geometries are about (10^7), two orders of magnitude higher than those of interdigitated devices. For logic gates, the I_{ON}/I_{OFF} ratio remains an important parameter that must be taken into account. Thus, a high current modulation ratio is a more important requirement than the high mobility for programmable electronic circuits [43,47–50]. This behaviour is supported by the fact that Corbino geometry eliminates parasitic sources to drain current flows, hence, allowing an enhanced I_{ON}/I_{OFF} ratio. This phenomenon, previously reported in [33], is explained by the increment of the differential output conductance of Corbino devices, which is defined as $\delta I_{DS}/\delta V_{DS}$ and can be described as follows: For circular OTFTs, the W/L relationship remains fairly constant because the channel length modulation is compensated by the channel width modulation. Hence, beyond the pinch-off, the differential output resistance of the interdigitated TFT is finite; whereas, that of the Corbino TFT is infinite, which is in agreement with previous works [31,33] and with the results obtained in Figure 3D.

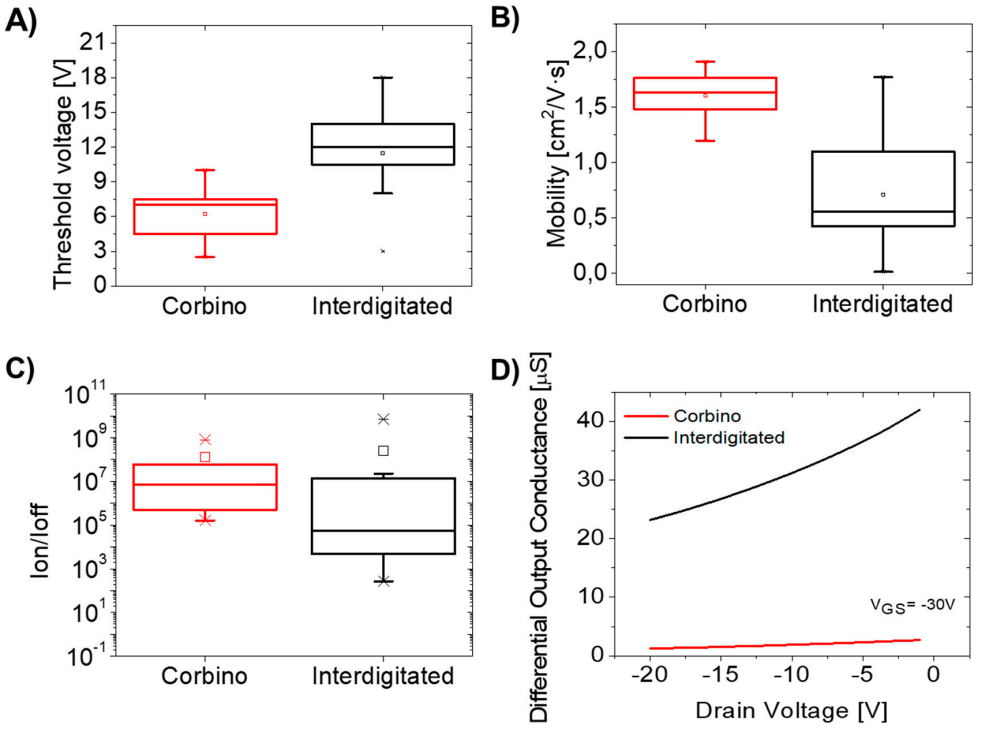


Figure 3. Electrical parameters such as (**A**) threshold voltage, (**B**) effective hole mobility and (**C**) I_{ON}/I_{OFF} ratio for Corbino and interdigitated geometries. The central mark represents the median, box limits indicate the 25th and 75th percentiles, and whiskers extend to the 5th and 9th percentiles. (**D**) Differential output conductance as a function of drain voltage at V_{GS} = −30 V.

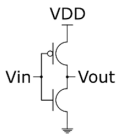
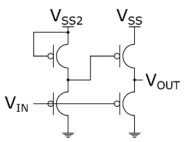
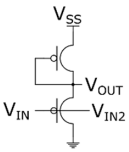
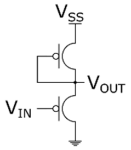
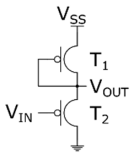
To conclude, these results reflect the fact that the electrical performances actually correlate with the overall geometric parameter ($\mu_h C_{INS} W/L$) as supported by the higher the effective hole mobility (μ_h), the higher the V_T and, the higher the I_{ON}/I_{OFF} ratios for Corbino geometry. For these reasons, and as a novelty compared with widely-reported logic gates based on interdigitated OTFTs, an inverter logic gate was implemented in further studies in this work.

3.2. Unipolar Organic Dual-Geometry Threshold Voltage Inverter

The Inverter is considered to be the most basic logic circuit element for Complementary Metal-Oxide Semiconductor (CMOS) technology [51]. However, unipolar logic circuits are widely employed in the organic electronics field.

Unipolar based circuits which present either n-type or p-type OSC, require a pull-up (n) or pull-down (p) load transistor polarized in *ON* state and, an input-controlled drive transistor which logically inverts its input [52,53]. Therefore, for a low voltage (in terms of Boolean algebra, it is known as '0') the input produces a high voltage (in terms of Boolean algebra, it is known as '1') at the output, and vice versa [54]. In order to obtain a pull-down load transistor different geometries can be implemented. One of the most common geometries is based on the short-circuit of the gate and drain terminals yielding a fixed gate-to-source voltage, i.e., V_{GS} = 0 V, which turns the load transistor into a diode. In fact, this configuration is referred to as diode-load or depletion-mode load configuration [55,56]. Based on the results of several works [57] which demonstrated that higher gain can be achieved by diode-load topology, this work will consider a diode-load topology for the inverter.

Table 1. Comparison of different topologies of OTFT design styles for basic inverters with key parameters.

Inverter Topologies	**CMOS** 	**Pseudo-CMOS** 	**Dual-Gate** 	**Diode-Load** 	**Dual-Threshold** 
Transistors	2	4	2	2	2
Power rails	2	3	3	2	2
Noise Margin	Most Robust	High Robust	Robust	Poor Robust	Medium Robust
Voltage swing	Full Swing	Full Swing	Non-Full Swing	Non-Full Swing	Almost-Full Swing
Power	Dynamic	Static and Dynamic	Static and Dynamic	Static and Dynamic	Static and Dynamic
Device Type	Complementary type	Mono-type	Mono-type	Mono-type	Mono-type

Different inverter topologies have been presented in the literature for monotype systems as shown in Table 1. From the simplest one using only one transistor and a resistor, to a more complex system where multiple devices are required. The most employed inverter topology for CMOS [58] technology involves two complementary transistors, meaning n-channel and p-channel. The advantage of this topology is full swing in the voltage achieved due to the alternative switching between *ON* and *OFF* state of the load and driver. Furthermore, this configuration allows a high gain with a significant robustness to the noise margin. The power consumption reaches minimum values because of the negligible power consumption in the static state of the inverter but, as a drawback, the fabrication processes involved are complex. For the monotype devices, the pseudo-CMOS [57,59] approach is the most robust topology since the polarization of the last transistor stage allows them to achieve full swing at the output. Despite this benefit, this topology requires four transistors and more power rails increasing the power consumption, which is detrimental for energy efficiency. In order to reduce the number of transistors and power sources required, the diode-load [60–63] is used because it operates with two unipolar transistors. However, this topology is less robust and presents non-full swing voltage at the output. Using dual-gate devices, [29,64,65] the diode-load configuration can have improved

noise margins since the drive transistor is more robust against noise. The drawback of dual-gate transistors is the requirement of a more complex fabrication process and the inclusion of an additional power rail in the design.

The solution presented in this work is the use of a dual-threshold configuration [66,67] which provides a lower noise margin and higher voltage swing at the output compared to the diode-load and the dual-gate topology, respectively. Dual-threshold technology has been studied for several years and applied to the silicon technology, achieving power consumption reductions [68,69] and increasing the performance of the system in different aspects as delay [68,70], robust designs [71], asynchronous circuits [72], speed improvement [73] or glitch minimization [74]. The interdigitated and Corbino devices developed in this work present different electrical characteristics, such as V_T. Taking advantage of this behaviour, a dual-threshold configuration was implemented using these two geometries in order to obtain enhanced performance and reduced power rails. An interesting feature of this approach is the extreme simplicity for fabricating logic gates because the electrical parameters of the transistors are totally dependent of its geometry, allowing a unique manufacturing process for the entire circuit area.

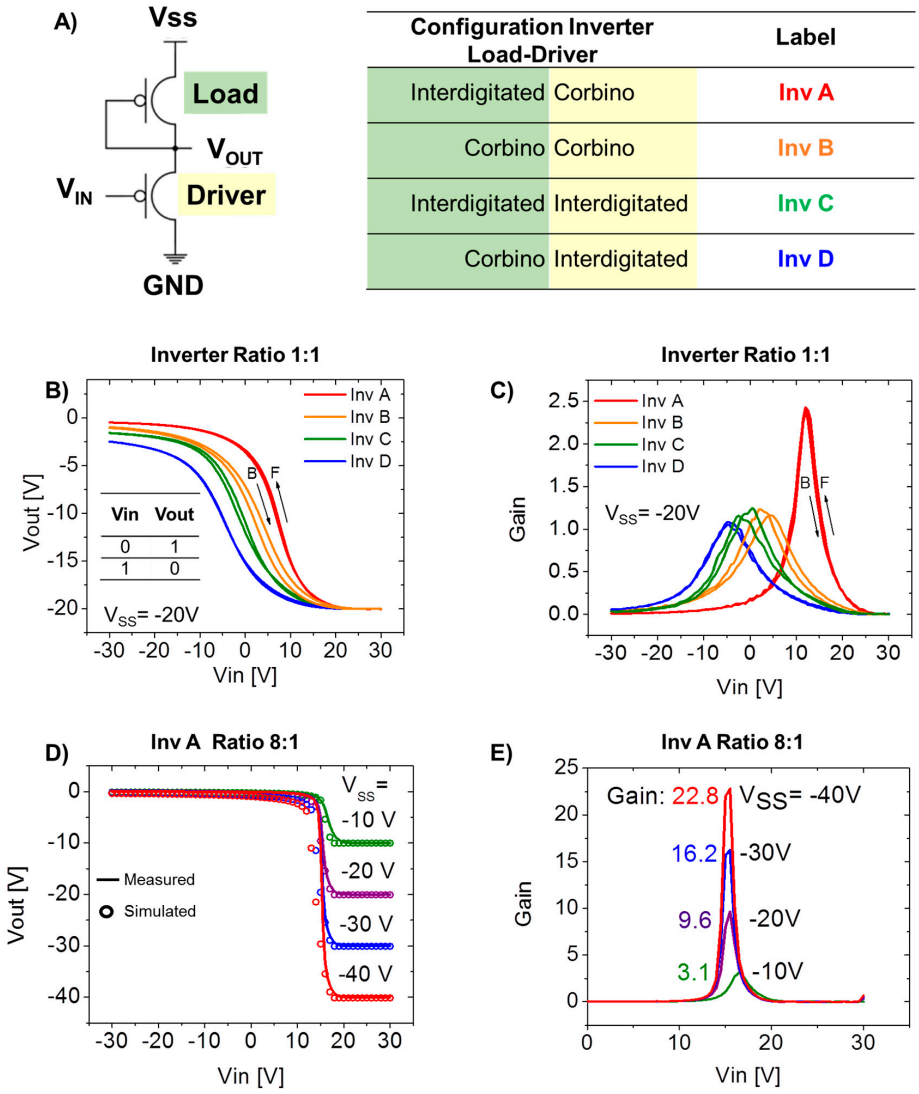


Figure 4. (**A**) Inverter circuits by using different combinations of transistor geometries: (**B**) Voltage transfer characteristics (VTC); (**C**) and gain. (**D**) VTC for Inv A geometry with a ratio 8:1; and (**E**) the respective gain. "F" and "B" denote forward and backward sweeps, respectively.

Figure 4A shows the schematic of the inverter. The load transistor is biased to the *ON* state, which allows the current to flow through itself by providing low resistance and the driver transistor switches between *ON* and *OFF* state controlled by the input. A figure of merit of the inverter circuit is the gain, which is defined as the maximum slope of the transfer curve of the system. Regarding gain, four different combinations of the two geometries for the driver and load were configured and characterized. The dimensions ratio, W/L, of the devices were equal (ratio 1:1) to be sure that the results were not influenced by the dimensions, as can be seen in Figure 4B. It can be noted that the configurations with a single type of geometry, i.e., interdigitated-interdigitated or Corbino-Corbino, provide higher hysteresis than the others. The best combination obtained was placing the interdigitated geometry as a load and the Corbino geometry as the driver (called Inv A), where the gain was double the rest of circuit configurations, as shown in Figure 4C. Moreover, this combination geometry offered the full output voltage swing. Taking into account the driver transistor commutating between the *ON* and *OFF* states, the Corbino geometry as used as a driver because it provides higher performance than the interdigitated geometry, in terms of the I_{ON}/I_{OFF} ratio, allowing high current in the *ON* state and a negligible current in the *OFF* mode. Furthermore, the interdigitated transistor working as a load provided lower output resistance and, thus, a lower voltage drop at the output of the system allowing it to reach ground (GND) and V_{SS} values. Additionally, both geometries presented different threshold voltages, which induced a more resistive load device when the driver was in an *ON* state. These behaviours occurred owing to the lower V_{SD} and resistance in the *OFF* state of the driver, permitting a full swing of the output voltage thus reducing the hysteresis of the inverter.

To assess the maximum gain obtained by the topology of Inv A, a variation on the ratio of dimensions between the load transistor and the drive transistor was implemented by increasing the driver 8 times with respect to the load, as can be seen in Figure 4D,E. The study of the electrical behaviour of the inverter for four different V_{SS} revealed a link between the power supply and gain. In fact, the increased gain correlated with a higher power supply and at the same time delivered higher swing and higher slope. Moreover, the simulation of electrical behaviour for Inv A depending on the V_{SS} was implemented in Virtuoso and by introducing the generated models of each geometry, as can be observed in Figure 4D. Well-fitting measurements at the transitions were obtained for low V_{SS}, meanwhile the model correctly predicted the V_{SS} and GND values for all V_{SS}. The increment in the ratio between the driver and the load provided almost four times higher gain compared with the previous 1:1 ratio. This configuration presented a gain of 22.8 of the V_{SS} to −40 V, as can be observed in Figure 4E.

4. Discussion

The implementation of inverter circuits in the organic electronics field has been a hot topic in recent years and different configurations have been tested using diverse circuit topologies. Until now, there have been no publications on improved inverter behaviour using two different geometries of transistors. However, as shown in this work improved inverter behaviour was achieved by exploiting the different electrical parameters, i.e., I_{ON}/I_{OFF} ratio, effective mobility and threshold voltage of interdigitated and Corbino geometries. In this work the two OTFTs were fabricated by means of the same fabrication process and materials to produce a novel, monotype dual threshold voltage organic inverter with two different transistor geometries for the load and the driver. An experimental comparison of geometries was presented, in which the same dimensions for the driver and inverter load were used in order to corroborate the advantages of the dual threshold technology. The best configuration with maximum gain and lowest hysteresis in the structure was found to be with a Corbino geometry as the driver and an interdigitated geometry as the load. This configuration provided a gain of up to 22.8 with a power supply of −40 V. The achieved gain was higher than most of the inverters presented with monotype systems. Additionally, the transistors were modelled with a modified MOSFET level 3 to improve fitting with the experimental data. Finally, the models were employed to simulate a circuit of the inverter and a good fit was achieved with the experimental data.

Supplementary Materials: The following are available online at http://www.mdpi.com/2073-4352/9/7/333/s1, Figure S1: Molecule structures of the small molecule organic semiconductor and the high-k polymer semiconductor binder used for the blend. Figure S2: Square root and logarithmic scale transfer curves of both geometries types for the two behavior of the transistors: (a) Lineal region, and (b) saturation region including the threshold voltage extraction procedure representation. Figure S3: Experimental transfer characteristics for Corbino and interdigitated geometries normalized to channel dimension (CD) for V_{DS} = −2 V. Figure S4: Experimental output characteristics of interdigitated geometry devices where gate voltage (V_{GS}) were swept by −10 V from −30 V to 10 V. The channel length is 10 µm. Figure S5: Output characteristics of the Corbino TFT for the two drain-bias conditions: (a) The inner circle as source and outer ring as drain; and (b) the inner circle as drain and outer ring as source. Figure S6: Turn on voltage of both geometries from the curve transfer curve with V_{DS} = −20 V. The central mark represents the median, box limits indicate the 25th and 75th percentiles, and whiskers extend to 5th and 9th percentiles.

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