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Microwave Photonic ICs for 25 Gb/s Optical Link Based on SiGe BiCMOS Technology

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Abstract: The design, simulation and experimental results of the integrated optical and electronic components for 25 Gb/s microwave photonic link based on a 0.25 μm SiGe:C BiCMOS technology process are presented. A symmetrical depletion-type Mach-Zehnder modulator (MZM) and driver amplifier are intended for electro-optical (E/O) integrated transmitters. The optical divider and combiner of MZM are designed based on the self-imaging theory and then simulated with EM software. In order to verify the correctness of the theory and material properties used in the simulation, a short test (prototype) MZM of 1.9 mm length is produced and measured. It shows an extinction ratio of 19 dB and half-wave voltage-length product of $V_\pi \cdot L$ = ~1.5 V·cm. Based on these results, the construction of the segmented modulator with several driver amplifier units is defined. The designed driver amplifier unit provides a bandwidth of more than 30 GHz, saturated output power of 6 dBm (output voltage of V_{pp} = 1.26 V), and matching better than −15 dB up to 35 GHz; it dissipates 170 mW of power and occupies an area of 0.4 × 0.38 mm^2. The optical-electrical (O/E) receiver consists of a Ge-photodiode, transimpedance amplifier (TIA), and passive optical structures that are integrated on a single chip. The measured O/E 3 dB analog bandwidth of the integrated receiver is 22 GHz, and output matching is better than −15 dB up to 30 GHz, which makes the receiver suitable for 25 Gb/s links with intensity modulation. The receiver operates at 1.55 μm wavelength, uses 2.5 V and 3.3 V power supplies, dissipates 160 mW of power, and occupies an area of 1.46 × 0.85 mm^2.

Keywords: microwave photonics; SiGe; IC; Mach-Zehnder modulator; driver amplifier; integrated optical receiver

1. Introduction

Modern RF and microwave telecommunication systems are built at the interface of several branches of science and engineering and extensively use the possibilities of combining various technologies in a single device. Such a «technical symbiosis» makes it possible to achieve system performances that would not be possible if implemented separately.

Nowadays, a new microwave photonics discipline exploring the possibilities of using optical devices and systems for processing and generating a microwave signal has appeared. It has become especially popular recently, since the cost of optical devices is constantly decreasing and a large number of inexpensive optical components (lasers, photodetectors, multiplexers, electro-optical modulators etc.) have appeared on the market. Great prospects for the use of microwave photonic devices in mass products open up with the embedding of SOI-based optical processes into traditional microelectronic technology based on Si/SiGe. Currently, this area is actively developing. Several foundries routinely

offer these process options to manufacture both optical and combined electro-optical devices [1–5]. In the case of successful extension of these technologies, a relatively inexpensive transition of giant silicon foundries to the production of electro-optical integrated circuits and their widespread introduction to the mass-market segment becomes possible.

Obviously, the main advantages of using microwave photonic devices for generating and transmitting radio frequency signals are due to the properties of the optical fiber transmission medium itself, which has ultra-low losses (a few tenths of a dB per km). This allows you to transmit a signal for many kilometers without the use of trunk amplifiers. In addition, the mass production technologies of optical fiber turned out to be significantly cheaper than the microwave cable and microwave trunk amplifier manufacturing technologies. Therefore, the cost of optical cable networks turns out to be an essential advantage. The benefits in weight and size are also significant, opening up enormous prospects for the use of these technologies in space and aircrafts. It should also be noted, that the fiber-optic systems are ultra-wideband with respect to the RF signal. The frequency band is only limited by electronic components (electro-optical and opto-electronic converters, microwave amplifiers etc.). This allows the successful use of wave division multiplexing methods (DWDM/CWDM) for the transmitting of several RF channels by means of single optical fiber lines. Finally, the fiber-optic systems are immune to electromagnetic interference and have complete galvanic isolation, which significantly increases the reliability of such a system. All these advantages make it possible to create RF and microwave systems with performances not available for traditional microelectronics [6–12]. At the moment, the most striking example of the benefits of microwave photonics is an optoelectronic generator with a phase noise level of −160 dB/Hz at 10 kHz [13].

The bottleneck of microwave photonic systems, limiting their widespread adoption, is the input and the output of the RF signal to/from the photonic system using E/O and O/E electronic converters. The technology of these converters does not allow to ensure low values of the conversion coefficient, which leads to significant RF signal loss (of the order of 10 dB) while input or output, in turn, increase the system noise figure (NF) of the transmission system [10]. It was shown in [12] that the use of high-power lasers and optimal biased optical modulators can reduce the noise level down to 8 dB. An improvement in noise figure can be achieved by using an additional low-noise amplifier (LNA) [14,15] at the input. However, the low efficiency of high-power lasers and additional LNAs leads to increased energy consumption and increased cost, which reduces the overall advantages of microwave photonic systems over traditional systems with relatively short- and medium-length signal transmission distances. In applications where the signals are transmitted over long distances, such as radio astronomy [16], over-the-horizon radar systems, where the antenna array is large or its components are substantially distant from each other, even such high conversion losses become insignificant against the general efficiency of using microwave photonic systems.

Thus, the main efforts of the scientific community in further development of microwave photonic systems are aimed at improving the performances of E/O and O/E converters. One of the possible ways for improvement is the integration of additional amplifiers together with the E/O and O/E converters on a single chip. Further miniaturization and integration efforts will reduce power consumption, losses and cost of such devices.

This article presents the design, simulation and experimental results for different microwave photonic components for a 25 Gb/s microwave photonic link based on a 0.25 μm SiGe:C BiCMOS technology process. In particular, the design of such parts of the E/O integrated transmitter as Mach-Zehnder modulator (MZM) and driver amplifier is considered. Also, we describe the simulation of the optical divider and combiner of MZM. To verify the correctness of the design theory and material properties used in simulation as well as to define the construction of a segmented modulator, the short test (prototype) MZM of 1.9 mm length is produced and measured. The driver amplifier unit for the segmented modulator provides a bandwidth of more than 30 GHz. The O/E integrated receiver combines Ge-photodiode and transimpedance amplifier (TIA) integrated on a single ship. The receiver provides a 3 dB analog bandwidth of 22 GHz and is suitable for 25 Gb/s link.

2. Symmetrical Depletion-Type Silicon Mach-Zehnder Modulator

The depletion type MZM is the most commonly used in various silicon photonic applications [17]. It has several advantages over other types of modulators such as injection-type modulators and microring modulators. Unlike the injection type modulator, it has lower power consumption due to almost zero current via reverse-biased pn-junction, and higher bandwidth due to lower capacitance. It also provides a higher extinction ratio due to lower MZM arm imbalance as compared to the injection-type modulators where optical signal absorption is caused by the carriers in forward-biased diodes.

The operational diagram of MZM is shown in Figure 1. First, the optical part of MZM contains two grating couplers (which are omitted on the diagram) for the input and output of optical signals. The couplers are designed to have a maximum efficiency at 1.55 μm wavelength. After entering, the optical signal is guided by the rib waveguide to the multimode interference (MMI) divider, which evenly splits it to two symmetrical paths. In order to design an MMI divider, the self-imaging theory (SIT) [18] was implemented. Within the framework of SIT, the optical intensity distribution in the multimode structures is repeated after a distance $3L_\pi$, where $L_\pi = \pi/(\beta_0 - \beta_1)$ is the beat length of two lower-order modes of the structure, while it splits into N repeating images at the distance $L = 3L_\pi/N$. If the designed device has a symmetrical structure, the minimum distance for N-folded image is reduced to $L = 3L_\pi/4N$. For the designed MMI divider, the beat length is $L_\pi = 263$ μm, and subsequently the distance for two folded images is $L_2 = 98$ μm. In order to verify the theory correctness and initial design, the physical simulation of the MMI divider with EM software is performed; this also allows us to adjust the initial design. The final MMI length for two folded images was chosen to be $L_2 = 94.5$ μm which is close to the theoretical value of 98 μm. The results of simulation for field distribution and transmission spectra of the MMI divider are shown in Figure 2a,b, respectively. The same MMI structure is used as a combiner in MZM, and the results of its simulation are presented in Figure 3 for in-phase (a) and out-phase (b) ports excitation.

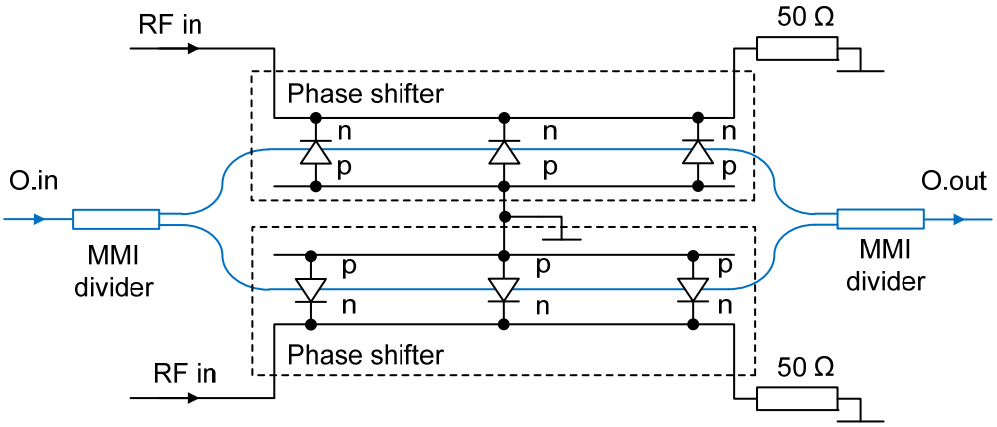

Figure 1. Operational diagram of MZM.

The modulation of the optical signal is performed independently by two arms of MZM by inducing additional phase delay to optical signals by the refractive index change inside the phase shifter. The RF signal is applied to electrodes forming the traveling wave in transmission line which is terminated by the matched (50 Ω) load. The E/O modulation can be performed either by applying an RF signal to one of the modulator arms or by feeding a differential signal to both arms (phase shifters). The bias point of the modulator is set by applying an additional DC voltage to one of the MZM electrodes.

The main metric of MZM is the half-wave voltage V_π that is required to induce the π phase shift. Generally, to improve the modulation efficiency, either higher driving voltages are needed (because of high V_π) or the MZM's length L needs to be increased. In the first case, the main limitations are the low breakdown voltages of SiGe BiCMOS technology (usually 2–3 V) and full depletion of the

pn-junction in the phase shifter, that significantly lowers the refractive index changes and modulation efficiency at the higher voltages. The second option leads to a higher MZM length that restricts the modulation bandwidth due to a mismatch between electrical and optical signal velocities and electrical losses in the phase shifters. To overcome these problems and reach high speed performance (up to 40 Gb/s), the segmented MZM excited with several driver amplifier units can be used [19]. Also, there are technological solutions of the V_π.L decreasing up to 0.74 V cm by using the special doping profiles, while maintaining high speed performance of 48 GHz [20]. In [21], the lowest value of $V_\pi \cdot L$ (0.2 V·cm) at 25 Gbps was reached with the help of barium titanate (BTO) thin film integrated into silicon photonic process.

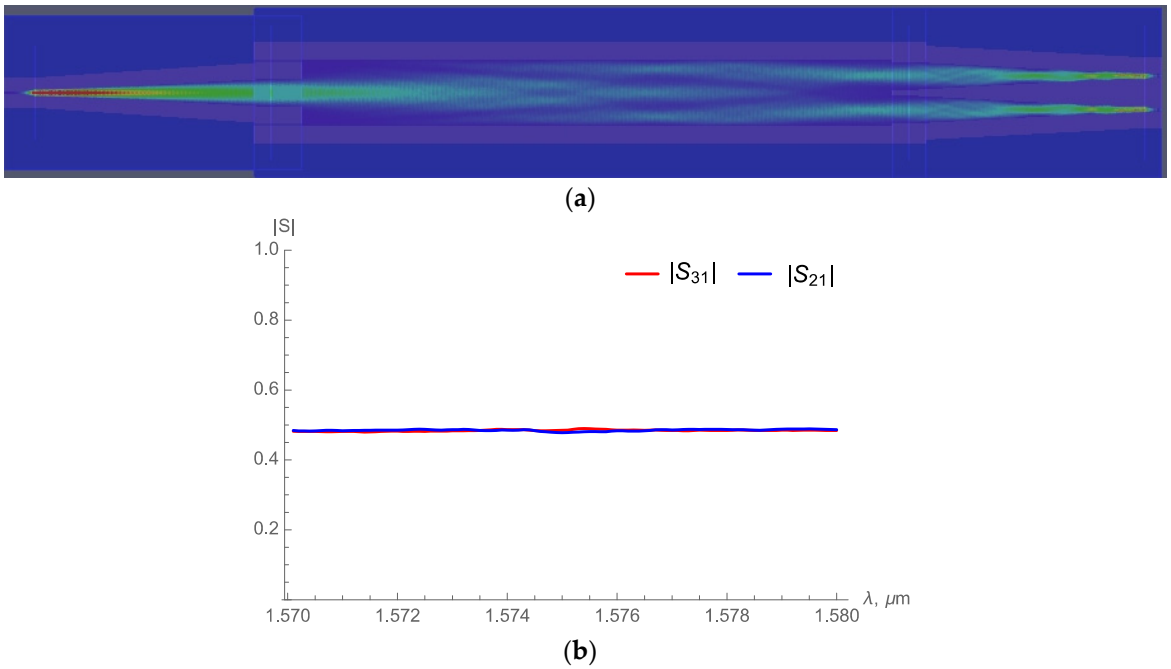

Figure 2. Optical intensity distribution along the MMI divider (**a**) and its transmission spectra (**b**).

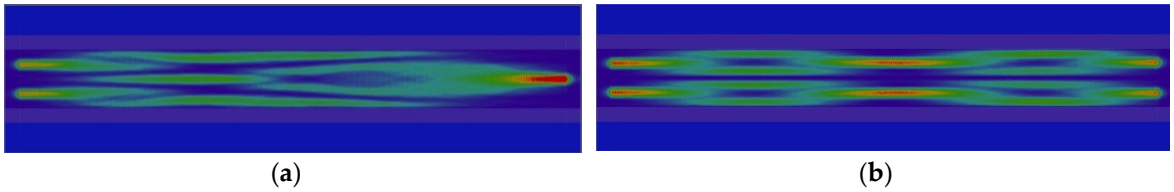

Figure 3. Optical intensity distribution inside the MMI combiner at in-phase (**a**) and antiphase (**b**) ports excitation.

In order to define the length of the modulator segment, the test (prototype) MZM is designed and produced (Figure 4). The phase shifter length for designed MZM was chosen to be 1.9 mm as a compromise between losses at high frequencies and half-wave voltage V_π. After producing, we can directly measure the key parameters of the test modulator such as half-wave voltage-length product, extinction ratio, load capacitance, and insertion losses.

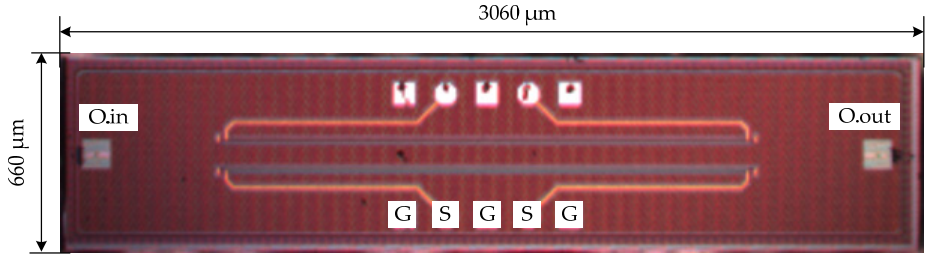

Figure 4. Photo of the test depletion-type MZM chip based on silicon technology (3.06 × 0.66 mm^2).

The measured RF S-parameters of the 1.9 mm MZM phase shifter are shown in Figure 5a. The phase shifter is matched up to 25 GHz, and the losses of electrical signal are −8 dB at 20 GHz. When designing a broadband segmented modulator [19,20], the mismatch and losses of MZM phase shifter must be taken into account. The dependence of the output optical signal power versus the control voltage is depicted in Figure 5b. According to the measurements, the half-wave voltage is equal V_π = 8 V, which means the voltage-length product of $V_\pi.L$ = ~1.5 V·cm; the initial optical signal loss is −15 dB; the extinction ratio is 19 dB. Based on these measurement results, the MZM structure of 12 segments with lengths of 400 µm is chosen to reach the desired 20–25 GHz bandwidth. According to the measured $V_\pi.L$ value and total modulator length of 4.8 mm, the half-wave voltage V_π of segmented MZM can be predicted as V_π = 3.2 V, which requires a differential peak-to-peak amplitude of V_{ppd} = 2.5–3 V from each driver unit.

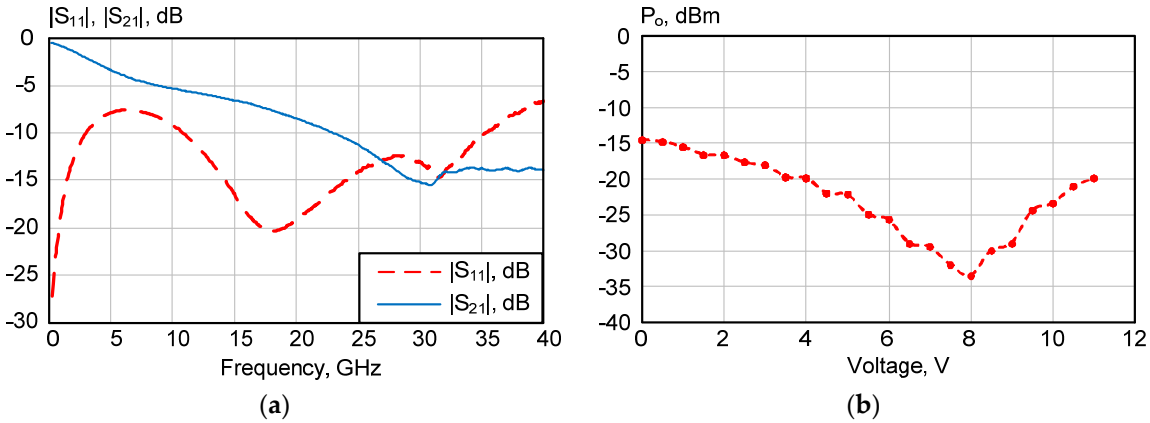

Figure 5. Measured MZM phase shifter RF *S*-parameters (**a**) and dependence of the output optical signal power versus control voltage (**b**).

3. Modulator Driver

As shown in the previous section, the MZM alone has a disadvantage that a high modulating voltage of several volts is necessary to reach high performances. Therefore, the use of an integrated driver amplifier is desirable to decrease required input power for the modulating signal. It is shown in [19,22–24] that the use of a segmented driver allows to slacken requirements for its output voltage and overcome the mismatch between the velocities of electrical and optical waves. In this solution, driver amplifier consists of several driver units that are distributed along the segmented MZM.

The driver unit schematic (Figure 6a) consists of input gain stage and output buffer stage to drive the segment of the modulator phase shifter. The input stage is implemented using a common-emitter configuration with parallel voltage feedback through the resistor R1 that provides matching and biasing for VT1. To increase the total voltage swing and output power of the driver unit, the second stage (VT3 and VT5, VT2 and VT4) is implemented as a cascode. In order to compensate the transistors' gain roll-off and insert predistortion for high-frequency losses of the MZM phase shifter, the emitter capacitive degeneration networks are used in both the stages. When designing the driver unit, the capacitive

load representing an input impedance of the MZM segment with length of L = 400 µm is taken into account. For this, the EM simulation of the modulator segment was performed.

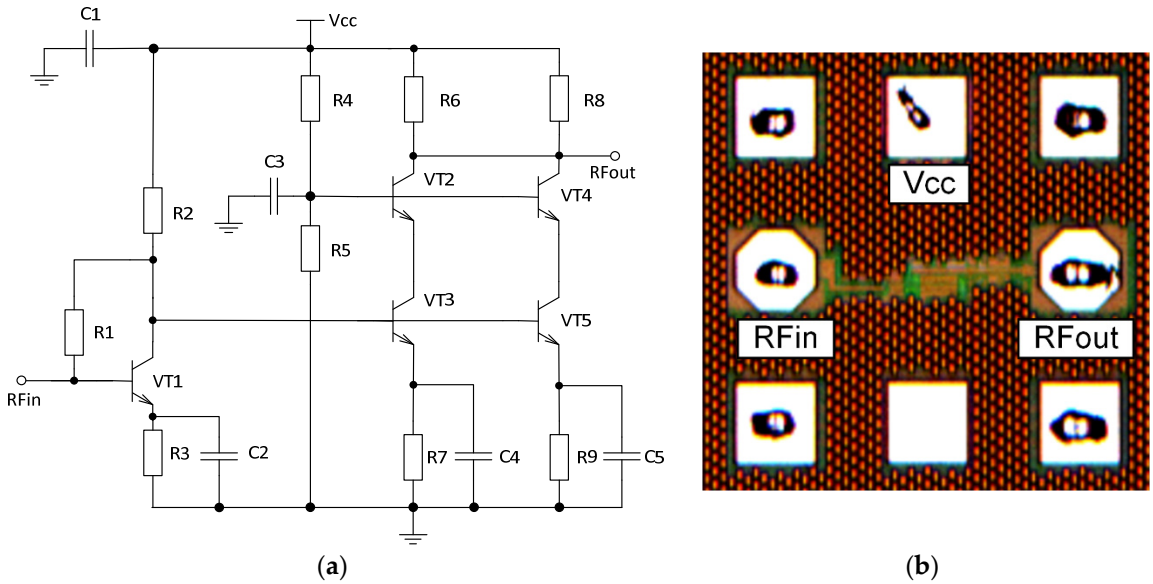

Figure 6. Driver unit schematic diagram (**a**) and photo of fabricated IC (**b**).

It should be mentioned that losses along the phase shifter line as well as the position and interaction of the driver units in the segmented MZM affect their load impedances. However, when designing the MZM integrated with the segmented driver, these effects can be accounted for by tuning elements of the emitter degeneration networks within different driver units [22].

A fabricated chip with a driver unit based on the 0.25 µm SiGe BiCMOS process is shown in Figure 6b. It occupies the area of 0.17 mm × 0.14 mm (0.024 mm^2) without the pads, and 0.4 mm × 0.38 mm (0.152 mm^2) with pads.

The driver unit was characterized on wafer using a probe station. Simulated and measured 50 Ohm S-parameters of the driver are presented in Figure 7. Also, its simulated generalized S-parameters taking into account the impedance of the modulator segment are also shown. The bias for the driver unit is V_{cc} = 5 V (I_{cc} = 34 mA), so the total power consumption equals to 170 mW. The difference between the simulated and measured 50-Ohm $|S_{11}|$ can be explained by the parasitic capacitance and inductance in the input stage's voltage feedback. The measured output power 1-dB compression point at the frequency of 20 GHz is $P_{1\mathrm{dB}}$ = 3.8 dBm, and the saturation output power is more than 6 dBm. For 50 Ω load, calculated peak-to-peak output voltage in saturation is V_{pp} = 1.262 V, which gives us a differential peak-to-peak voltage V_{ppd} = 2.5 V when the driver will be implemented as a differential stage. The measured eye diagram for the driver unit at 25 Gb/s (Figure 7c) demonstrates an open eye with an amplitude of 1.15 V and small variation of the group delay value.

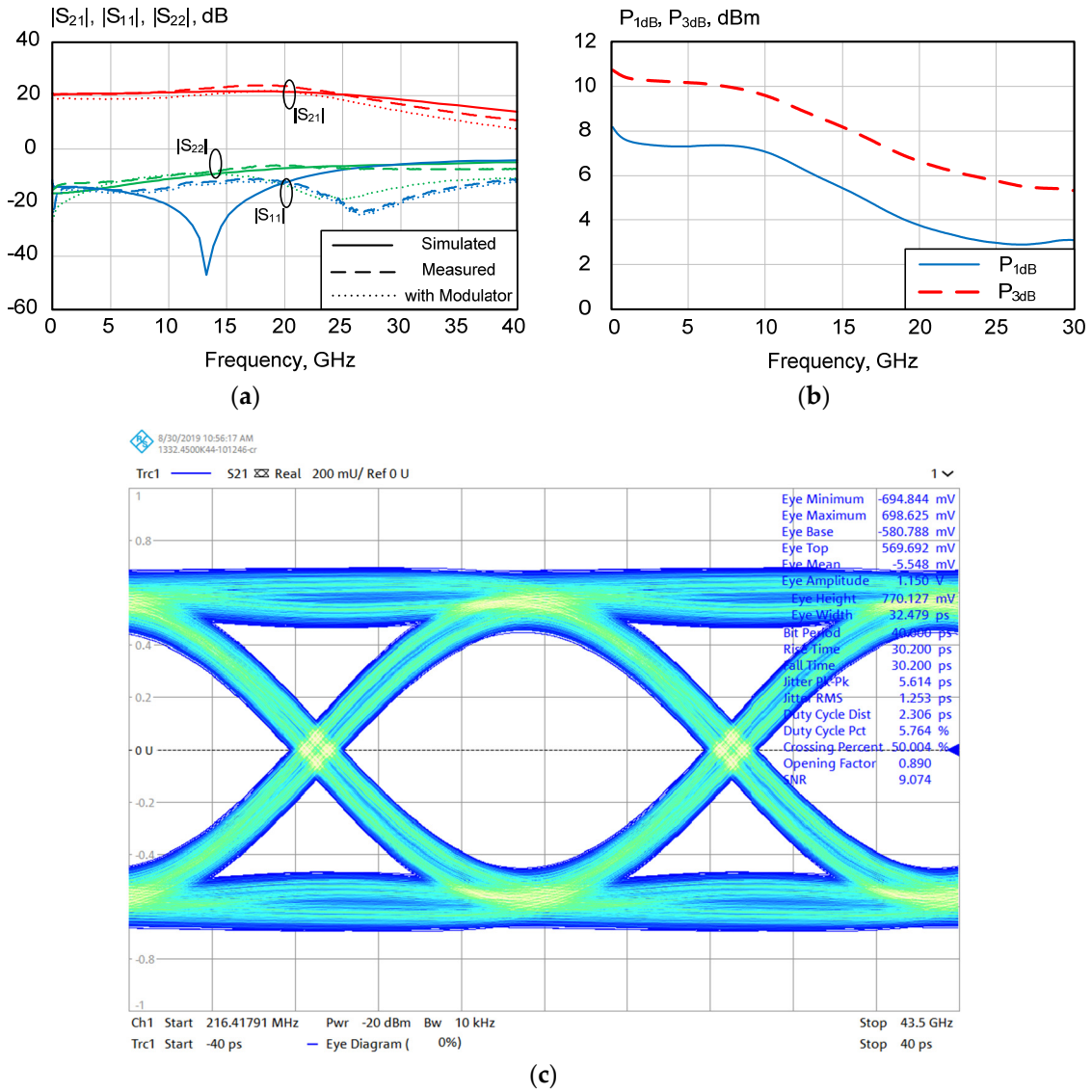

Figure 7. (**a**) Simulated and measured S-parameters of driver amplifier unit, (**b**) output power and (**c**) eye diagram at 25 Gb/s.

4. Optical Receiver with Integrated Photodiode and Transimpedance Amplifier

The receiver for the optical communication link contains PD, which detects the modulated signal and generates the electrical current, and TIA, which amplifies PD current and converts it to the differential voltage. The block diagram of the TIA with integrated PD is illustrated in Figure 8.

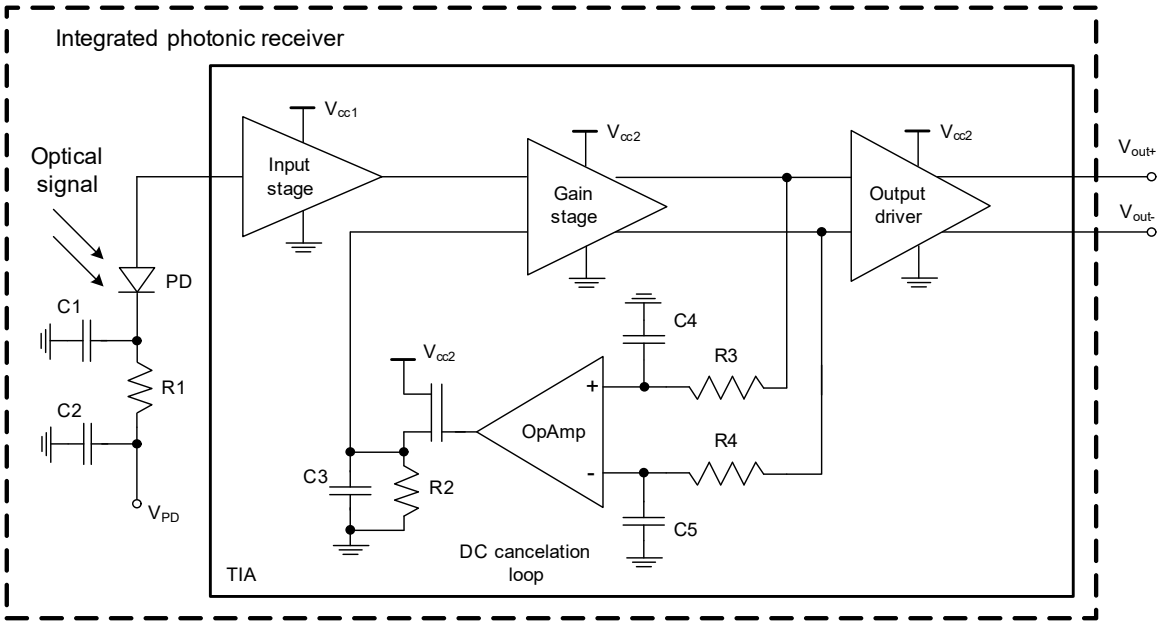

Figure 8. Block diagram of the TIA with integrated PD (integrated optical receiver).

The presented TIA consists of three functional stages: input, gain and output ones. The inputs stage is designed based on requirements of high transimpedance gain and low added noise. The gain stage amplifies the electrical signal, corrects the frequency response and bandwidth, and converts it to signal the differential one. Output buffer stage has usually low gain (0–1 dB), its role is a transfer of output power to the load and a matching of TIA with a differential load of 100 Ohm. The optical signal with intensity modulation is detected by the PD, which in turn generates a photocurrent and parasitic DC current. This parasitic DC current is the result of the direct detection principle, the modulated signal is squared on the PD and, as a result, the photocurrent consists of a DC component, modulating informational signal, and harmonics [25]. The generated DC depends on the input optical signal power and changes the bias point of the input transistor, limits the linearity, and leads to the imbalance of the other circuitry.

To exclude the influence of the parasitic DC current on the integrated photonic receiver performances, the DC cancellation loop is designed (Figure 8) [25]. The output voltages of the gain stage are taken using the low-pass filter (R3–R4, C4–C5) and are compared by the operational amplifier (OpAmp). The resulting low frequency error signal at the OpAmp output adjusts the voltage at the gain stage input. In addition, this DC loop performs a cancellation of the possible imbalance between two differential signal paths due to temperature, process variation, etc. The OpAmp is implemented on CMOS transistors using a differential amplifier circuit with an active load.

The schematic diagram of the designed three-stage TIA with a differential output and DC cancellation loop is illustrated in Figure 9.

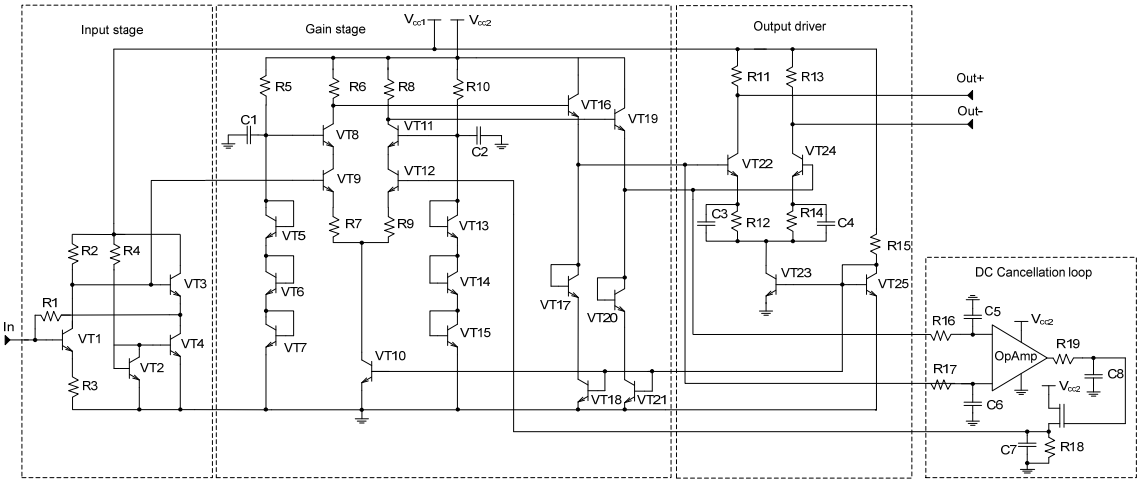

Figure 9. Schematic diagram of TIA.

The first stage of the TIA uses a shunt feedback circuit based on common-emitter amplifier stage (VT1) and following a common collector or emitter follower stage (VT3). The alternative common base amplifier approach has higher noise performance and poor gain, but lower input impedance and stable performance over the temperature variations [26]. The feedback resistor R1 and transconductance of VT1 determine transimpedance, bandwidth and noise performance. The size and bias of VT1 were accordingly chosen to reduce the noise performance of the TIA. For a high transimpedance gain and low input-referred noise, the value of the feedback resistor R1 should be maximized; however, on the other side, this will lead to the bandwidth limitation of the TIA. So, the value of R1 = 300 Ohm was used to achieve the bandwidth of 20 GHz and appropriate noise performance and transimpedance gain. The input stage uses a bias voltage of V_{cc1} = 2.5 V and consumes a current of I_{cc1} = 6 mA.

Another way of bandwidth extension is the inductor peaking technique [27,28], which is usually used in the collector or drain of an input transistor. The use of a planar inductor significantly complicates the layout design and increases the overall chip size. Instead of inductor peaking, the capacitive correction circuits is used in the output stage.

The second stage of TIA is implemented based on the differential cascode circuit (VT8, VT9, VT11, VT12) and emitter followers (VT16 and VT19). The signal for one differential channel of gain stage is taken from the base of VT3, while the second differential channel is controlled by the DC cancellation loop. The emitter followers are used to match the gain stage with an output driver and reduce the capacitance load for the cascode circuit, which increases the overall bandwidth of TIA. Output differential driver utilizes the common emitter circuit with capacitive degeneration (C3, C4, R12, R14), which compensates the frequency-dependent PD conversion gain and flattens the overall gain of the photonic IC receiver. To match the TIA and deliver output power to the differential 100 Ohm load, the value of resistors R11 = R13 = 60 Ohm is chosen. The gain and output stages use a bias voltage of V_{cc2} = 3.3 V and consume a current of I_{cc2} = 44 mA.

The layout of the manufactured photonic IC receiver is depicted in Figure 10; the chip size with optical and electrical pads is 1460 µm × 850 µm. The optical signal at the λ = 1550 nm wavelength passes in IC through the grating coupler and goes to the PD via a strip waveguide. Additionally, the PD is biased by reverse voltage V_{PD} = 2 V to increase the sensitivity of the optical receiver. The bias circuits for PD are realized on the chip (Figure 8).

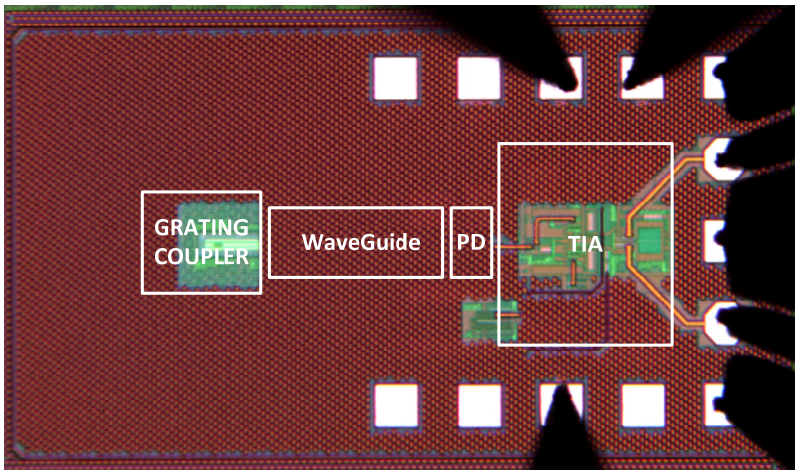

Figure 10. Integrated photonic receiver with analog bandwidth of DC-20 GHz (1.46 × 0.85 mm^2).

At first, the designed integrated photonic receiver was characterized on wafer using a probe station (Figure 11). The output signal was taken by GSGSG probe, while PD bias and supply voltage of TIA were fed using DC probes (Figure 9). The losses of the grating coupler are about 3 dB and depend on the incidence angle, wavelength and polarization. To get a maximum of optical coupling, special micropositioners at an incidence angle of 10–14° were used.

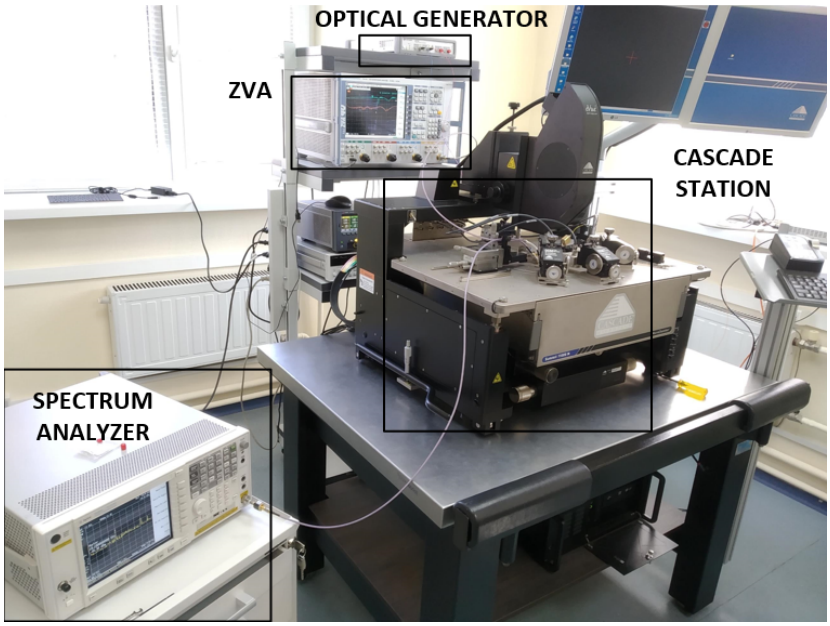

Figure 11. Photograph of the test bench for photonic IC receiver measurements.

The optical heterodyne method [29–31] was used to evaluate the bandwidth of designed IC. The measurement test bench is depicted in Figure 11 and consists of probe station, spectrum analyzer, optical generator, and vector network analyzer. Two optical signals at closed wavelengths λ_1 and λ_2, generated by the optical source, enter to the IC; then, PD detects the difference $\Delta f = c \cdot (\lambda_2 - \lambda_1)/\lambda_2 \cdot \lambda_1$. Then, this difference frequency Δf is amplified and registered by the microwave spectrum analyzer. Changing the difference frequency, one can measure the bandwidth of the photonic IC receiver. A four-port vector network analyzer up to 40 GHz was used to measure the reflection coefficient at both output pads.

The measured normalized O/E conversion gain G_{norm} and output reflection coefficients are illustrated in Figure 12. The measured value of f_{-3dB} analog bandwidth is 22.5 GHz, which is enough

for 25 Gb/s datalinks and agreed with simulated results [32]. The reflection coefficients at both output ports of photonic IC receiver ($|S_{22}|$ and $|S_{33}|$) are better than −15 dB up to 30 GHz.

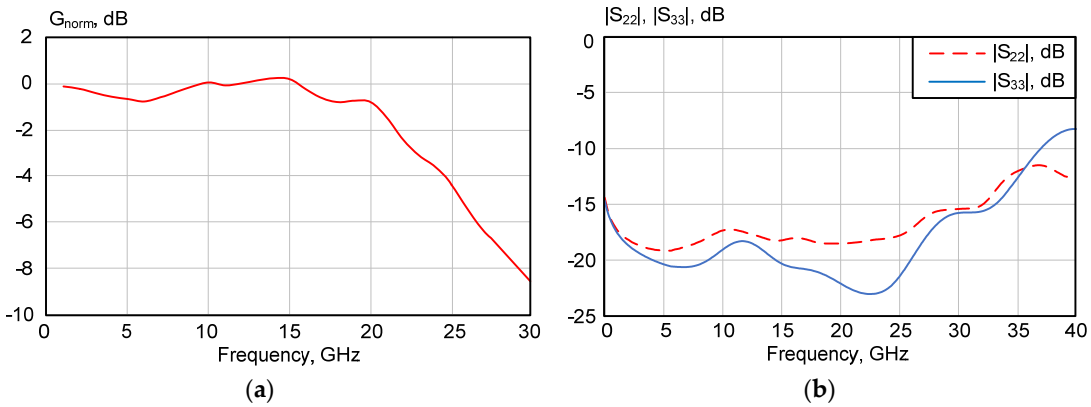

Figure 12. Measured normalized O/E conversion gain of photonic IC receiver (**a**) and output reflection coefficients (**b**).

The second step is to measure the total conversion gain of the microwave photonic link that includes the E/O modulator and designed integrated receiver. For this purpose, the PCB with a photonic IC receiver using Rogers 4350B was designed. The chip was mounted and wire bonded on the PCB as depicted in Figure 13.

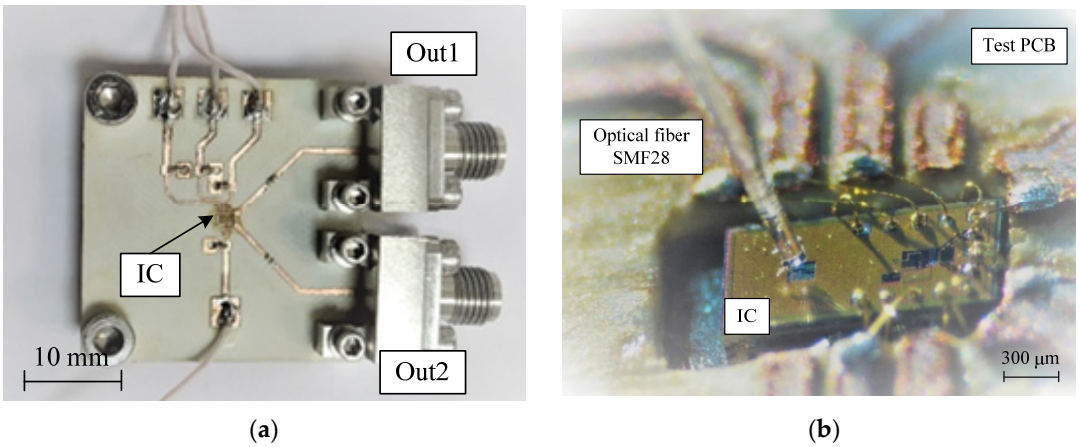

Figure 13. Photograph of the test PCB for photonic IC receiver (**a**) and optical fiber with a chip (**b**).

A block diagram of a setup for microwave photonic link measurement is depicted in Figure 14a. The optical signal with output power P_O = +15 dBm at λ = 1550 nm is modulated by vector network analyzer (VNA) ZVA40 (P_{RF} = 0 dBm) and E/O modulator Lucent 2623NA. A polarizer was used to tune the light polarization and maximize the coupling coefficient for the grating coupler at the chip. The total losses of 13 dB consist of the external E/O modulator insertion losses (around 3–4 dB), its quadrature bias point (about 3 dB), optical fiber (SMF28), and optical connectors.

Then, the modulated light enters the IC through the optical fiber and grating coupler (Figure 13b). Demodulated and amplified electrical signal are taken by VNA, while another output port of the receiver is terminated at 50 Ohm.

The conversion gain of the microwave photonic link as well as reflection coefficients of the E/O modulator and PCB receiver are shown in Figure 14b. The conversion gain varies from −13 dB up to −23 dB, and the receiver's reflection coefficient is better than −10 dB up to 17.5 GHz. The reduction of the overall bandwidth is caused by limited E/O modulator bandwidth and wire bonding. As can be seen from the results, E/O modulator Lucent 2623NA is matched only up to 12–13 GHz. The gain slope

of 10 dB from 1 GHz up to 20 GHz is determined by E/O modulator frequency response (6 dB slope up to 18 GHz) and losses in PCB transmission lines and connectors. Also, the linearity of the presented microwave photonic link with an external E/O modulator was measured. Figure 15 illustrates the measured output power at harmonics (f_1, f_2 and f_3) at f = 1.5 GHz. The IIP3 value of 10 dBm at 1.5 GHz was obtained.

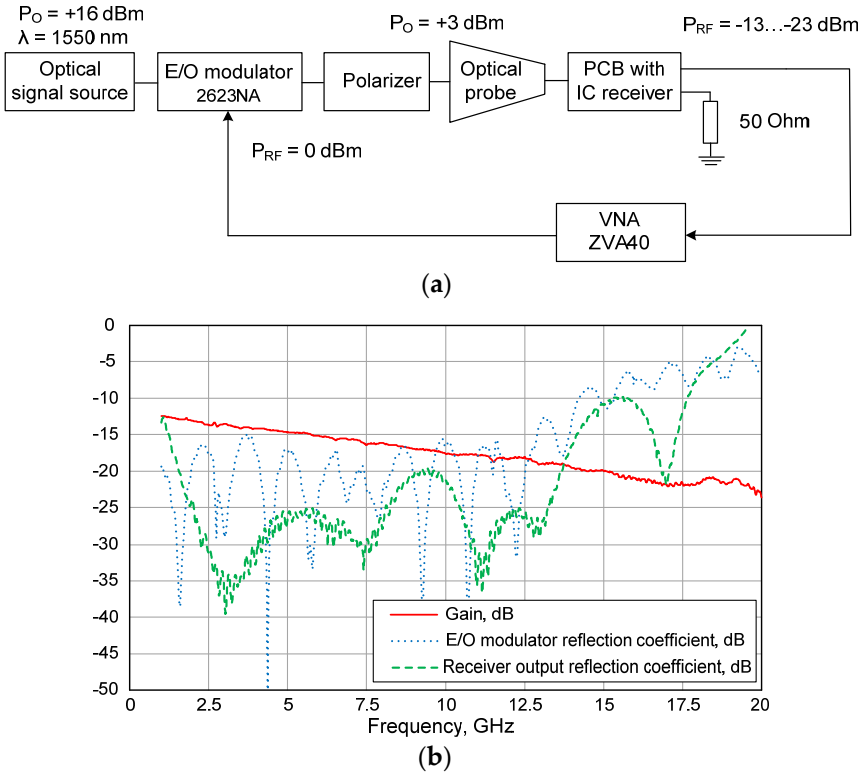

Figure 14. Block diagram of measurement setup (**a**) and measured conversion gain of the microwave photonic link, E/O modulator and PCB receiver reflection coefficients (**b**).

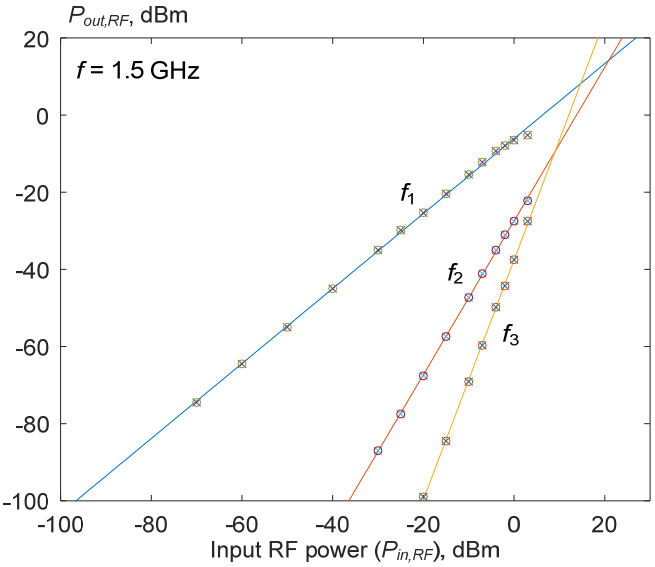

Figure 15. Measured output power at harmonics (f_1, f_2 and f_3) vs. input RF power for microwave photonic link at f = 1.5 GHz.

Measured and simulated performance of designed integrated photonic receiver as well as comparison with the state-of-the art monolithic receivers and TIAs are summarized in Table 1.

Table 1. State-of-the-art integrated photonic receivers with bandwidths more than 15 GHz.

Ref.	Δf, GHz	Z_T, Ω	i_n, pA/√Hz	P_{diss}, mW	Technology, Chip Size
[27]	15	1200	22	32	0.18 μm BiCMOS SiGe:C, 0.54 × 0.55 mm^2
[28]	20	3400	22.6	295	65 nm CMOS, 0.5 × 0.715 mm^2
[33]	20	5500	40	-	0.13 μm CMOS, 1.2 × 0.8 mm^2
[34]	31	1800	28.1	275	0.25 μm BiCMOS SiGe:C, 1 × 3.2 mm^2
[35]	34	7000	-	416	0.25 μm BiCMOS SiGe:C, 2.5 × 1.1 mm^2 (dual)
[36]	20.5	3500	18	57	0.25 μm BiCMOS SiGe:C, 0.9 × 0.6 mm^2
[37]	22	2000	22	75	90 nm CMOS, 0.86 × 0.65 mm^2
[38]	26	800	21.3	28.2	0.25 μm BiCMOS SiGe:C, 0.96 × 0.78 mm^2
[39]	30	6300	11.5	45	55 nm BiCMOS SiGe, 0.72 mm^2
[40]	34	4500	20	313	0.13 μm BiCMOS SiGe:C, 2.24 mm^2 (dual)
This work	22	1400	15.6 [1]	160	0.25 μm BiCMOS SiGe:C, 1.46 × 0.85 mm^2

[1] simulated data.

The integrated optical receivers [35,40] have the highest analog bandwidth of 34 GHz, also they were developed for coherent communication systems (for multiple QAM or QPSK modulation schemes). However, Ref. [40] uses more high-frequency 0.13 μm BiCMOS technology, while in [35], the dissipated power is 208 mW for one channel of the receiver. The photonic receiver [39] has the lowest input-referred noise i_n of 11.5 pA/Hz and low P_{diss}, while it uses a more expensive 55 nm technology node. Among photoreceivers [34,36,38], which are based on 0.25 μm BiCMOS technology, the presented IC has comparable performance and the lowest input-referred noise value.

5. Conclusions

The design, simulation and experimental results of the integrated optical and electronic components for the 25 Gb/s microwave photonic link based on the 0.25 μm SiGe:C BiCMOS technology process are presented. A depletion-type Mach-Zehnder modulator (MZM) and driver amplifier are intended for E/O integrated transmitter. The optical divider and combiner of MZM are designed based on the self-imaging theory and then simulated. In order to verify the correctness of the theory and material properties used in simulation, and to define the construction of the segmented modulator with several driver amplifiers, the short test (prototype) MZM of 1.9 mm length is produced and measured. It shows an extinction ratio of 19 dB and half-wave voltage-length product of $V_\pi \cdot L$ = ~1.5 V·cm. The designed driver amplifier unit provides a bandwidth of more than 30 GHz, saturated output power of 6 dBm (output voltage of V_{pp} = 1.26 V), and matching better than −15 dB up to 35 GHz; in addition, it dissipates 170 mW of power and occupies an area of 0.4 × 0.38 mm^2. The O/E receiver consists of a Ge-photodiode and transimpedance amplifier that are integrated on a single chip. The measured O/E 3 dB analog bandwidth of the integrated receiver is 22 GHz, and output matching is better than −15 dB up to 30 GHz, which makes the receiver suitable for 25 Gb/s links with intensity modulation. The receiver operates at 1.55 μm wavelength, uses 2.5 V and 3.3 V power supplies, dissipates 160 mW of power, and occupies an area of 1.46 × 0.85 mm^2.

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