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Two New Asymmetric Boolean Chaos Oscillators with No Dependence on Incommensurate Time-Delays and Their Circuit Implementation

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Received: 17 February 2020; Accepted: 7 March 2020; Published: 1 April 2020



Abstract: This manuscript introduces two new chaotic oscillators based on autonomous Boolean networks (ABN), preserving asymmetrical logic functions. That means that the ABNs require a combination of XOR-XNOR logic functions. We demonstrate analytically that the two ABNs do not have fixed points, and therefore, can evolve to Boolean chaos. Using the Lyapunov exponent's method, we also prove the chaotic behavior, generated by the proposed chaotic oscillators, is insensitive to incommensurate time-delays paths. As a result, they can be implemented using distinct electronic circuits. More specifically, logic-gates-, GAL-, and FPGA-based implementations verify the theoretical findings. An integrated circuit using a CMOS 180nm fabrication technology is also presented to get a compact chaos oscillator with relatively high-frequency. Dynamical behaviors of those implementations are analyzed using time-series, time-lag embedded attractors, frequency spectra, Poincaré maps, and Lyapunov exponents.

Keywords: chaotic oscillator; lyapunov exponents; poincare map; integrated circuit; fpga; time-delay; boolean networks

1. Introduction

Chaos behavior is one of the most studied topics in nonlinear dynamics in recent years. Such interest relies mainly on its extreme sensitivity to the initial conditions. From a real-world application point of view, the random-like patterns generated by chaotic oscillators are currently pointed out as the core for obtaining significant engineering applications, for instance, secure-communications schemes [1–7]; radars [8–10]; sonars [11,12]; liquid mixing [13,14]; adaptive logic gates [15,16]; true random number generators (TRNGs) [17,18]; collective phenomena in physics and biology [19,20]; navigation and control of autonomous mobile robots [21–23]; Internet of Things [24–29]; and so forth. Thereupon, the cutting edge chaos-based applications may need reliable, robust, compact, and faster chaos oscillators.

A remarkable solution to obtain chaotic behavior consists of exploiting the delay paths in autonomous Boolean networks (ABNs) [30–34]. Kauffman proposed the Boolean networks in 1969 as a mathematical framework for studying gene regulatory networks. The mathematics describing ABNs has shown that they could display aperiodic patterns if the Boolean functions have instantaneous response times, the link time-delays are incommensurate, and their nodes perform asymmetric Boolean operations, such as the combination of logic exclusive-OR (XOR) and XNOR functions.

In the context of ABNs, deterministic chaos, also known as Boolean chaos, was initially demonstrated by using Boolean functions implemented with electronic logic circuits (logic gates and field-programmable gate arrays FPGAs) [10,35–38]. At circuit level, the basic principle for obtaining Boolean chaos depends on three main characteristics; the asymmetry between the logic states, the short-pulse rejection phenomenon, and, most importantly, the degradation effect [30,31].

As is well-known, the incommensurate delay between two different nodes of an ABN is the critical parameter to obtain chaotic behaviors since it induces the degradation effect [30–34]. Rosin et al. analyzed two ABNs, one composed of a logic XOR function and two delays τ_{n_k} and τ_{n_l} , and the other one with a logic XNOR function and three delays τ_{n_k} , τ_{n_l} , and τ_{n_m} [38]. They showed that Boolean chaos arises in an FPGA-based implementation when the delays for each of the three delay paths are $\tau_{n_k} \geq 2.8$ ns, $\tau_{n_l} \geq 1.7$ ns, and $\tau_{n_m} \geq 0.56$ ns, respectively. To attain the time-delays, they required 18 extra logic NOT gates to connect the nodes of ABN. Besides, if those time-delays reduce below the minimum, the ABN does not show chaos and evolves to periodic oscillations only, as was analyzed in Ref. [35]. Park et al. presented an ABN composed of a logic XOR gate and ring oscillator [39]. The proposed logic circuit synthesized on an application-specific IC (ASIC), but the design is not straightforward because it also demands specific incommensurate delays in the feedback path to observe Boolean chaos.

Based on the discussion mentioned above, we note a possible benefit of using ABNs can be to get Boolean chaos oscillators with relatively high oscillation frequencies and small form factors since they depend on logic functions only. However, we also found that the proposed ABNs have high sensitivity to the time-delay among network nodes for generating chaos behavior. From a practical point of view, that condition is very complicated to satisfy since the time-delays are heavily related to the electronics technology chosen for implementation. Due to the electronic logic gates being heterogeneous, they do not have the same intrinsic time-delay. As a consequence, the dynamical behaviors of the ABN can be affected by placing the oscillator on a different area into an integrated circuit or FPGA. In conclusion, the previously reported Boolean chaos oscillators may not be suitable for physical realizations with multiple hardware approaches.

In this paper, we propose two ABNs with three and two nodes, respectively. The nodes perform the logic XOR and XNOR operations. This asymmetric approach avoids fixed points in the ABNs, and therefore, their dynamics can converge to chaotic oscillations. By applying the Lyapunov exponent method, we experimentally demonstrate that the Boolean chaos oscillators do not require specific incommensurate time-delays to show chaotic behaviors. Indeed, the Boolean chaos was observed under a wide range of the time-delays for the ABNs nodes. We prove our findings by implementing the proposed ABNs using various logic electronic circuits without any modification neither of the proposed networks nor adding additional path delays. Three discrete physical realizations using commercial logic gates, a Generic Array Logic (GAL), and FPGA are presented. Besides, we design an integrated circuit realization at 180nm fabrication technology.

The structure of the manuscript is as follows. Section 2 introduces the two ABNs and gives the mathematical demonstrations of their equilibrium points. Section 3 shows the analysis based on the Lyapunov exponents to determine the insensibility to time-delays. Section 4 presents the Lyapunov exponents for three different discrete implementations to prove that the ABNs are not affected by the technology. Section 5 introduces a straightforward methodology to design an integrated circuit of the Boolean chaos oscillators. Time-series, phase space reconstruction, Lyapunov exponents, and Poincare maps validate the observed chaos behavior. Finally, the last section concludes the paper.

2. Mathematical Preliminaries

A Boolean network consists of a number of logical nodes interconnected through direct or indirect links. These are nonlinear networks requiring a mathematical base for analysis. Among the present models there are: the Kauffman (N-K) networks, Boolean differential equations, and piecewise-linear

differential equations [33,34]. This work uses the Boolean differential equations to develop important mathematical considerations.

2.1. Boolean Differential Equations

Let us consider a system with state variables $\{v_1, v_2, \dots, v_n\}$, $v_i \in \mathbb{R}$, $i = 1, \dots, n$. If a Boolean variable x_i is related to each state v_i , depending on a set of thresholds $\sigma_i \in \mathbb{R}$. Then, the set of Boolean variables $x = \{x_1, x_2, \dots, x_n\}$ gives a simple qualitative description of the system with 2^n possible states. By adding the time dependence through a set of delays $\{\tau_{ij}\}$, $i = 1, \dots, n$, $j = 1, \dots, n$, $\tau_{ij} > 0$, where τ_{ij} is the time it takes for x_j to affect x_i , there is an associated time delay for each pair of state variables not necessarily obeying $\tau_{ij} = \tau_{ji}$. In this manner, the feedbacks among the Boolean variables can be described by a system of Boolean differential equations as follows [33,34]:

$$\begin{aligned} x_1(t) &= f_1(x_1(t - \tau_{11}), x_2(t - \tau_{12}), \dots, x_n(t - \tau_{1n})), \\ x_2(t) &= f_2(x_1(t - \tau_{21}), x_2(t - \tau_{22}), \dots, x_n(t - \tau_{2n})), \\ &\vdots \\ x_n(t) &= f_n(x_1(t - \tau_{n1}), x_2(t - \tau_{n2}), \dots, x_n(t - \tau_{nn})), \end{aligned} \quad (1)$$

with $f_i : \mathbb{B}^n \rightarrow \mathbb{B}$, $i = 1, \dots, n$, being a set of Boolean functions where $\mathbb{B} = \{0, 1\}$. The system (1) determines the dynamics of a Boolean network considering time delays, thereby defining an *Autonomous Boolean Network* (ABN) [33,34]. The dynamics of the ABN given by Equation (1) is numerically solved once the Boolean functions are defined with initial conditions on an interval $x_i(t) = x_{i0}(t)$ for $t_0 - \tau \leq t \leq t_0$, $i = 1, \dots, n$, where $\tau = \max\{\tau_{ij}\}$ is the memory length of the system.

2.2. Boolean Chaos

In an ideal ABN, the transitions of the signals are arbitrarily fast and the number of transitions increases with time, following a power law. These increasingly fast dynamics result in an unlimited growth of frequency over time, referred to as an ultraviolet catastrophe [30]. However, that phenomenon does not occur in nature because the information-transmitting links and the processing nodes (for instance real logic gates) have a maximum operation frequency, which are physically realized. Hence, they cannot transmit or generate signals above a certain frequency [31]. As a result, the nonideal behaviors of real logic devices are responsible for the origin of chaos in ABNs [30,31]. Those behaviors are (i) Short-pulse rejection (SPR), known as pulse filtering, preventing pulses shorter than a minimum duration from passing through the gate (Theorem 1). (ii) The asymmetry between the logic states, making the propagation delay time through the gate depending on whether the transition is a fall or rise. (iii) The degradation effect triggering a change in the events propagation delay time when they appear in rapid succession. Among them, the degradation effect is the main nonideal behavior source of deterministic chaos in an ABN [32], since Boolean chaos originates from a history-dependent delay [30,31], as defined Lemma 1.

Theorem 1. For a symmetric ABN consisting of a single XOR logic operation with two self-inputs having delays τ_1 and τ_1 , and with τ_{spr} sufficiently small not collapsing to the always-off state occurs before $t = \tau_2$, the trajectory will never reach the always-off state.

Lemma 1. For a class of experimental ABN containing at least one XOR connective and feedback loop, deterministic chaos may arise if and only if the degradation effect, which is exhibited at some level in any real ABN, is presented.

On the other hand, if the ABN has equal delays, the links will produce only regular oscillations. In addition, the fixed points caused by using only symmetric logic functions in the network nodes

conduct that the dynamics will always collapse into a low or high logic state, respectively. Theorem 2 and Lemma 2 postulates the conditions. As a reference, the complete proofs of Theorems and Lemmas can be found in [31,35].

Theorem 2. For a symmetric ABN consisting of a single exclusive-OR (XOR) logic operation with two self-inputs having delays τ_1 and τ_2 , the attractors are always periodic.

Lemma 2. The experimentally realized ABNs should not include a Boolean fixed point, for which all Boolean functions are satisfied simultaneously.

2.3. Lyapunov Exponents for ABNs

One of the most reliable tools to demonstrate chaotic behavior is computing the Lyapunov exponent's spectrum [1–29]. A positive Lyapunov exponent is a signature of chaos [40]. It is defined as the exponential divergence of trajectories with nearly identical initial conditions. For the ABNs case, since the states are discrete, indicating a phase space composed just by 2^N states, the Lyapunov exponent's needs to be computed from distance measures tailored for Boolean systems [41].

Zhang et al. proposed a method to estimate the largest Lyapunov exponent using the Boolean distance definition [30]. The approach works as follows. (i) Acquire experimentally a long time series from an output voltage of the ABN. (ii) Convert that voltage to a Boolean variable $x(t)$. (iii) Given any two segments of starting at times t_a and t_b , define a Boolean distance with $d(s) = \frac{1}{T} \int_s^{s+T} x(t' + t_a) \oplus x(t' + t_b) dt'$, where T is a fixed parameter, \oplus is the XOR logic operation, and the Boolean distance $d(s)$ evolves as a function of the time s . (iv) Search in $x(t)$ for all the pairs t_a and t_b corresponding to the earliest times in each interval T over which $d(0) < 0.01$. (v) Finally, (v) compute $\ln\langle d(s) \rangle$, where $\langle \rangle$ means an average over all matching (t_a, t_b) pairs.

As a conclusion, the divergence $\ln\langle d(s) \rangle$ increases exponentially, as expected for an adequate definition of distance between trajectories in a chaotic system [40].

3. The Proposed Boolean Chaos Oscillators (BCOs) and Their Fixed Points

Motivated by Ref. [30], this work introduces two ABNs composed by three and two nodes, respectively. The nodes of ABNs perform asymmetric logic functions, i.e., a combination of Boolean operations XOR and XNOR. We detail the proposed ABNs as follows.

3.1. BCO-1

Figure 1a shows the first Boolean chaos oscillator (BCO). It consists of three nodes where each node has three inputs and one output that propagates to three different nodes. Nodes A and B perform the XOR logic operation while node C executes the XNOR. Expressing BCO-1 in the form of Equation (1), we obtain the following system of Boolean delay equations:

$$\begin{aligned} X_a(t) &= X_a(t - \tau_{aa}) \oplus X_b(t - \tau_{ab}) \oplus X_c(t - \tau_{ac}), \\ X_b(t) &= X_a(t - \tau_{ba}) \oplus X_b(t - \tau_{bb}) \oplus X_c(t - \tau_{bc}), \\ X_c(t) &= X_a(t - \tau_{ca}) \oplus X_b(t - \tau_{cb}) \oplus X_c(t - \tau_{cc}) \oplus 1, \end{aligned} \quad (2)$$

with Boolean functions $f_i : \mathbb{B}^3 \rightarrow \mathbb{B}$, $i = 1, \dots, 3$, and \oplus the logic XOR operation. The signal propagation time from node j to node i is τ_{ij} for $i, j = a, b, c$.

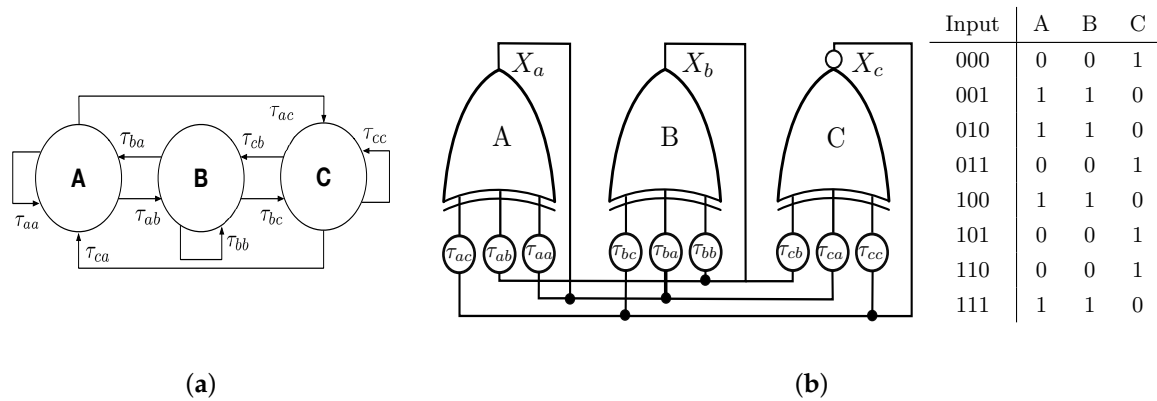


Figure 1. (a) Autonomous Boolean networks (ABN) for the proposed Boolean chaos oscillator (BCO-1). (b) An implementation of BCO-1 using electronic logic gates and its look-up table.

Theorem 3. For an autonomous Boolean network given by the system of Equation (2), the orbits are always oscillating [36].

Proof. A Boolean fixed point provokes nonoscillating dynamics due to some orbits eventually collapsing into the fixed point. To demonstrate the proposed Boolean chaos oscillator converges to sustained oscillations indefinitely, we must prove that there is not a fixed point. By contradiction, we demonstrate this theorem. Let us assume that the BCO-1 has a fixed point (X_a^*, X_b^*, X_c^*) , such that:

$$\begin{aligned} X_a^* &= X_a(t - \tau), \\ X_b^* &= X_b(t - \tau), \\ X_c^* &= X_c(t - \tau), \end{aligned}$$

for $t \gg \tau = \max\{\tau_{aa}, \tau_{ab}, \tau_{ac}, \tau_{ba}, \tau_{bb}, \tau_{bc}, \tau_{ca}, \tau_{cb}, \tau_{cc}\}$. In this manner, the system of Equation (2) recast as:

$$X_a(t) = X_a(t) \oplus X_b(t) \oplus X_c(t), \tag{3}$$

$$X_b(t) = X_a(t) \oplus X_b(t) \oplus X_c(t), \tag{4}$$

$$X_c(t) = X_a(t) \oplus X_b(t) \oplus X_c(t) \oplus 1. \tag{5}$$

By substituting Equations (3) and (4) into (5), we obtain:

$$\begin{aligned} X_c(t) &= X_a(t) \oplus X_b(t) \oplus X_c(t) \oplus X_a(t) \oplus X_b(t) \oplus \\ &X_c(t) \oplus X_c(t) \oplus 1. \end{aligned} \tag{6}$$

Equation (6) implies $X_c(t) = \overline{X_c(t)}$. Since the Boolean space is 2^n , the possible states for $X_c(t)$ are $\{1, 0\}$. Thus, “1” = “0”, or vice-versa indicates a contradiction which leads us to conclude that Boolean network (2) does not have fixed points, and therefore, always oscillates. \square

3.2. BCO-2

Figure 2a shows the second Boolean chaos oscillator introduced in this work. The proposed topology consists of two nodes, where each node has three inputs and one output connecting to two different nodes. While node A performs the XOR logic operation, node B executes the XNOR. Additionally, the ABN includes two logic NOT operations to obtain the opposed Boolean states for both nodes. The set of Boolean delay equations for the BCO-2 are:

$$\begin{aligned}
 X_a(t) &= X_a(t - \tau_{aa}) \oplus X_b(t - \tau_{ab}) \oplus \neg X_a(t - \tau_{a\bar{a}}), \\
 X_b(t) &= X_a(t - \tau_{ba}) \oplus X_b(t - \tau_{bb}) \oplus \\
 &\quad \neg X_b(t - \tau_{b\bar{b}}) \oplus 1,
 \end{aligned}
 \tag{7}$$

with \oplus and \neg indicating the logic XOR and NOT operations, respectively. In addition, the Boolean functions $f_i : \mathbb{B}^2 \rightarrow \mathbb{B}, i = 1, \dots, 2$. Similarly to the previous case, it is necessary to prove that the system (7) does not have a Boolean fixed point.

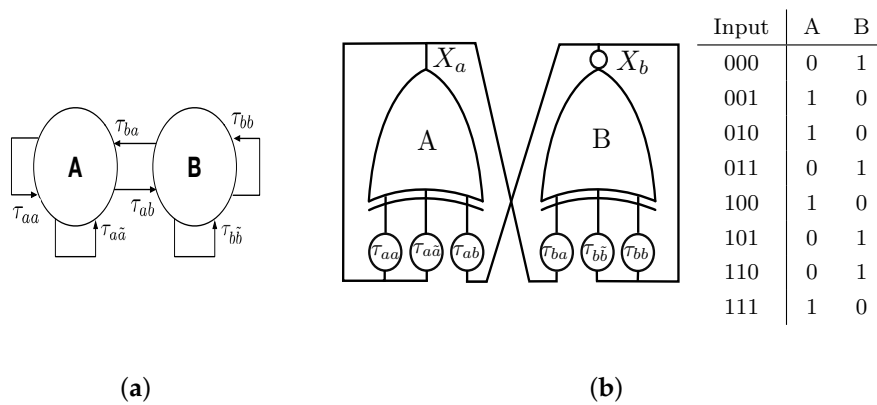


Figure 2. (a) ABN for the second Boolean chaos oscillator (BCO-2). (b) An implementation of BCO-2 using electronic logic gates and its look-up table.

Theorem 4. For an autonomous Boolean network given by the system of Equation (7), the orbits are always oscillating [36].

Proof. We assume that the BCO-2 has the fixed point (X_a^*, X_b^*) , such that $X_a^* = X_a(t - \tau)$ and $X_b^* = X_b(t - \tau)$, for $t \gg \tau = \max\{\tau_{aa}, \tau_{ab}, \tau_{a\bar{a}}, \tau_{ba}, \tau_{bb}, \tau_{b\bar{b}}\}$. Therefore, system (7) is rewritten as:

$$X_a(t) = X_a(t) \oplus X_b(t) \oplus \neg X_a(t), \tag{8}$$

$$X_b(t) = X_a(t) \oplus X_b(t) \oplus \neg X_b(t) \oplus 1, \tag{9}$$

By inserting Equation (8) into (9), we obtain:

$$\begin{aligned}
 X_b(t) &= X_a(t) \oplus X_b(t) \oplus \neg X_a(t) \oplus X_b(t) \oplus \\
 &\quad \neg X_b(t) \oplus 1.
 \end{aligned}
 \tag{10}$$

Equation (10) means $X_b(t) = \overline{X_b(t)}$. This again implies a contradiction and it is possible to claim that the autonomous Boolean network (7) does not have a fixed point and it will oscillate permanently. \square

3.3. Boolean Sensitivity Caused by Asymmetric Logic Functions

As demonstrated in the previous subsection, the presented BCOs do not have fixed points. In this manner, when an autonomous Boolean network is realized experimentally it should include asymmetric Boolean functions to achieve chaotic dynamics [31,35]. As a result, the preference for using logic XOR and XNOR functions in the proposed BCOs lies on the look-up table for these logic operations. Firstly, the idea is considering an equal number of “1”s and “0”s as the output of the XNOR operation to avoid converging into a physical Boolean fixed-point, i.e., where all entries of the

look-up table have the same value, and hence inputs and outputs can be the same. From the look-up tables in Figures 1b and 2b, the outputs are different for all inputs, including the cases “000” and “111”. On the other hand, since the number of “0”s and “1”s in the look-up tables is equal, the proposed BCOs can have a higher Boolean sensitivity $E = 2K\rho(1 - \rho)$ [30,35]. This is possible with randomly chosen Boolean functions of bias $\rho = 0.5$ (equal number of zeros and ones) and high in-degree K (the number of input connections to a node) or most effectively by using XOR and XNOR Boolean functions as herein.

4. Boolean Chaos Robust to Different Incommensurate Time-Delays

The chaos-based applications demand the exploration of different typologies and implementations to find those that are the most suitable. In addition, the chaotic behavior must be robust. It means that the chaos should be generated consistently for a wide range of parameter values. In the ongoing literature, the reported autonomous Boolean networks only show chaos in certain ranges of the feedback delays [10,30,31,35–39], as was discussed in the Introduction section. At the experimental level, those approaches incorporate an even number of logic NOT gates in the link to act as a time-delay buffer to add extra signal propagation times. Then, the published works need several pairs of NOT gates to satisfy the specific incommensurate time-delays for each one of their links connecting nodes. Otherwise, the chaotic behavior converges to either periodic oscillations or stable dynamics in the Boolean levels high or low.

Conversely, the proposed BCOs in Figures 1 and 2 do not require additional logic NOT gates to generate chaotic oscillations. This means that the chaos behavior depends solely on the incommensurate time-delays, arising only from the intrinsic delay associated with each XOR and XNOR gate. In this manner, we state the following Lemma and Corollary.

Lemma 3. *The Boolean chaotic oscillators of Figures 1 and 2 composed only by logic XOR-XNOR functions evolve to sustained chaotic oscillations not only for different time-delays of the feedback path (additional pairs of logic NOT gates) but also when the time-delays in their links are a function just of the intrinsic delay of each XOR-XNOR gates (no extra logic NOT gates).*

Corollary 1. *As a consequence of Theorems 3 and 4, an autonomous Boolean network without fixed points always presents periodic behavior if its delays are commensurate.*

Proof. To demonstrate Lemma 3 and Corollary 1, we show the physical implementation of the BCOs in Figures 1 and 2 using commercial off-the-shelf logic gates (74HCXXX family), as shown in Figure 3a. The discrete implementation makes it possible to change the time-delay between feedback nodes easily. Then, we study the dynamics of the proposed BCOs using the Lyapunov exponent method.

The scenario is as follows. First, we consider different cases for the incommensurate time-delays of the links. Those time-delays were realized using a pair of two NOT gates wired in series. Thus, from the experimental output signal of nodes C (BCO-1) and B (BCO-2) for each case in Tables 1 and 2, respectively, we collect a long enough time series. For instance, the BCO-1 output signal of node C for cases 1, 3, and 7 is given in Figure 4a,d,g, respectively. On the other hand, Figure 5a,d present the results for the output signal of node B of BCO-2 for cases 1 and 5, respectively.

Next, we compute the largest Lyapunov exponent, λ_{max} , applying the Boolean distance algorithm introduced in Section 2.3. The results in Tables 1 and 2 shows the largest Lyapunov exponent, λ_{max} , is positive for all cases indicating the proposed BCOs generate robust Boolean chaos. Besides, the chaotic behavior was also verified in the BCOs (both cases 1 in Tables 1 and 2, respectively), without extra time-delays with exception from those incommensurate intrinsic delays of the logic XOR and XNOR gates, i.e., the BCO-1 and BCO-2 do not include any logic NOT gates in the feedback paths. □

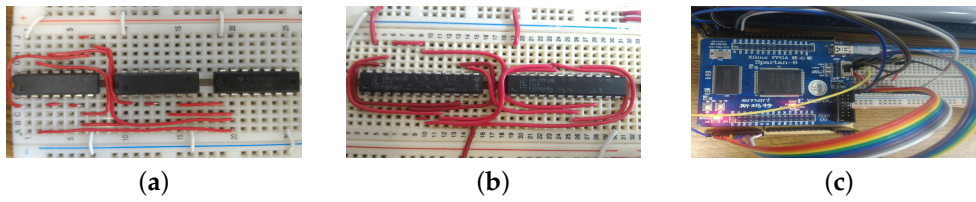


Figure 3. Experimental setup for BCOs in Figures 1 and 2 using (a) logic gates 74HCXXX, (b) GAL 22V10, and (c) FPGA Spartan6.

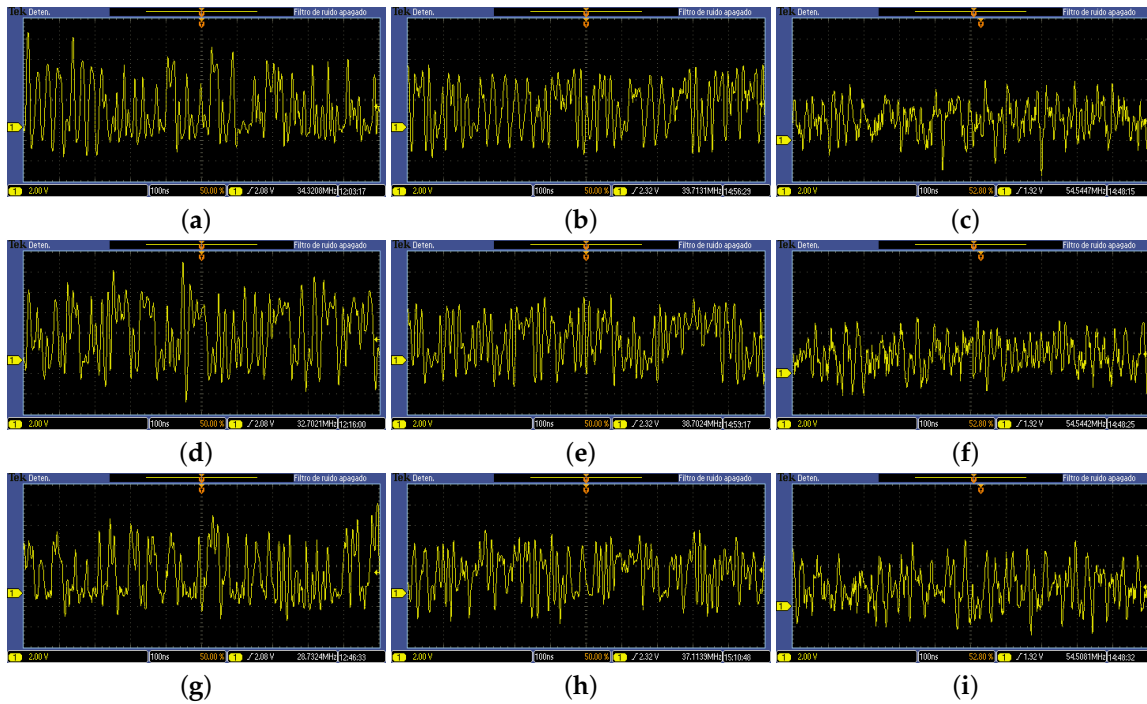


Figure 4. Chaotic oscillations from the output voltage in the node C for BCO-1. The measurements exhibit a 100 ns of time and a 2 V of voltage grid per square. Case 1 in Table 1 with (a) logic gates 74HCXXX, (b) GAL22V10, and (c) FPGA Spartan6. Case 3 in Table 1 with (d) logic gates 74HCXXX, (e) GAL22V10, and (f) FPGA Spartan6. Case 7 in Table 1 with (g) logic gates 74HCXXX, (h) GAL22V10, and (i) FPGA Spartan6.

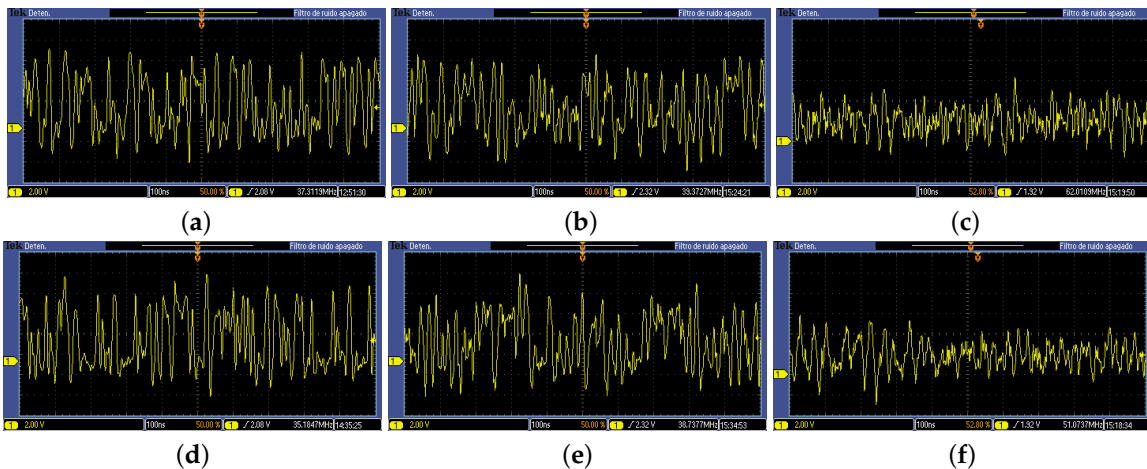


Figure 5. Chaotic oscillations from the output voltage in the node B for BCO-2. The measurements exhibit a 100 ns of time and a 2 V of voltage grid per square. Case 1 in Table 2 with (a) logic gates 74HCXXX, (b) GAL22V10, and (c) FPGA Spartan6. Case 5 in Table 2 with (d) logic gates 74HCXXX, (e) GAL22V10, and (f) FPGA Spartan6.

Tables 1 and 2 suggest the most suitable case for obtaining Boolean chaos is when no other delay paths are incorporated in the links because the higher the time-delays, the lower the magnitude of the largest Lyapunov exponent. From the physical implementation point of view, that is a remarkable feature because we can get a small form factor with the proposed Boolean chaos oscillators. Moreover, since the chaos generation does not depend on determined time-delays, the proposed BCOs can be implemented with several hardware technologies, as demonstrated in the next subsection.

Table 1. Largest Lyapunov exponent (λ_{max}) of the BCO in Figure 1 for different time-delays in the feedback paths. The symbol “-” means no extra time-delay, while “√” refers to a time-delay composed of two logic NOT gates.

Case	Time-Delay									Lyapunov Exponent
	τ_{aa}	τ_{ab}	τ_{ac}	τ_{ba}	τ_{bb}	τ_{bc}	τ_{ca}	τ_{cb}	τ_{cc}	
1	-	-	-	-	-	-	-	-	-	0.2306
2	-	-	-	-	-	-	-	-	√	0.2079
3	√	-	-	-	-	-	-	-	-	0.2275
4	√	-	-	-	-	-	-	-	√	0.2057
5	√	-	-	-	√	-	-	-	√	0.2076
6	√	√	√	-	-	-	-	-	-	0.2101
7	-	-	-	-	-	-	√	√	√	0.2121
8	√	√	√	-	-	-	√	√	√	0.1774
9	√	√	√	√	√	√	-	-	-	0.1808
10	√	√	√	√	√	√	√	√	√	0.1896
11	-	√	√	√	√	√	√	√	√	0.1862
12	-	√	√	√	√	√	√	√	-	0.1707

Table 2. Lyapunov exponent of BCO in Figure 2 for different time-delays in the feedback paths.

Case	Time-Delay						Lyapunov Exponent
	τ_{aa}	τ_{ab}	$\tau_{a\bar{a}}$	τ_{bb}	τ_{ba}	$\tau_{b\bar{b}}$	
1	-	-	-	-	-	-	0.1644
2	-	-	√	-	-	-	0.0960
3	-	-	-	-	-	√	0.1495
4	√	-	-	√	-	-	0.1442
5	-	√	-	-	-	-	0.1525
6	-	-	-	-	√	-	0.1448

Boolean Chaos Robust to Distinct Discrete Physical Implementation

This subsection presents three different physical implementations of the Boolean chaos oscillators. The dynamics are affected by physical constraints and hardware differences. This may lead to time-delay variations where the boolean chaos displays. Therefore, the BCO-1 and BCO-2 are constructed with three different electronic devices (i) commercial-off-the-shelf logic gates (introduced previously), (ii) a GAL, and (iii) an FPGA. The experiments in Figure 3 demonstrate the robust generation of Boolean chaos. From the circuit conception, the implementations show the chaotic behavior source is the degradation effect [32]. In addition, there are no additional procedures to calculate the delay paths to achieve chaotic oscillations.

The implementation considers all cases of Tables 1 and 2, but for the sake of simplicity, the Table 3 displays only the examples where the largest Lyapunov exponent is higher. In particular, case 1 for both BCOs is of particular interest because they do not need extra time-delays for generating chaos. More specifically, we use the GAL22V10 for realizing both BCOs, as given in Figure 3b. The programming of the GAL was performed with VHDL language. Figure 4b,e,h give the experimental results for the cases 1, 3, and 7 of BCO-1; while Figure 5b,e shows the results for cases 1 and 5 of BCO-2. For FPGA implementation, the Spartan 6 was employed (Figure 3c). The experimental

results are shown in Figure 4c,f,i for cases 1, 3, 7 in Table 1, respectively. Figure 5c,f display the output signal for cases 1 and 5 in Table 2, respectively.

The measurements exhibit a 100 ns of time and a 2V of voltage grid per square. For all the three presented implementations, the output voltages (Figures 4 and 5) show the cumbersome temporal oscillations without evident periodicity. This continuous-time evolution can be identified as Boolean chaos. To verify the chaotic behavior, we compute the largest Lyapunov exponent for each implemented case of the corresponding technology, as shown in Figure 6. Table 3 also shows that the Lyapunov exponents for the three physical implementations have a similar value. This behavior suggests the Boolean chaos of proposed BCOs is robust to the distinct physical implementations changing the technology.

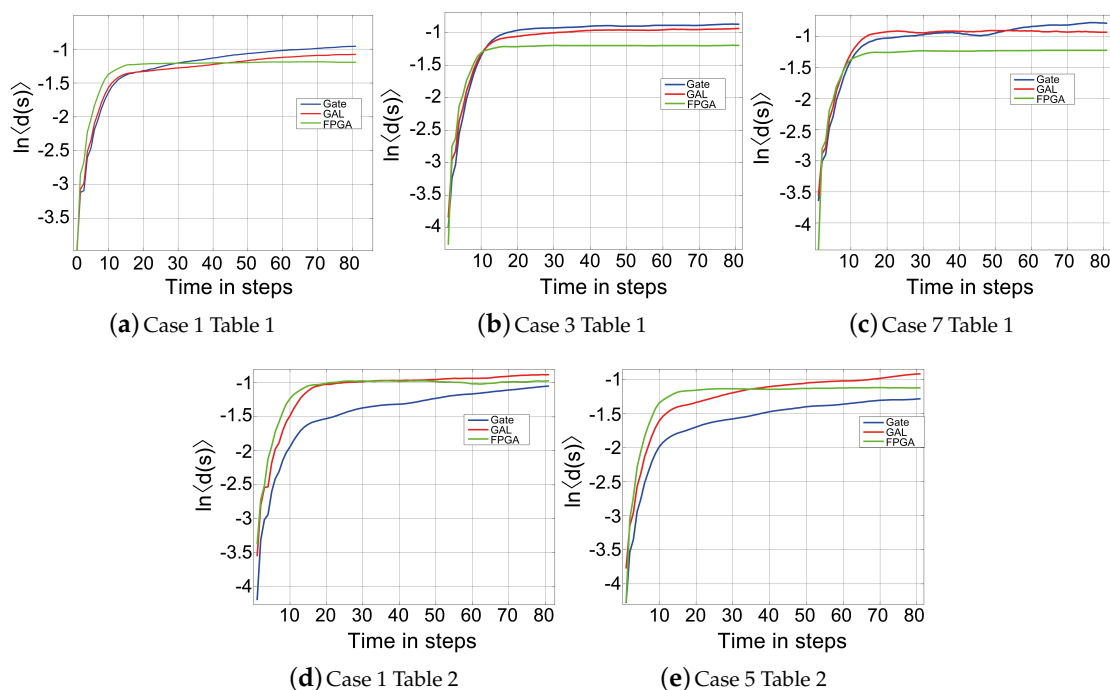


Figure 6. The divergence $\ln\langle d(s) \rangle$ to determine the largest Lyapunov exponent of the attractor for cases in Table 3 from each discrete physical implementation (Logic gates, GAL, FPGA).

Table 3. Largest Lyapunov exponent (λ_{max}) for BCOs in Figures 1 and 2 implemented experimentally with different design technologies considering the time-delays of Tables 1 and 2.

	Logic Gates	GAL	FPGA
BCO-1			
λ_{max} (case 1, Table 1)	0.230	0.224	0.209
λ_{max} (case 3, Table 1)	0.227	0.221	0.194
λ_{max} (case 7, Table 1)	0.212	0.211	0.185
BCO-2			
λ_{max} (case 1, Table 2)	0.164	0.160	0.157
λ_{max} (case 5, Table 2)	0.152	0.150	0.148

It is worth to noting that, although the intrinsic time-delays of the logic XOR and XNOR gates change among the physical realizations, Case-1 for both BCOs continues generating chaotic behavior. In agreement with Lemma 4, the fact that there is Boolean chaos, for various implementations without extra time-delays in the feedback links, demonstrates that the proposed BCOs are not overly sensitive to heterogeneous intrinsic time-delays.

5. An Application Specific Integrated Circuit for the Proposed Boolean Chaos Oscillators

5.1. Chip Design

This section describes the integrated circuit-based implementation of the prospected BCOs in this work. The Boolean chaos generators are described with Verilog, a Hardware Description Language (HDL), using the UMC 180 nm Generic Core Cell Library. The BCO-1 hardware description in Figure 7a uses one XNOR3S and two XOR3S cells from the Generic Core library. That verilogHDL code synthesizes the three logic gates, whereas the Encounter tool (from Cadence Design Systems) executes a generic routing algorithm. Similarly, the BCO-2 of Figure 7b uses one XOR3S and one XNOR3S for the description with the verilogHDL code. The integrated circuit was part of a multiprocess wafer run and is shown in Figure 8 (Left). The size of BCO-1 is $75 \mu\text{m} \times 60 \mu\text{m}$ while the BCO-2 has physical dimensions of $32 \mu\text{m} \times 26 \mu\text{m}$. The area for biasing rails is considered in both scenarios. In any case, it is possible to reduce the size with routing optimization.

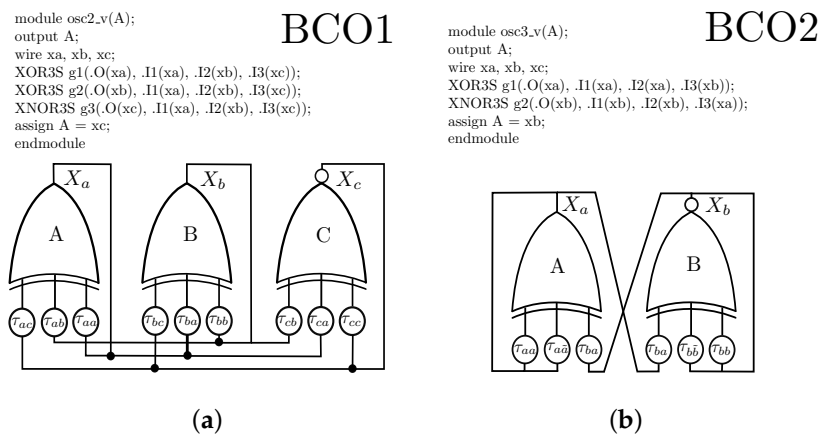


Figure 7. (a) Synthesis codes in VerilogHDL for (a) BCO-1, and (b) BCO-2, respectively.

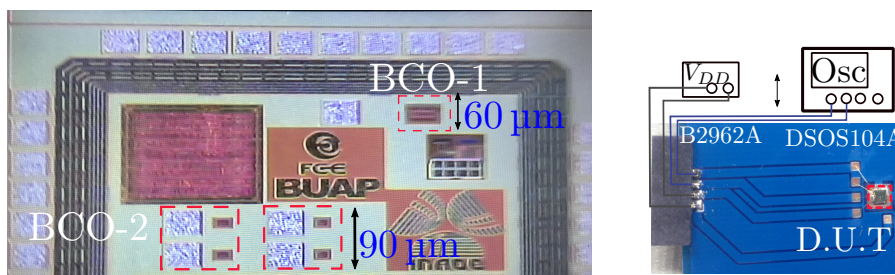


Figure 8. Microphotography of the chip and the test-bench for the integrated circuit.

It is worth noting that the design process of the IC is straightforward, and it does not depend on critical design considerations. However, all the design processes were executed in a semiautomated way using the generic cells and routing tool from Cadence software and UMC 180 nm fabrication technology. Therefore, this demonstrates, once again, the flexibility and robustness of the proposed BCOs.

On the other hand, Figure 8 (Right) shows the test-bench for the integrated circuit. The chip-die is mounted on an FR4 printed circuit board. It is biased with a low-noise $V_{DD} = 1.8 \text{ V}$ voltage source model B2962A while the oscilloscope DSOS104A captures the voltage time-series for further analysis.

5.2. Experimental Results of the Integrated BCO-1 and BCO-2

Now, we present the continuous-time behavior of both BCO-1 and BCO-2 on the integrated circuit. Figure 9 shows the real-time obtained waveforms and the respective dynamical analysis considering:

(i) time-series of the output voltage; (ii) frequency spectra; (iii) time-lag reconstructions of the attractors; (iv) Poincaré mapping set; (v) and largest Lyapunov exponent.

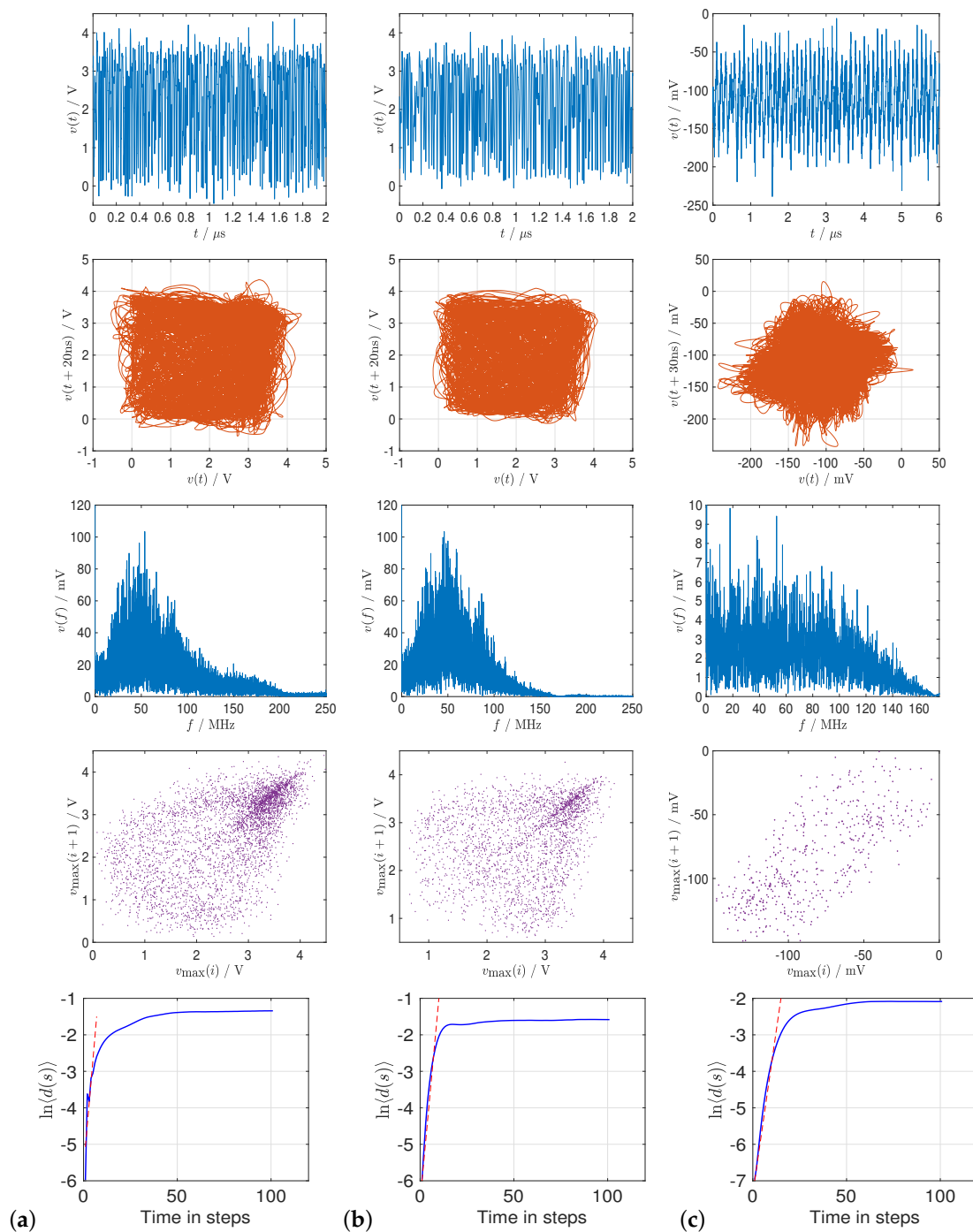


Figure 9. Chaotic dynamics measured experimentally from the integrated circuit of 180 nm at distinct settings for both Boolean chaos oscillators. Top to bottom: Time-series, time-lag embedded attractor, frequency spectrum, Poincaré map, the divergence $\ln\langle d(s) \rangle$ to determine the largest Lyapunov exponent λ_{\max} of the attractor. (a) Experimental results for BCO-1 @ $V_{DD} = 3.3$ V with $\lambda_{\max} = 0.4496$; (b) Experimental results for BCO-1 @ $V_{DD} = 2.8$ V with $\lambda_{\max} = 0.4243$; (c) Experimental results for BCO-2 @ $V_{DD} = 3.3$ V with $\lambda_{\max} = 0.2492$.

Figure 9a presents the BCO-1 features for $V_{DD} = 3.3$ V. The time-series shows a random evolution since it has variable cycle amplitudes regarding maxima and minima, and the frequency content is characterized for a predominant broad distribution and with strong content up to 200 MHz, therefore suggesting chaotic oscillations. Besides, the time-lag embedded attractor (lag equal to the first minimum of the time-lag mutual information function) exhibits a chaotic behavior in phase space, whose underlying complexity can be more properly appreciated on the corresponding Poincaré map for amplitudes of successive local maxima. In this manner, the arbitrarily chosen plane sections the attractor in two and thereby enables the visualization of its complex geometry. We found that the Poincaré map has a dense set of points, which has been identified as characteristic dynamics of the chaotic behavior. To quantify these observations, we determine the largest Lyapunov exponent (λ_{max}) of the attractor. The result shows the time evolution of the $\ln\langle d(s) \rangle$. This divergence presents an almost constant slope for the first part of the curve and then it saturates at a maximum value, corresponding to the uncorrelated signals $x(s + T + t_a)$ and $x(s + T + t_b)$. Next, we estimate the value of λ_{max} , assuming that the divergence of the initially similar segments is exponential in the region of constant slope. As a result, the average of all pairs of similar segments is our estimate of the largest Lyapunov exponent for the BCO-1, giving $\lambda_{max} = 0.4496$, which demonstrates that the CMOS Boolean oscillator integrated at 180 nm is chaotic.

Figure 9b shows the dynamical analysis for the same BCO-1 but now with $V_{DD} = 2.8$ V. This BCO-1 displays a clear chaotic attractor in the 0–4 V range and is validated with the Poincaré set. The results for time-series, frequency spectrum up to 150 MHz, Poincaré map, and $\lambda_{max} = 0.4243$ have a similar response to the previous case. Therefore, we can conclude the BCO-1 is robust against bias voltage variations.

The same test is included for the BCO-2 biased to $V_{DD} = 3.3$ V. The circuit presents a chaotic oscillation but the on-chip pad originates an explicit limitation of the voltage swing. This prototype uses internal pad connections and the reduced swing is a consequence of the extended bonding and absence of I/O cells. Therefore, the on-die probes represent an important load impedance and limit output swing to 200 mV. Figure 9c shows the time evolution, spectral content up to 160 MHz, chaotic attractor, and Poincaré map showing the expected results. Finally, Figure 9c also shows the largest Lyapunov exponent, which has a slope less abrupt but still presents a positive exponent ($\lambda_{max} = 0.2492$) in spite of the small values of the continuous-time sequence.

5.3. Comparison with Similar Implementations

For the sake of reference, Table 4 highlights the principal features of the recent True Random Number Generator (TRNG), systems based on chaotic circuits. The two new boolean chaotic oscillators exhibit competitive numbers compared to the references [20,42]. The comparison includes the most recent works with attempts to fully integrate the system-on-chip. The work in [20] presents a set of inverted-based chaotic oscillators. The area and power consumption are affordable, but the system uses additional off-chip biasing circuits. The chaotic circuit in [42] is fully integrated with the disadvantage of increasing the circuit resources. This is the result of the multiattractor analog system requiring a large bandwidth but the band limitation or frequency centroid is not reported. The two new boolean chaotic oscillators in this work present a reduced circuit size and power dissipation, not considering the chip input-output cells. The proposed boolean chaotic circuits present the most extended frequency span content compared to the recent on-chip implementations.

Table 4. Comparison of the principal features of recent TRNG based on chaotic systems.

	This Work BCO-1	This Work BCO-2	[20]	[42]
Chaos source	Boolean chaos	Boolean chaos	Chaotic oscillation	Multiattractor
Integrated Technology	Fully	Fully	Partially	Fully
Size (μm) ²	180 nm	180 nm	180 nm	180 nm
Static power (μW)	4500	832	28,000	(315,000 \times 383,000)
Speed limit (MHz)	0.2	0.09	25	3660
	200	160	10	NA

6. Conclusions

Two autonomous Boolean networks that generate Boolean chaos have been introduced. From the mathematical model, it was shown that the logical states would never reach a fixed-point, and therefore, will oscillate permanently. The proposed Boolean chaos oscillators exhibited no dependence on incommensurate time-delays, as demonstrated by computing the Lyapunov exponents under various scenarios for the delay paths. The correct physical implementations of the two Boolean chaos oscillators are good evidence of the predicted conditions. Therefore, the BCOs are reliable and robust to be implemented with multiple circuit implementations, both discrete as integrated.

In particular, the synthesis of the chaotic oscillators in an integrated circuit has shown the benefits of a compact CMOS chaos generator with areas 0.0045 mm^2 and 0.000832 mm^2 for BCO-1 and BCO-2, respectively, as well as high-speed chaotic oscillations with relevant amplitude content up to 200 MHz. Several dynamical analyses such as time-series, chaotic attractors, Poincaré maps, and Lyapunov exponents validated the experimental results.

In this manner, the proposed Boolean chaos oscillators could be useful for various engineering applications, for instance, random number generators, since the design is straightforward, robust, compact, and can be implemented in many options of hardware without needing special considerations.

Author Contributions: Conceptualization, J.M.M.-P. and T.G.-C.; methodology, J.M.M.-P. and V.R.G.-D.; software, J.M.M.-P., V.R.G.-D., G.d.L.F.-C.; validation, V.R.G.-D., T.G.-C. and G.d.L.F.-C.; formal analysis, J.M.M.-P.; investigation, J.M.M.-P., T.G.-C., and L.d.C.G.-P.; writing—original draft preparation, J.M.M.-P. and T.G.-C.; writing—review and editing, J.M.M.-P., V.R.G.-D., L.d.C.G.-P. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: J.M. Munoz-Pacheco acknowledges the National Council of Science and Technology (CONACYT) MEXICO for the financial support through Project No. 258880 (Proyecto Apoyado por el Fondo Sectorial de Investigación para la Educación). The Authors also thank CONACYT for the Lab project INFRA-2013-1-205873. The authors thankfully acknowledge computer resources, technical advice, and support provided by Laboratorio Nacional de Supercómputo del Sureste de México(LNS), a member of the CONACYT national laboratories, with project No. 202001025C.

Conflicts of Interest: The authors declare no conflict of interest.

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