

Article

28 GHz Single-Chip Transmit RF Front-End MMIC for Multichannel 5G Wireless Communications

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Abstract: Millimeter-wave wireless networks of the new fifth generation (5G) have become a primary focus in the development of the information and telecommunication industries. It is expected that 5G wireless networks will increase the data rates and reduce network latencies by an order of magnitude, which will create new telecommunication services for all sectors of the economy. New electronic components such as 28 GHz (27.5 to 28.35 GHz) single-chip transmit radio frequency (RF) front-end monolithic microwave integrated circuits (MMICs) will be required for the performance and power consumption of millimeter-wave (mm-wave) 5G communication systems. This component includes a 6-bit digital phase shifter, a driver amplifier and a power amplifier. The output power P_{3dB} and power-added efficiency (PAE) are 29 dBm and 19.2% at 28 GHz. The phase shifter root-mean-square (RMS) phase and gain errors are 3° and 0.6 dB at 28 GHz. The chip dimensions are 4.35 × 4.40 mm.

Keywords: 5G communications; massive MIMO; transceivers; RF front-end; single-chip; mm-wave; MMIC; GaAs; phase shifter; power amplifier

1. Introduction

The population of our planet is gradually increasing and has already exceeded 7 billion people. The information needs of the population are growing; at the same time, new technologies such as the Internet of Things (IoT), intelligent transport systems (such as Vehicular Ad hoc Network (VANETs)) and virtual and augmented reality are actively developing [1]. The growth of data traffic and device connections will require data rates to increase by more than an order of magnitude [2]. Responding to these requests, the International Telecommunication Union (ITU) decided to develop a new generation of 5G wireless communications with high transmission speeds (>10 Gbit/s) and ultralow response times (<1 ms). However, an increase in the transmission data rate is mainly possible due to the expansion of the band that the frequencies use. The requirements for 5G networks can only be implemented in the millimeter-wave frequency range [3].

The advantages of millimeter waves (mm-waves) when used for radio communications have been well known for many years [4]. The advantageous features of millimeter-wave radio waves are responsible for their widespread use in radar systems, remote sensing, navigation and communications. Interest in millimeter waves has increased due to the need to expand the radio frequency spectrum for commercial applications. Compared with previous generations, mm-wave 5G wireless communication systems have higher data rates and data transfer density, millisecond latency and enhanced spectral energy. The International Telecommunication Union (ITU) has specified a number of the mm-wave

frequency bands for 5G [5] wireless networks, but the 27.5–28.35 GHz band was proposed for wide usage in many countries and was licensed by the Federal Communications Commission (FCC) [6].

Power consumption is one of the most significant technical barriers for practical mm-wave 5G wireless communications because multiple devices connected at the same time increase the power consumption of the base stations and data centers. Photonic technologies can be utilized in order to solve this problem. In data centers, chip-to-chip optical or electro-optical interconnects enable an increase in the bandwidth and capacity of those systems as well as a reduction in power consumption [7,8].

In a conventional 4G communication system, one or more passive antennas are used. Wireless 5G networks are based on active massive-element antenna systems that improve the capacity, efficiency and coverage of RF streams [9] (Figure 1).

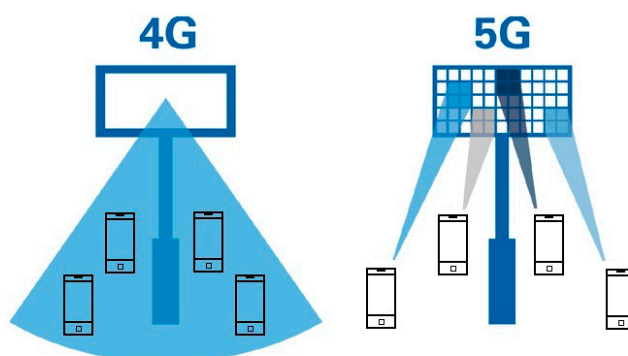


Figure 1. Conventional 4G and 5G antenna systems.

To improve the bandwidth and data rate, the multiple-input multiple-output (MIMO) transceivers based on phased beamforming arrays are used [10–13]. Usually, active antenna systems consist of massive antenna arrays with integrated MIMO transceiver RF front-ends.

Figure 2 shows the design of a multichannel transmit RF front-end (RFFE) module for 5G MIMO transceivers. There is a symmetrical antenna array where each channel consists of a phase shifter, a driver amplifier and a power amplifier. The input splitter divides the RF signal into a number of channels. The symmetry of the RFFE module architecture allows for a balance between input and output losses and power consumption.

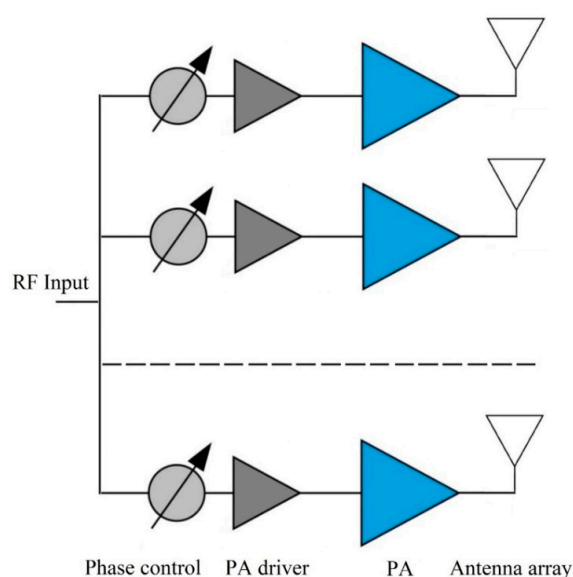


Figure 2. Design of the multichannel symmetry transmit RF front-end.

The performance and power consumption of millimeter-wave 5G communication systems are mainly dependent on the electrical parameters of using RF electronic components based on semiconductor monolithic integrated circuits, which are the key elements for mm-wave RF transmit/receive modules. The development of such elements is a difficult challenge.

A previous study presented the results of the development of a 28 GHz phase adjustable power amplifier monolithic microwave integrated circuit (MMIC) for 5G front-ends [14]. It consisted of a 4-bit digitally controlled phase shifter and power amplifier. The MMIC was designed by Plextek RFI and fabricated by Win Semiconductors using a 0.15 μm GaAs pHEMT process. The main disadvantage of this MMIC is a low phase shift resolution of 22.5° , which results in reduced beamforming opportunities and low antenna gain.

In this study, the design approach for a 28 GHz single-chip transmit RFFE MMIC with high phase shift resolution (5.625°) for multichannel 5G wireless communications is presented, along with its electrical performance. The integrated circuit (IC) consists of a 6-bit digital phase shifter, a driver amplifier and a power amplifier and was designed using a 0.25 μm GaAs pHEMT process of JSC Micran (Tomsk, Russian Federation) for low-cost volume production.

2. Single-Chip RF Front-End MMIC

2.1. Design Approach

Figure 3 shows a photo of a fabricated one-channel single-chip transmit RF front-end MMIC. The chip dimensions are 4.35 mm \times 4.40 mm. The single-chip IC consists of a 6-bit phase shifter with a transistor-transistor logic (TTL) driver, a driver amplifier and a power amplifier (PA) and was designed using a 0.25 μm GaAs pHEMT process for low-cost volume production.

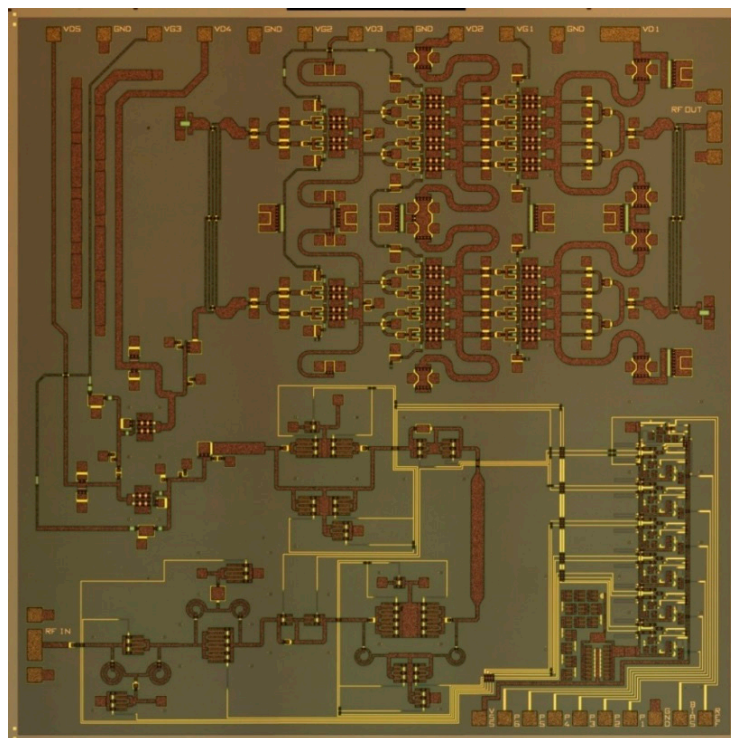


Figure 3. Photo of one-channel single-chip transmit RF front-end (RFFE) monolithic microwave integrated circuit (MMIC).

The phase shift level of a single-chip transmit RFFE MMIC is controlled by an integrated TTL driver. The 6-bit digital driver can precisely adjust a phase from 0 to 360° with a step of 5.625° . Table A1 in Appendix A shows the phase shifter state table. There are two control levels (0 and 1) for all bits.

Low (0) and high (1) TTL control levels are 0 and +5 V. Applying different control levels for all 6 bits of the digital phase shifter may change the phase shift across the full 360° range.

The high- and low-pass (HP-LP) RF filters were used to design the 6-bit digital phase shifter [15]. The applied TTL control voltages across all bits allowed the switching of states between HP-LP filters to form the required output phase shift level. This solution exhibits good return losses, phase shift performance in RMS phase and gain errors.

The electrical schemes and layout plots of 180° , 90° , 45° , 22.5° , 11.25° and 5.625° bits are presented in Figures 4–9. For 180° and 90° bits, a circuit was selected with switchable filters using an inactive arm in the filter. The classical solution of using switchable filters does not provide a sufficient level of decoupling of the active and inactive arms, which leads to an increase in the initial bit losses. The 45° and 22.5° bits were designed according to the scheme with switched elements in the filter. This is the only possible solution for the 27.5–28.35 GHz band. For 11.5° and 5.625° bits, a circuit was designed with a serial connection of filters due to a very small inductance. In this circuit, the inductance is shunted because the required phase shift requires a large length of the microstrip.

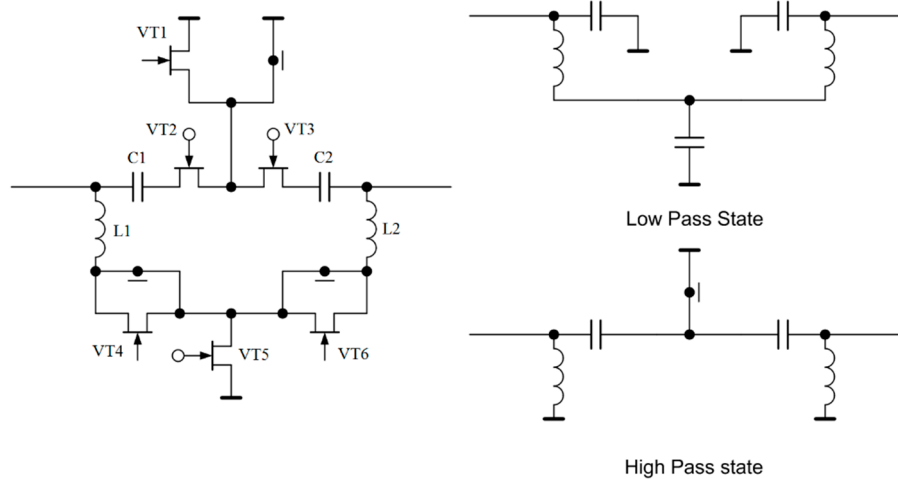


Figure 4. Electrical scheme of the 180° and 90° bits of the phase shifter.

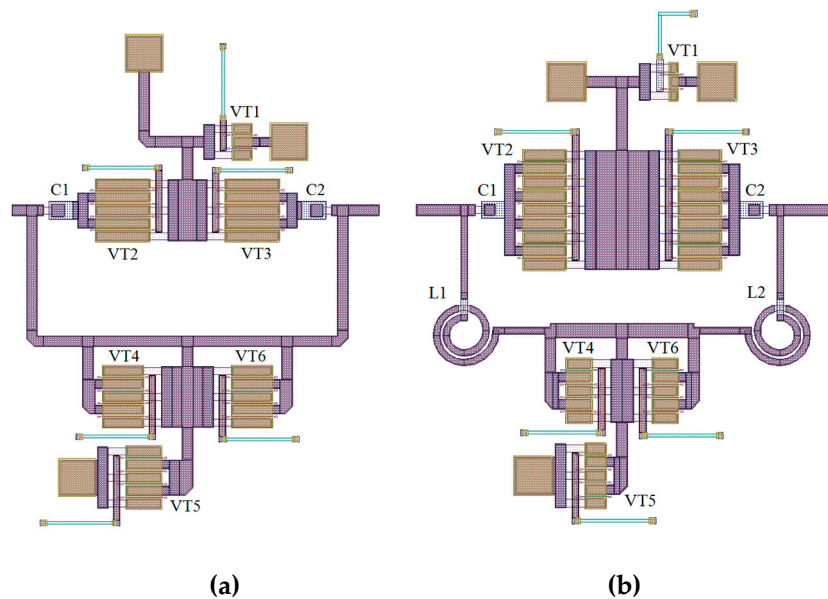


Figure 5. Layout plot of the 180° (a) and 90° (b) bits of the phase shifter.

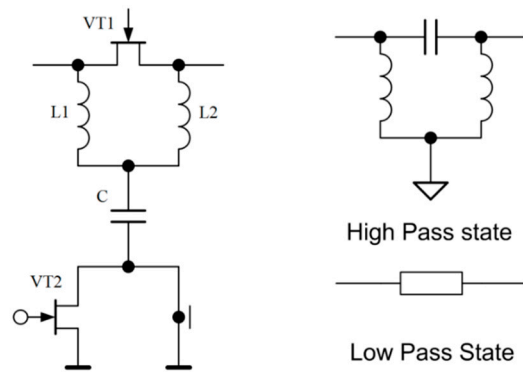


Figure 6. Electrical scheme of the 45 and 22.5° bits of the phase shifter.

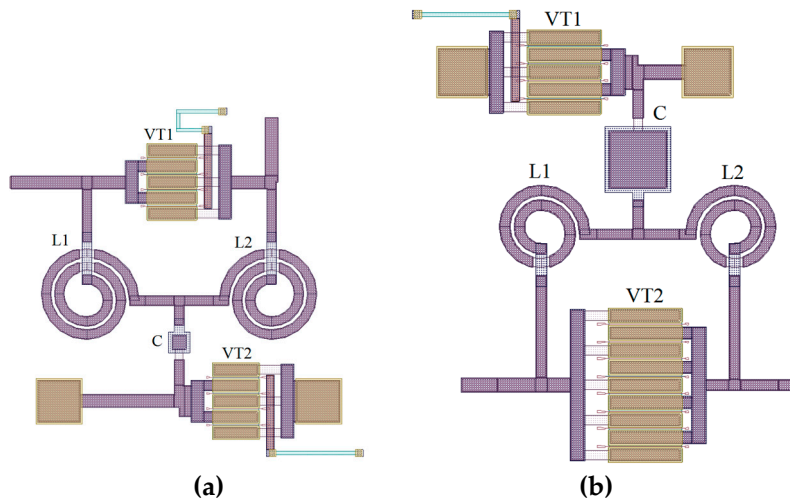


Figure 7. Layout plot of the 45 (a) and 22.5° (b) bits of the phase shifter.

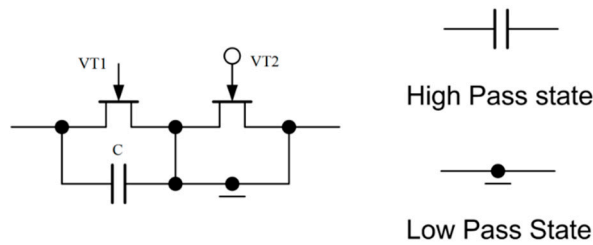


Figure 8. Electrical scheme of the 11.25 and 5.625° bits of the phase shifter.

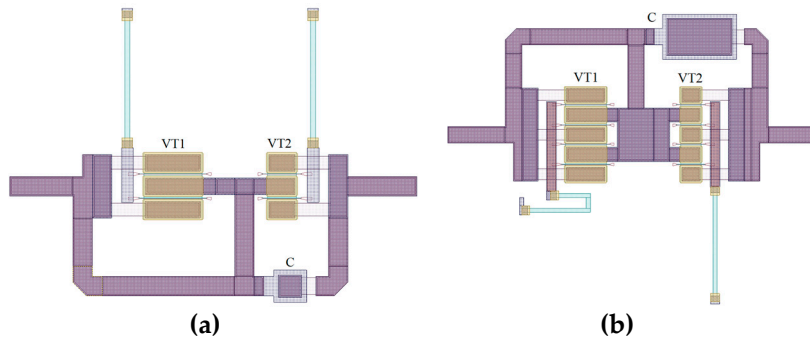


Figure 9. Layout plot of the 11.25 (a) and 5.625° (b) bits of the phase shifter.

The choice in the order of the phase shifter bits was carried out strictly on the principle of minimal influence of the reflection coefficient between the bits. To do this, the sections with the lowest similarity of the reflection coefficient are placed between the sections with the highest similarity of the reflection

coefficient. The most stable bits are 180 and 90° , and the least stable bits are 11.25 and 5.625° . Therefore, the optimal bit ordering is selected as follows: 22.5 to 11.25 to 90 to 5.625 to 180 to 45° . This ordering allows the RMS phase shift error to be reduced.

The power amplifier (PA) of a single-chip transmit front-end MMIC consists of three power stages and matching networks (Figure 10a). The base active element of the PA is a GaAs pHEMT with a $0.25 \mu\text{m}$ length gate. To achieve a balance between output power capability and cutoff frequency, the transistor gate width is $100 \mu\text{m}$ (Figure 11). The increase in gate width can improve the output power of the transistor, but higher parasitic capacitance will reduce the cutoff frequency. The peripheries of the transistors are $1600 \mu\text{m}$ ($16 \times 100 \mu\text{m}$) for the first stage (Q1), $3200 \mu\text{m}$ ($32 \times 100 \mu\text{m}$) for the second stage (Q2) and $3200 \mu\text{m}$ ($32 \times 100 \mu\text{m}$) for the third stage (Q3). The supply voltage for all power stages is $V_d = 6 \text{ V}$.

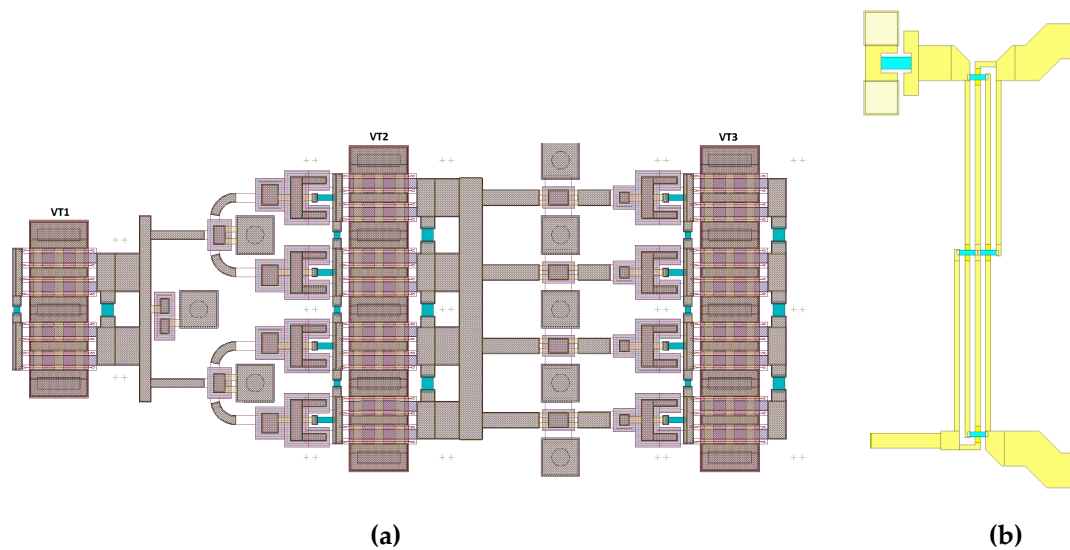


Figure 10. Layout plot of the three stages of the power amplifier (a) and the Lange quadrature coupler (b).

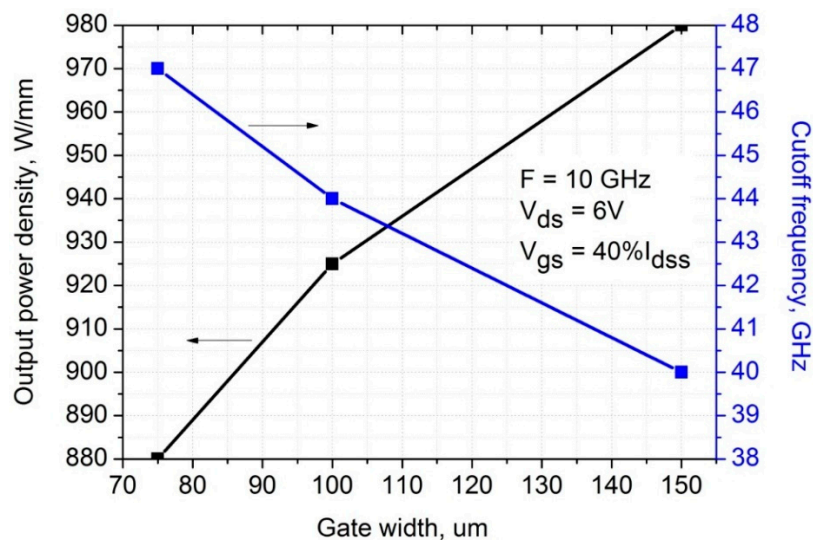


Figure 11. Dependences of output power density and cutoff frequency on the gate width of the $0.25 \mu\text{m}$ GaAs pHEMT.

The matching networks of the power amplifier consist of thin-film NiCr-based resistors, metal-insulator-metal (MIM) capacitors based on silicon nitride, Au-based transmission lines and Lange quadrature couplers (LQCs). The proposed LQCs (Figure 10b) are used in input and output

matching networks to improve the bandwidth and achieve a compact PA size. The symmetrical design of the PA layout and electromagnetic simulation were completed at the AWR Microwave Office [16].

2.2. Electrical Performance

Figure 12 shows the dependences of the simulated phase shift performance on the frequency for 64 states of a one-chip RF front-end MMIC.

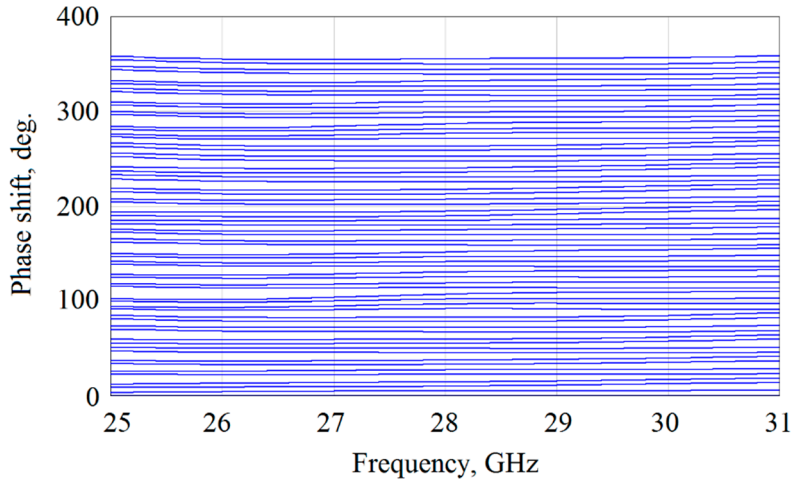


Figure 12. Phase shift versus frequency of the single-chip RF front-end MMIC.

Figure 13 shows the dependence of the RMS phase shift error (PSE) of the single-chip RF front-end MMIC on frequency in the range of 26 to 30 GHz. The measured RMS PSE was calculated according to Equation (1):

$$\sigma_{\varphi} = \sqrt{\frac{(\varepsilon_{\varphi 1} - \langle \varepsilon_{\varphi} \rangle)^2 + (\varepsilon_{\varphi 2} - \langle \varepsilon_{\varphi} \rangle)^2 + \dots + (\varepsilon_{\varphi(N-1)} - \langle \varepsilon_{\varphi} \rangle)^2}{N}} = \sqrt{\frac{\sum_{i=1}^{N-1} (\varepsilon_{\varphi i} - \langle \varepsilon_{\varphi} \rangle)^2}{N}} \quad (1)$$

where N is the number of phase states number, ε_{φ} is the measured phase shift in degrees and $\langle \varepsilon_{\varphi} \rangle$ is the average phase shift for states of the 6-bit phase shifter.

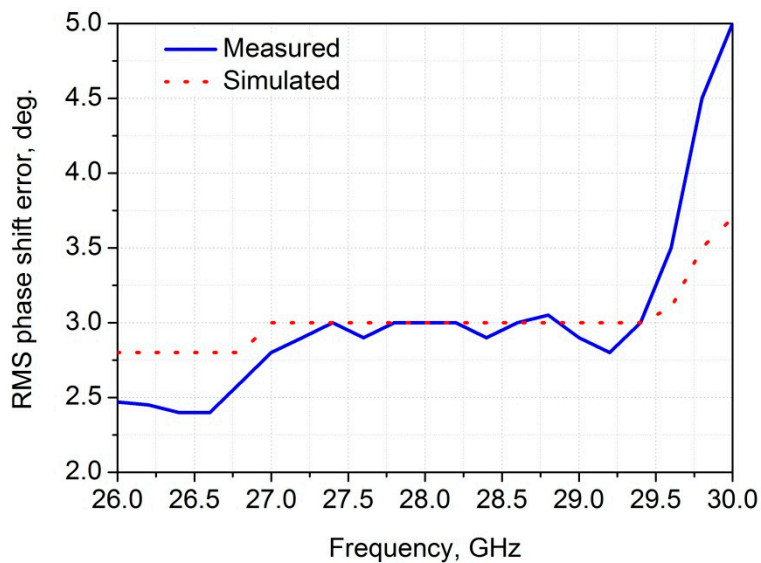


Figure 13. Dependence of RMS phase shift error of the single-chip RF front-end MMIC on the frequency.

According to the results presented in Figure 13, RMS phase shift error is about 3° across the entire 27.5–28.35 GHz range.

Figure 14 shows the dependence of small signal gain in all phase states of the single-chip RF front-end MMIC on frequency in the 26 to 30 GHz frequency range. There is a nominal small signal gain of over 20 dB in the frequency range of 27.5 to 28.35 GHz. The maximum gain of 22.7 dB is achieved at 29 GHz.

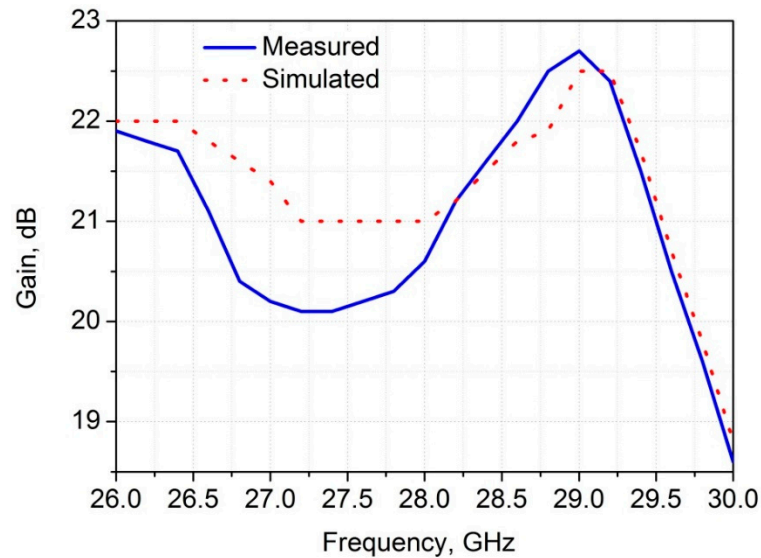


Figure 14. Dependence of gain of the single-chip RF front-end MMIC on the frequency.

Figure 15 shows the dependence of RMS gain error (GE) of the single-chip RF front-end MMIC on frequency in the 26 to 30 GHz frequency range. The measured RMS (GE) was calculated according to Equation (2):

$$\sigma_{|S_{21}|} = \sqrt{\frac{\sum_{i=0}^{N-1} (|S_{21}|_i - \langle |S_{21}| \rangle)^2}{N}} \quad (2)$$

where N is the number of phase states, $|S_{21}|$ is the measured gain in dB and $\langle |S_{21}| \rangle$ is the average gain for states of the 6-bit phase shifter.

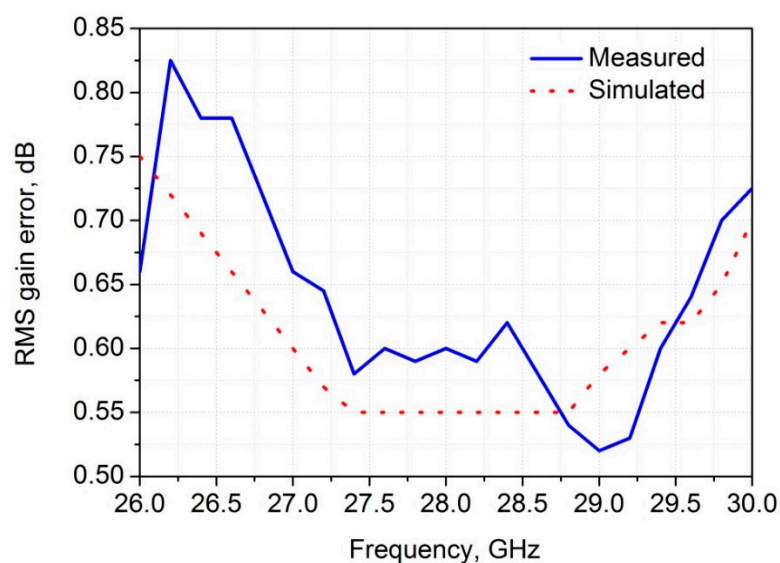


Figure 15. Dependence of RMS gain error of the single-chip RF front-end MMIC on the frequency.

According to the results presented in Figure 15, RMS GE is 0.6 dB for the entire 27.5–28.35 GHz range.

Figure 16 shows the dependence of the output power capability at 3 dB gain compression (P_{3dB}) for the 0° phase state of the single-chip RF front-end MMIC on frequency. The output power P_{3dB} is 29 dBm across the full 27.5 to 28.35 GHz band. The maximum P_{3dB} of about 29.5 dBm is achieved at 30 GHz.

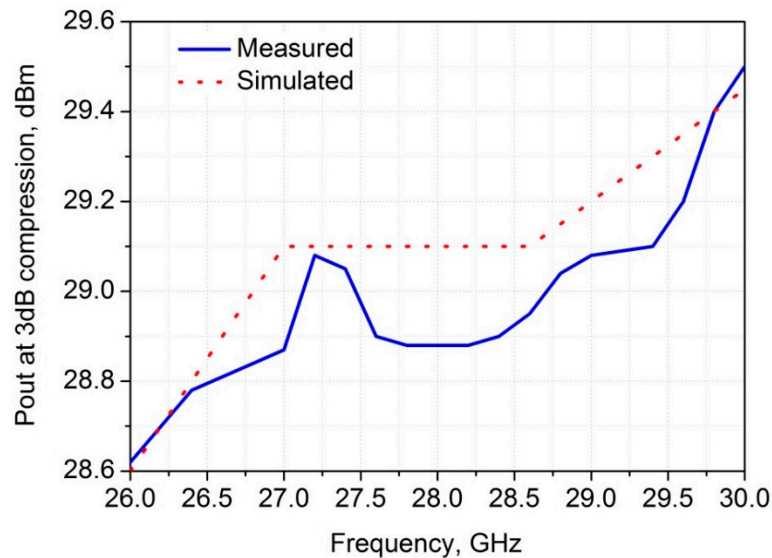


Figure 16. Dependence of output power (P_{3dB}) at the 0° phase state of the single-chip RF front-end MMIC on the frequency.

Figure 17 shows the power-added efficiency (PAE) at 1 dB gain compression for the 0° phase state of the single-chip RF front-end MMIC frequency. A maximum PAE of 19.3% is achieved in the 27.5 to 28.35 GHz frequency range. Further optimization of the input and output matching networks in power amplifier stages can improve the PAE and the output power capability.

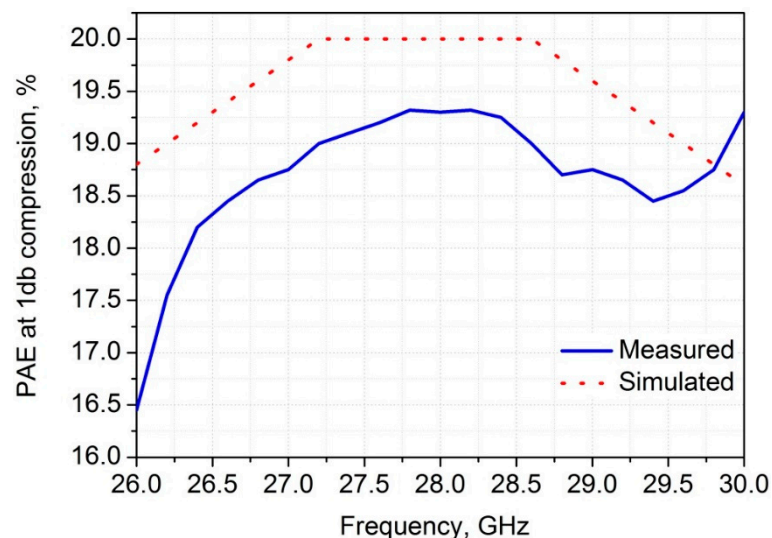


Figure 17. Dependence of PAE at 1 dB gain compression at the 0° phase state of the single-chip RF front-end MMIC on the frequency.

Table 1 shows the electrical performance of the developed single-chip transmit RFFE MMIC in comparison with state-of-the-art single-chip transmit RFFE MMICs [14]. The fabricated MMIC has a comparable performance and a higher phase shift resolution. The improved output power and PAE of the RF front-end presented in [14] can be attributed to the use of the $0.15 \mu\text{m}$ GaAs pHEMT process of Win Semiconductors, with lower gate length resulting in better high-frequency performance.

Table 1. State-of-the-art single-chip transmit RFFE MMICs.

Parameter	This Work		Ref. [14]		Units
	Min	Max	Min	Max	
Frequency	27.5	28.35	27.5	28.35	GHz
RMS Phase Error		3		2.38	deg.
RMS Gain Error		0.63		0.23	dB
Gain	20.0	21.3	20.5	21.5	dB
P1dB at 0°	-	-	29.8	30.2	dBm
P3dB at 0°	28.7	29.0	-	-	dBm
PAE at P1dB at 0°	19.2	19.3	23	24.2	%

3. Conclusions

Millimeter-wave wireless networks have attracted the most interest as 5G communication systems of the new generation (5G). The 27.5 to 28.35 GHz band was licensed for 5G wireless networks by the FCC. The performance and power consumption of millimeter-wave 5G communication systems mainly depend on the electrical parameters of the electronic RF components used inside RF transmit/receive modules.

The design approach for a 28 GHz single-chip transmit RF front-end MMIC is presented in this paper, along with its electrical performance. The IC includes a 6-bit digital phase shifter, a driver amplifier and a power amplifier. It was designed using a 0.25 μm GaAs pHEMT process for low-cost volume production. The output power P3dB and PAE are 29 dBm and 19.2% at 28 GHz. The phase shifter RMS phase and gain errors are 3° and 0.6 dB at 28 GHz. The fabricated single-chip RF front-end MMIC can be used in multichannel transmit 5G front-end modules based on phased antenna arrays.

Author Contributions: Conceptualization, V.A.; methodology, V.A.; software, M.S.; validation, M.S.; formal analysis, A.V.; investigation, A.K. and V.K.; resources, M.S.; data curation, E.E.; writing—original draft preparation, E.E.; writing—review and editing, E.E.; visualization, A.K. and V.K.; supervision, E.E.; project administration, E.E.; funding acquisition, V.A. and E.E. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Table A1. Phase shifter state table («0» is low control level and «1» is high control level).

Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Relative Phase Shift, deg.
0	0	0	0	0	0	0.000
1	0	0	0	0	0	5.625
0	1	0	0	0	0	11.250
1	1	0	0	0	0	16.875
0	0	1	0	0	0	22.500
1	0	1	0	0	0	28.125
0	1	1	0	0	0	33.750
1	1	1	0	0	0	39.375
0	0	0	1	0	0	45.000
1	0	0	1	0	0	50.625
0	1	0	1	0	0	56.250
1	1	0	1	0	0	61.875
0	0	1	1	0	0	67.500
1	0	1	1	0	0	73.125
0	1	1	1	0	0	78.750
1	1	1	1	0	0	84.375
0	0	0	0	1	0	90.000
1	0	0	0	1	0	95.625
0	1	0	0	1	0	101.250
1	1	0	0	1	0	106.875
0	0	1	0	1	0	112.500
1	0	1	0	1	0	118.125
0	1	1	0	1	0	123.750
1	1	1	0	1	0	129.375
0	0	0	1	1	0	135.000
1	0	0	1	1	0	140.625
0	1	0	1	1	0	146.250
1	1	0	1	1	0	151.875
0	0	1	1	1	0	157.500
1	0	1	1	1	0	163.125
0	1	1	1	1	0	168.750
1	1	1	1	1	0	174.375
0	0	0	0	0	1	180.000
1	0	0	0	0	1	185.625
0	1	0	0	0	1	191.250
1	1	0	0	0	1	196.875

Table A1. Cont.

Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Relative Phase Shift, deg.
0	0	1	0	0	1	202.500
1	0	1	0	0	1	208.125
0	1	1	0	0	1	213.750
1	1	1	0	0	1	219.375
0	0	0	1	0	1	225.000
1	0	0	1	0	1	230.625
0	1	0	1	0	1	236.250
1	1	0	1	0	1	241.875
0	0	1	1	0	1	247.500
1	0	1	1	0	1	253.125
0	1	1	1	0	1	258.750
1	1	1	1	0	1	264.375
0	0	0	0	1	1	270.000
1	0	0	0	1	1	275.625
0	1	0	0	1	1	281.250
1	1	0	0	1	1	286.875
0	0	1	0	1	1	292.500
1	0	1	0	1	1	298.125
0	1	1	0	1	1	303.750
1	1	1	0	1	1	309.375
0	0	0	1	1	1	315.000
1	0	0	1	1	1	320.625
0	1	0	1	1	1	326.250
1	1	0	1	1	1	331.875
0	0	1	1	1	1	337.500
1	0	1	1	1	1	343.125
0	1	1	1	1	1	348.750
1	1	1	1	1	1	354.375

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