Article

Soft-Switching Full-Bridge Converter with Multiple-Input Sources for DC Distribution Applications

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Abstract: Due to the advantages of power supply systems using the DC distribution method, such as a conversion efficiency increase of about 5–10%, a cost reduction of about 15–20%, etc., AC power distribution systems will be replaced by DC power distribution systems in the future. This paper adopts different converters to generate DC distribution system: DC/DC converter with PV arrays, power factor correction with utility line and full-bridge converter with multiple input sources. With this approach, the proposed full-bridge converter with soft-switching features for generating a desired voltage level in order to transfer energy to the proposed DC distribution system. In addition, the proposed soft-switching full-bridge converter is used to generate the DC voltage and is applied to balance power between the PV arrays and the utility line. Due to soft-switching features, the proposed full-bridge converter can be operated with zero-voltage switching (ZVS) at the turn-on transition to increase conversion efficiency. Finally, a prototype of the proposed full-bridge converter under an input voltage of DC 48 V, an output voltage of 24 V, a maximum output current of 21 A and a maximum output power of 500 W was implemented to prove its feasibility. From experimental results, it can be found that its maximum conversion efficiency is 92% under 50% of full-load conditions. It was shown to be suitable for DC distribution applications.

Keywords: multiple input power sources; DC distribution system and full-bridge converter

1. Introduction

In general, power distribution systems are divided into AC distribution systems and DC distribution systems. In the past century, AC distribution systems have always been used for human environments. The overuse of fossil fuels has caused environmental pollution, leading to serious greenhouse effects. This has disturbed the balance of the global climate. In particular, effluent gas emissions and increases in CO_2 levels in the atmosphere have affected global surface temperatures, which have increased at a rate of 0.6 °C/century [1,2]. To save energy, a multiple energy source policy has been widely adopted in regard to power distribution systems. Compared to AC distribution systems, power systems using a DC distribution method have many advantages, such as a conversion efficiency increase of about 5–10%, a cost reduction of about 15–20% etc. Therefore, AC power distribution systems will be replaced by DC power distribution systems [3].The DC system is a popular distribution system. For the DC distribution system, a power processor with a high conversion efficiency is adopted to transfer power to load. In addition, to implement carbon reductions, zero-emissions renewable energy approaches have been rapidly applied to power processors, in applications such as power generation for grid connections, DC/DC converters, electric vehicle construction, battery charge/discharger development, satellite power systems, etc.

In renewable systems, the technologies of PV arrays and wind turbines, which are devices used to transfer renewable energy into electrical power, are important developments [4,5]. When renewable energy is used in cities, PV arrays have fewer limitations compared with those of wind turbines. Therefore, PV arrays are widely used to transfer

power to load. Due to the unstable generation of electrical power by PV arrays, power supplied by a utility line can be adopted to balance power between PV arrays and DC loads. This is shown in Figure 1. In Figure 1, it can be observed that the voltage V_s of the utility line varies from AC 90 V to 264 V. In order to generate a proper voltage level (about DC 48 V) to be supplied to a full-bridge converter, a high step-down converter is required, such as push-pull, full-bridge, half-bridge, forward, or fly-back converters [6–8]. Due to a simple circuit structure and low cost, a flyback converter can be chosen to generate the DC voltage from the utility line to the DC load, and is used to achieve power factor correction (PFC). Due to the flyback converter adopted in the proposed DC distribution system [9–11], a soft switching circuit is required to increase its conversion efficiency, as shown in Figure 2. In Figure 2, it can be seen that an active clamp circuit is introduced into the flyback converter to recover energy stored in the leakage inductor. When the energy stored in the leakage inductor is recovered, the conversion efficiency of the flyback converter can be increased. In addition, the current of the leakage inductor can eliminate the effect of the parasitic capacitor on switches, allowingswitches M_1–M_4 to be operated with zero-voltage switching (ZVS) at the turn-on transition.
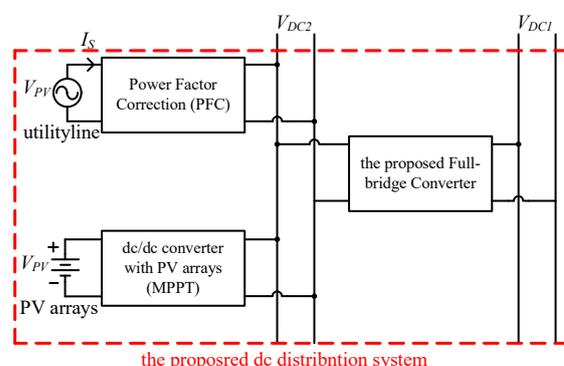

Figure 1. Block diagram of the proposed DC distribution system with multipleinput power sources.
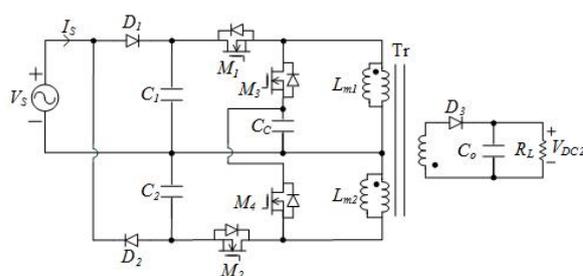

Figure 2. Schematic diagram of power factor correction (PFC) inthe proposed DC distribution system for generating power from the utility line.

When a DC/DC converter uses PV arrays as its input power source, it needs a step-up converter to generate a desired DC voltage level due to the lower voltage output of PV arrays, such as boost, buck-boost, Cuk, Zeta, or SEPIC converter. In order to generate the desired voltage, a boost converter can be adopted, as shown in Figure 3. When a boost converter is used in the proposed DC power system, an interleaving circuit structure is applied to the DC/DC converter in order to generate a higher output power to DC loads. In Figure 3, the active single-capacitor snubber can store energy in the capacitor to smooth out the switch voltage. As a result, switches M_1 and M_2 can be operated with zero-voltage transition (ZVT) features at the turn-on transition. In order to operate the maximum power point of the PV arrays, there are many methods to implement maximum power point tracking (MPPT) of PV arrays, such as power matching [12,13], curve-fitting [14,15], perturb-and-observe [16,17], and incremental conductance [18,19] methods. When MPPT is implemented using the power matching method, a specific insolation condition or load

is required, resulting in application limitations. If the curve-fitting technique is adopted to achieve MPPT, a prior establishment characteristic curve of PV arrays is required. It cannot predict the characteristics including other factors, such as aging, temperature, and the possible breakdown of individual cells. Since the incremental conductance technique requires an accurate mathematical operation, it leads to more complexity and higher costs. Due to the simpler control and lower cost of implementing the perturb-and-observe method for PV array applications, the DC power system proposed herein adopts the perturb-and-observe method to implement MPPT.
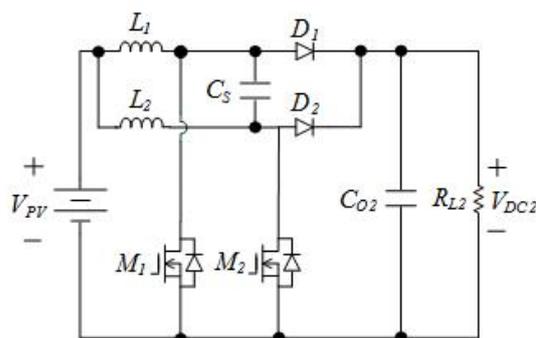

Figure 3. Schematic diagram of DC/DC converter with PV arrays of the proposed DC distribution system for generating power from PV arrays.

The proposed DC distribution system is applied to a DC load. In order to generate a specific output voltage (about DC 24 V) with safety considerations, a DC/DC converter with galvanic isolation is required. Since the output voltage V_{DC1} is less than the input voltage V_{DC2}, the power processor needs a step-down converter. As mentioned above, flyback, forward, half-bridge, full-bridge or push-pull converters can be used. Due to the lower power level processing capability of flyback and forward converters, half-bridge, full-bridge, or push-pull converters can be applied to the proposed DC distribution system. When the proposed power system using a half-bridge or push-pull converter generates the desired output voltage, it will result in an unbalanced operation of the transformer. To avoid the unbalanced operation of the transformer, a full-bridge converter is adopted in the proposed power system. In this paper, we will focus on the power management of the proposed DC distribution system and the design of the full-bridge converter. In addition, all the acronyms and abbreviations used herein are listed in Table 1.

Table 1. Acronyms and abbreviations.

Acronyms/Abbreviations	Parameter/Definition
ZVS	Zero-voltage switching
PFC	Power factor correction
ZCS	Zero-current switching
ZCT	Zero-current transition
ZVT	Zero-voltage transition
IC	Integrated circuit
PWM	Pulse-width modulation
PV	Photovoltaic
MPPT	Maximum power point tracking
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode

2. Related Work

As a full-bridge converter has been selected for the proposed DC power system, one needs a transformer to transfer power from the input source to the load, as shown in Figure 4. Due to the leakage inductance of the transformer, the energy stored in leakage inductance will induce a serious spike voltage across switches when switches are in the

off state. There are many methods to solve this problem. One of these methods, an asymmetrical pulse-width modulation technique, was introduced in [20]. Its gate signal is shown in Figure 5a. Although this has many advantages, such as ZVS features, no extra conduction loss, and fixed operational frequency, its chief drawback is that the maximum duty ratio is limited to 0.5 and the transfer ratio is lower under the same turns ratio of the transformer.
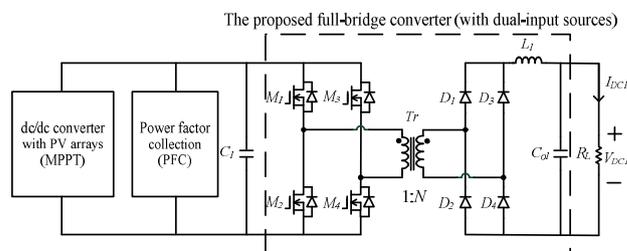

**Figure 4.** Schematic diagram of the proposed DC distribution system.

(a)

(b)

(c)
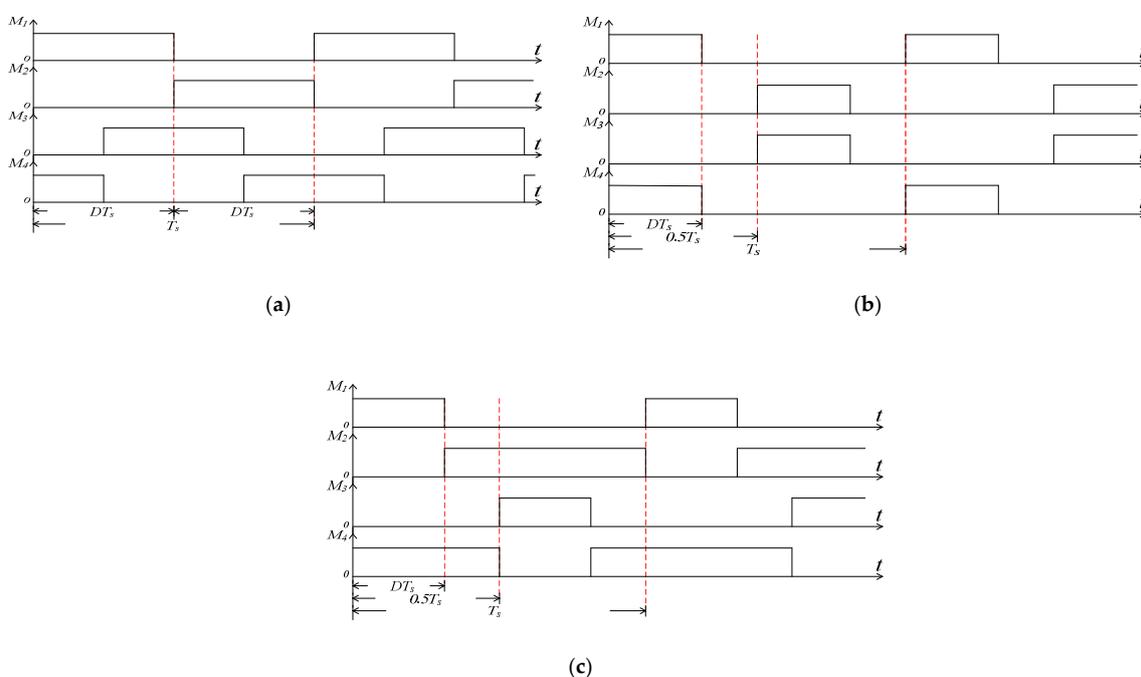
Figure 5. Conceptual gate signal waveforms of switches M_1–M_4 for full-bridge converter: (**a**) phase-shift control method, (**b**) the conventional PWM control method, and (**c**) the proposed PWM control method.

In order to reduce switching losses, the full-bridge converter can use a snubber to help switches to achieve soft-switching features. Its gate signal can be generated by a general PWM IC, as shown in Figure 5b. Snubbers can be divided into two types—active and passive snubbers. In passive snubbers [20–25], the full-bridge converter uses a capacitor, inductor, or diode to achieve soft-switching features, such as ZVS, zero-current switching (ZCS), zero-current transition (ZCT), and ZVT. In [20–24], the snubber circuit is placed in the primary winding side of the transformer. It is inserted into the primary and secondary winding sides of the transformer [25]. When a passive snubber is used, the cost and volume of the full-bridge converter are increased. Its design becomes more complex. Another approach has been proposed—to add active components onto the primary winding side or the secondary side of transformer. For the active snubber [26–28], when the active snubber is added into the full-bridge converter, it generates an extra current to discharge the output capacitances of the switches. As a result, the switches in the full-bridge converter can be operated with ZVS at the turn-on transition. In addition, the switches can be operated with

ZCS features, reducing switching losses. Although the active snubber can reduce switching losses, it will result in a higher cost, a more complex driving circuit, and a larger volume.

In general, the full-bridge converter adopts the phase-shift control method to achieve soft-switching features. With this approach, the duty ratio of the PWM control IC is limited to 0.5. In addition, the PWM control IC selection in the full-bridge converter is also restricted by the phase-shift algorithm control function, resulting in a lower transfer ratio under the same turns ratio of the transformer. Due to the advanced technology of semiconductor manufacturing, the conduction resistance of the switch is extremely low during switching under turn-on conditions. This can substantially reduce the conduction losses of switches. Therefore, when the switches of the full-bridge converter are operated with ZVS features to induce a circulating current, flowing through the primary winding of the transformer, the effect of conduction losses on the circulating current will be reduced significantly. In this paper, the switches of the proposed full-bridge converter are divided into two legs—left leg and right leg switches, as shown in Figure 4. The left leg switches include switches M_1 and M_2, where as the right leg ones include switches M_3 and M_4. In order to achieve ZVS features, switches M_1 and M_2 are operated in a complementary fashion. The operation of switches M_3 and M_4 is the same as that of switches M_1 and M_2. In addition, switches M_1 and M_3 are operated at $180°$ out of phase. The gate signal is shown in Figure 5c. Using this approach, switches M_1—M_4 can be operated in ZVS at the turn-on transition to increase the conversion efficiency. The duty ratios of the switches can be varied to achieve various transfer ratios for the proposed system. The proposed system only adds two inverters in the control circuit to implement soft-switching features. Although the proposed system will induce a circulating current to increase the conduction losses of the switches, this will be significantly reduced due to the extremely low conduction resistance of the switches. As mentioned above, the proposed full-bridge converter adopts the gate signal control method to achieve ZVS features and to increase conversion efficiency.

3. Topology and Operational Method of the Proposed DC Distribution Power

The proposed DC distribution power includes three converters: DC/DC converter with PV arrays, power factor correction (PFC) with utility line and the proposed full-bridge converter with multi-input sources. The power management of the proposed DC distribution power and soft-switching features of the proposed full-bridge converter are focus in this paper. In order to implement power management and soft-switching features, topology of the proposed DC distribution one and operational method of the proposed full-bridge converter are described as follows.

*3.1. Topology of the Proposed DC Distribution System*

The proposed DC distribution system is used in a multi-input power source system. The input power sources include a utility line and PV arrays. Therefore, the utility line and PV arrays can separately adopt the converter to transfer power into a desired voltage level. When the desired voltage level is generated, the proposed full-bridge converter uses the desired voltage level to supply power for the DC loads. Therefore, the proposed DC distribution system consists of power factor correction (PFC) with the utility line as the input source, a DC/DC converter with PV arrays as the input source and the full-bridge converter with multi-input sources to generate the DC voltage supplied to DC loads, as shown in Figure 4.

When the proposed DC distribution system is in the working state, it requires a proper control method to supply power for DC loads. Since this paper focuses on the design and implementation of the proposed full-bridge converter, power management among converters in the proposed DC distribution system is adopted to implement the control method for the proposed system. In addition, the measured results of the proposed full-bridge converter include switch waveforms, dynamic load variation, and conversion efficiency, which are used to verify the feasibility of the proposed full-bridge converter. This will be shown in the Measured Results and Discussion sections.

3.2. Operational Method of the Proposed Full-Bridge Converter

In general, when the load is greater than 20–30% of the full-load condition, the full-bridge converter is designed to operate in continuous conduction mode (CCM). This paper only describes the operational method for CCM in the proposed full-bridge converter. To achieve a higher conversion efficiency, the operator of the proposed full-bridge converter must adopt a different operational method to control the switches in the proposed system. According to the operational method of the proposed converter, its operational modes are divided into 14 modes, as shown in Figure 6, and their key waveforms are illustrated in Figure 7. Since the operational modes between t_0–t_7 are similar to those modes between t_7–t_{14}, except that the operational main switch changes from M_1 to M_3, each operational mode during half of one switching cycle is briefly described as follows.
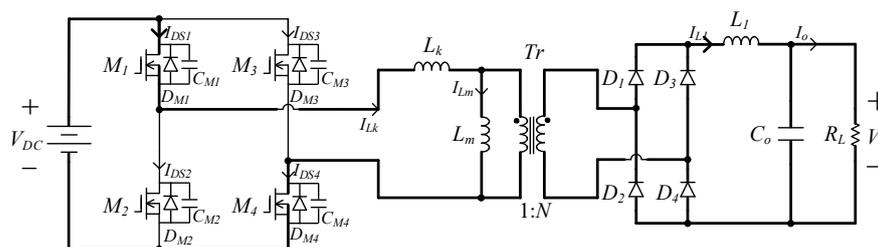
(**a**) Mode 0 (before t_0).
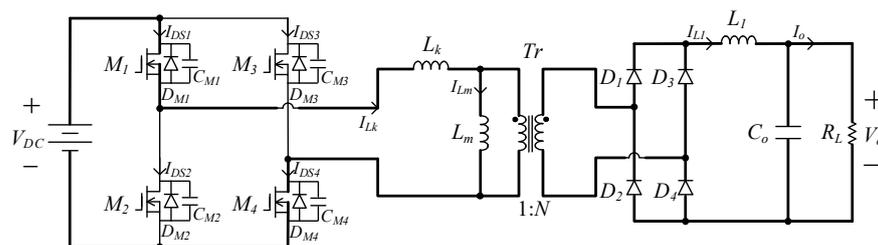
(**b**) Mode 1 ($t_0 \leq t < t_1$).
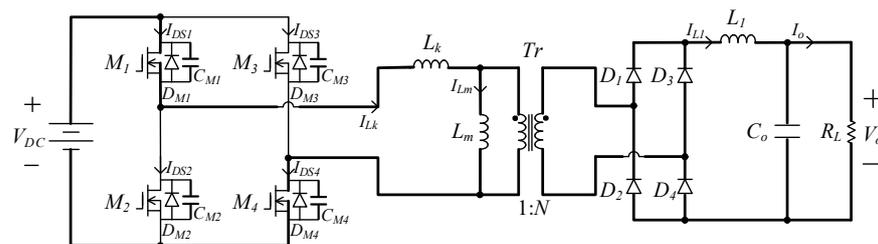
(**c**) Mode 2 ($t_1 \leq t < t_2$).
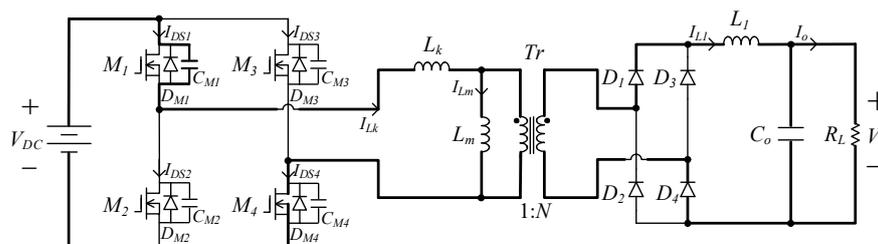
(**d**) Mode 3 ($t_2 \leq t < t_3$).

Figure 6. *Cont.*
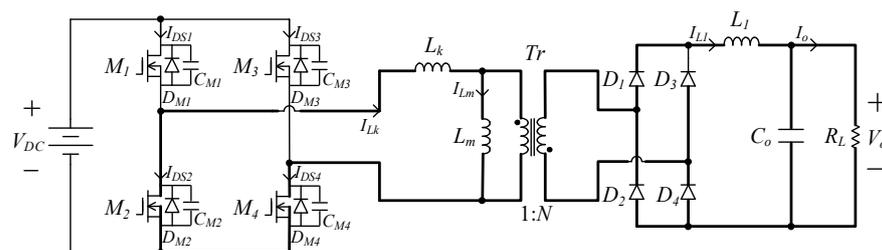
(**e**) Mode 4 ($t_3 \leq t < t_4$).
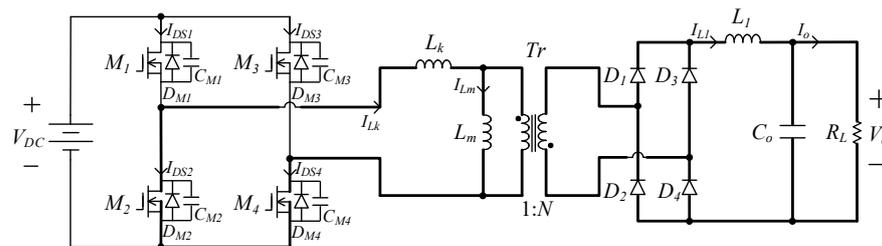
(**f**) Mode 5 ($t_4 \leq t < t_5$).
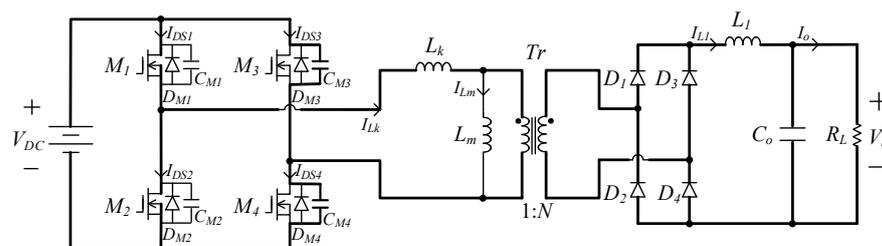
(**g**) Mode 6 ($t_5 \leq t < t_6$).
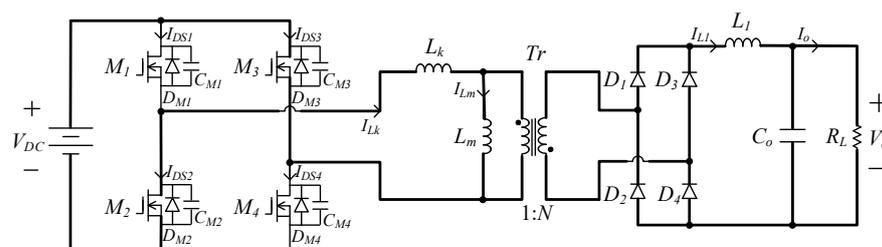

(**h**) Mode 7 ($t_6 \leq t < t_7$).

Figure 6. Equivalent circuit of the proposed full-bridge converter with dual-input sources operated in a complete switching cycle.

Mode 1 (Figure 6b: $t_0 \leq t < t_1$):Before t_0, the current I_{DS1} of switch M_1 has a negative value. The body diode D_{M1} of switch M_1 is forwardly biased. Switches M_1, M_2, and M_3 are in the off state, whereasswitch M_4 is in the turn-on state. Diodes D_1–D_4 are in the forward biased state, as shown in Figure 6a. When $t = t_0$, switch M_1 is turned on and switch M_1 is operated with ZVS at the turn-on transition, as shown in Figure 6b. Switch M_4 is kept in the turn-on state, whereas M_2 and M_3 are still in the turn-off state. Within this time interval, diodes D_1–D_4 are in a freewheeling state by inductor L_1. Current I_{DS1} abruptly increases from a negative value to an initial value, which is the initial value of inductor current I_{L1}, reflected in the secondary winding to the primary winding of the transformer T_r when the proposed system is operated in CCM. Inductor current I_{L1} linearly decreases.
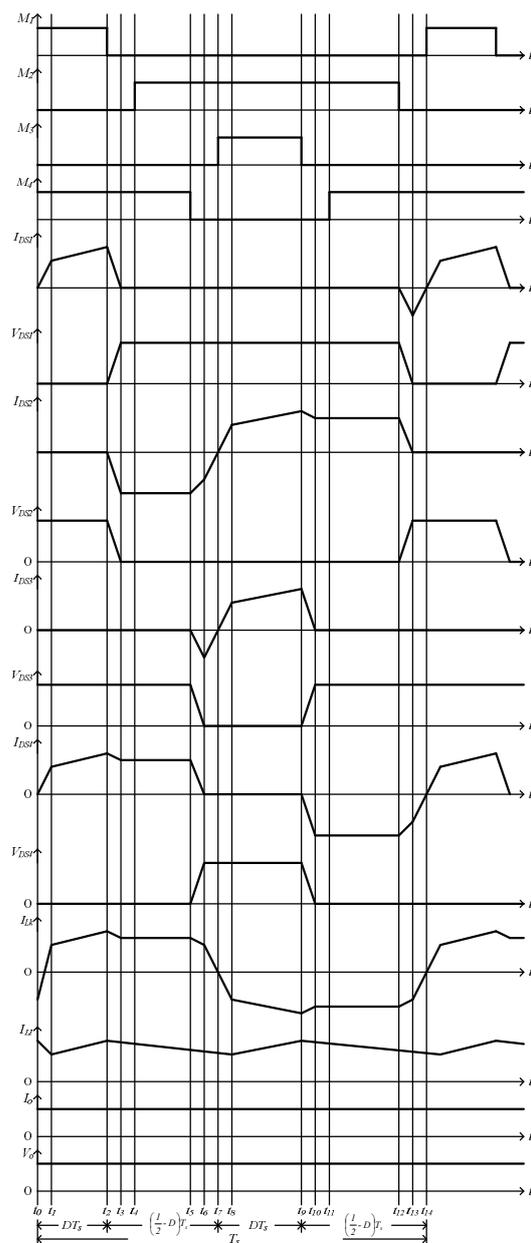
Figure 7. Conceptual waveforms of the proposed full-bridge converter with dual-input sources over a switching cycle.

Mode2 (Figure 6c: $t_1 \leq t < t_2$): At t_1, the current I_{DS1} reaches the initial value. Diodes D_1 and D_4 are kept in the forward biased state, whereas D_2 and D_3 change their operated states from the forward biased state to the reverse biased state. Current I_{DS1} increases in a linear manner. On the secondary side of transformer T_r, inductor current I_{L1} linearly increases.

Mode 3 (Figure 6d: $t_2 \leq t < t_3$): when $t = t_2$, the current I_{DS1} reaches the maximum value. Switch M_1 is turned off, whereasswitches M_2 and M_3 are in the turn-off state and M_4 is in the turn-on state. The energy trapped in the leakage inductor L_K is released by parasitic capacitors C_{M1} and C_{M2}. Therefore, voltage V_{DS2} is changed from V_{DC} to 0 V, whereasvoltage V_{DS1} is varied from 0 V to V_{DC}. Diodes D_1 and D_4 are in the forward biased state, and D_2 and D_3 are in the reverse biased state. Inductor current I_{L1} linearly increases.

Mode 4 (Figure 6e: $t_3 \leq t < t_4$): When $t = t_3$, voltage V_{DS1} reaches V_{DC} and voltage V_{DS2} is down to 0 V. At that moment, body diode D_{M2} is forwardly biased. The primary winding of transformer T_r is in a short-circuit state. Current I_{LK} is kept at a fixed value.

Since inductor current I_{L1} needs to remain in the continuous conduction state, diodes D_1–D_4 are in a freewheeling state by inductor L_1. Inductor current L_1 linearly decreases.

Mode 5 (Figure 6f: $t_4 \leq t < t_5$): At t_4, body diode D_{M2} is in a forward biased state. At that moment, switch M_2 is turned on. Switch M_2 is operated with ZVS at the turn-on transition. Diodes D_1–D_4 are kept in the forward biased state. Inductor current I_{L1} is reduced ina linear manner.

Mode 6 (Figure 6g: $t_5 \leq t < t_6$): At t_5, switch M_4 is turned off. The energy stored in leakage L_K is released by parasitic capacitors C_{M3} and C_{M4}. Voltage V_{DS3} across capacitor C_{M4} is increased from 0 V to V_{DC}. Diodes D_1–D_4 are kept in a forward biased state. Inductor current I_{L1} linearly decreases.

Mode 7 (Figure 6h: $t_6 \leq t < t_7$): when $t = t_6$, voltage V_{DS3} reaches 0 V and voltage V_{DS4} varies to V_{DC}. The body diode D_{M3} is forwardly biased. Current I_{DS3} abruptly changes from a negative value to an initial value. During this interval, diodes D_1–D_4 are in the forward biased state. Inductor current I_{L1} linearly decreases. When switch M_3 is turned on at the end of mode 7, the other half of one switching cycle starts.

4. Design Method of Full-Bridge Converter with Multiple Input Sources

In the proposed full-bridge converter, component design and selection are very important. Therefore, component design and selection are derived as follows:

4.1. Component Design of the Proposed Full-Bridge Converter

For the design of the proposed full-bridge converter with dual input sources, the determination of the duty ratio D, turns ratio N of transformer T_r, inductance L_1, and capacitance C_{DC1} are important. Their designs are analyzed briefly as follows.

(a) Duty ratio D

When deriving the duty ratio D of the proposed full-bridge converter, the input to output voltage transfer ratio M must be first obtained. According to the volt-second balance of inductor L_1, the following equation can be obtained:

$$(NV_{DC\,2} - V_{DC\,1})DT_s + (-V_{DC\,1})(\frac{1}{2} - D)T_s = 0 \tag{1}$$

where T_s is the switching period and N is the turns ratio of the transformer T_r. From (1), it can be found that transfer ratio M can be expressed as

$$M = \frac{V_{DC1}}{V_{DC2}} = 2ND \tag{2}$$

According to (2), the duty ratio D can be rewritten as

$$D = \frac{V_{DC1}}{2NV_{DC2}} \tag{3}$$

According to the operational principle of the proposed full-bridge converter with dual input sources, a larger duty ratio D corresponds to a smaller turns ratio N of transformer T_r. As a result, less current stress is imposed on switches M_1–M_4 and diodesD_1–D_4. However, in order to accommodate for the variations of the load, line voltage and component value, it is better to select an operating range of $D = 0.35$–0.4.

(b) Turns ratio N of Transformer T_r

When the duty ratio D is specified, turns ratios N of transformer T_r can be determined by (3), which is expressed as

$$N = \frac{V_{DC1}}{2DV_{DC2}} \tag{4}$$

In addition, the magnetizing inductor L_m must be much greater than L_1/N^2. It needs to satisfy the inequality, which yields

$$L_m \geq \frac{10L_1}{N^2} \tag{5}$$

According to the inequality listed in (5), the magnetizing current of transformer T_r can be neglected.

(c) Inductor L_1

Figure 8 shows the conceptual waveforms of the proposed full-bridge converter operated within the boundaries of discontinuous-conduction mode (DCM) and CCM. When the proposed converter is operated in these boundaries, the output current I_{DC1} can be determined by

$$I_{DC1} = \frac{\Delta I_{L1(max)}}{2} \tag{6}$$

where $\Delta I_{L1(max)}$ representsthe maximum variation value. In general, $\Delta I_{L1(max)}$ can be expressed by

$$\Delta I_{L1(max)} = \frac{(NV_{DC2} - V_{DC1})DT_s}{L_{1B}} \tag{7}$$

where L_{1B} is the inductance operated at the boundary of DCM and CCM. In the design consideration of I_{DC1} from (6), it is equal to $KI_{DC1(max)}$, where $I_{DC1(max)}$ is the maximum output current. Note that the K value ranges from 0 to 1. According to (6) and (7), the inductance L_1 can be determined by

$$L_1 = L_{1B} = \frac{(NV_{DC2} - V_{DC1})DT_s}{2KI_{DC1(max)}} \tag{8}$$
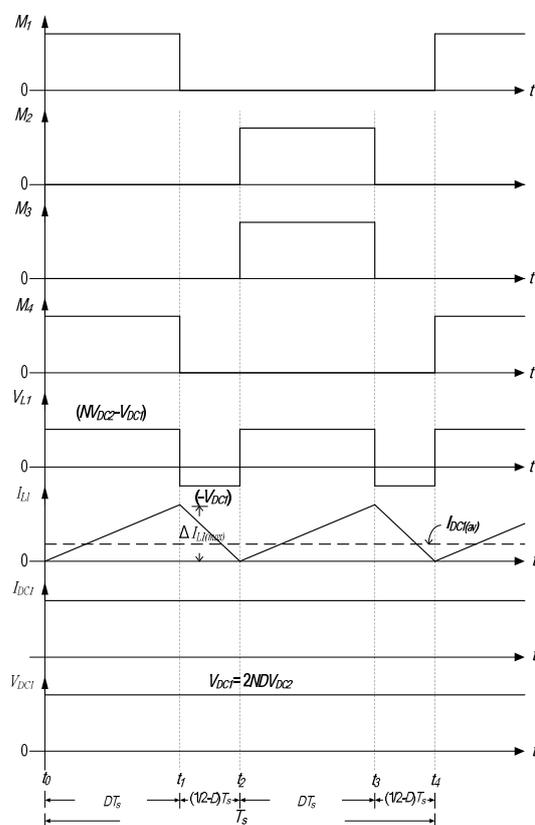
Figure 8. Conceptual waveforms of the proposed full-bridge converter operated in the boundaries of DCM and CCM.

(d)   Output capacitor C_{DC1}

In order to reduce the ripple of the output voltage V_{DC1}, the output capacitor C_{DC1} must be large enough. The ripple voltage across output capacitor C_{DC1} is expressed as follows:

$$\Delta V_r = \frac{\Delta T_{L1(max)}}{L_{DC1}}(\frac{1}{16f_s} + C_{DC1} \times ESR) \tag{9}$$

where ESR is the equivalent series resistance of the output capacitor C_{DC1}. For aluminum electrolytic capacitors, the product of ($C_{DC1} \times ESR$) is much less than ($1/16f_s$) and it can be neglected. Thus, capacitor C_{DC1} is selected as

$$C_{DC1} = \frac{\Delta I_{L1(max)}}{16f_s\Delta V_r} \tag{10}$$

4.2. Component Selection of the Proposed Full-Bridge Converter

To select the semiconductors for the proposed full-bridge converter, the voltage and current stresses of the switches and diodes are very important. Figure 9 illustrates a schematic diagram of the proposed full-bridge converter. The maximum voltage stress $V_{DS1(max)}(=V_{DS2(max)} = V_{DS3(max)} = V_{DS4(max)})$ of switch M_1 can be determined by

$$V_{DS1(max)} = V_{DC2} \tag{11}$$
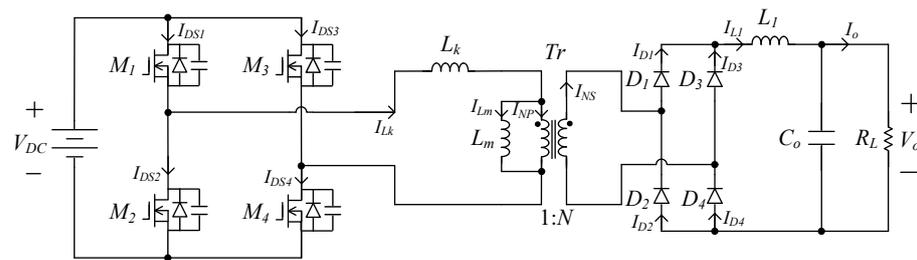
Figure 9. Schematic diagram of the proposed full-bridge converter.

The maximum voltage stress $V_{D1(max)}(=V_{D2(max)}=V_{D3(max)}=V_{D4(max)})$ of diode D_1 can be expressed as

$$V_{D1(max)} = NV_{DC2} \tag{12}$$

The conceptual waveforms of the component currents are shown in Figure 10. According to the conceptual current waveforms of switch M_1, its maximum rms current $I_{DS1(rms)}(=I_{DS3(rms)})$ is expressed as

$$I_{DS1(rms)} = \sqrt{(I_{D(max)}{}^2+I_{P(max)}{}^2+I_{D(max)}I_{P(max)})\frac{D}{3}} \tag{13}$$

where $I_{D(max)}$ is the initial current of inductor L_1 from secondary winding, reflected to primary winding when the proposed converter is operated in CCM and the output current I_o is under full-bridge conditions. In addition, the maximum rms current $I_{DS2(rms)}(=I_{DS4(rms)})$ can be expressed as

$$I_{DS2(rms)} = \sqrt{I_{P(max)}{}^2(1-2D) + (I_{D(max)}{}^2 + I_{P(max)}{}^2 + I_{D(max)}I_{P(max)})\frac{D}{3}} \tag{14}$$
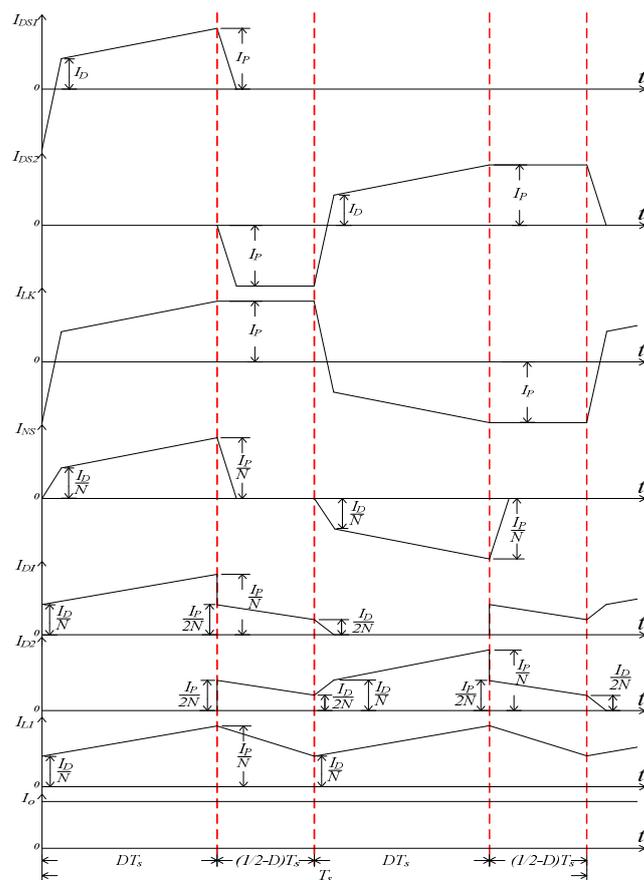
Figure 10. Conceptual waveforms of the key component currents in the proposed full-bridge converter.

In Figure 10, according to current waveform of diode D_1, the maximum rms current $I_{DS1(rms)}(=I_{DS2(rms)} = I_{DS3(rms)} = I_{DS4(rms)})$ can be derived by

$$I_{D1(rms)} = \frac{1}{N}\sqrt{(\frac{10D-1}{24})(I_{D(max)}{}^2 + I_{P(max)}{}^2 + I_{D(max)}I_{P(max)})} \tag{15}$$

5. Power Loss Analysis of the Proposed Full-Bridge Converter

Due to soft-switching features, conversion efficiency of the proposed full-bridge converter is higher than that of the counterpart with hard-switching method. In order to verify the measured conversion efficiency of the proposed one, its power analysis is very important. The proposed full-bridge converter is shown in Figure 9. Its key component current waveforms are illustrated in Figure 10. According to the current waveforms, the power losses of the proposed system include losses from the switches, diode, transformer core, and inductor core. In the following, a power loss analysis is conducted.

5.1. Losses of Switches

Figure 11 shows the conceptual waveforms of switching losses for switches M_1, M_2, M_3, and M_4. Switches M_1–M_4 are operated in ZVS at the turn-off transition of the switches. Therefore, switching losses P_{Soff} of switches M_1–M_4 can be derived as

$$P_{Soff} = \frac{1}{2T_S}V_{DS1(max)}(t_{Soff}I_P) \tag{16}$$

where t_{Soff} is the falling time of switch M_1. In addition, the conduction loss of switch M_1 can be determined by

$$P_{CD} = I_{DS1(max)}{}^2 R_{DS(on)} \tag{17}$$

where $R_{DS(on)}$ is a resistance of the switch during the turn-on interval.
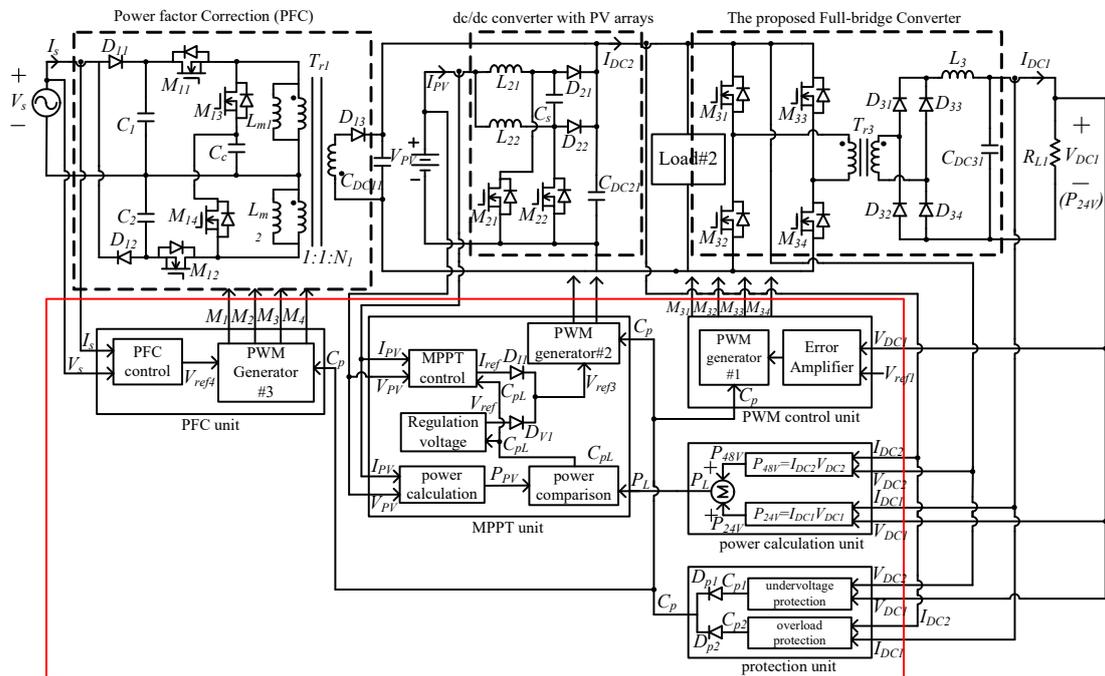
Figure 11. Block diagram of the control circuit of the proposed DC distribution system.

5.2. Losses of Diodes

When diodes D_1–D_4 are in the forward biased state, the forward drop V_F of the diode will induce diode loss. This can be expressed as

$$P_{D1} = I_{D1(rms)}V_F \tag{18}$$

5.3. Losses of Transformer T_r and Inductor L_1

The losses of the transformer T_r and inductor L_1 include core loss and copper losses. In the following, core loss and copper loss of transformer T_r and inductor L_1 are respectively derived.

(a) Transformer T_r

The core loss of transformer T_r is derived based on the maximum flux density B_m. The maximum flux density B_m can be determined as

$$B_m = \frac{u_o u_r N_1 I_{Lm(P)}}{l_{e1}} \tag{19}$$

where $\mu_0 = 4\,\pi\,\times\,10^{-7}\frac{\text{H}}{\text{m}}$, μ_r is permeability, N_1 indicates the turns of primary winding, $I_{Lm(P)}$ represents the peak current of magnetizing inductance, and l_{e1} expresses the effective magnetic path length. When B_m is determined, the core loss coefficient C_{P1} can be obtained based on the core loss curve. The core loss $P_{C1(T_r)}$ is derived by

$$P_{C1(T_r)} = C_{P1}V_{e1} \tag{20}$$

where V_{e1} is the effective core volume of the transformer core. In addition, copper loss $P_{CP(T_r)}$ can be determined as

$$P_{CP(T_r)} = I_{LK(rms)}{}^2 R_{DC1(T_r)} + I_{NS(rms)}{}^2 R_{DC2(T_r)} \tag{21}$$

Where $R_{DC1(T_r)}$ is the resistance of primary winding and $R_{DC2(T_r)}$ represents that of secondary winding. Their values are listed in Table 2. In order to determine the copper loss of transformer T_r, the magnetizing current $I_{LK(rms)}$ can be determined by

$$I_{LK(rms)} = \sqrt{(I_D{}^2 + I_P{}^2 + I_D I_P)(\frac{2D}{3}) + I_P{}^2(1 - 2D)} \tag{22}$$

Table 2. Key component parameters of the proposed full-bridge converter.

Component	Part Number	Voltage/Current Ratings or Formula	Features		
			Symbol	Parameter	Values
Switches $M_1, M_2,$ M_3, M_4	AOW2918	100 V/90 A	$R_{DS(on)}$	Drain-source on resistance	<7 mΩ
			t_{on}	Turn-on transition time	41 ns
			t_{off}	Turn-off transition time	51 ns
Diodes $D_1 \sim D_4$	STPS41H100CT	100 V/40 A	$V_{F(max)}$	Maximum forward voltage	0.67 V
Transformer T_r	EE-55Core (PC 40, manufactured by TDK)	$B_m = \frac{u_o u_r N_1 I_{Lm(P)}}{l_{e1}}$ (T) u_o: $4\pi \times 10^{-7}$ H/m $I_{Lm(P)}$: Peak Current of magnetizing inductor for primary winding $R_{DC1(Tr)} =$ $\frac{R_{DC(28)} N_1 l_{m1(Tr)} *10^{-6}}{40}$ (Ω) $R_{DC2(Tr)} =$ $\frac{R_{DC(28)} N_2 l_{m2(Tr)} *10^{-6}}{80}$ (Ω)	u_r	Permeability	2300
			l_{e1}	Effective Magnetic Path length	123 mm
			V_{e1}	Effective core volume	43.7 cm³
			$l_{m1(Tr)}$	Approximate mean length of turn for primary winding	92.2 mm
			$l_{m2(Tr)}$	Approximate mean length of turn for secondary winding	100.6 mm
			$R_{DC1(Tr)}$	Resistance using 40 strands of AWG#28 for primary winding	8.37 mΩ
			$R_{DC2(Tr)}$	Resistance using 80 strands of AWG#28 for secondary winding	3.71 mΩ
			N_1	Turn of primary winding	16 T
			N_2	Turn of secondary winding	13 T
			$R_{DC(28)}$	Resistance of AWG#28	227 $\frac{m\Omega}{m}$
Inductor L_1	EE-55Core (PC 40 manufactured by TDK)	$B_{m(L1)} = \frac{u_o u_r N_3 I_{L1(P)}}{l_{e2} + u_r l_g}$ (T) $I_{L1(P)}$: Peak Current of inductor L_1 $R_{DC3(L1)} =$ $\frac{R_{DC(28)} N_3 l_{m3(L1)} *10^{-6}}{80}$ (Ω)	u_r	permeability	2300
			l_{e2}	Effective Magnetic Path length	123 mm
			V_{e2}	Effective core volume	43.7 cm³
			$l_{m3(L1)}$	Approximate mean length of turn	96.4 mm
			$R_{DC3(L1)}$	Resistance using 80 strands of AWG#28	4.38 mΩ
			l_g	Air gap	3.08 mm
			N_3	Turn of inductor l_1	16 T

Moreover, the secondary current $I_{NS(rms)}$ can be derived as

$$I_{NS(rms)} = \frac{1}{N}\sqrt{(I_D{}^2 + I_P{}^2 + I_D I_P)\frac{2D}{3}} \tag{23}$$

(b) Inductor L_1

The core loss of inductor L_1 is derived based on the maximum flux density $B_{m(L_1)}$. The maximum flux density $B_{m(L_1)}$ can be determined as

$$B_{m(L_1)} = \frac{u_o u_r N_3 I_P}{N(l_{e2} + u_r l_g)} \tag{24}$$

where N_3 is the turns of inductor L_1, N expresses the turns ratio of transformer, l_{e2} indicates the effective magnetic path length, and l_g represents the air gap length. When $B_{m(L_1)}$ is

obtained, the core loss coefficient C_{P2} can be obtained through the core loss curve of the inductor core. The core loss $C_{P2(L_1)}$ is derived by

$$C_{P2(L_1)} = C_{P2}V_{e2} \tag{25}$$

where V_{e2} is the effective magnetic path length. To calculate the copper loss $C_{CP(L_1)}$, the rms current $I_{L1(rms)}$ must be determined. The current $I_{L1(rms)}$ can be derived by

$$I_{L1(rms)} = \frac{1}{N}\sqrt{\frac{1}{3}(I_D{}^2 + I_P{}^2 + I_D I_P)} \tag{26}$$

When the current $I_{L1(rms)}$ is obtained, the copper loss $P_{CP(L_1)}$ is expressed as

$$P_{CP(L_1)} = I_{L1(rms)}{}^2 R_{DC3(L1)} \tag{27}$$

The $R_{DC3(L1)}$ is illustrated in Table 2.

6. Power Management of the Proposed DC Distribution System

The proposed DC distribution system adopts a utility line and PV arrays to supply power to DC loads. There are three power processors, which are the PFC, DC/DC converter, and the full-bridge converter with multiple input sources, as shown in Figure 11. The PFC supplies power from the utility line (AC90 V–264 V) to DC 48 V, where as the DC/DC converter supplies power from the PV arrays (DC 34 V–43 V) to DC 48 V. The two power supplies provide power to the full-bridge converter with multiple input sources. In order to operate the proposed DC distribution system, each power processor must be operated at the appropriate power level, which is limited by the maximum output power of each power processor. In the following, the control algorithm and power management of the proposed DC distribution system are briefly described.

6.1. Control Algorithm of the Proposed DC Distribution System

The proposed DC distribution system includes three power processors. The circuit topology of the proposed system is divided into two parts: the power stage and the control stage. The power stage consists of three power processors, where the control stage consists of the control circuit. The control circuit consists of the PFC unit, MPPT unit, PWM control unit, power calculation unit, and protection unit. The PFC unit helps the PFC with utility line as its input source to achieve power factor correction, ensuring that the input voltage V_S and current I_S are controlled in this phase. According to the relationships between P_{PV} and P_L, in which P_{PV} is the power supplied by the PV arrays and P_L is the consumption power of the loads, the MPPT unit can control the operating states of the DC/DC converter with the PV arrays as the input source. There are two operating states: MPPT and regulation voltage states. When $P_{PV} \geq P_L$, the signal C_{PL} changes from a low level to a high level. This can enable the regulation voltage to generate the reference voltage V_{ref2} and disable MPPT control. Therefore, reference voltage V_{ref3} is equal to voltage V_{ref2}. PWM generator #2 can generate PWM signals M_{21} and M_{22} by voltage V_{ref3}. The DC/DC converter, using PV arrays as its input source, is operated in the regulation voltage mode. If $P_{PV} < P_L$, C_{PL} varies from a high level to a low level. MPPT control is enabled by the signal C_{PL}, whereas the regulation voltage is disabled. Thus, reference voltage V_{ref3} equals I_{ref1}. PWM generator #2 can generate signals M_{21} and M_{22} to control the DC/DC converter by voltage V_{ref3}. The DC/DC converter is operated in MPPT mode.

The proposed full-bridge converter can regulate the output voltage V_{DC1} by means of the PWM control unit. When the protection unit generates a signal C_P, which is a high level, PWM generator #1, PWM generator #2, and PWM generator #3 are disabled by signal C_P. Signal C_P varies from a low level to a high level when voltages V_{DC1} and V_{DC2} are in the under-voltage state or currents I_{DC1} and I_{DC2} are in the overload state. Signal C_P is

generated by the protection unit. The control algorithm of the proposed DC distribution system was described previously.

6.2. Power Management of the Proposed DC Distribution System

The maximum output power of the PFC is set at $P_{ac(max)}$, whereas that of the DC/DC converter is specified by $P_{PV(max)}$. In addition, the maximum power of the proposed full-bridge converter with dual input sources is limited at $P_{24SV(max)}$. In the proposed DC distribution system, it can supply two different voltage levels to DC loads: DC 48 V and DC 24 V, respectively. Therefore, load powers can be indicated by $P_{24\ V}$ and $P_{48\ V}$, separately. According to the power management of the proposed DC power system, there are three operational states $0 \leq P_{24\ V} + P_{48\ V} < P_{PV(max)}$, $P_{PV(max)} \leq P_{24V} + P_{48V} < P_{PV(max)} + P_{ac(max)}$, and $P_{24\ V} + P_{48\ V} > P_{PV(max)} + P_{ac(max)}$. Its operational states are illustrated in Table 1. Note that the DC 24 V load and DC 48 V load are simultaneously turned on or turned off since some loads require powers of DC 24 V and 48 V at the same time.

As shown in Table 3, when the operational state of the proposed DC distribution system is in the $0 \leq P_{24\ V} + P_{48\ V} < P_{PV(max)}$ state, the PFC is shut down, and the DC/DC converter is working, which is operated at $P_{PV} = P_{24\ V} + P_{48\ V}$. The proposed DC distribution system supplies power to load #1 (DC 24 V) and load #2 (DC 48 V). If operational state is kept at $P_{PV(max)} \leq P_{24\ V} + P_{48\ V} < P_{PV(max)} + P_{ac(max)}$, the PV arrays are operated at $P_{PV(max)}$, where as the PFC supplies power at $P_{ac} = P_{24\ V} + P_{48\ V} - P_{PV(max)}$. Therefore, three power processors in the proposed DC distribution system are in the working state. When $P_{24\ V} + P_{48\ V} > P_{PV(max)} + P_{ac\ (max)}$, the proposed DC power system is shut down since the generation power of the proposed system is not enough to supply load #1 and load #2. According to operational state mentioned above, the proposed DC distribution system can meet the requirements of a DC power distribution system.

Table 3. Power management of the proposed DC distribution system.

Operating States / Power System	State 1 $0 < P_{24V} + P_{48V} \leq P_{PV(max)}$	State 2 $P_{PV(max)} < P_{24V} + P_{48V} \leq P_{PV(max)} + P_{ac(max)}$	State 3 $P_{PV(max)} + P_{ac(max)} < P_{24V} + P_{48V}$
Power factor correction (utility line) $P_{ac(max)}$	shutdown	working	shutdown
DC/DC converter with PV arrays (MPPT) $P_{PV(max)}$	working	working	shutdown
The proposed full-bridge converter (with multiple input sources) $P_{24\ V(max)}$	working	working	shutdown
Load#1 $P_{24\ V}$	ON	ON	OFF
Load#2 $P_{48\ V}$	ON	ON	OFF

7. Measured Results and Discussion

In order to verify the performances of the proposed full-bridge converter, a prototype with the following specifications was implemented.

- Input voltage V_{DC2}: DC 48 V,
- Switching frequency f_s: 50 kHz,
- Output voltage V_{DC1}: DC 24 V,
- Maximum output current $I_{DC1(max)}$: 21 A,
- Maximum output power $P_{24SV(max)}$: 500 W.

According to the previously outlined specifications and design of the proposed full-bridge converter with dual input sources, the duty ratio $D = 0.35$ and turns ratio $N = 0.8$ were determined. When $k = 0.1$, as illustrated in Equation (8), the proposed full-bridge converter is operated in the boundaries of DCM and CCM. Therefore, inductance L_1 is

specified and its value is equal to 38.7 μH. The other components of the power stage in the proposed full-bridge converter were determined as follows:

- Switches $M_1 \sim M_4$: AoW2918,
- Transformer core: EE-55,
- Diodes $D_1 \sim D_4$: STPS41H100CT,
- Capacitor C_{DC1}: 3300 μF/35 V,
- Leakage inductor L_K: 3.8 μH,
- Magnetizing inductor L_m: 1.72 mH.

According to the specifications and component selection of the proposed full-bridge converter, its key component parameters are listed in Table 2.

Figure 12 shows the measured waveforms of switch voltage V_{DS} and current I_{DS} under 30% of full-load conditions for the full-bridge converter operated in a hard-switching manner. Figure 12a shows those waveforms of voltage V_{DS1} and I_{DS1}, whereas Figure 12b illustrates those waveforms of voltage V_{DS2} and I_{DS2}. Figure 13 shows those waveforms for the proposed full-bridge converter under 30% of full-load conditions, in which the waveforms exhibit soft-switching features. In Figure 13, it can be observed that the proposed full-bridge converter was operated with approximately ZVS at the turn-on transition, reducing switching losses and increasing conversion efficiency. Figure 14 illustratesthe measured output voltage V_{DC1} and current I_{DC1} waveforms under a step-load change between 10% of full-load conditions and full-load conditions, in which it can be observed that the regulation of output voltage V_{DC1} was within ±1% and the dynamic load variation of the proposed full-bridge system was able to meet its power rating.
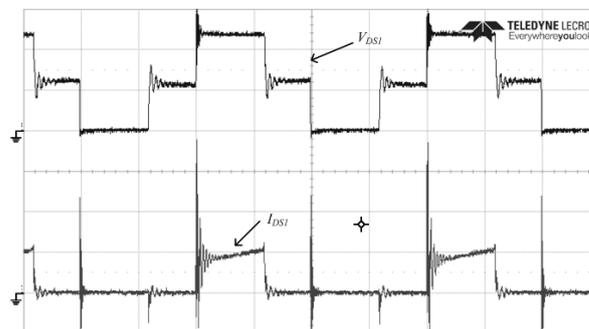
(V_{DS1}: 20 V/div, I_{DS1}: 1 A/div, 5 us/div)

(**a**)
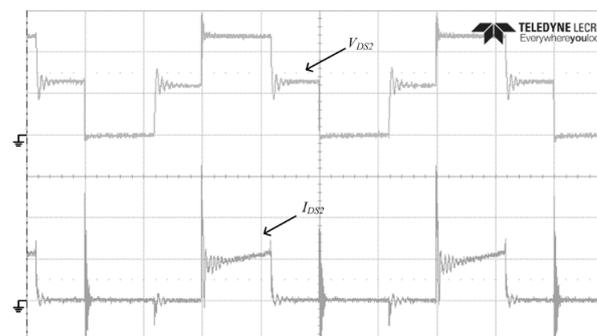
(V_{DS2}: 20 V/div, I_{DS2}: 1 A/div, 5 us/div)

(**b**)

Figure 12. Measured waveforms of switch voltage and current under 30% of full-load conditions for the full-bridge converter operated in a hard-switching manner: (**a**) switch voltage V_{DC1} and current I_{DS1}, and (**b**) switch voltage V_{DS2} and current I_{DS2}.
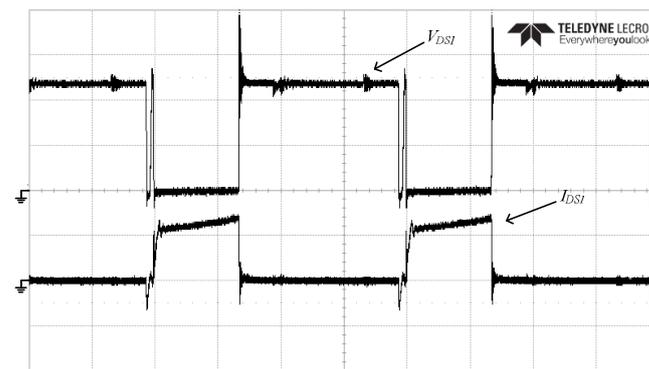
(V_{DS1}: 20 V/div, I_{DS1}: 3 A/div, 5 *u*s/div)

(**a**)
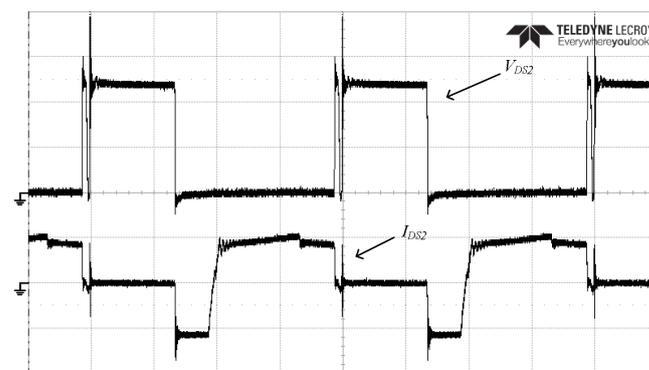
(V_{DS2}: 20 V/div, I_{DS2}: 3 A/div, 5 *u*s/div)

(**b**)

Figure 13. Measured waveforms of switch voltage and current under 30% of full-load conditions for the full-bridge converter operated in asoft-switching manner: (**a**) switch voltage V_{DC1} and current I_{DS1}, and (**b**) switch voltage V_{DS2} and current I_{DS2}.
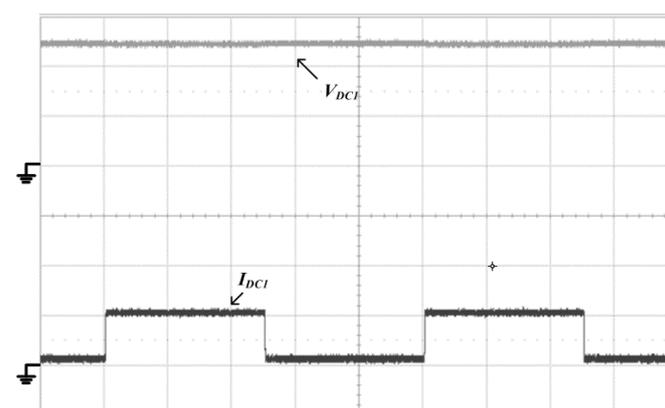
(V_{DC1}: 10 V/div, I_{DC1}: 20 A/div, time: 100 ms/div)

Figure 14. Measured output voltage V_{DC1} and current I_{DC1} waveforms under step-load change between 10% of full-load conditions and full-load conditions.

An efficiency comparison between the proposed full-bridge converter and a conventional system from a light load to a heavy load is shown in Figure 15. The components and parameter values of the conventional system were the same as the proposed full-bridge converter, except the soft-switching features were not the same as those of the proposed system. As shown in Figure 15, the maximum conversion efficiency was located at 50% of

the full load and its value was about 92%. Its conversion efficiency was higher than that of its counterpart with the hard-switching manner. In order to prove this conversion efficiency, as shown in Figure 15, a power loss analysis of the proposed full-bridge converter was derived. Table 4 lists the semiconductor losses of the proposed full-bridge converter under different load conditions. Since switches M_1–M_4 are operated with ZVS at the turn-on transition, their switching loss was calculated based on that of the turn-off transition. In order to calculate the switch loss and diode loss, the key component peaks and *rms* currents under different loads are listed in Table 5. Table 6 illustrates the parameters of core material and core loss analysis for the proposed full-bridge converter. Power loss analyses of the proposed full-bridge converter at core loss efficiencies of transformer T_r and inductor L_1 are respectively provided in Figures 16 and 17. A power loss analysis of the proposed full-bridge converter under different loads is provided in Table 7. In Table 7, it can be seenthat the calculation efficiency η_c was higher than 0.6–3.7% of the practical efficiency η_p. When the load was under 30% and below 30% of full-load conditions, the leakage inductor current I_{LK} did not eliminate the energy stored in the parasitic capacitor of the switches. Its switching loss at turn-on transition was approximately0.5% of the input power of the proposed converter under different loads. In addition, the stray loss of the proposed converter was about 0.6–3.5% under different loads. Particularly, when the load was increased, the stray loss also increased. When the proposed full-bridge converter adopted the proposed gate signal control method to drive switches M_1–M_4, the power loss increases due to the circulating current flowing through switches M_2 and M_4 and the primary winding side of the transformer. The extra loss in switches M_2 and M_4 are equal to $2(P_{c2}\text{-}P_{c1})$. In the primary winding side of the transformer, $I_{LK(rmsp)}$ is the reflected current from the secondary winding side to the primary winding side, where $I_{LK(rmsp)} = NI_{NS(rms)}$. The increase in copper loss of transformer for the circulating current is equal to $P_{C(Trl)} = (I_{LK(rms)}^2 - I_{LK(rmsp)}^2)R_{dc1(Tr)}$. When the proposed full-bridge converter is operated under full-load conditions, the extra loss is equal to $2(P_{C2}-P_{C1}) + P_{C(Trl)} = 2.674$ W. This reduces conversion efficiency by 0.49%. Therefore, the extra power loss for the circulating current is very low in the proposed full-bridge converter.
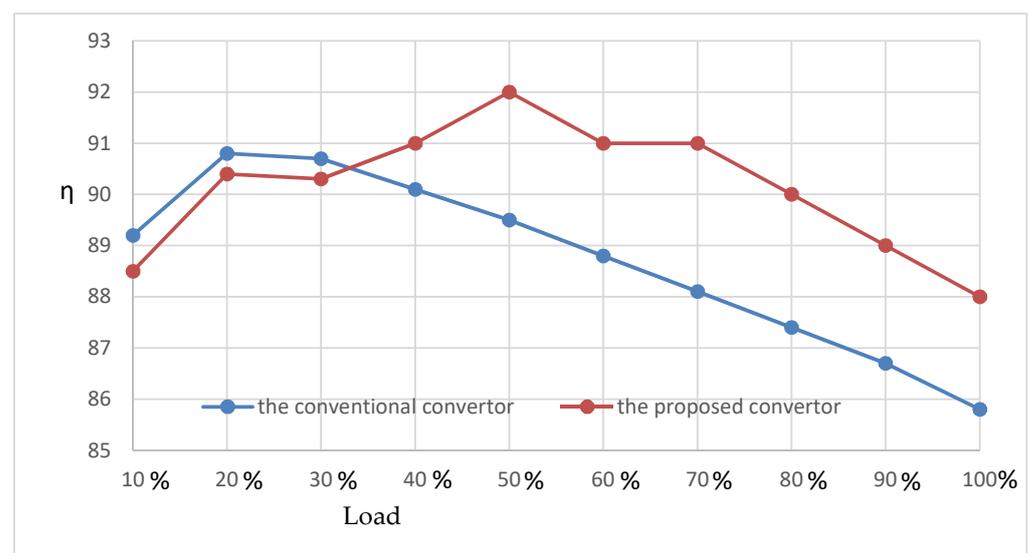

Figure 15. Efficiency comparison between the proposed full-bridge converter and the conventional one from a light load to a heavy load.

Table 4. Semiconductor loss analysis of the proposed full-bridge converter under different load conditions.

Load (%)	Switch M_1 or M_3 Loss		Switch M_2 or M_4		Diodes D_1–D_4
	Switch Loss $P_{soff1}=\frac{1}{2T_s}V_{DS}(t_{soff}I_P)$ (W)	Conduction Loss $P_{c1}=I_{DS1(rms)}^2 R_{ds(on)}$ (W)	Switching Loss $P_{soff2}=\frac{1}{2T_s}V_{DS}(t_{soff}I_P)$ (W)	Conduction Loss $P_{c2}=I_{DS2(rms)}^2 R_{ds(on)}$ (W)	Forward Drop Voltage Loss $P_{D1}=I_{D1(rms)}V_F$ (W)
10	160 m	7 m	160 m	25 m	0.76
20	263 m	25 m	263 m	36 m	1.47
30	365 m	56 m	365 m	150 m	2.19
40	468 m	99 m	468 m	253 m	2.91
50	571 m	155 m	571 m	384 m	3.63
60	674 m	223 m	674 m	541 m	4.36
70	777 m	303 m	777 m	726 m	5.08
80	880 m	396 m	880 m	938 m	5.81
90	982 m	501 m	982 m	1.18	6.53
100	1.085	618 m	1.085	1.44	7.26

Table 5. Key component currents of the proposed full-bridge converter under different load conditions.

Load (%)	I_o (A)	I_D (A)	I_P (A)	$I_{DS1(rms)}=I_{DS3(rms)}$	$I_{DS2(rms)}=I_{DS4(rms)}$	$I_{LK(rms)}$	$I_{NS(rms)}$	$I_{D1(rms)}=I_{D2(rms)}=I_{D3(rms)}=I_{D4(rms)}$	$I_{L1(rms)}$	Operational Condition
10	2.1	0.75	2.611	0.986	1.879	2.122	1.743	1.136	2.205	$V_{DC2}=48$ V, $V_o=24$ V, $I_{o(max)}=21$ A, $N=0.8$, $D=0.3125$, $T_s=20$ µS, $L_1=38.7$ µH, $\Delta I_{L1}=\frac{(NV_{DC2}-V_o)}{L_1}\times DT_S=2.326$ A, $I_DN=I_o-\frac{\Delta I_{L1}}{2}$, $I_P=I_D+\Delta I_{L1}$, and $I_{Lm(P)}=\frac{V_{DC2}}{Lm}DT_s=0.174$ A
20	4.2	2.43	4.291	1.902	2.269	3.76	3.362	2.192	4.253	
30	6.3	4.11	5.971	2.834	4.626	5.425	5.01	3.266	6.337	
40	8.4	5.79	7.651	3.769	6.013	7.097	6.663	4.344	8.428	
50	10.5	7.47	9.331	4.706	7.402	8.772	8.319	5.423	10.523	
60	12.6	9.15	11.011	5.643	8.793	11.448	9.976	6.563	12.618	
70	14.7	10.83	12.691	6.581	10.184	12.125	11.634	7.584	14.716	
80	16.8	12.51	14.371	7.519	11.575	13.803	13.292	8.665	16.813	
90	18.9	14.19	16.051	8.458	12.967	15.482	14.952	9.747	18.913	
100	21	15.87	17.731	9.397	14.36	17.161	16.612	10.829	21.012	

Table 6. Core parameters and core loss analysis for the proposed full-bridge converter.

| Load (%) | Core Loss and Core Parameters | | | | | | | |
| | Transformer T_r | | | | Inductor L_1 | | | |
	Maximum Flux Density $B_m = \frac{u_o u_r N_1 I_{Lm(P)}}{l_{e1}}$ (mT)	Core Loss Efficiency C_{P1} (mw/cm³)	Core Loss $P_{C1(Tr)}$ (V_{e1} = 43.7 cm³) (W)	Copper Loss $P_{CP(Tr)}$ (W)	Maximum Flux Density $B_m = \frac{u_o u_r N_1 I_{Lm(P)}}{l_{e2} + u_r l_g}$ (mT)	Core Loss Efficiency C_{P2} (mw/cm³)	Core Loss $P_{C2(L_1)}$ (V_{e2} = 43.7 cm³) (W)	Copper Loss $P_{CP(L_1)}$ (W)
10	65.3	7	306 m	49 m	20.9	2	87 m	21 m
20	65.3	7	306 m	160 m	34.4	2.8	122 m	79 m
30	65.3	7	306 m	339 m	47.9	4	175 m	176 m
40	65.3	7	306 m	586 m	61.3	7	360 m	311 m
50	65.3	7	306 m	900 m	74.8	8	350 m	485 m
60	65.3	7	306 m	1.47	88.2	20	874 m	697 m
70	65.3	7	306 m	1.73	101.7	32	1.40	949 m
80	65.3	7	306 m	2.25	115.2	40	1.75	1.24
90	65.3	7	306 m	2.84	128.6	60	2.62	1.57
100	65.3	7	306 m	3.49	142.1	70	3.06	1.93
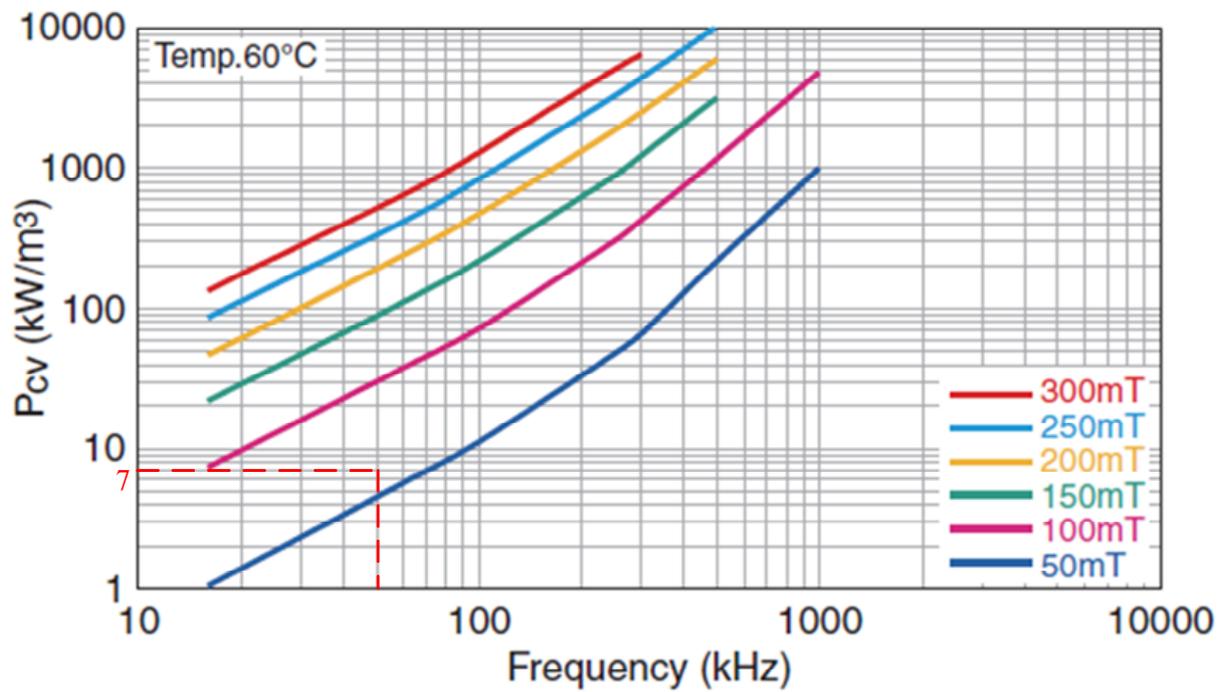
Figure 16. Core loss (mW/cm^3) curves of transformer T_r, manufactured by PC 40 material of TDK.
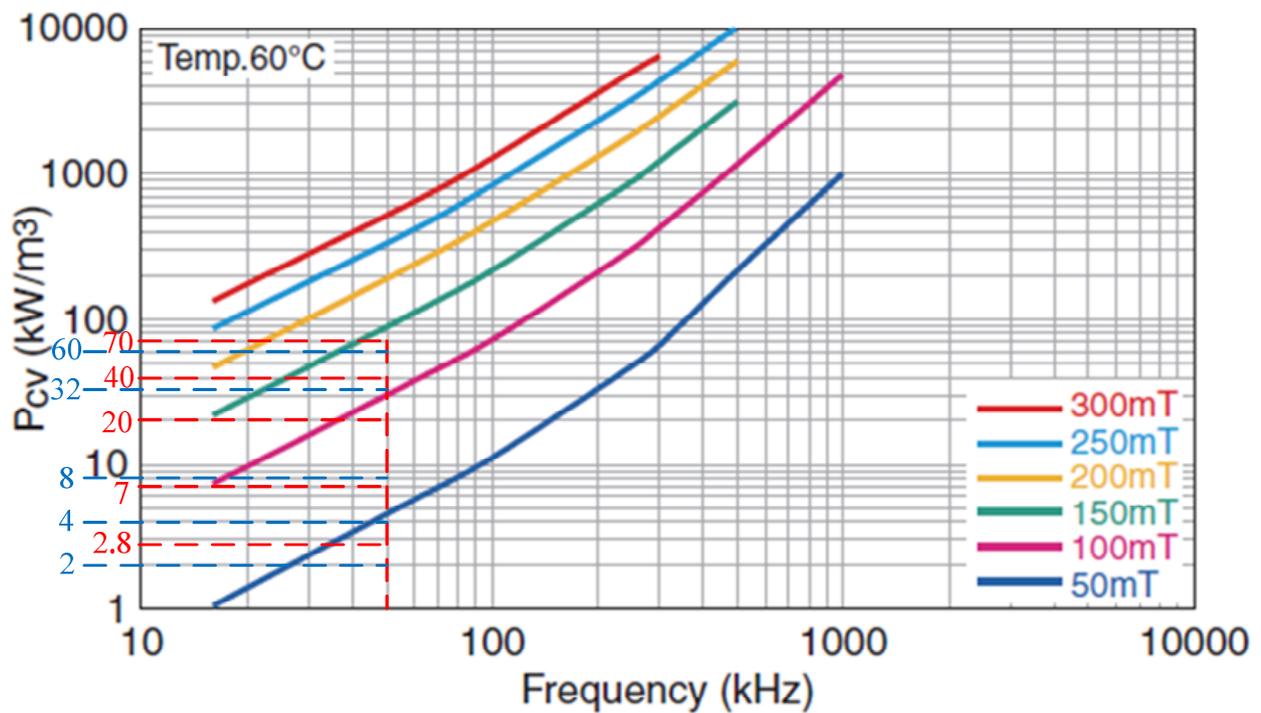
Figure 17. Core loss (mW/cm^3) curves of inductor L_1, manufactured by PC 40 material of TDK.

Table 7. Power loss analysis for the proposed full-bridge converter under different load conditions.

Load (%)	Practical Efficiency η_p (%)	Switch Losses		Diode Losses	Total Core Losses $P_{TC} = P_{C1(Tr)}$ $+ P_{CP(Tr)}$ $+ P_{C2(L1)}$ $+ P_{CP(L1)}$ (W)	Total Power Losses P_{loss} (W)	Calculation Efficiency η_c (%)
		Switching Losses $P_{TS1} = 2P_{son1}$ $+ 2P_{son2}$ (W)	Conduction Loss $P_{TC} = 2P_{C1} + 2P_{C2}$ (W)	$P_{TD} = 4P_{D1}$ (W)			
10	88.5	640 m	64 m	3.04	463 m	4.21	92.2
20	90.5	1.05	122 m	5.88	667 m	7.72	92.8
30	90.4	1.46	412 m	8.76	996 m	11.63	92.8
40	91	1.87	704 m	11.64	1.56	15.77	92.7
50	92	2.28	1.08	14.52	2.04	19.92	92.6
60	91	2.70	1.53	17.44	3.35	25.02	92.3
70	91	3.11	2.06	20.32	4.39	29.88	92.1
80	90	3.52	2.67	23.24	5.55	34.98	91.9
90	89	3.93	3.36	26.12	7.34	40.75	91.7
100	88	4.34	4.11	29.04	8.79	46.28	91.5

In order to demonstrate the power management of the proposed DC distribution system, a block diagram of the proposed system is shown in Figure 18. Concerning the contents of Figure 18, the DC/DC converter with PV arrays was previously shown in Figure 2, where as the power factor correction was illustrated in Figure 3. In addition, the proposed full-bridge converter with dual-input sources was plotted in Figure 4. The proposed DC distribution includes three converters: theDC/DC converter with PV arrays, the power factor correction system, and the proposed full-bridge converter. Figure 11 shows a block diagram of control circuit of the proposed DC distribution system. Since the DC/DC converter with PV arrays and power factor correction are connected in parallel, they will supply power to load #1 and load #2, where load #1 is the output load of DC 24 V and load #2 is the output load of DC 48 V. The total maximum power of the DC/DC converter with PV arrays and power factor correction is greater than or equal to the sum of the maximum power of load #1 and load #2. Since the maximum processing power of the proposed full-bridge converter is equal to 500 W and its conversion efficiency is 88%, the maximum input power of the proposed full-bridge converter is limited by 568 W. Therefore, the total maximum power requirement is equal to 1928 W at the DC 48 V terminal. This is close to 1920 W, which is the sum of 1200 W for the maximum output power of the DC/DC converter with PV arrays and 720 W for that of the power factor correction system. The maximum output power of each converter is listed in Table 8. Because the proposed DC distribution system is designed using power factor correction, the DC/DC converter with PV arrays, and the proposed full-bridge converter, its power management is divided into three states, as listed in Table 3. The output power of load #1 is at the DC 24 V terminal, where as that of load #2 is at the DC 48 V terminal. In order to calculate the total load power, $P_{24\ V}$ must be transferred from the DC 24 V terminal and reflected to the DC 48 V terminal. Therefore, $P_{24\ V}$, divided by η where η is the conversion efficiency of the proposed full-bridge converter, as shown in Figure 15, can be equivalent to the DC 48 V terminal. When the proposed DC distribution power is operated in state 1, its current and voltage waveforms are as shown in Figure 19. In Figure 19, before t_o, $P_{24\ V} = P_{48\ V} = 0$ W. At $t = t_0$, $P_{48\ V}$ varies from 0 W to 300 W. Since $P_{PV(max)} = 600$ W, $P_{PV(max)} > P_{24\ V} + P_{48\ V}$ and the operational condition is in the state 1 condition. When $t = t_1$, $P_{24\ V}$ changes from 0 W to 240 W. The total load power is equal to 560 W (= (240/η(=0.9)) + 300 = 560 W). Therefore, $P_{PV(max)} > P_{24\ V} + P_{48\ V}$ and the proposed system is still operated in the state 1 conditions. When $P_{PV(max)} = 550$ W, $P_{ac(max)} = 720$ W, $P_{48\ V} = 480$ W and $P_{24\ V} = 480$ W. Its measured waveform is illustrated in Figure 20. As shown in Figure 20, before t_o, $P_{24\ V} = P_{48\ V} = P_{ac} = 0$ W. When $t = t_0$, $P_{24\ V} = P_{48\ V} = 480$ W. The total load power is equal to 1030 W (= (480/η(=0.88)) + 480 = 1030 W). Since $P_{PV(max)} = 550$ W and $P_{ac} = (P_{24\ V}/\eta) + P_{48\ V} - P_{PV(max)}$, $P_{ac} = 480$ W. Therefore, $P_{PV(max)} < P_{24\ V} + P_{48\ V} < P_{PV(max)} + P_{ac(max)}$.

The proposed systemis operated in the state 2 condition. When $P_{PV(max)}$ = 600 W, $P_{ac(max)}$ = 720 W, $P_{24\ V}$ = 500 W, and $P_{48\ V}$ = 480 W, the waveforms are as shown in Figure 21. As seen in Figure 21, before t_o, $P_{24\ V}$ = $P_{48\ V}$ = P_{ac} = 0 W. At t = t_0, $P_{48\ V}$ = 960 W and $P_{24\ V}$ = 500 W. The total load power is equal to 1528 W (= 960 + (500/η(=0.88)) = 1528 W). Since $P_{PV(max)}$ + $P_{ac(max)}$ = 1320 W, $P_{PV(max)}$ + $P_{ac(max)}$ < $P_{24\ V}$ + $P_{48\ V}$. This will result in a linear drop of voltage at the DC48 V terminal. When t = t_1, voltage V_{DC2} (DC 48 V terminal) is less than the minimum set value of output voltage at the DC 48 V terminal. The proposed DC distribution power is shut down, and load#1 and load #2 are turned off. In that moment, the DC/DC converter with PV arrays and power factor correction are turned on again. After 10 s, load #1 and load #2 are turned on again. The proposed DC distribution system is shut down again until itis operated in state 1 or state 2 conditions. As mentioned above, the proposed DC distribution system can use a single chip to achieve power management. Its operational states meet the desired operational states listed in Table 3.
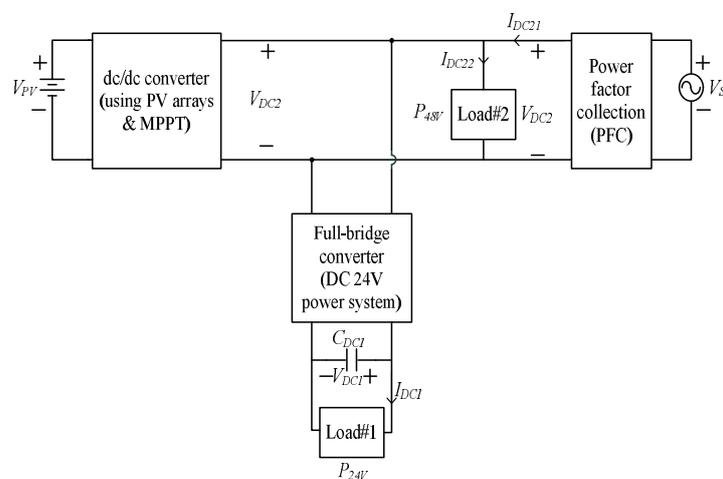

Figure 18. Block diagram of the proposed DC distribution system with multipleinput power sources.

Table 8. Power rating of each power processor in the proposed DC distribution system.

| Power Sources	Symbol	Definition	Value
Utility line (using power factor correction(PFC))	P_{ac}	output power of utility line at present	
	$P_{ac(max)}$	maximum output power of utility line	720 W
PV arrays (using DC/DC converter with PV arrays)	P_{PV}	output power of PV arrays	
	$P_{PV(max)}$	maximum output power of PV arrays	1200 W
Load	$P_{24\ V}$	consumption power at present (Load#1)	$P_{24\ V(max)}$ = 500 W
	$P_{48\ V}$	consumption power at present (Load#2)	$P_{48\ V(max)}$ = 1360 W
	P_{24SV}	output power of the proposed full-bridge converter	
	$P_{24SV(max)}$	maximum output power of the proposed full-bridge converter	500 W
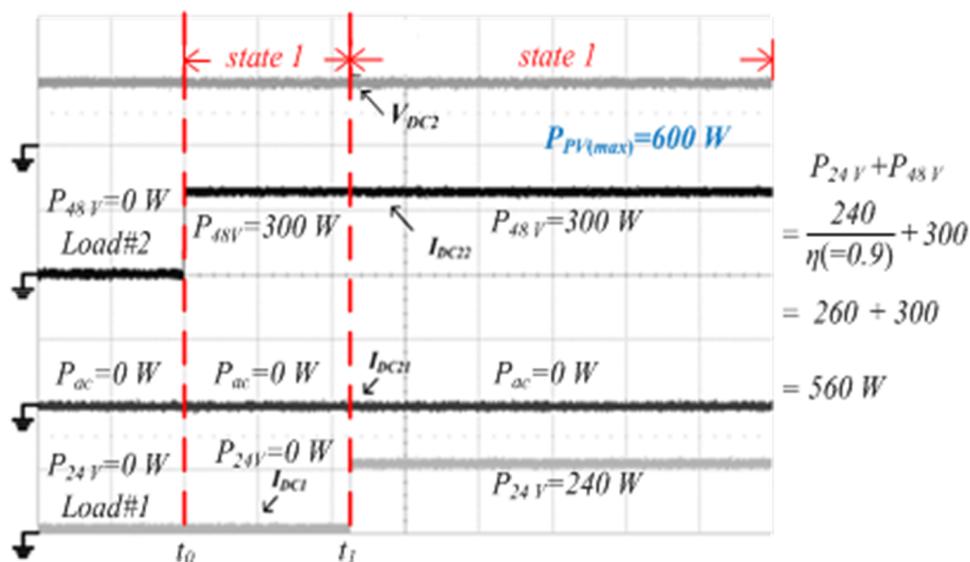
(V$_{DC2}$: 50 V/div, I$_{DC22}$: 10 A/div, I$_{DC21}$: 5 A/div, I$_{DC1}$: 10 A/div, time: 500 ms/div)

Figure 19. Measured currents I_{DC1}, I_{DC21}, and I_{DC22} and voltage V_{DC2} waveforms when $0 < P_{24\,V} + P_{48\,V} \leq P_{PV(max)}$.
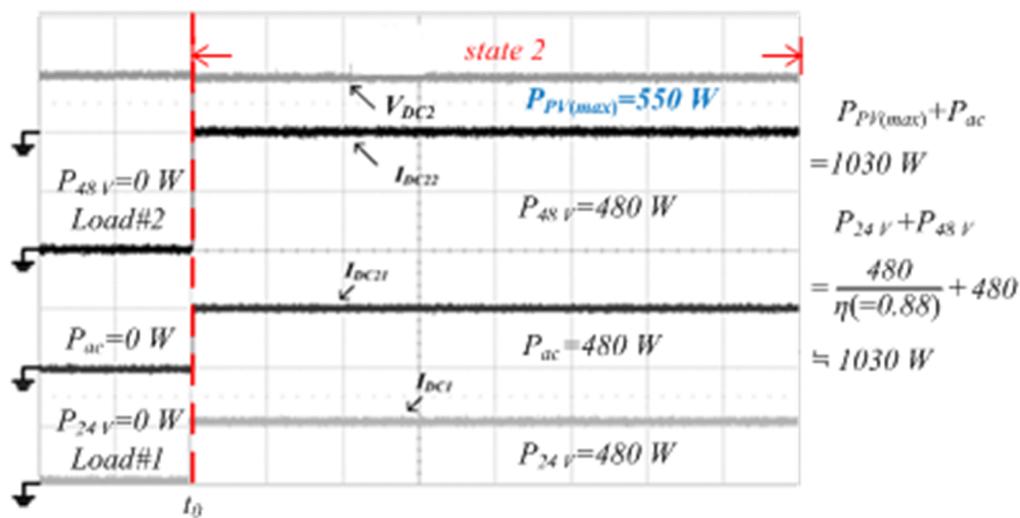
(V$_{DC2}$: 50 V/div, I$_{DC22}$: 5 A/div, I$_{DC21}$: 10 A/div, I$_{DC1}$: 20 A/div, time: 500 ms/div)

Figure 20. Measured currents I_{DC1}, I_{DC21}, and I_{DC22} and voltage V_{DC2} waveforms when $P_{PV(max)} < P_{24\,V} + P_{48\,V} \leq P_{PV(max)} + P_{ac(max)}$.
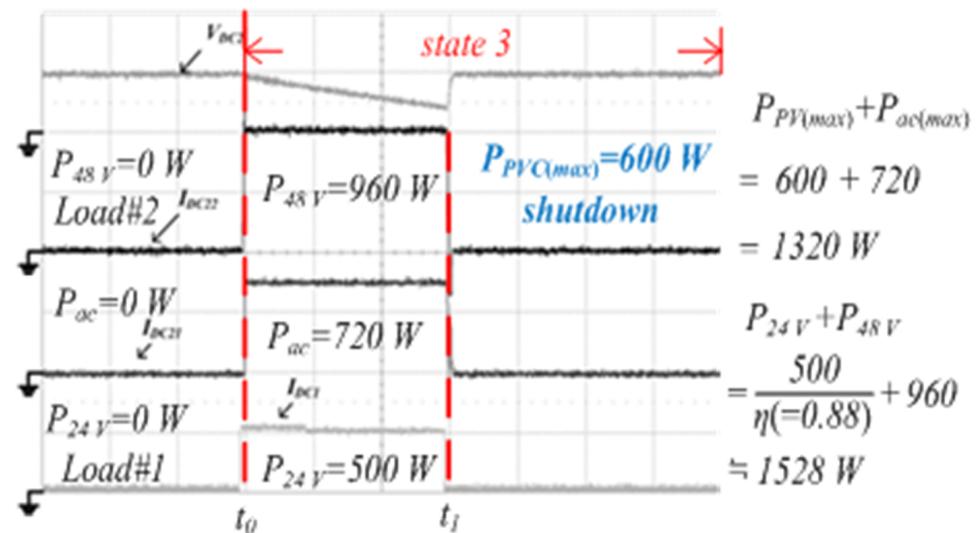
(V_{DC2}: 50 V/div, I_{DC22}: 10 A/div, I_{DC21}: 10 A/div, I_{DC1}: 20 A/div, time: 50 ms/div

Figure 21. Measured currents I_{DC1}, I_{DC21}, and I_{DC22} and voltage V_{DC2} when $P_{ac(max)}$ + $P_{BS(max)}$ < $P_{24\ V}$ + $P_{48\ V}$.

8. Conclusions

In this paper, the proposed full-bridge converter with dual input sources is applied to a DC power distribution system. The topology and control method of the proposed DC distribution system are proposed in this paper. In addition, the operational method, design, and power loss analysis of the proposed full-bridge converter are described in detail. The measured results verified that the proposed full-bridge converter can be applied to DC distribution applications. Based on the power loss analysis and experimental results, it can be seen that the calculation efficiency η_c is higher than 0.6–3.7% of the practical efficiency η_p. The reason for this is that the stray loss of the proposed converter induces the different value. In addition, the extra power loss caused by the circulating current reduces the conversion efficiency by 0.49% in the proposed full-bridge converter. This does not affect the conversion efficiency of the proposed converter significantly. Its maximum conversion efficiency is 92% under 50% of full-load conditions. In particular, the measured results have proven that different operational states among the converters in the proposed DC distribution system can be implemented. Therefore, the proposed full-bridge converter with multiple input sources is suitable for DC distribution applications.

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