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Grid Harmonics Suppression for Three Phase Dual-Frequency Grid-Connected Inverter Based on Feedforward Compensation

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Abstract: Using a low pulse ratio, the electromagnetic interference and switching loss of an inverter can be effectively reduced, particularly in high-power applications. However, due to variations in grid impedance, it is a challenging task to achieve stable operation of an LCL-type grid-connected inverter (GCI) using the active damping method with low pulse ratio. Thus, a novel three-phase dual-frequency GCI is presented to ensure the symmetry of the output power and the stable operation of the system address stability issues. The proposed inverter topology in this article is composed of two inverters in parallel, which are, respectively, a power inverter unit (PIU) and an auxiliary harmonic elimination unit (AHEU). To reduce the switching loss and improve the inverter efficiency, the switching frequency of the PIU is relatively low, injecting current into the grid. Moreover, the feedforward compensation method is used in AHEU. AHEU operates at high switching frequency to generate a current component that is symmetrical with the ripple com-ponent, improving the power quality, without extracting the current harmonic as the current reference. The operating principle of feedforward compensation is explained, and a proper parameter design procedure is presented in this paper. Since L filters are used for the proposed inverter, the system can operate stably where the ratio of switching frequency to fundamental frequency is low. A 10 kW laboratory prototype was built. The experimental results showed that the grid current ripple could be effectively eliminated and the THD of the grid current was 3.01%. The proposed inverter has good stability in a weak grid, and the efficiency of the proposed inverter is 95.98% at rated current, which is 0.81% higher than the traditional GCI, effectively increasing the efficiency of the system.

Keywords: three-phase grid-connected inverter; current ripple; power quality

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1. Introduction

In recent years, photovoltaics has become one of the most promising energy sources due to its ease of installation, environmental friendliness and low maintenance costs [1–4]. As a result, solar photovoltaic power generation systems have attracted a lot of attention. As an interface between generation systems and the grid, the grid-connected inverter (GCI) can inject high quality power into the grid.

To improve the quality of grid current, the inverter is connected to the grid through various filters, such as L, LC and LCL filters [5]. The L filter has the simplest structure and high reliability but only −20 dB/dec attenuation. As a result, using an L filter, a high switching frequency is needed by the inverter, or the inductance must have a large value to comply with grid standards such as IEEE929-2000 and IEEE 519 [6,7]. It is not helpful for improving system efficiency and power density [8,9]. The LC filter is used to increase the harmonic attenuation which has −40 dB/dec attenuation rate, but it is not usually used in GCIs, because the resonance frequency varies with the change in the grid inductance. Compared with the previous two, the LCL filter is advantageous with

a harmonic attenuation rate of −60 dB/dec [10]. Therefore, the LCL filter is an attractive solution in practical applications.

In [11], an algorithm for LCL filter design was implemented by analyzing the interrelationships between parameters. Nevertheless, various constraints must be considered to calculate the range of each parameter, such as the reactive power, grid-connected current harmonics, and inductor current ripple [12–14]. Inevitably, the design of the three-order LCL filter is extremely complex. It is worth noting that, even if the LCL filter is designed with various constraints, there are stability problems in the GCI due to the inherent resonance phenomenon of the LCL filter [15–17]. Generally, active damping solutions are used to suppress the resonance of the LCL filter, which only change the control loops without damping resistance. In [18], a filter-based damping method was proposed to prevent the resonance without additional sensors. Nevertheless, the variation in LCL filter resonance frequency had a significant influence on the stability. To increase the robustness, an additional state variable could be fed back. However, the digital control delay is generated by algorithm execution, which affects the characteristics of the virtual resistor. In addition, for high-power voltage source inverters (VSIs) with a low switching frequency, the ratio of switching to fundamental frequency is generally small [19,20]. To improve stability, the crossover frequency of the filters was supposed to be much lower than the switching harmonics, but higher than the current control bandwidth [14,21–23]. It brings great challenges for the design of LCL filters [24].

To solve the above-mentioned problems, a novel single-phase inverter was proposed in [25–27], which included two converters operating at different switching frequencies. One converter operated at low pulse ratio to inject current into the grid, while the other converter eliminated the grid current ripple with a high pulse ratio, using the feedforward compensation method. Thus, compared to the LCL inverter, the proposed inverter was highly robust concerning changes in grid impedance and grid voltage harmonics without the need for high current sampling accuracy. Furthermore, the power loss generated by the converter operating at a low switching frequency was significantly reduced. Accordingly, the efficiency of the inverter near the rated power was improved. However, the above research was aimed at single-phase GCI. Since three-phase systems have lower current per phase and lower hardware requirements than single-phase systems at the same power level, in high-power applications, three-phase GCIs are more appropriate. It is expected that the idea of the dual-frequency inverter is more suitable for the application of a three-phase inverter due to its lower switching losses.

In this paper, the topology of the three-phase GCI is proposed, the harmonic elimination principle is analyzed, and the control scheme based on feedforward compensation is proposed. In addition, the inverter parameter design method is proposed, including the inductance of the power inverter unit (PIU), the dc-link voltage of the auxiliary harmonic elimination unit (AHEU) and the inductance of the AHEU. The main contributions of this paper are given as follows:

1. The feedforward compensation method is used to control the AHEU to generate the output current which is symmetric with the current ripple of the PIU. Compared with an active power filter, it avoids extracting harmonics as current reference, which reduces the requirements for sampling accuracy and current control bandwidth.
2. A parameter design method for switching frequency and filter inductance is proposed considering system efficiency, and the influence of switching frequency and inductance changes on power loss is discussed. The experimental results verify that the proposed inverter has a significant improvement in efficiency.
3. A three-phase dual-frequency GCI topology is presented which consists of PIU and AHEU. The PIU operates at a low pulse ratio to reduce the switching loss, and electric energy is transmitted to the power grid by PIU. The AHEU operates at high switching frequency to improve power quality. Furthermore, the stability of the system under a weak grid is analyzed; the proposed inverter can address the stability issue of the LCL filter in low pulse-ratio VSIs with high power in weak grid.

The remainder of the paper is organized as follows. The topology and harmonic elimination principle is introduced in Section 2. In Section 3, a detailed introduction is given to the design method of the proposed inverter parameters. In Section 4, the analysis of stability under weak grid conditions is presented. In Section 5, the control scheme of the PIU and AHEU is presented, based on feedforward compensation. Section 6 presents the experiment and simulation results and verifies the effectiveness of the theory and prototype. In the final section, the conclusion is given.

2. Proposed Inverter's Topology and Principle of Operation

2.1. Proposed Topology

As shown in Figure 1, the main circuit topology of the proposed inverter is presented, which consists of a PIU and an AHEU. Here, V_{dc1} and V_{dc2} are the dc-links of the PIU and AHEU, v_{gn} is the grid voltage of phase n, $n = a, b, c$. The filters of PIU and AHEU are L_{Pn} and L_{An}, respectively. To reduce the switching loss and improve the inverter efficiency, the switching frequency of the PIU is relatively low, injecting current into the grid. The AHEU generates the output current which is symmetric with the current ripple of the PIU. In addition, it operates at high switching frequency; hence, its current ripple is very low. As shown in Figure 1, the grid current is the sum of the AHEU current i_{An} and the PIU current i_{Pn} in each phase. So, the grid current does not include the current ripple generated by the PIU current, which guarantees the quality of the grid current.

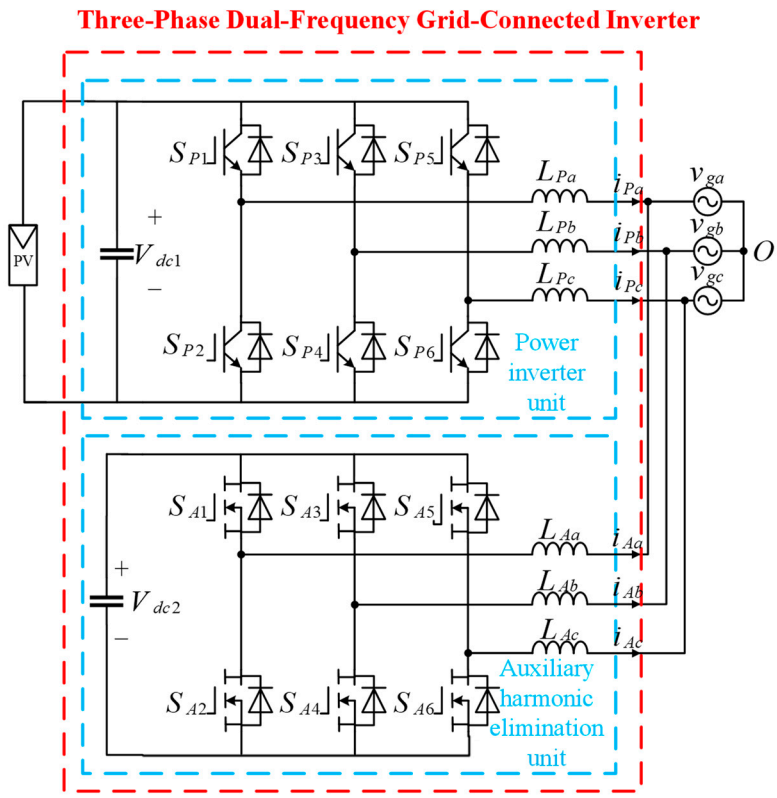


Figure 1. Proposed three-phase dual-frequency grid-connected inverter (GCI) topology.

Since the operating current of the AHEU is relatively low, the cost of switching elements and inductors is much lower than that of the PIU. Moreover, the proposed inverter does not primarily rely on filters to suppress ripple, indicating the total inductance can be reduced. Although the output voltage of the power inverter unit is used in the control loop of the AHEU, it can be estimated by drive signals without an additional voltage sampling circuit. The topology of the proposed inverter is similar to an active power filter [28]; thus, there has not been a significant increase in hardware costs, compared with existing

solutions. In addition, for the proposed inverter, extracting harmonics as current reference is avoided, which reduces the requirements for sampling accuracy. Therefore, although more devices are used in the proposed inverter, the cost will not significantly increase.

If the common dc-link is shared by the PIU and the AHEU, the circulating current is generated due to the differences in the two units of the switching frequency and other parameters [29]. The circulating current can increase power loss, distort the harmonics of the output current and reduce the useful life of inverters [30,31]. According to [30], circulating current problems are more severe in space-vector modulation-controlled inverters. However, the circulating current is blocked with an isolated dc-link for the proposed inverter, so there is no circulating current with the traditional space-vector modulation. In order to maintain the dc-link voltage of the AHEU V_{dc2}, the voltage loop is used in the control strategy.

L filters are used in the proposed inverter, as shown in Figure 1. Compared with an LCL filter, there is no inherent filter resonance for an L filter. As a result, the system stability is greatly enhanced. Additionally, the system parameter design and the current control strategy can be simplified significantly.

2.2. Proposed Inverter's Principle of Harmonic Elimination

In Figure 2, for the proposed inverter, neglecting the series resistances, the voltages $\boldsymbol{u}_P$ and $\boldsymbol{u}_A$ can be expressed as

$$\boldsymbol{u}_P = \boldsymbol{u}_{PL} + \boldsymbol{v}_G \tag{1}$$

$$\boldsymbol{u}_A = \boldsymbol{u}_{AL} + \boldsymbol{v}_G \tag{2}$$

where $\boldsymbol{u}_P = \begin{bmatrix} u_{Pa} & u_{Pb} & u_{Pc} \end{bmatrix}^T$ and $\boldsymbol{u}_A = \begin{bmatrix} u_{Aa} & u_{Ab} & u_{Ac} \end{bmatrix}^T$ are the output voltages of PIU and AHEU, $\boldsymbol{u}_{PL} = \begin{bmatrix} u_{PLa} & u_{PLb} & u_{PLc} \end{bmatrix}^T$ and $\boldsymbol{u}_{AL} = \begin{bmatrix} u_{ALa} & u_{ALb} & u_{ALc} \end{bmatrix}^T$ are the voltages across the L_P and L_A, $\boldsymbol{v}_g = \begin{bmatrix} v_{ga} & v_{gb} & v_{gc} \end{bmatrix}^T$ are the grid voltages. The grid currents can be expressed as

$$\boldsymbol{i}_g = \boldsymbol{i}_P + \boldsymbol{i}_A \tag{3}$$

where $\boldsymbol{i}_g = \begin{bmatrix} i_{ga} & i_{gb} & i_{gc} \end{bmatrix}^T$, $\boldsymbol{i}_P = \begin{bmatrix} i_{Pa} & i_{Pb} & i_{Pc} \end{bmatrix}^T$ and $\boldsymbol{i}_A = \begin{bmatrix} i_{Aa} & i_{Ab} & i_{Ac} \end{bmatrix}^T$ are the output currents of inverter in PIU and AHEU, respectively.

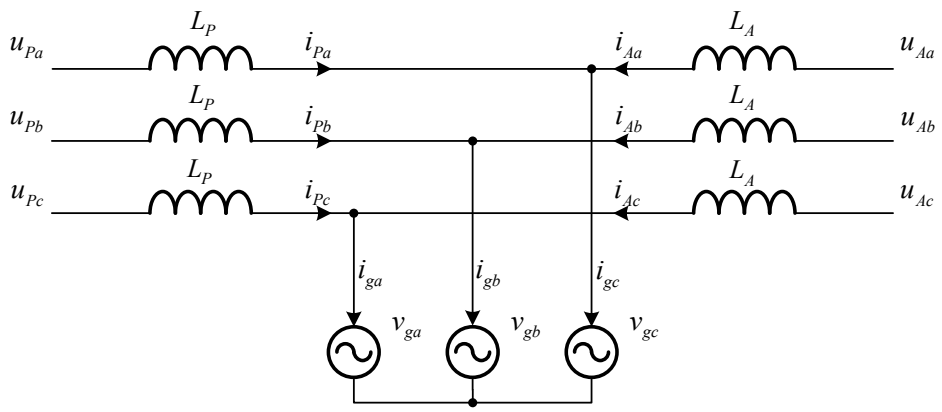


Figure 2. Equivalent circuit of the three phase dual-frequency GCI.

Since the PIU operates at a low pulse ratio, the output currents $\boldsymbol{i}_P$ contain obvious current ripples. Then, $\boldsymbol{i}_P$ can be resolved into fundamental component $\boldsymbol{i}_{Pf}$ and current ripple component $\boldsymbol{i}_{Ps}$, so $\boldsymbol{i}_P$ can be expressed as

$$\boldsymbol{i}_P = \boldsymbol{i}_{Pf} + \boldsymbol{i}_{Ps} \tag{4}$$

Similarly, $\boldsymbol{u}_{PL}$ can be resolved into fundamental component $\boldsymbol{u}_{Pf}$ and switching harmonic component $\boldsymbol{u}_{Ps}$, i.e.,

$$\boldsymbol{u}_{PL} = \boldsymbol{u}_{Pf} + \boldsymbol{u}_{Ps} \tag{5}$$

In the steady state, $\boldsymbol{i}_{Pf}$ can be expressed as

$$\boldsymbol{i}_{Pf} = \frac{1}{L_P}\int \boldsymbol{u}_{Pf}dt \tag{6}$$

Correspondingly, $\boldsymbol{i}_{Ps}$ can be derived using (1), (4), (5) and (6), as follows

$$\boldsymbol{i}_{Ps} = \frac{1}{L_P}\int \boldsymbol{u}_{Ps}dt = \frac{1}{L_P}\int \boldsymbol{u}_P - \boldsymbol{v}_g - L_P\frac{d\boldsymbol{i}_{Pf}}{dt}dt \tag{7}$$

Then, from (3) and (7), the expression of grid current $\boldsymbol{i}_g$ can be obtained as

$$\boldsymbol{i}_g = \boldsymbol{i}_{Pf} + \boldsymbol{i}_A + \frac{1}{L_P}\int \boldsymbol{u}_P - \boldsymbol{v}_g - L_P\frac{d\boldsymbol{i}_{Pf}}{dt}dt \tag{8}$$

Since the switching frequency of the AHEU is far above than that of the PIU, the influence of high-frequency voltage harmonics on the output currents of the proposed inverter can be ignored.

To suppress current ripple, the ripple compensation voltage $\boldsymbol{u}_E$ is designed as

$$\boldsymbol{u}_E = -\frac{L_A}{L_P}\left(\boldsymbol{u}_P - \boldsymbol{v}_g - L_P\frac{d\boldsymbol{i}_{Pf}}{dt}\right) + \boldsymbol{v}_g \tag{9}$$

From Figure 2, the $\boldsymbol{i}_A$ can be expressed as

$$\boldsymbol{i}_A = \frac{1}{L_A}\int \boldsymbol{u}_E - \boldsymbol{v}_g dt \tag{10}$$

Substitute (10) and (9) into (8), the grid current $\boldsymbol{i}_g$ is

$$\boldsymbol{i}_g = \boldsymbol{i}_{Pf} \tag{11}$$

From (11), the current ripple component in $\boldsymbol{i}_{Ps}$ is completely eliminated by $\boldsymbol{i}_A$. Obviously, the resonance phenomenon of the LCL-type GCI can be eliminated by the proposed inverter. In consequence, the system stability can be improved, and the control algorithm is simplified significantly.

3. Proposed Inverter's Parameter Design

3.1. Design of the PIU Filter Inductance L_P

Due to low switching frequency of the PIU, its current ripple is significant compared with rated current. When the current ripple increases, it leads to an increase in the switching stress of the power semiconductor devices and the inductor loss, which can reduce the efficiency of the inverter [32]. Accordingly, it is essential to limit the current ripple. In general, the current ripple is limited to no more than 20% of the grid current amplitude I_{gm}. However, the amplitude of the current ripple is subjected to the filter inductance of the PIU. Therefore, the lower limit of the filter inductance L_P can be determined as follows

$$L_P = \frac{V_{dc1}}{20\% \times 4\sqrt{3}I_{g\_peak}f_P} \tag{12}$$

where the f_P is the switching frequency of the PIU.

3.2. Design of the AHEU Filter Inductance L_A

The series resistances of the filter inductor L_A can be neglected. For the AHEU, the transfer function from iA to $\boldsymbol{u}_A$ is given as

$$\frac{\boldsymbol{i}_A(s)}{\boldsymbol{u}_A(s)} = \frac{1}{L_A s} \tag{13}$$

In this paper, the magnitude of $1/(L_A\mathrm{S})$ <−50 dB at the switching frequency of the AHEU must be satisfied. Consequently, LA can be obtained as

$$L_A = \frac{10^{2.5}}{2\pi f_A} \tag{14}$$

3.3. Design of the DC-Link Voltage of the AHEU

In order that the current ripple can be eliminated by the output current of the AHEU completely, the dc-side voltage V_{dc2} of the AHEU should be larger than a certain voltage. In this paper, V_{dc2} is maintained at its reference $V_{dc2}{}^*$ by the voltage control loop.

$\boldsymbol{v}_g$ and $\boldsymbol{i}_g$ can be expressed as

$$\boldsymbol{v}_g = \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = \begin{bmatrix} V_{gm}\cos\omega_g t \\ V_{gm}\cos(\omega_g t + \frac{2\pi}{3}) \\ V_{gm}\cos(\omega_g t + \frac{4\pi}{3}) \end{bmatrix} \tag{15}$$

$$\boldsymbol{i}_g = \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} = \begin{bmatrix} I_{gm}\cos\omega_g t \\ I_{gm}\cos(\omega_g t + \frac{2\pi}{3}) \\ I_{gm}\cos(\omega_g t + \frac{4\pi}{3}) \end{bmatrix} \tag{16}$$

where V_{gm} and I_{gm} are the grid voltage and current amplitude, respectively, ω_g is the angular frequency of the grid. According to (9) and (11), the ripple compensation voltage $\boldsymbol{u}_E$ can be expressed as

$$\boldsymbol{u}_E = \begin{bmatrix} V_m\cos(\omega_g t + \varphi) - \frac{L_A}{L_P}u_{Pa} \\ V_m\cos\left(\omega_g t + \frac{2\pi}{3} + \varphi\right) - \frac{L_A}{L_P}u_{Pb} \\ V_m\cos\left(\omega_g t + \frac{4\pi}{3} + \varphi\right) - \frac{L_A}{L_P}u_{Pc} \end{bmatrix} \tag{17}$$

where

$$V_m = \sqrt{\left[(1 + L_A/L_P)V_{gm}\right]^2 + \left(L_A\omega_g I_{gm}\right)^2} \tag{18}$$

$$\varphi = \tan^{-1}\frac{L_A\omega_g I_{gm}}{(1 + L_A/L_P)V_{gm}} \tag{19}$$

Considering the different switch states of the PIU, the peak value of $\boldsymbol{u}_E$ can be expressed as

$$u_{Em} \le V_m + \frac{2L_A}{3L_P}V_{dc1} \tag{20}$$

According to the space vector pulse width modulation (SVPWM) technique, the dc-link voltage of the AHEU V_{dc2} should satisfy

$$V_{dc2}^* \ge \sqrt{3}u_{Em} \tag{21}$$

3.4. Design of the Switching Frequency

The switching frequency of the two units is selected by combining the power loss and dead time of the inverter. The switching loss of the power electronic devices is increased with increasing the switching frequency, but the inductance of the filter decreases correspondingly with increasing the switching frequency, which may reduce the power loss on the inductance. Therefore, it is necessary to comprehensively consider the impact of switching frequency on switch loss and filter loss.

In Figure 3, the power loss at different switching frequencies of the PIU when the switching frequency of AHEU f_A is 60 kHz is shown. It can be seen that the power loss of the system is the lowest at about 6 kHz. However, the switching frequency of the GCI is usually set below 3 kHz in high-power applications. In order to simulate a high-power GCI and analyze the stability under low switching frequency, combined with the loss analysis results, a switching frequency of the PIU f_P of 2.5 kHz was chosen in this paper.

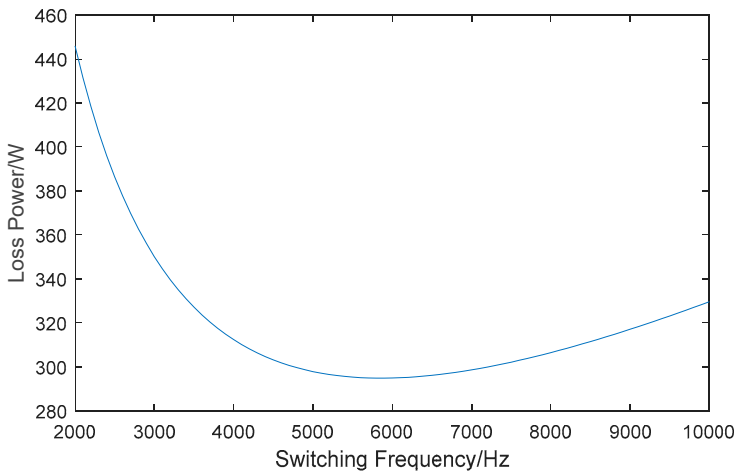


Figure 3. System loss curve at different switching frequencies of PIU when f_A = 60 kHz and grid current is 21 A.

Figure 4 shows the loss curve of the system at different switching frequencies of AHEU when the f_P was 2.5 kHz. From Figure 4, it can be seen that the change in f_A had no significant impact on the system loss, because the output currents of the AHEU were small. With increasing the f_A, the loss of the system was gradually decreased. When the switching frequency was higher than 60 kHz, the total loss of system hardly changed. Considering the dead time effect of the power switching device, the f_A is 60 kHz.

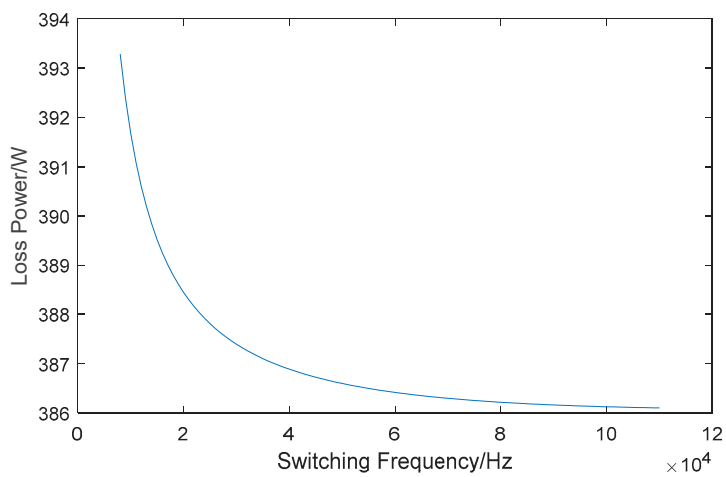


Figure 4. System loss curve at different switching frequencies of AHEU when f_P = 2.5 kHz and grid current is 21 A.

4. Stability Analysis of Proposed Inverter

The current control block diagram of the PIU is shown in Figure 5. From Figure 5, i_{Pref} is the current reference. $G_{IP}(s)$ is the current controller. The Δi_P is the error between i_{Pref} and i_P. $G_{DP}(s)$ is the system delay. K_{PWM} is the gain of the inverter, which is equal to $V_{dc1}/\sqrt{3}$, $G_{FP}(s)$ is the grid voltage feedforward coefficient, which is equal to $1/K_{PWM}$. Z_g is the grid impedance. u_{PCC} is the voltage at the point of common coupling (PCC). The grid equivalent resistance can provide certain damping, which can improve the stability of the system. In order to discuss the most unstable conditions, only the influence of the grid inductance L_g is considered here; that is, $Z_g = L_g s$.

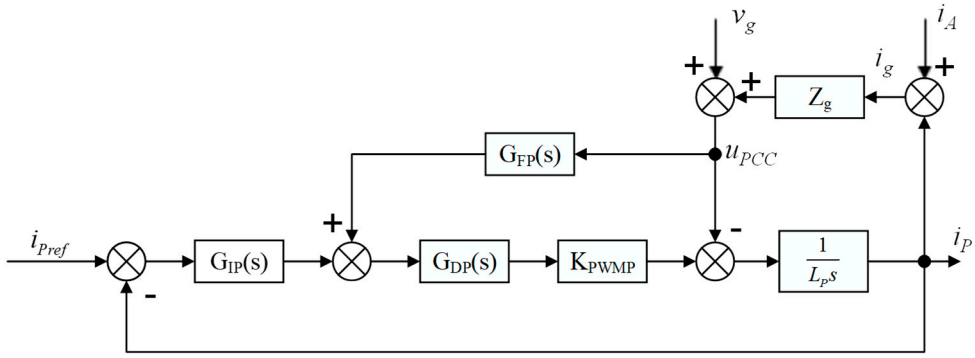


Figure 5. Current control block diagram of PIU.

The open-loop transfer function in Figure 5 from Δi_P to i_P can be expressed as

$$G_{\Delta iP\_iP}(s) = \frac{K_{PWMP}G_{DP}(s)G_{IP}(s)}{L_P s + Z_g - K_{PWMP}Z_g G_{DP}(s)G_{FP}(s)} \tag{22}$$

The Bode plots of $G_{\Delta iP\_iP}$ under different grid conditions is shown in Figure 6. When L_g = 0 mH, the PIU operates with an ideal grid, the phase margin (PM) of $G_{\Delta iP\_iP}$ is 51.3°. As L_g increases, the PM of $G_{\Delta iP\_iP}$ decreases slightly. When L_g = 1 mH, the PM of $G_{\Delta iP\_iP}$ is 47.1°, and when L_g = 2 mH, the PM of $G_{\Delta iP\_iP}$ is 43.6°, indicating the PIU has good stability under weak grid conditions.

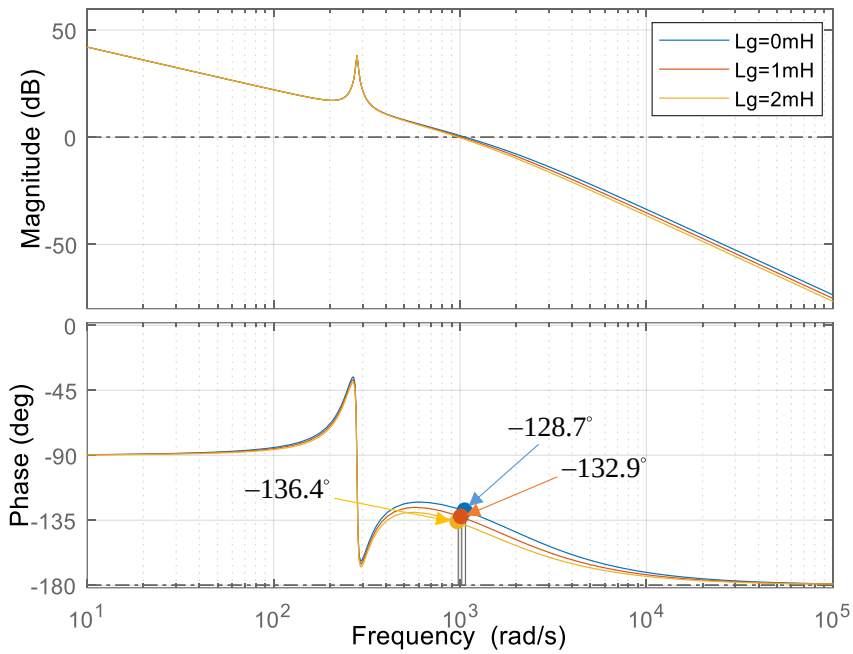


Figure 6. Bode plots of $G_{\Delta iP\_iP}$ under different grid conditions.

The current control block diagram of AHEU is the same as the PIU; the open-loop transfer function of the AHEU from Δi_A to i_A can be expressed as

$$G_{\Delta iA\_iA}(s) = \frac{K_{PWMA} G_{DA}(s) G_{IA}(s)}{L_A s + Z_g - K_{PWMA} Z_g G_{DA}(s) G_{FA}(s)} \tag{23}$$

The Bode plots of $G_{\Delta iA\_iA}$ under different grid conditions is shown in Figure 7. When L_g = 0 mH, the PM of $G_{\Delta iA\_iA}$ is 78.6°. When L_g = 1 mH, the PM is 67.5°, and when L_g = 2 mH, the PM is 59.2°. According to Figures 6 and 7, the proposed inverter improved the stability.

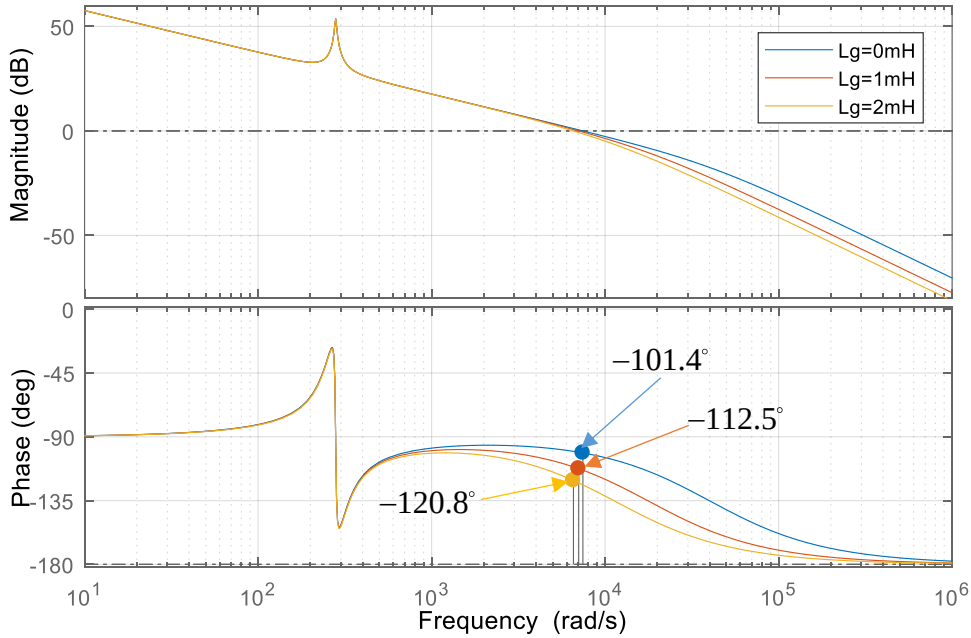


Figure 7. Bode plots of $G_{\Delta iA\_iA}$ under different grid conditions.

5. Proposed Inverter's Control Scheme

A reference-frame transformation-based control scheme is used for dual-frequency three-phase GCI as shown in Figure 8. The control structure consists of two independent control loops which are the power control loop and the auxiliary control loop, respectively. The synchronous reference frame phase-locked loop is used to extract the phase angle θ_g of the grid. The SVPWM is used to drive power electronic devices. Although the SVPWM algorithm has large amplitude harmonics near the switching frequency and its doubling frequency [33], the SVPWM method has a higher DC voltage utilization and lower THD [34]. And there is significant flexibility in switching state selection [35]. In this paper, the SVPWM used can suppress the low-order harmonics significantly and decrease the requirement for a dc-link voltage. The lower capacitance of AHEU is available, reducing the system cost.

The power control loop is used to control the output currents $\boldsymbol{i}_P$ to transfer active power to the grid. The output currents $\boldsymbol{i}_P$ are transformed into the dq-reference frame. In Figure 8, i^*_{gd} and i^*_{gq} are the grid current references in the dq-reference frame. In the power control loop, the current references i^*_{gd} and i^*_{gq} are compared with i_{Pd} and i_{Pq}, respectively. The power current controller block consists of two proportional resonant (PR) regulators [36,37]. u_{Pd} and u_{Pq} are the sum of the grid compensation voltages, outputs of the current controller and the coupling components, as shown in Figure 8.

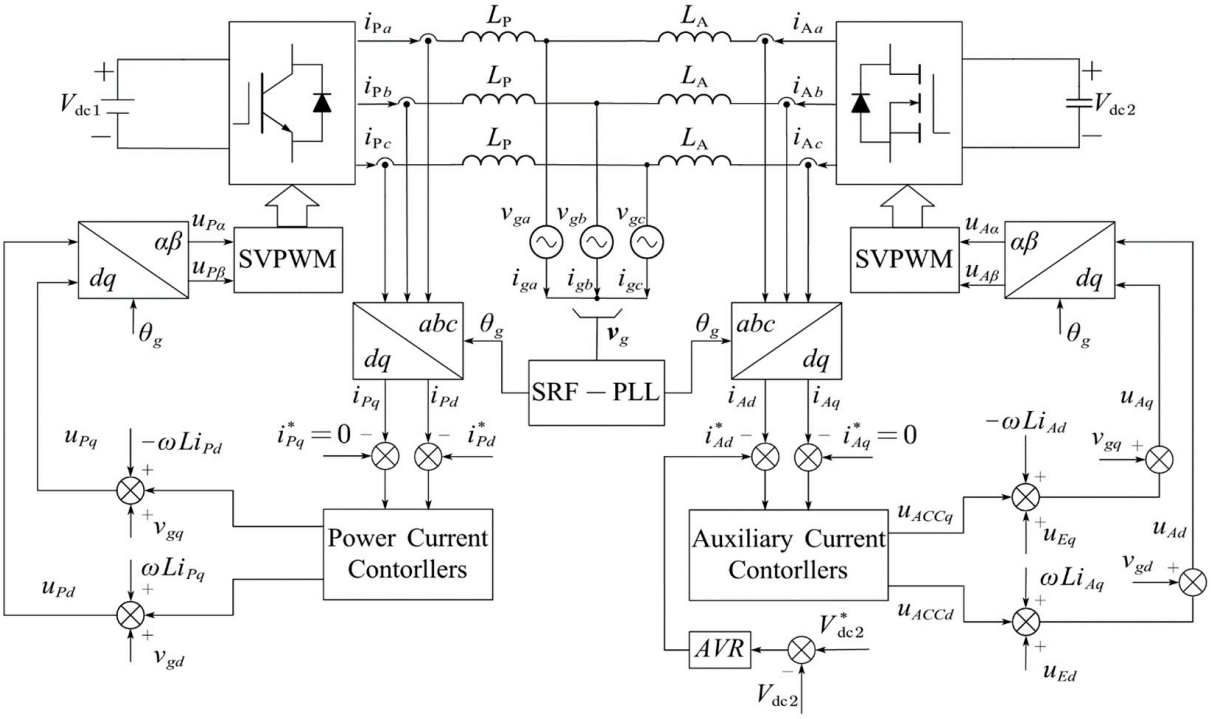


Figure 8. Block diagram of three-phase dual-frequency GCI.

The auxiliary control loop generates $\boldsymbol{i}_A$ to eliminate the current ripple generated by the PIU. Similarly, the auxiliary current controller block consists of two PR regulators. In addition, the dc-link voltage V_{dc2} is controlled by the auxiliary control loop to track its reference V^*_{dc2}. From Figure 8, the output of the voltage regulator AVR is i^*_{Ad} which is compared with i_{Ad}. The q-axis reference current i^*_{Aq} is equal to zero.

It was noted that $\boldsymbol{i}_{Pf}$ can be approximated as $\boldsymbol{i}^*_g$ in steady state. In (9), the differential item $d\boldsymbol{i}_{Pf}/dt$ can be substituted as:

$$\frac{d\boldsymbol{i}_{Pf}}{dt} \approx \begin{bmatrix} -\omega_g I^*_{gm} \sin \omega_g t \\ -\omega_g I^*_{gm} \sin(\omega_g t + \frac{2\pi}{3}) \\ -\omega_g I^*_{gm} \sin(\omega_g t + \frac{4\pi}{3}) \end{bmatrix} \tag{24}$$

where I^*_{gm} is the reference amplitude of the grid current.

According to (9), the ripple compensation voltages $\boldsymbol{u}_E$ can be determined by

$$\boldsymbol{u}_E = -\frac{L_A}{L_P}\left(\hat{\boldsymbol{u}}_P - \boldsymbol{v}_g - L_P \frac{d\boldsymbol{i}^*_g}{dt}\right) + \boldsymbol{v}_g \tag{25}$$

where the $\hat{\boldsymbol{u}}_P$ is the estimation of $\boldsymbol{u}_P$. Since the control scheme of the proposed inverter is realized by one micro controller, the $\hat{\boldsymbol{u}}_P$ can be obtained by the drive signals of the PIU. The modulation signals of auxiliary control loop can be expressed as

$$\begin{aligned} u_{Ad} &= u_{ACCd} + \omega L i_{Aq} + u_{Ed} + v_{gd} \\ u_{Aq} &= u_{ACCq} - \omega L i_{Ad} + u_{Eq} + v_{gq} \end{aligned} \tag{26}$$

where u_{ACCd} and u_{ACCq} are the output of auxiliary current controllers, u_{Ed} and u_{Eq} represent the ripple compensation voltages in dq-reference frame, $\omega L i_{Ad}$, $\omega L i_{Aq}$ and v_{gd} and v_{gq} are coupling components and grid compensation voltages, respectively.

For the above ripple elimination method, it is not necessary to sample the output voltage of the PIU. As a result, the hardware complexity of the control system can be reduced. $\boldsymbol{i}^*_g$ are current references rather than the measured values, thus, the differential item $d\boldsymbol{i}^*_g/dt$ is a dc component which can eliminate the amplification effect of differential items on the measurement of noise. It can improve the inverter performance. Consequently, compared with other methods extracting the harmonics as the reference, the proposed method is not necessary for the requirements of current sampling accuracy, pulse ratio of the PIU or current control bandwidth.

6. Experiment Results

A laboratory prototype of a 10 kW three-phase dual-frequency GCI was developed to verify the performance of the proposed inverter. The laboratory prototype is shown in Figure 9. The IGBTs (IKW40N120T2) and the SiC-MOSFET (IMW120R220M1H) were used in the PIU and the AHEU respectively. The controller of the proposed inverter is based on a digital controller (STM32F407ZET6) and CPLD (EPM1270T144C5N). The control algorithm shown in Figure 8 was implemented by digital controller, and CPLD was used to generate PWM signals to drive the power electronic devices. According to the modulated signal generated from the ARM, the CPLD generated 12 gate pulses, which were fed to the respective eight switches of the proposed topology. The system parameters are listed in Table 1. The phase grid voltage (RMS) was 220 V, and the grid frequency was 50 Hz.

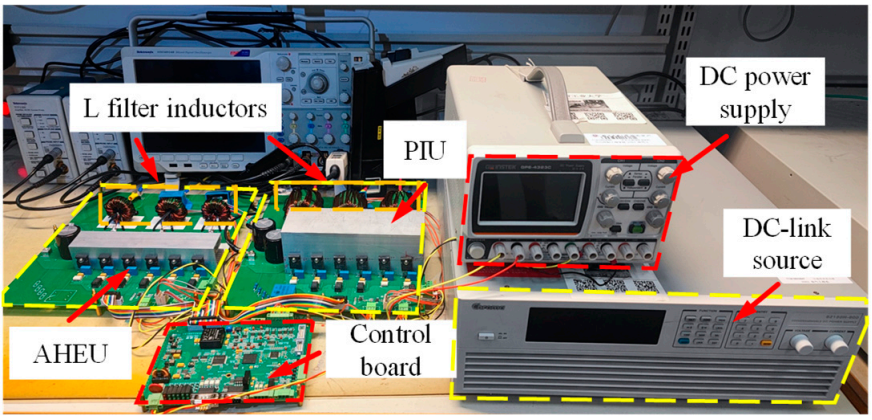


Figure 9. Photograph of the laboratory prototype.

Table 1. Parameters of three-phase dual-frequency GCI.

Parameters	Power Inverter Unit (PIU)	Auxiliary Harmonic Elimination Unit (AHEU)
Switching frequency	2.5 kHz	60 kHz
Dc-link voltage	700 V	700 V
Filter inductance	4.8 mH	0.8 mH
Output power	10 kW	-

6.1. Suppression Effect of Current Ripple

The simulation results of the PIU output currents i_P, grid currents i_g and phase-a AHEU output current i_{Aa} are shown in Figure 10a,b,c, respectively. Figure 11 shows the FFT analysis of the output current of the PIU and the grid current. From Figure 10a, it can be observed that the output current ripple by the PIU was large, especially at the zero crossing. The THDs of i_{Pa} was 12.18%, and did not satisfy the grid standards, as shown in Figure 11. The peak-to-peak values of the AHEU output current in Figure 10b were relatively large near 0.205 s and 0.215 s, corresponding to the zero crossing of the phase-a PIU output current i_{Pa}. It indicates that the power quality was improved by the AEHU output current, according to the amplitude of the ripple component. It can be seen that

the current ripple was suppressed effectively compared with i_P, as shown in Figure 10c, particularly at the zero crossing. The improvement effect of the grid current could also be proven, as shown in Figure 11. The THD of i_{ga} was 3.91%, satisfying grid standards.

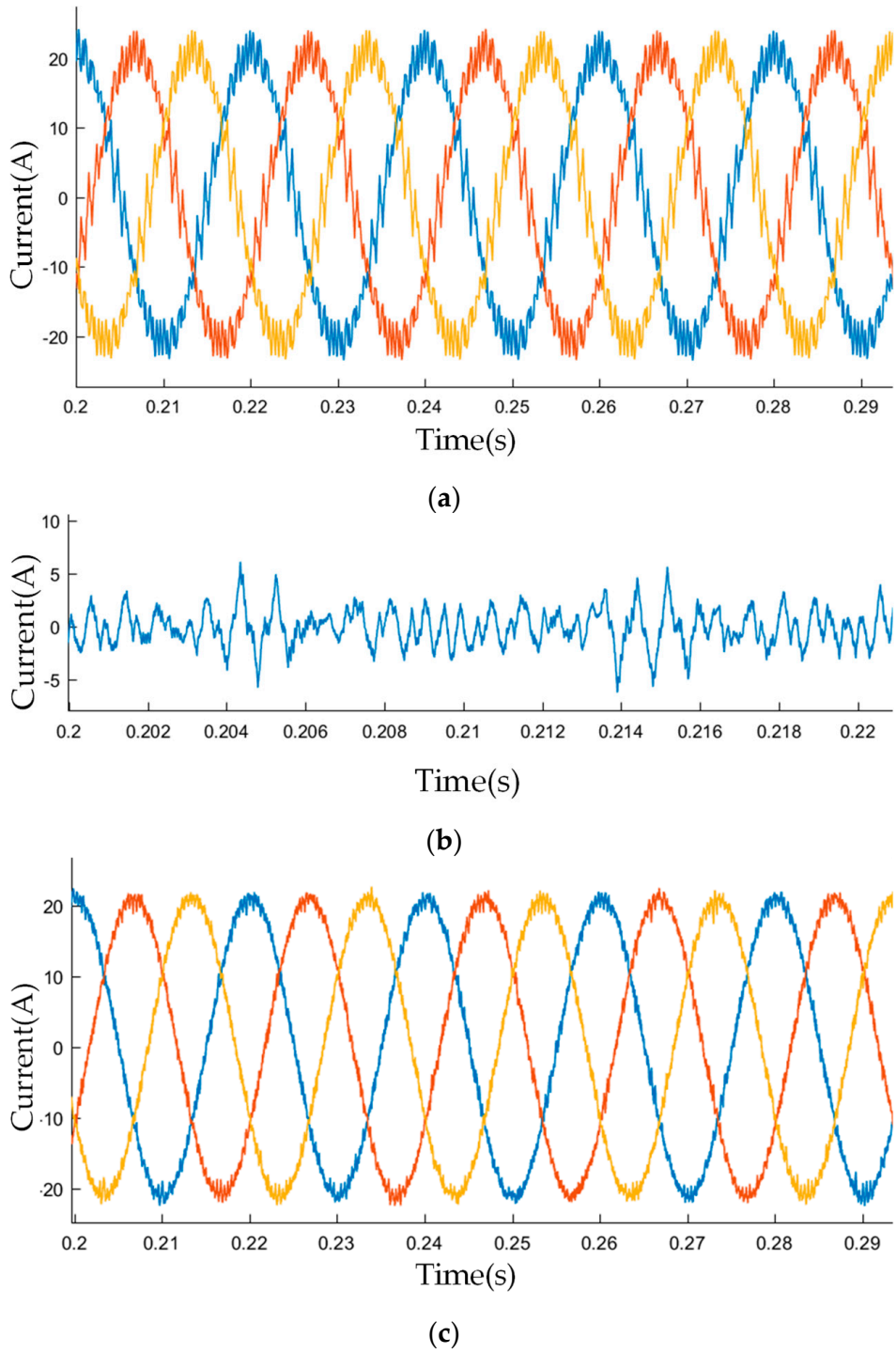


Figure 10. The simulation of proposed inverter output currents. (**a**) PIU output currents i_P, (**b**) grid currents i_g, (**c**) phase-a AHEU output current i_{Aa}.

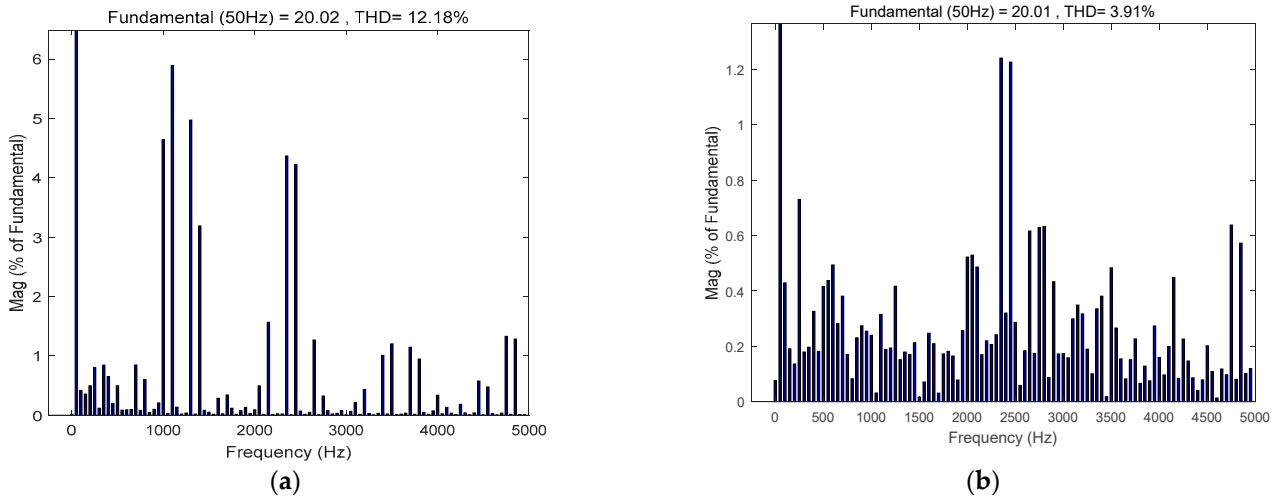


Figure 11. FFT analysis of the output current of PIU and grid current. (**a**) FFT of i_{Pa}; (**b**) FFT of i_{ga}.

The PIU output currents $\boldsymbol{i}_P$, AHEU output currents $\boldsymbol{i}_A$ and grid currents $\boldsymbol{i}_g$, are shown in Figure 12a,b,c,d, respectively. In Figure 12a, the RMS value of $\boldsymbol{i}_P$ was about 15 A. The current ripples in the output currents of the PIU were significant. The three phase output currents of AHEU $\boldsymbol{i}_A$ are shown in Figure 12b. The average value of $\boldsymbol{i}_A$ was approximately 0, indicating that the power consumed by the AHEU is very small. Figure 12c shows the three phase grid currents $\boldsymbol{i}_g$. In Figure 12d, it can be observed that i_{Aa} was opposite to i_{Pa}. As a consequence, compared with $\boldsymbol{i}_P$, the current ripples of $\boldsymbol{i}_g$ were reduced significantly. Meanwhile, the peak value of i_{Aa} was about 2 A, indicating that it was far less than the rated current. This shows that the conduction loss and cost of the AHEU are much lower than the PIU.

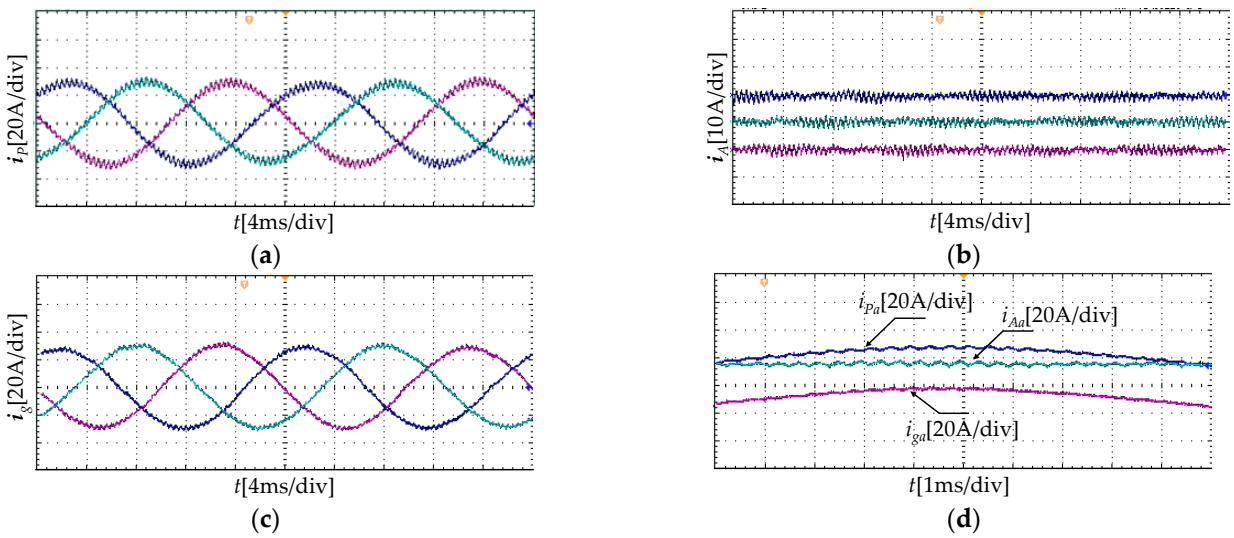


Figure 12. Output currents of the proposed inverter. (**a**) Three-phase PIU output currents; (**b**) three-phase AHEU output currents; (**c**) three-phase grid currents; (**d**) zoomed-in view of i_{Pa}, i_{Aa}, and i_{ga}.

The FFT analysis of i_{Pa} and i_{ga} are shown in Figure 13. The THDs of i_{Pa} and i_{ga} were 7.33 and 3.01%, respectively. Compared to i_{Pa}, the THD of i_{ga} was significantly reduced, less than 5%, complying with grid standards.

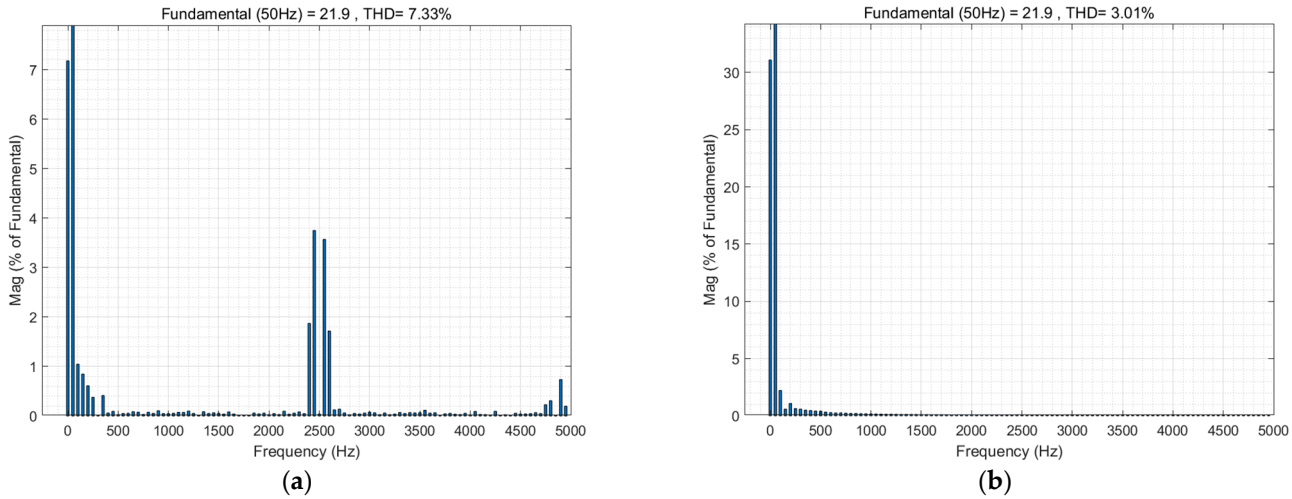


Figure 13. FFT analysis of the output current of PIU and grid-connected current. (**a**) FFT of i_{Pa}; (**b**) FFT of i_{ga}.

From Figure 13, the harmonics around the switching frequency f_P were reduced from about 3.7 to 0%. Furthermore, the harmonics around the integral multiple of the switching frequency f_A could also be eliminated by the AHEU. The fundamental component of i_{Pa} was same as that of i_{ga}. This means that the active power is transmitted to the grid by the PIU.

6.2. Performance of the Proposed Inverter under Dynamic Changing Load Conditions

When the grid current reference was changed, the responses of i_{ga}, i_{Aa} and i_{Pa} are shown in Figure 14. From Figure 14, it can be seen that when the grid current reference changed, i_{Pa} responded quickly, without a large current overshoot and oscillation, and tracked the current reference value again within three cycles. Compared with i_{Pa}, i_{ga} had a decrease in ripple content and changed synchronously with i_{Pa} as the grid current reference changed, indicating that the dynamic process had no significant impact on the harmonic suppression effect.

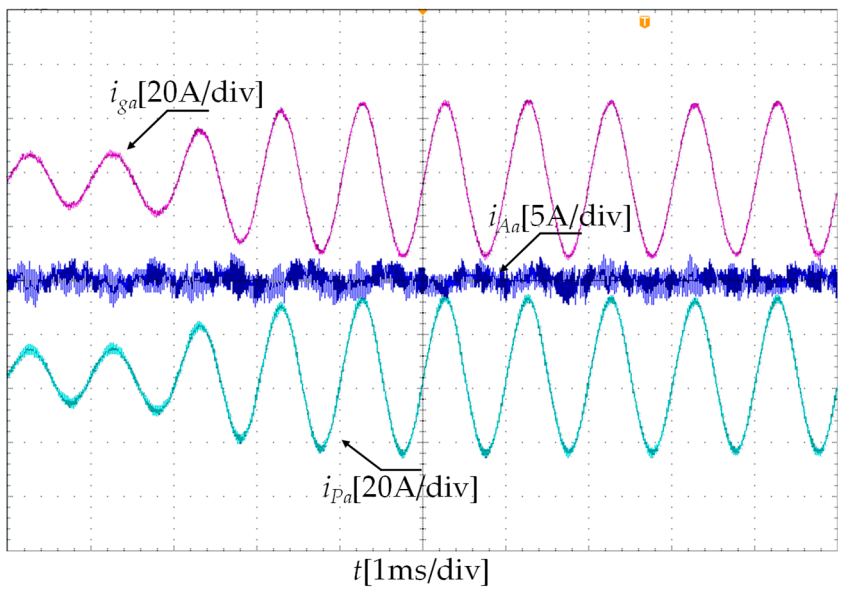


Figure 14. The response of i_{ga}, i_{Aa} and i_{Pa} when grid current reference is changed.

6.3. Performance of the Proposed Inverter under a Weak Grid

To simulate the grid impedance, the inductors were added into the grid, as shown in Figure 15. The inductance of Lg was 2 mH. Figure 16 shows the a-phase u_{PCC} and output currents of the proposed inverter under a weak grid. In Figure 16a, the harmonic component in u_{PCC} was obviously affected by Lg. In Figure 16b, the harmonic component of i_{Pa} was also eliminated effectively by i_{Aa}. The THD of the grid current i_{ga} was 4.83%, lower than 5%, which satisfies the grid standard. The proposed inverter still had good performance and stability under weak grid conditions.

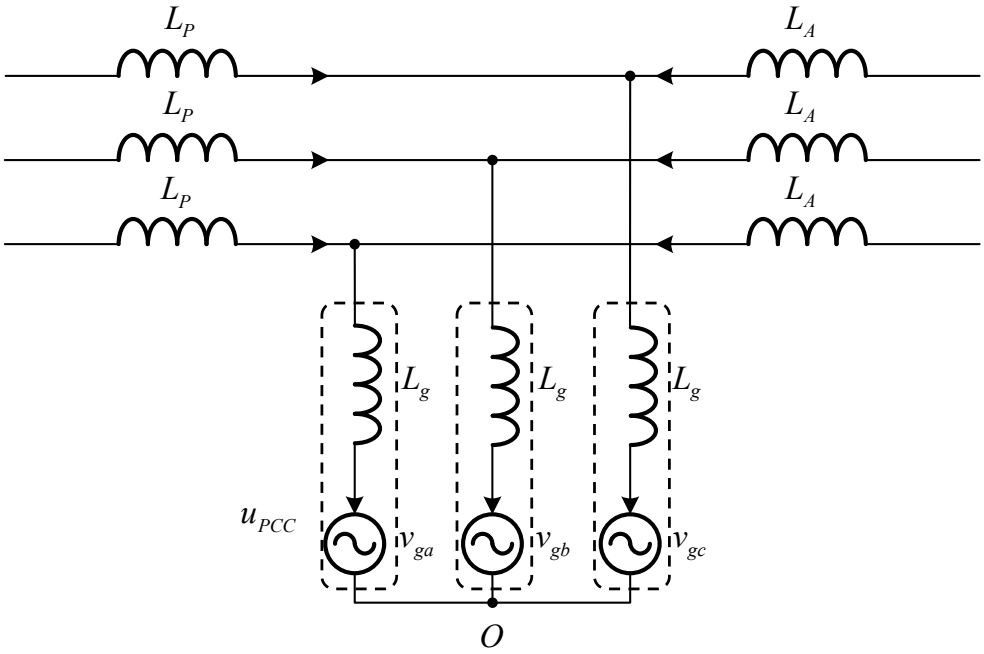
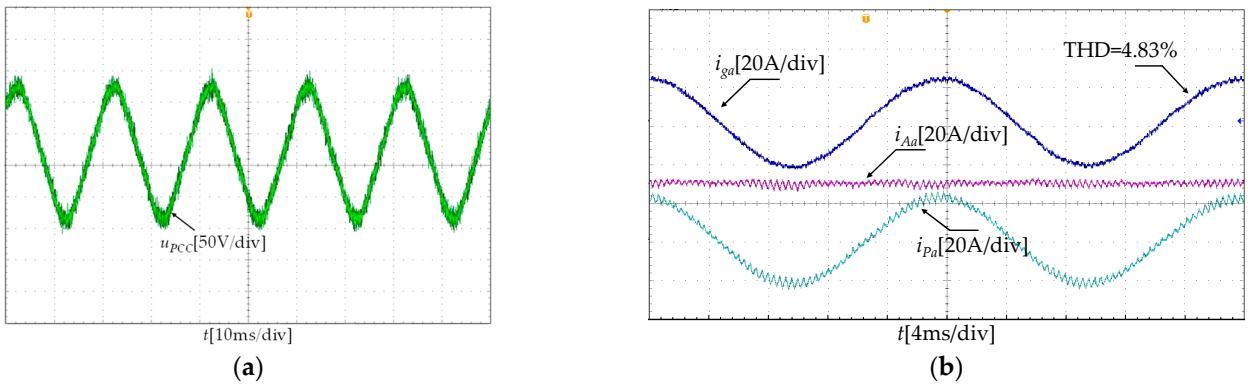


Figure 15. Equivalent circuit under weak grid.



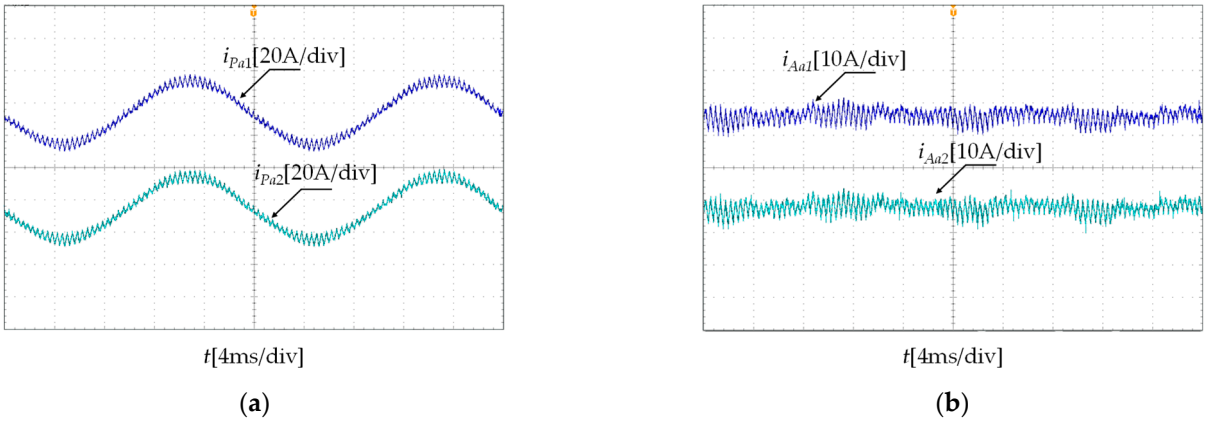
(**a**) (**b**)

Figure 16. The a-phase u_{PCC} and output currents of the proposed inverter under weak grid. (**a**) Waveform of a-phase u_{PCC}; (**b**) waveforms of i_{ga}, i_{Aa} and i_{Pa}.

6.4. Circulating Current Analysis

The circulating current is generated among the parallel inverters owing to the inconsistency of system impedance and the switching action. However, regardless of the switching state of the power electronic devices, the circulating currents need to pass through a common dc-link to form a circulating current path, and the two units of the proposed inverter do not share a common dc-link. The experimental results are shown in Figure 17. It can be seen that for the waveforms of the filter inductance currents i_{Pa1}, i_{Pa2}, i_{Aa1} and i_{Aa2}, as

shown in Figure 17a,b, that i_{Pa1} is equal to i_{Pa2}, and i_{Aa1} is equal to i_{Aa2}. This means that the inverter proposed in this paper does not have circulation problems.



(**a**) (**b**)

Figure 17. The waveforms of the filter inductance currents: (**a**) i_{Pa1} and i_{Pa2}, (**b**) i_{Aa1} and i_{Aa1}.

6.5. Efficiency Analysis

The efficiency curves of the three-phase dual-frequency GCI and the traditional GCI are shown in Figure 18, reflecting the efficiency advantages of the three-phase dual-frequency GCI. The switching frequency of the traditional GCI operates at approximately 9 kHz to comply with grid code requirements. To decrease the switching loss, the PIU operates at 2.5 kHz switching frequency. Due to the relatively low switching frequency of the proposed inverter in this paper, when the same switching frequency is used by traditional inverters, such as the PIU, the filter needs to use more inductance to satisfy the grid standards.

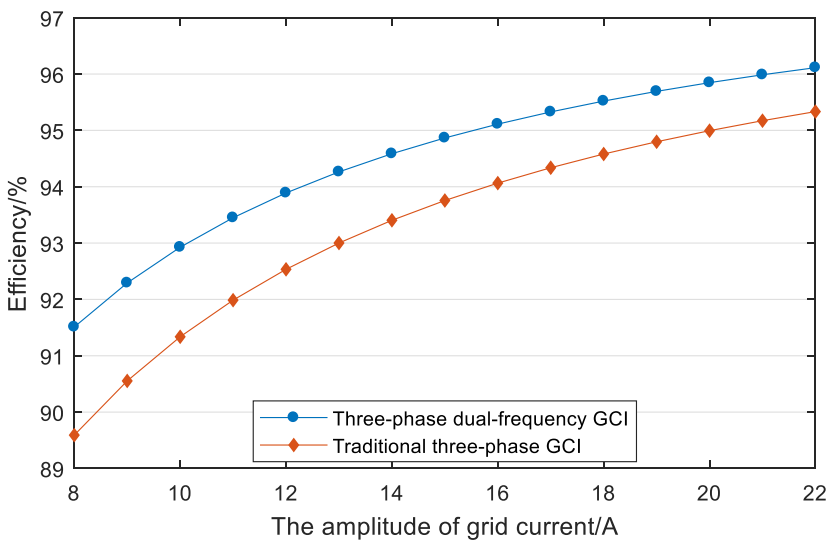


Figure 18. Efficiency of the three-phase dual-frequency GCI and the traditional three phase GCI for different grid current amplitudes.

Figure 18 shows the efficiency curves of the traditional inverter and the proposed inverter at different currents. When the amplitude of the grid current was 21 A (rated current), the efficiency of the three-phase dual-frequency GCI was 95.99%, which is approximately 0.82% higher than the traditional GCI.

According to [38], the power losses of two inverters can be evaluated at rated current, as shown in Table 2. It can be seen that although the traditional inverter reduces switching losses, the power loss generated on the passive filter is too large, resulting in a much greater

power consumption on the filter than on the AHEU. Therefore, under different currents, the efficiency of traditional inverters is lower than that of the proposed inverters.

Table 2. Losses of the proposed GCI and traditional GCI at rated current.

Parameters	Proposed GCI		Traditional GCI
	PIU	AHEU	
Switching loss	59 W	3 W	59 W
Conduction loss	55 W	-	55 W
Copper loss of the inductor	279 W	1 W	383 W
Total power loss	397 W		497 W

7. Conclusions

In this paper, a novel three-phase dual-frequency GCI was proposed. The active power is supplied to the grid by the PIU at a low switching frequency. Based on a simple feedforward compensation method, the AHEU operates at a high switching frequency to eliminate the grid current ripple. The circulating current between the two units can be blocked by isolated dc-links. As the switching frequency of PIU is low, the efficiency of the inverter can be improved. Moreover, the proposed GCI addresses the stability issues arising from the inherent resonance of the LCL filter by using an L filter. The efficiency of the proposed inverter was more than 0.82% higher than the traditional GCI at rated current.

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