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Capacitor Clamped Coupled Inductor Bi-Directional DC-DC Converter with Smooth Starting

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Abstract: In this paper, a new type of capacitor clamped coupled inductor bidirectional DC–DC converter is proposed, which offers high voltage gain with smooth starting current transients, as well as reduced stresses on the capacitor. Steady state operation, mathematical modelling, and state space modelling for the proposed converter are presented in detail. A simplified single voltage clamped circuit is developed to mitigate the voltage spikes caused due to the coupled inductor by recovering the leakage energy effectively. Moreover, the clamping capacitor helps in reducing the ripples in output voltage, which in effect significantly reduces the stress on the switch and offers less ripple content at the load terminals. Simulation of the proposed converter is carried out using Simulink/MATLAB for the conversion of 24V DC to 200V DC. For this conversion, simulation results have proven that there is reduction of 13.64% of capacitor voltage stresses. Further, under line varying conditions, converter responses have proven that there is a 119% and 25.25% reduction in input current and output voltage transients, respectively. Similarly, 25.25% and 76.5% transient reductions of input current are observed for line and control parameter variations. The hardware investigation of the converter was carried out with a 100 W, 24 V/200 V setup. The converter achieved efficiency of 93.8%. The observations supplement the simulation results.

Keywords: bi-directional converter; DC-DC power converter; coupled inductor bi-directional converter; bi-directional power flow

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1. Introduction

In the modern era, the environment is prone to pollution caused due to various aspects, especially vehicles powered by fossil fuels. As the pollution prone system is becoming of greater concern, replacing these vehicles with plug-in electric vehicles (PEV) is becoming an attractive proposition. To take this technology forward to next level of sophistication, one needs to provide not only an optimal charging system, but also the most effective power conditioning unit to drive the motor more effectively. This results in more flexibility for PHEV customers [1–4]. Usually, a bi-directional DC-DC converter (BDC) is associated with the design of charger as well as the power conditioning unit of an EV or PHEV, as shown in Figure 1, as it allows bidirectional power flow (charging and discharging and similarly during motoring and braking periods respectively).

The broad categorization of these BDCs refers to isolated (transformer based) converters and non-isolated (transformer less) converters. Conventional isolated converters are used to meet the high gain requirements of EVs, which provides the flexibility of reduced operating voltages at the battery side in the design of EVs. For this purpose, step-up natured isolated converters, e.g., flyback, push-pull, current-fed half bridge, and current-fed

full bridge topologies, are preferred with the adoption of a suitable transformer turns ratio. However, this solution suffers from large voltage spikes due to the leakage inductance of the transformer, in turn, leading to a power loss in the switch. Thus, non-isolated BDC is preferred when compared with isolated BDC, as it has several advantages, such as high efficiency, more reliability, and less component count, which lead to a reduced size and overall cost [5,6]. In general, high gain is obtained in the case of transformerless converters by having a high duty cycle. However, the price to pay is the increasing reverse recovery losses and reduced efficiency. Moreover, the reliability of the switches is also affected due to high voltage stress because of the high duty ratio. To overcome these issues, ample converter topologies have been proposed in the literature, namely cascading boost converters [7], interleaving topology, soft switching technique to mitigate voltage spikes, and incorporating a coupled inductor in the conventional boost topologies [8].

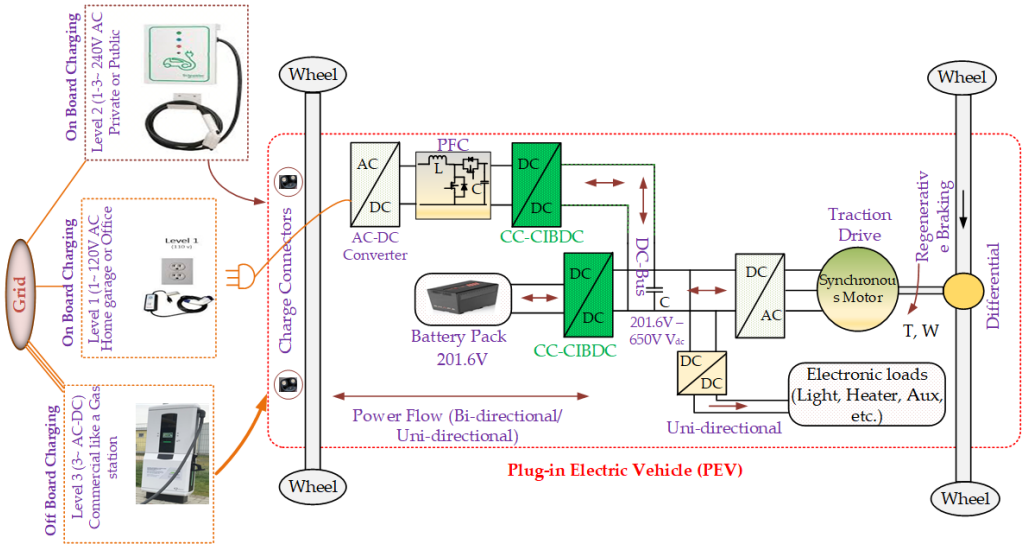


Figure 1. Architecture of a PEV.

Among all, coupled inductor (CI) based topologies have received more attention to achieve high conversion gain due to their merits, such as compactness and high power density in both charging and discharging modes [9,10]. Moreover, such topologies can mitigate the disadvantages of both isolated and non-isolated BDC, such as voltage stresses, high voltage diversity factor with huge duty cycle, and high cost. However, there are still few more problems with CI–BDC converters, such as leakage energy due to the coupled inductor, causing voltage stress during the turn off process, apart from complexity in circuit design. To address this issue, the resistor-capacitor-diode (RCD) voltage-clamp technique is proposed. Apart from that, the Voltage-Clamp (VC)—CI–BDC converter has been proposed in [11]. However, in all these topologies, a capacitor is placed at the output side [12–20]. As the system in energized, the voltage levels increase to the rated value, thus enabling an inrush of current in uncharged output capacitors. The inrush current magnitude flowing inwards to the capacitors is proportional to the rate of change of voltage, as illustrated in Equation (1)

$$I_{inrush} = C_o \frac{dV_o}{dt} \quad (1)$$

where I_{inrush} = inrush current produced by capacitance, C_o = total capacitance, dV_o = change in voltage across the capacitor, and dt = rise time during voltage ramp up.

Two important factors of interest regarding inrush current are noteworthy. Firstly, the inrush current may exceed the rated value of currents in PCB modules, which can affect the power routing, and ultimately the overall system may deteriorate. However, if one designs by considering the maximum value of a large inrush current, the PCB component

sizes will increase. Thus, the overall cost will increase, and resistance of the path will be affected. Secondly, the capacitor at the load side, when added, will cause instability when the capacitor is charged from the supply.

Inrush current minimization has been achieved by using a soft start technique which reduces the duty cycle and thus reduces the capacitor charging, which in turn minimizes the inrush current [21–23]. However, this solution slows down the response, which in turn decreases the system dynamics. On the other hand, the other ways of reducing inrush current are voltage regulation, by the design of a discrete load switch and aggregate load switches [24]. The discrete load switch method requires more components. The aggregate method requires a dc-dc converter to control multiple load switches. In both the cases, the inclusion of a load switch will result in greater ease of design but increase the component count and cost.

From Equation (1), it can be inferred that by minimizing the capacitor voltage, the inrush current can be minimized, which can be used as an alternative solution to the above-mentioned problem. This fact has motivated the derivation of a new converter, which can offer reduced voltage across the capacitor. In this regard, the capacitor clamped boost inverter (CCBI) concept has been found to be a suitable solution [25]. However, this paper does not deal with the inrush concept and bi-directional power flow application in dc-dc power conversion. This knowledge gap has motivated the utilization of the CCBI concept along with the coupled inductor concept to derive a new converter and to carry out its performance investigation in the above-mentioned directions. This newly derived converter has been named the capacitor clamped coupled inductor BDC (CCCI–BDC). All the reviewed dc-dc power converter topologies have been presented as a flowchart in Figure 2.

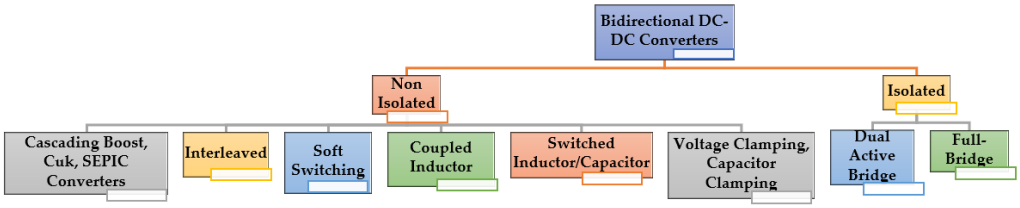


Figure 2. Flowchart of the reviewed topologies.

The organization of the paper is as follows. Section 1 contains the introduction and thorough review of the state-of-the-art technologies. Section 2 entails in-depth mathematical modeling along with various modes of operation and analysis of the proposed CCCI–BDC. The proposed converter performance improvement has been validated using simulation in a Simulink environment and verified through hardware implementation and performance investigation. Section 3 describes simulation results and discussions. Section 4 details experimental results and analysis. Section 5 incorporates the conclusions.

2. Proposed System

The CI–BDC is an improvement over the conventional BDC, designed for high voltage variant applications. The main function of this coupled inductor is to absorb and deliver energy during the converter operating period. The power absorbed and released by the CI is not the same in all durations because of the operating conditions. By using CI, one can make the converter size compact as it uses a single core in place of multiple cores. In the literature concerning CI technology, a single core is treated as a Flyback transformer and the windings of CI behave as magnetic switches used to store and release energy. The conventional converter necessitates two capacitors (one C_{HV} for boost mode and another C_{LV} for buck mode respectively), but the proposed converter uses only one capacitor (C_C) to support both modes of operation [11].

Figure 3 shows the proposed CICC–BDC with single voltage clamping, which is an improvement over the CI–BDC, proposed in [11]. For simple analysis, the CI can be repre-

sented mathematically as an ideal transformer inclusive of magnetizing inductances (L_{m1} and L_{m2}) and leakage inductances (L_{k1} and L_{k2}). The turns ratio and coupling coefficients of the ideal transformer are given by

$$N = \frac{n_1}{n_2} \tag{2}$$

$$k_1 = \frac{L_{m1}}{L_{m1} + L_{k1}} = \frac{L_{m1}}{L_1} \text{ and } k_2 = \frac{L_{m2}}{L_{m2} + L_{k2}} = \frac{L_{m2}}{L_2} \tag{3}$$

where n_1 and n_2 are the number of inductor turns of L_1 and L_2, respectively, while k_1 and k_2 are the coupling coefficients of the inductors L_1 and L_2, respectively, which are set to 1 to equalize $L_{m1} = L_1$ and $L_{m2} = L_2$. In discharging (boost) mode, L_1 is more effective, and in charging (buck) mode both L_1 and L_2 are more effective. Assume that the coefficient of coupling is 1. Then, the mutual inductance $M = k\sqrt{L_1 L_2} = NL_1$. As a result, both L_1 and L_2 can be treated as single winding. Thus, the equalizing magnetizing inductance is given by

$$L_m = (L_1 + L_2 + 2M) = (1 + N)^2 L_1 = \left(1 + \frac{1}{N}\right)^2 L_2 \tag{4}$$

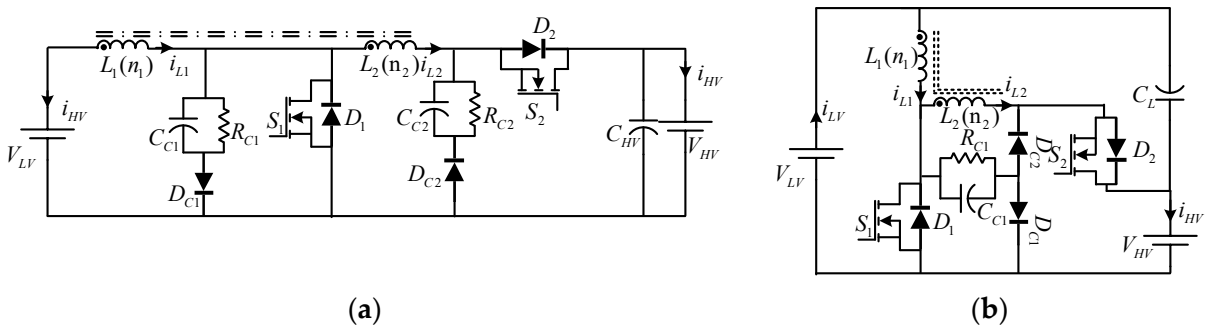


Figure 3. (**a**) Conventional CI-BDC with single voltage clamping (**b**) CCCI -BDC with single voltage clamping.

I. Boost Mode of Operation:

Figure 4 illustrates the characteristic waveforms of the CCCI-BDC converter boost mode operation. The gate pulses of switch (V_{g1}) which triggers boost mode and gate pulses of switch (V_{g2}) which triggers buck mode are complimentary. Let boost switch (S_1) and buck switch (S_2) duty cycles be assumed as δ_1 and δ_2, respectively. Here, T represents the time period of switches S_1 and S_2. In the forward boost mode, switch (S_1) operates in pulse width modulated mode and diode D_2 operates in freewheeling mode. The boost mode operation is further classified into four operating modes in a switching period, and equivalent circuits of individual modes are illustrated in Figure 5.

A. Mode-1 ($t_0 < t < t_1$): (S_1 ON, D_2 ON)

During this mode, switch S_1 is triggered to ON state and diode D_2 continues in conduction from the previous state. The switch S_1 enables linear charging of inductor L_1 and the inductor L_2 discharge path is through the load R_H. Clamped diodes D_{c1} and D_{c2} are in reverse bias, and the current through the inductor L_1 and L_2 is given by

$$V_{L1} = V_{LV} = L_1 \frac{di_{L1}}{dt} \tag{5}$$

$$i_{L1}(t) = \frac{V_{LV}}{L_1}(t - t_0) + i_{L1}(t_0) \tag{6}$$

$$L_2 \frac{di_{L2}}{dt} + V_{RH} = 0 \tag{7}$$

$$i_{L2}(t) = \frac{-V_{RH}}{L_2}(t - t_0) + i_{L2}(t_0) \tag{8}$$

The expression for voltage clamping diode (D_{c1}) current and voltage clamping capacitor (C_{c1}) voltage is given as

$$i_{Dc1} = i_{Dc2} = 0 \tag{9}$$

$$V_{Cc1}(t) = V_{Cc1}(t_0)e^{\frac{-t}{R_{c1}C_{c1}}} \tag{10}$$

At the instant $t = t_1$ the current through L_1 and L_2 is equal. Then, the diode D_2 will be reverse biased and clamped diode D_{c2} will become forward biased, because of the clamped capacitor C_{c1}.

B. Mode-2 ($t_1 < t < t_2$): (S_1 ON, D_2 OFF D_{C2} ON)

In this mode, S_1 is continuing the conduction from the previous state, so the current through L_1 (i_{L1}) reaches its maximum value and the current i_{L2} reaches zero. In this mode, the inductor L_2 leakage energy is freewheeled through C_{C1} and D_{C2}. So, the diode D_2 will become reverse bias. Now, the current through L_1 and L_2 is

$$i_{L1}(t) = \frac{V_{LV}}{L_1}(t - t_1) + i_{L1}(t_1) \tag{11}$$

$$i_{L2}(t) = 0 \tag{12}$$

The voltage across the clamped diode D_{C1} and current through the clamped capacitors are expressed as

$$V_{Dc1} = -V_{L2} \text{ and } i_{Dc1} = i_{Dc2} = 0 \tag{13}$$

C. Mode-3 ($t_2 < t < t_3$): (S_1 OFF, D_2 ON, D_{C1} ON)

This mode begins after S_1 is turned off at $t = t_2$. So, the polarities of L_1 will change and at the same time both inductor L_1 and source together are ready to discharge. However, during this instant, the diode D_2 will come to forward bias. During this period, the stress due to leakage inductance on S_1 will divert through D_{c1}. After that, the diode D_2 will become forward bias, and the voltage across the clamped capacitor and the input current is expressed as

$$V_{Cc1} = \frac{1}{C_{c1}}\int_{t_2}^{t_3}(i_{L1} - i_{L2})\frac{R_{C1}}{Z_{C1}}dt \tag{14}$$

where $Z_{C1} = R_{C1} - jX_{C1}$

$$\begin{gathered} V_{Cc1}(t_3 - t_2) = \tfrac{1}{C_{c1}}(i_{L1} - i_{L2})(t_3 - t_2)\tfrac{R_{C1}}{Z_{C1}} \\ \backslash C_{c1} = \frac{(i_{L1} - i_{L2})(t_3 - t_2)\frac{R_{C1}}{Z_{C1}}}{V_{Cc1}(t_3 - t_2)} \\ i_{D_{C1}} = i_{L1} - i_{L2} \end{gathered} \tag{15}$$

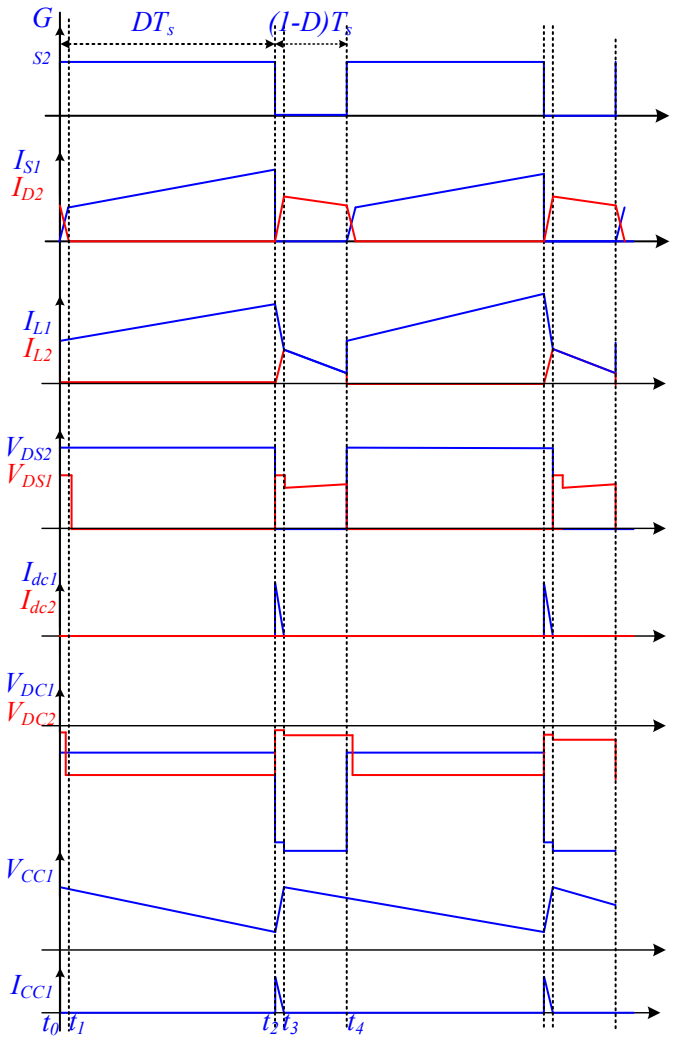


Figure 4. Characteristic waveforms during various modes of boost operation.

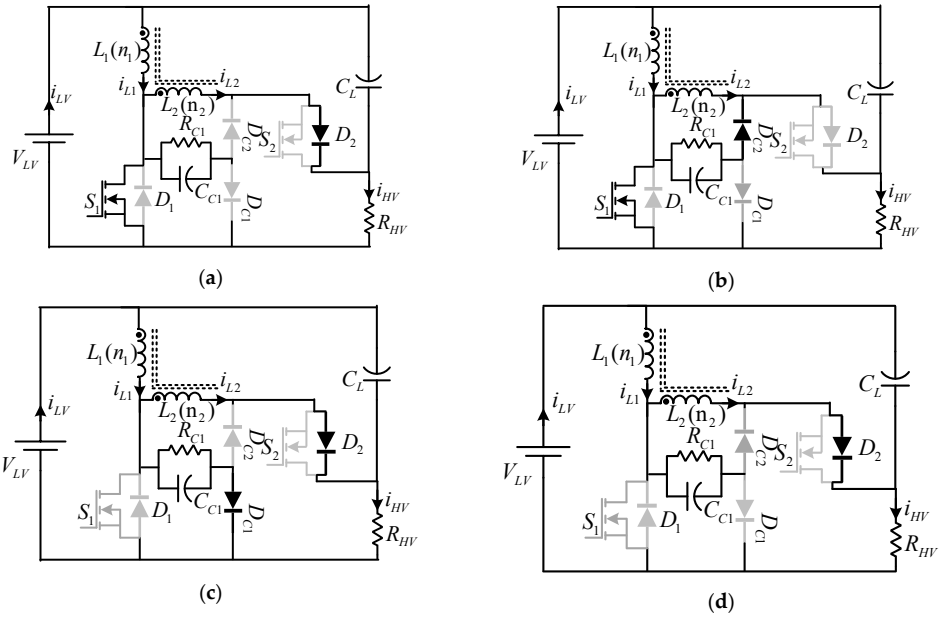


Figure 5. Equivalent circuit of boost operation (**a**) in mode-1 (**b**) in mode-2 (**c**) in mode-3 (**d**) in mode-4.

D. Mode-4 ($t_3 < t < t_4$(T)): (S_1 OFF, D_2 ON, D_{C1} OFF)

In this mode, S_1 remains off and D_2 is in forward bias. The clamping diodes D_{c1} and D_{c2} are both in reverse bias. This mode begins at t_3 where current i_{L1} is equal to i_{L2}. In this duration (t_3–t_4), the inductor L_1 is completely discharged to the load. The magnetizing current reduces linearly while the coupled inductor supplies energy to the load. The absorbed energy in the coupled inductor is delivered through the route V_{LV}–L_1–L_2–D_2–R_H–V_{LV}. Therefore, the voltage across L_1 is expressed as

$$V_{L1} = \frac{V_{LV} - V_{RH}}{1 + k} \tag{16}$$

The current through the windings L_1 and L_2 is

$$i_{L1}(t) = \frac{V_{LV} - V_{RH}}{L_1(1 + k)}(t - t_3) + i_{L1}(t_3) \tag{17}$$

II. Buck Mode of Operation

The buck mode operation is further classified into four modes of operation (i.e., mode-5 to mode-8) across a switching period, and equivalent circuits of individual modes are illustrated in Figure 6. Modes 5–8 are almost a repetition of Modes 1–4 in boost mode. This is reverse buck mode where switch (S_2) is operating in pulse modulated mode and the diode D_1 is operating in freewheeling mode. The magnetizing current ($i_{LM} = i_{L1}$) path runs from the DC bus, primary and secondary windings (L_1 and L_2) of the coupled inductor, and finally to the battery. The equivalent circuit for buck mode operation is shown in Figure 6. Figure 7 depicts idealized graphs of the converter operating in buck mode. Further division of modes is illustrated in Figure 8.

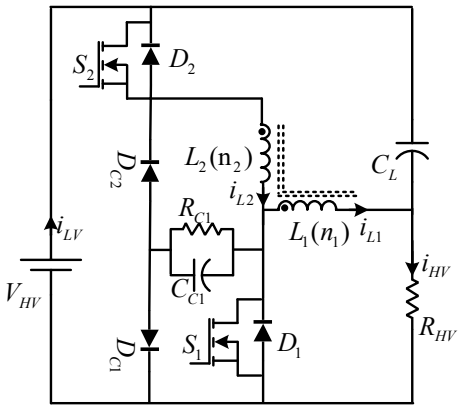


Figure 6. Equivalent circuit in buck operation.

E. Mode-5 ($t_0 < t < t_1$): (S_2 ON, D_1 ON)

In this mode, diode D_1 is already in conduction from the previous state and at instant t_0, S_2 gets triggered. The supply V_{HV} directly connected to inductor L_2 which is energized through S_2, while L_1 energy is discharged to load through D_1. The current through the CIs L_2 and L_1 increases and decreases linearly. At instant t_1, the current i_{L1} is equal to i_{L2}, and diode D_1 becomes reverse bias, so the polarities of L_1 are reversed. The clamping diode D_{c1} is in forward biasing mode and the leakage energy due to L_1 charges the capacitor C_{c1}. The CI currents i_{L1} and i_{L2} are given as

$$i_{L1}(t) = \frac{-V_{RH}}{L_1}(t - t_0) + i_{L1}(t_0) \tag{18}$$

$$i_{L2}(t) = \frac{V_{HV}}{L_2}(t - t_0) + i_{L2}(t_0) \tag{19}$$

F. Mode-6 ($t_1 < t < t_2$): (S_2 ON, D_1 OFF)

In this interval, S_2 is continuing its conduction up to $t_{on}(=t_2)$ from the previous interval, and at instant t_1 the diode D_1 becomes reverse bias, as both the currents are equal. At this instant, the inductor L_1 changes its polarities. Thus, the clamped diode D_{c1} is in forward biasing mode and the leakage energy due to L_1, charges the capacitor C_{c1}. The energy stored in L_2 discharges at load. The clamping diode current and voltage across L_1 and C_{c1} are expressed as:

$$i_{Dc1} = -(i_{cc1} + i_{Rc1}) \tag{20}$$

$$V_{L1} = \frac{V_{HV} - V_{RL}}{1 + k} \tag{21}$$

$$V_{Cc1} = V_{RL} - V_{L1} \tag{22}$$

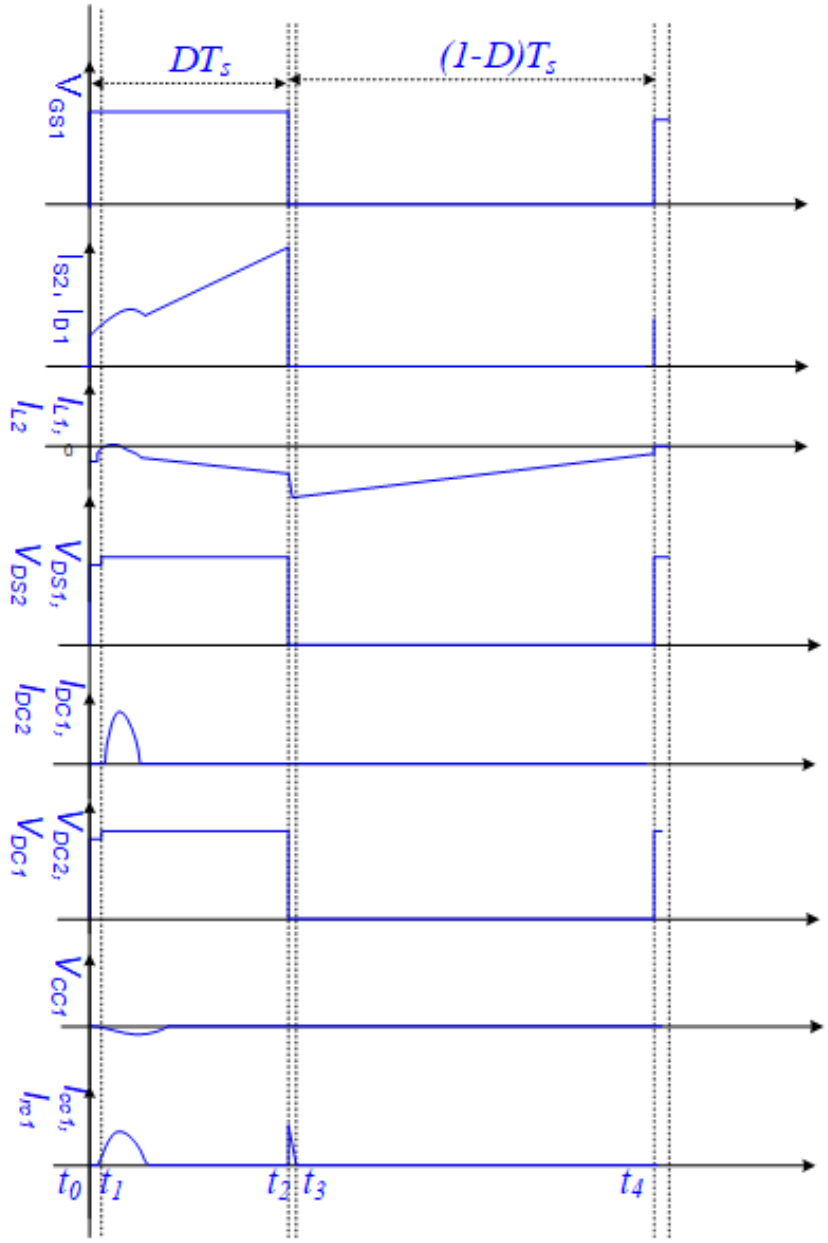


Figure 7. Characteristic waveforms during various modes in buck operation.

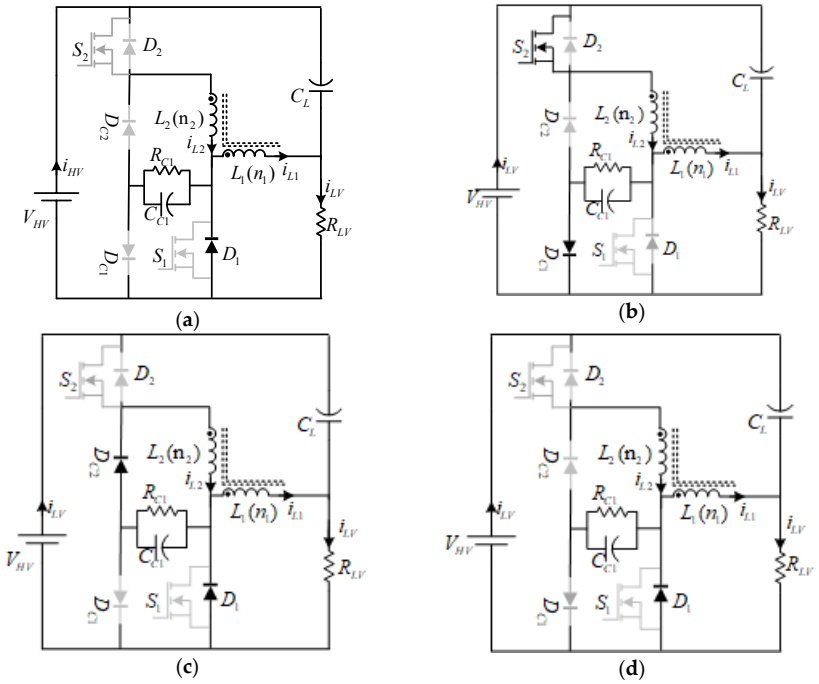


Figure 8. Equivalent circuit of buck operation (**a**) in mode-1 (**b**) in mode-2 (**c**) in mode-3 (**d**) in mode-4.

G. Mode-7 ($t_2 < t < t_3$): (S_2 OFF, D_{C2} ON, D_1 ON)

During this interval, the switch S_2 and diode D_{c1} are triggered off, which will change the polarities of L_1 and L_2. Therefore, the diodes D_1 and D_{c2} are forward biased and the energy absorbed from L_1 freewheels through D_1. The leakage energy stored in L_2 is recovered by charging C_{c1} through D_{c2}. During this period, the turn off voltage of S_2 due to the leakage inductance is reduced by the clamping circuit. The current through both the CIs is expressed as shown below:

$$i_{L2} = i_{Dc2} = i_{Rc1} + i_{Cc1} \tag{23}$$

$$i_{L1}(t) = \frac{-V_{RL}}{L_1}(t - t_2) + i_{L1}(t_2) \tag{24}$$

By assuming the voltage ripple on C_{c1}, the commutating voltage across S_2 is given as

$$V_{s2} = V_{HV} - V_{L2} \tag{25}$$

H. Mode-8 ($t_3 < t < t_4$(=T)) (S_2 OFF, D_{C2} OFF, D_1 ON)

In this interval, the switch S_2 remains off. The current i_{L2} is completely discharged and reaches zero, so the diode D_{c2} will get reverse bias and the current i_{L1} freewheels through diode D_1 until the next cycle starts. The clamped diode D_{c1} is again forward biased due to clamped capacitor C_{c1}. At instant $t = t_4$, the switch S_2 again starts conduction and will repeat the cycle. During this mode, the current through CIs are expressed as:

$$i_{L1}(t) = \frac{-V_{RL}}{L_1}(t - t_2) + i_{L1}(t_2) \tag{26}$$

$$i_{L2}(t) = 0 \tag{27}$$

From the above equations, output and switch voltages can be calculated as

$$V_o = \frac{1 + ND}{1 - D} V_{in} \tag{28}$$

$$V_{sw} = \frac{1+ND}{1-D} V_{in} \tag{29}$$

III. Selection of Voltage Clamping Circuits

The problem of voltage spikes during turn off of both the switches is resolved using the single voltage clamping circuit. The proposed voltage clamping RCD circuit contains a diode in parallel with the series connection of resistor and capacitor, not only clamping the spike in voltage during turn off, but also minimizing the leakage inductance of the coupled inductor. The corresponding graphs of boost mode and buck mode of the circuits discussed above are illustrated in Figures 5 and 8. For the right choice of these clamping circuit component (clamping capacitors and resistance) values, after the design, several iterations of MATLAB/Simulink based simulations were carried out. The I_{Dc1} and I_{DC2} (current through RCD snubber circuit diodes D_{C1} or D_{C2}) present less pulse width. Therefore, D_{c1} and D_{C2} are of smaller rating as compared with conventional solutions. For hardware validation, the values of C_{C1} and C_{C2} are obtained from (15). The proposed single voltage clamping circuit has the advantages of less component count, simple structure, size reduction, and cost reduction.

IV. Inrush Current

The instant a device is triggered on; a maximum instantaneous flow of current occurs through the device due to the initially uncharged energy storage elements. This peak current is called inrush current. Inrush current is far greater than the steady state current. The reason for the occurrence of inrush current is the input capacitor, as shown in Figure 9. Usually, capacitors are placed at the input of non-linear loads (power electronics converters) and those capacitors get charged up during the time when the device is powered on. If left uncontrolled, it will cross fewer times higher than its rating, even with nominal value. Inrush current is visible in the case of DC supply in proportion to the magnitude of voltage. Figure 10 illustrates the current waveform when the device is powered ON. The shape of the waveform indicates a rising peak, decreasing gradually to reach the steady state value after a certain time. This transient current waveform is the inrush current. The inrush current seriously damages the input rectifier, power switching device, and fuse and reduces the reliability and lifetime of the system.

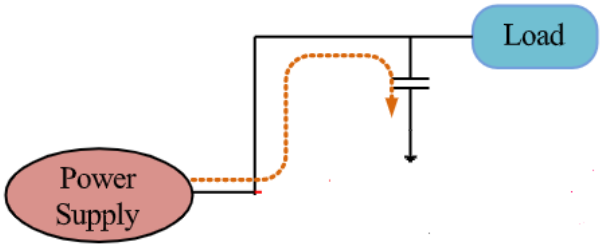


Figure 9. A Typical Power Supply Rail: Source of inrush current.

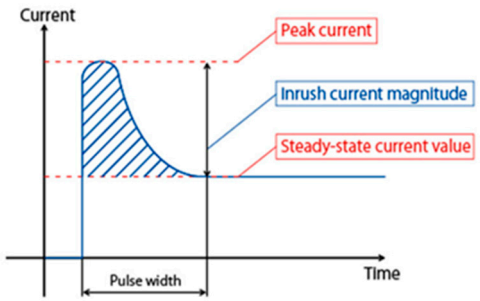


Figure 10. Inrush Current Waveform during power up of a device.

To investigate the inrush current profile in the proposed converter with the simulation parameters for the conversion of 24 V to 200 V, the changes in inrush current are observed in the input current with respect to changes in input voltage, load current, and duty ratio during starting.

V. Control-to-Source Current and Control-to-Output Transfer Function

Control-to-source current and control-to-output transfer functions are obtained by using the state space averaging technique, which can be given as

$$\frac{I_{in}}{d} = \frac{(R + r_{c1})(k_1 s^2 + k_2 s + k_3)}{k_4(k_5 s^2 + k_6 s + k_7)} \tag{30}$$

$$\frac{V_0}{d} = \frac{-R(R + r_{c1})(C_1 r_{c1} s + 1)(k_8 s + k_9)}{k_{10}(k_{11} s^2 + k_{12} s + k_{13})} \tag{31}$$

where k_1–k_{10} are detailed in Appendix A.

To establish the conclusion from the derived transfer functions, step responses for the load, line, and duty cycle variations are plotted as presented in Figure 11.

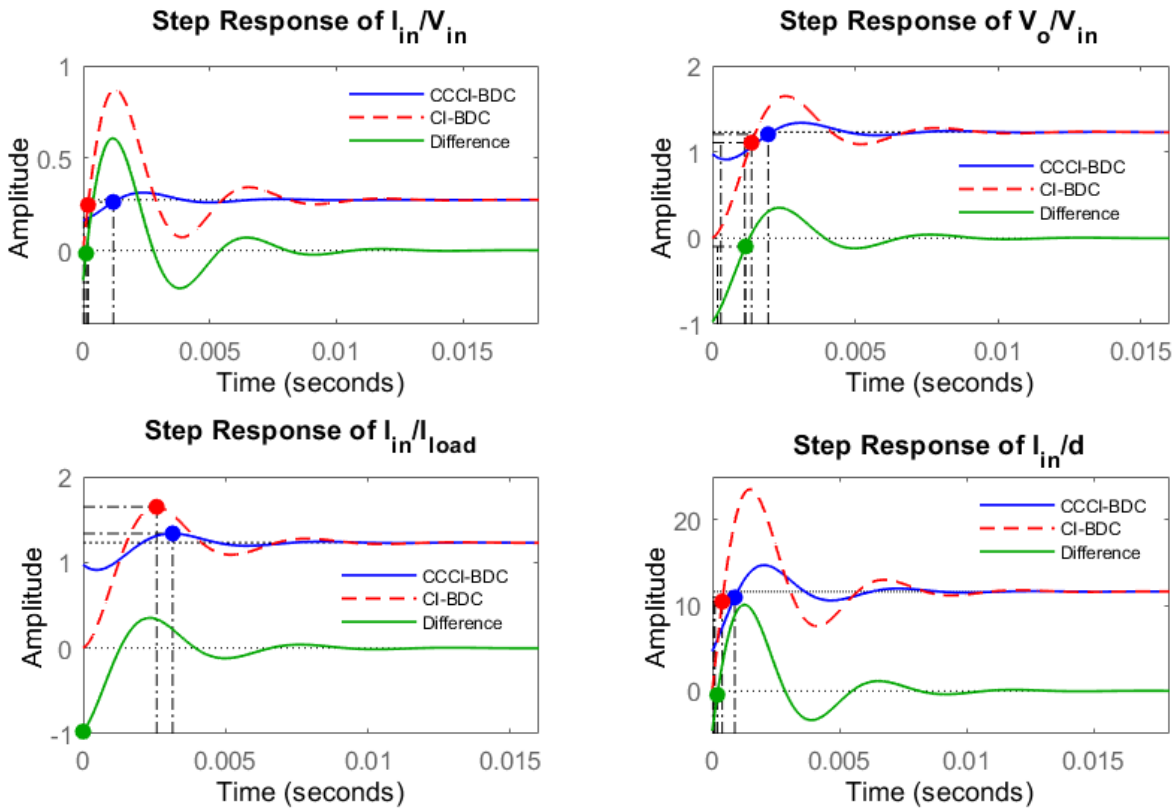


Figure 11. Comparative step response analysis of existing (CI–BDC) and proposed (CCCI–BDC) converters.

From Table 1, it is observed that, for the step response of input current to input voltage in the transfer function, there is a 37.5% reduction in inrush current as one compares conventional and proposed converters subjected to changes in line voltage. It is also observed that the inrush current of the proposed converter reduces by 9% of overshoot with respect to the conventional converter, when one measures the step response of the output voltage to the input voltage transfer function. Further, it is noted that there is a 6.8% reduction in inrush current between conventional and proposed converters, when there are load variations. Finally, one can see that the percentage reduction in inrush current is

10.71% with respect to the changes in duty ratio, comparing conventional and proposed converters. These responses show that, for the line and load variations, variations in the input current and output voltage are much less in the proposed converter with respect to the conventional converter.

Table 1. Time response comparison of conventional (CI–BDC) and proposed CCCI–BDC converter.

S No	Transfer Function	Conventional Converter (CI BDC)				Proposed Converter (CC CI BDC)			
		Peak Overshoot	Settling Time (sec)	Peak Time (sec)	Rise Time (sec)	Peak Overshoot	Settling Time (sec)	Peak Time (sec)	Rise Time (sec)
1	I_{in}/V_{in}	0.807	0.0101	0.00123	0.000175	0.607	0.00862	0.00112	0.000998
2	V_o/V_{in}	34	0.00932	0.00258	0.00107	8.75	0.00877	0.00314	0.00082
3	I_{in}/I_{load}	34	0.01	0.00258	0.00082	8.75	0.00932	0.00314	0.00082
4	$I_{in}/_d$	103	0.01	0.00146	0.000777	26.5	0.0084	0.00202	0.00351

3. Simulation Results and Discussion

The following are simulation studies of the single voltage clamping CCCI–BDC. Buck and boost modes have been implemented on the MATLAB/Simulink platform. Parameters considered for the simulations are given below in Table 2.

Table 2. Specifications of the proposed CCCI-BDC converter.

Parameter	Boost Mode (LV to HV)	Buck Mode (HV to LV)
Input voltage, V	24 V	200 V
MOSFETs (S_1 and S_2)	IRFP 250 N SIHG32N50D-GE3-ND	IRFP 264 N SIHG32N50D-GE3-ND
Fast Acting Diodes (D_1 and D_2)	UG15HT-E3/45-ND	UG15HT-E3/45-ND
Output voltage, V	200 V	24 V
Output voltage ripple, %	≤0.5	≤0.5
Output power, W	100 W	100 W
Output current, A	0.5 A	4.1667 A
Switching frequency, kHz	50 kHz	50 kHz
Inductor	$L_1 = 200$ µH $L_2 = 800$ µH $L_m = 392$ µH	
Turns ratio of L_1 and L_2	N = 2	
Clamp capacitors C_{C1} and C_{C2}	1 µF/100 V	
Clamp resistors R_{C1} and R_{C2}	1 KΩ	
Clamp diodes D_{C1} and D_{C2}	UG15HT-E3/45-ND (2)	
Filter capacitors	$C_H = 220$ µF/500 V $C_L = 220$ µF/50 V	

For the purpose of highlighting the performance of the proposed CCCI–BDC, a single voltage clamping circuit has been employed to augment the capabilities, and it is denoted as Voltage Clamping CCCI–BDC (VCCCCI–BDC). The MATLAB/SIMULINK platform is used to obtain the simulation results of the proposed converter. Table 2 details the design specifications of the CCCI–BDC converter during different modes of operation. Figures 12–15 contain the waveforms of both CCCI–BDC and VCCCCI–BDC during steady state condition in both boost and buck modes, respectively. Figures 12a and 13a show the switch (S_1), voltage (V_{ds1}), and current (I_{ds1}) of CCCI–BDC and VCCCCI–BDC in boost mode while Figures 13a and 14a show the switch (S_2), voltage (V_{ds2}), and current (I_{ds2}) of CCCI–BDC and VCCCCI–BDC in buck mode, respectively.

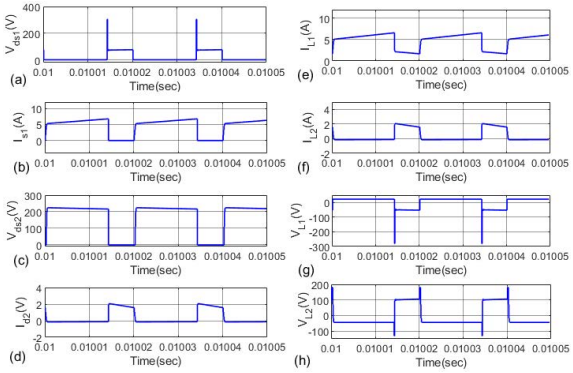


Figure 12. Simulation results of discharging (boost) mode of operation switch (S_1) (**a**) voltage and (**b**) current, (**c**) switch (S_2) voltage and (**d**) diode (D_2) current, coupled inductor (**e**) primary current and (**f**) secondary current, and coupled inductor (**g**) primary voltage and (**h**) secondary voltage with CCCI-BDC.

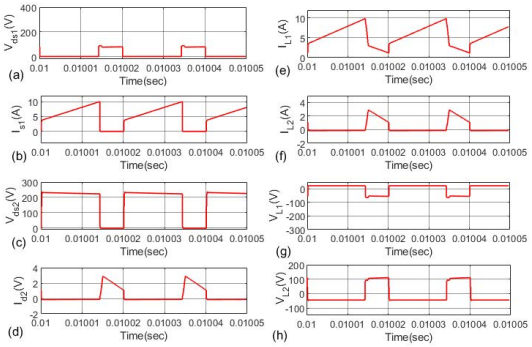


Figure 13. Simulation results of discharging (boost) mode of operation switch (S_1) (**a**) voltage and (**b**) current, (**c**) switch (S_2) voltage and (**d**) diode (D_2) current, coupled inductor (**e**) primary current and (**f**) secondary current, and coupled inductor (**g**) primary voltage and (**h**) secondary voltage with VCCCCI–BDC.

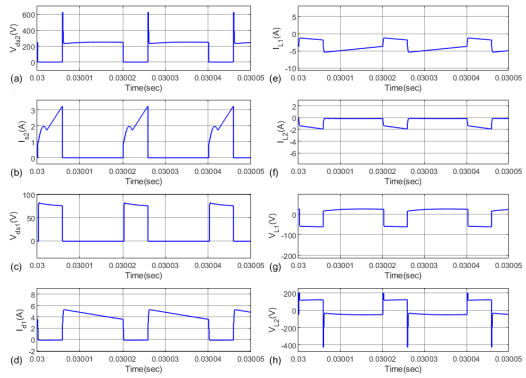


Figure 14. Simulation results of discharging (buck) mode of operation switch (S_2) (**a**) voltage and (**b**) current, (**c**) switch (S_1) voltage and (**d**) diode (D_1) current, coupled inductor (**e**) primary current and (**f**) secondary current, and coupled inductor (**g**) primary voltage and (**h**) secondary voltage with CCCI–BDC.

Simulation results of switch (S_1) voltage and current, switch (S_2) voltage, diode (D_2) current, and coupled inductor currents in both sides (primary and secondary), as well as the coupled inductor primary voltage and secondary voltage during discharging (boost) mode of CCCI–BDC operation are presented in Figure 12a–h, respectively. Similar results have been captured during discharging (boost) mode of VCCCCI–BDC for the purpose of comparative analysis and presented in Figure 13a–h, respectively.

From these results, it can be noted that stresses on the main device (S_1) during discharging (boost) mode are significantly reduced. A similar kind of analysis is carried out for the charging (buck) mode of CCCI–BDC and presented in Figure 14. Simulation results of voltage and current at switch (S_2), switch (S_1), diode (D_1), as well as the primary and secondary currents and voltages in the coupled inductor, during charging (buck) mode of CCCI–BDC operation, are presented in Figure 14a–h, respectively. Similar results have been captured during charging (buck) mode of VCCCCI–BDC for the purpose of comparative analysis and presented in Figure 15a–h, respectively. From these results, it can be noted that stresses on the main device (S_2) during charging (buck) mode are significantly reduced.

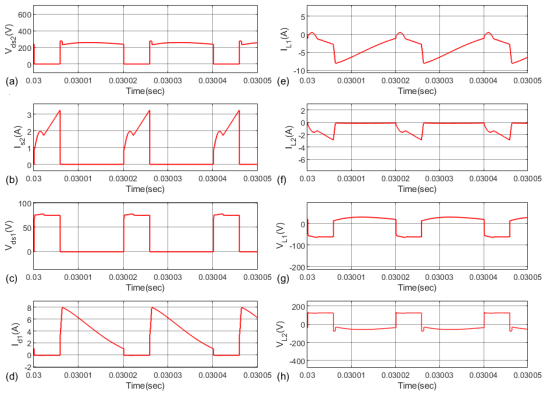
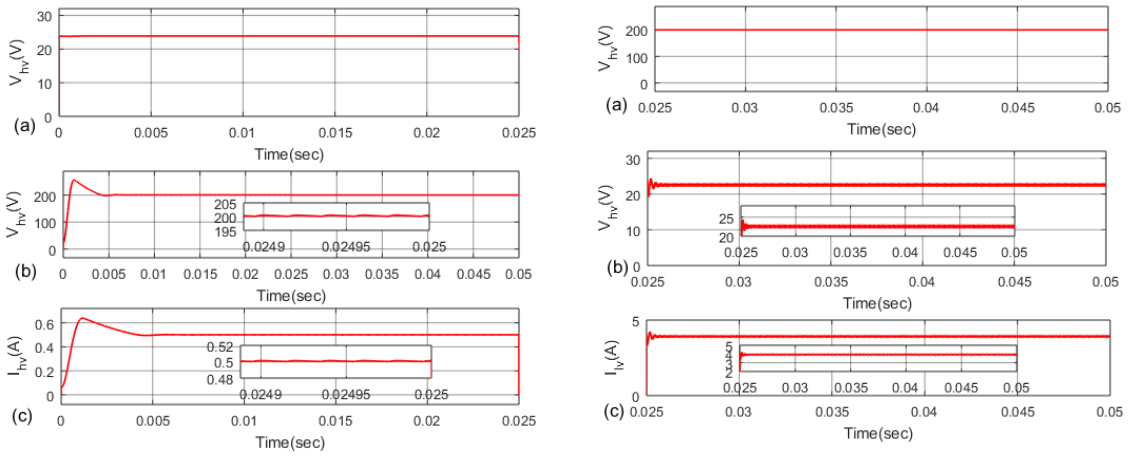


Figure 15. Simulation results of discharging (buck) mode of operation switch (S_2) (**a**) voltage and (**b**) current, (**c**) switch (S_1) voltage and (**d**) diode (D_1) current, coupled inductor (**e**) primary current and (**f**) secondary current, and coupled inductor (**g**) primary voltage and (**h**) secondary voltage with VCCCCI–BDC.

The observation from Figures 12a and 13a are that V_{ds1} is 312 V in CCCI–BDC and it is 96 V in VCCC–CI BDC. Further, the observation from Figures 14a and 15a are that V_{ds2} of S_2 is 608 V in CCCI–BDC and it is 240 V in VCCCCI–BDC. Figures 12a and 13a show the value of reduced switching spike of V_{ds1} in S_1. Figures 14a and 15a show the corresponding reduction in switching spike of V_{ds2} in S_2. Figures 13d and 15d show that buck and boost modes are realized. Figure 16A,B illustrate the bidirectional operation of the converter, with 200 V as high voltage and 24 V as low voltage. The voltage ripple is also within the limits of 1% as is evident from Figure 16, for both buck mode and boost mode.



(**A**) Boost Mode (**B**) Buck Mode

Figure 16. Simulation results of (a) input voltage, (b) output voltage and (c) output current, (**A**) discharging (boost) mode of operation (**B**) charging (buck) mode of operation.

4. Hardware Results and Discussion

The proposed CCCI-BDC has been verified by experimental investigation in both modes of operation, i.e., boost and buck modes. For the experimental validations, a laboratory scale prototype was developed, as illustrated in Figure 17. It primarily comprises of two IRFP 250 N MOSFETs driven by optically separated TLP250 driver circuits, one EZPE50506MTA capacitor, and one coupled inductor. A TELCON-25-based current sensor and AD202JN-based isolation amplifier sense the inductor current and capacitor voltage, respectively. As shown in Figure 17, sensed quantities are processed by a signal conditioning circuit to control these state variables (i.e., inductor current and capacitor voltage). The corresponding values of different device specifications and variables used for such an investigation are mentioned in Table 3. The suggested CCCI-BDC was proven to satisfactorily operate in boost and buck modes during experimental investigation, the setup of which is shown in Figure 17. The CCCI-BDC hardware prototype was built with the help of SiC MOSFETs and an FPGA controller, illustrated in Figure 17. Two lamps of 12 V and 50 W rating were used as a load for this test setup. The system parameters are validated for steady state and transient modes.

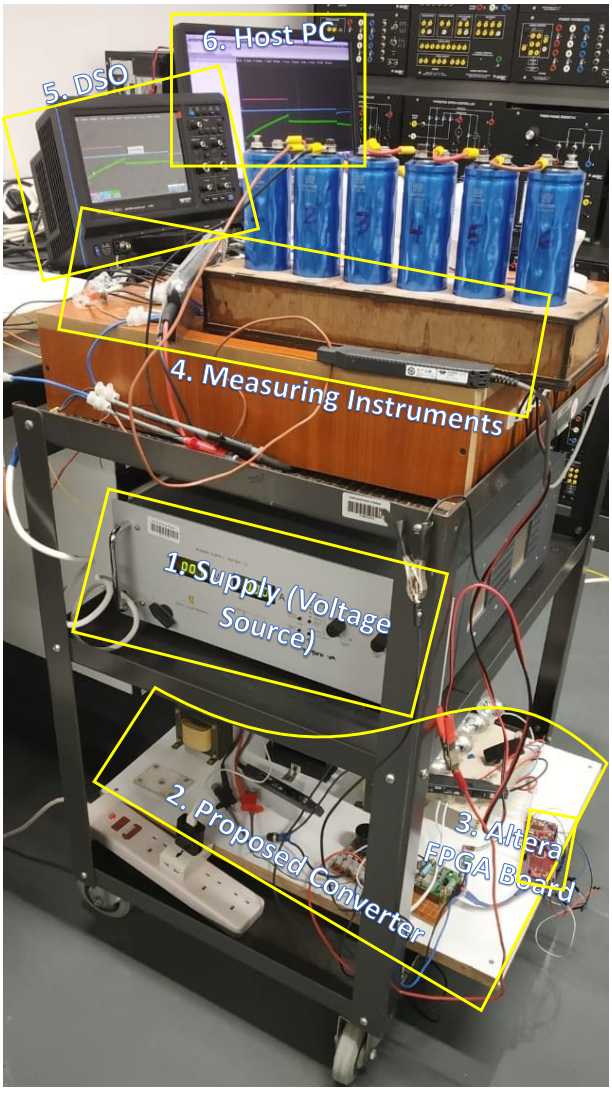


Figure 17. Hardware setup of CCCI-BDC (1. Supply and Load Terminals, 2. Proposed Converter, 3. FPGA Altera Kit, 4. Voltage sensors along with conditioning elements and Current sensors along with conditioning elements 5. DSO, and, 6. Host PC).

Table 3. Design specification and circuit parameters of the proposed converter.

Parameter	Proposed		Conventional	
	Boost Mode (LV to HV)	**Buck Mode (HV to LV)**	**Boost Mode (LV to HV)**	**Buck Mode (HV to LV)**
Input voltage	12 V	24 V	12 V	24 V
Turns ratio	2	2	2	2
Output voltage	24 V	12 V	24 V	12 V
Output voltage ripple (%)	≤0.5	≤0.5	≤0.5	≤0.5
Load	12 V, 50 W of 2 Lamps in series	12 V, 50 W of 2 Lamps in series	12 V, 50 W of 2 Lamps in series	12 V, 50 W of 2 Lamps in series
Output current	4.1667 A	8.33 A	8.33 A	4.1667 A
Switching frequency	10 kHz	10 kHz	10 kHz	10 kHz
Inductor	0.5 mH		0.5 mH	
Filter capacitors	500 µF/500 V		500 µF/500 V	

The input voltage levels are 12 V and 24 V. The corresponding graphs of device voltages, input current, load current, and capacitor voltages are extracted for both conventional as well as proposed converters. Their performances have been compared experimentally. The conventional converter necessitates two capacitors (one C_{HV} for boost mode and another C_{LV} for buck mode respectively), but in the proposed converter, only one capacitor (C_C) supports both modes of operation, thus acting as an equivalent for both capacitors in the conventional system.

The input current, load current, and capacitor voltage corresponding to gate pulses are recorded herein in Figure 18. A first observation regarding input current peak shows 8.57 A in the traditional converter but 8.27 A in the proposed converter for similar load current values. Similarly, the capacitor voltages for the traditional converter and proposed converter are 23.2 V and 12.1 V, respectively (a reduction of 46.25%).

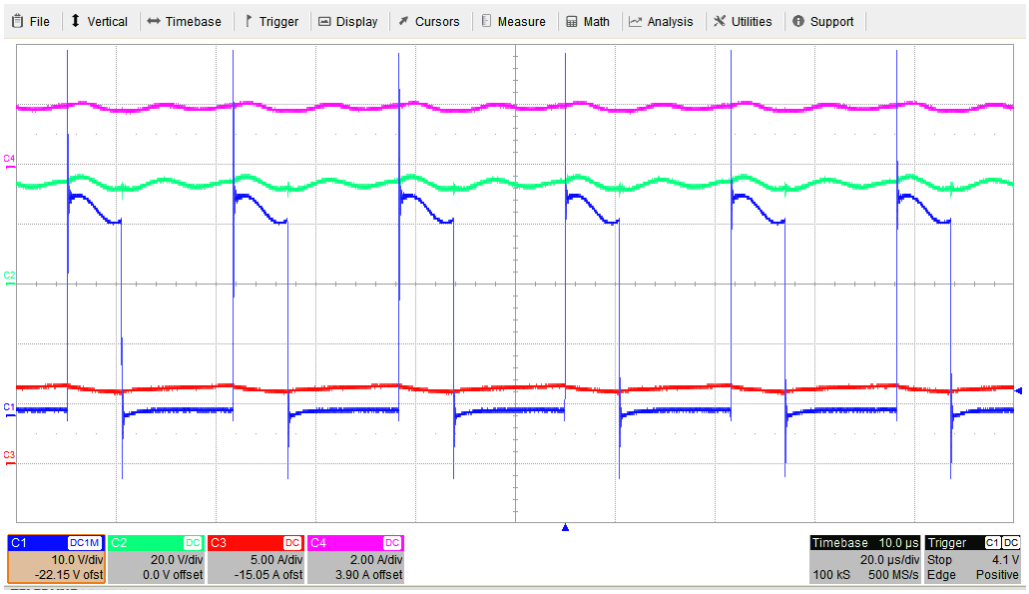


Figure 18. CCCI–BDC parameters in boost mode: The device parameters of lower switch (S_2) (blue) (10 V/div), load voltage (green) (20 V/div), load current (red) (5 A/div) and input current (pink) (2 A/div).

For real time performance validation, various features of a vehicle, e.g., faster load turn off, smooth turn on, and converter switching ON and OFF with different duty cycle variations, are simulated. The various capacitor voltages, input currents, and load currents are measured for these features to be obtained. A closer look at the variation of maximum values of these signals during ON and OFF are illustrated here in Table 4.

Table 4. Comparison of the various parameters in boost mode during steady-state conditions.

Parameter	Conventional		Proposed	
	Peak Value	Average Value	Peak Values	Average Values
Capacitor voltage	24.8 V	23.2 V	12.6 V	12.2 V
Input current	9.02 A	8.32 A	8.8 A	8.32 A
Load Current	4.3 A	4.2 A	4.3 A	4.2 A

It can be inferred from Table 5 that the proposed converter outperforms the conventional converter during steady state conditions, in terms of input current and capacitor voltage ripple values.

Table 5. Comparison of ripple values for the proposed and conventional converters in boost mode.

Ripples	Conventional	Proposed
Capacitor voltage	6.67%	3.33%
Input current	8.16%	5.76%
Load Current	2.4%	2.4%

The microscopic view of input current, capacitor voltage, and load currents was obtained for the purpose of analyzing the ripple content. The findings are reported in Table 5. This clearly shows the capacitor voltage in proposed converter is 3.33% less with regard to the conventional converter. Similarly, the input current is 2.4% less for similar load current ripples. The graphs of the current in the inductor, voltage in capacitor, current in load, and gate pulse for the top switch were obtained for four switching cycles, in the reverse buck mode of operation. The following observations have been made from these readings. Firstly, the maximum value of input current is 9.02 A for the CCCI-BDC converter but 8.8 A for the corresponding input current in the traditional converter. Likewise, the capacitor voltage in the proposed converter is 12.6 V, but the capacitor voltage for the traditional converter is 24.8 V, equivalent to a 50.8% reduction.

The various capacitor voltages, input currents, and load currents measured for these features in buck mode were obtained and are presented in Figure 19. The performance of the converter was checked for various criteria, such as smooth startup, quick load turn off, and turning the converter on and off under different duty cycle values. This was estimated using the values of input current, capacitor voltage, and load current. Detailed analyses of the maximum values of these parameters during steady state condition have been performed and the results are tabulated in Table 6. It can be inferred from Table 6 that the proposed converter demonstrates better performance than the conventional converter not only during steady state conditions.

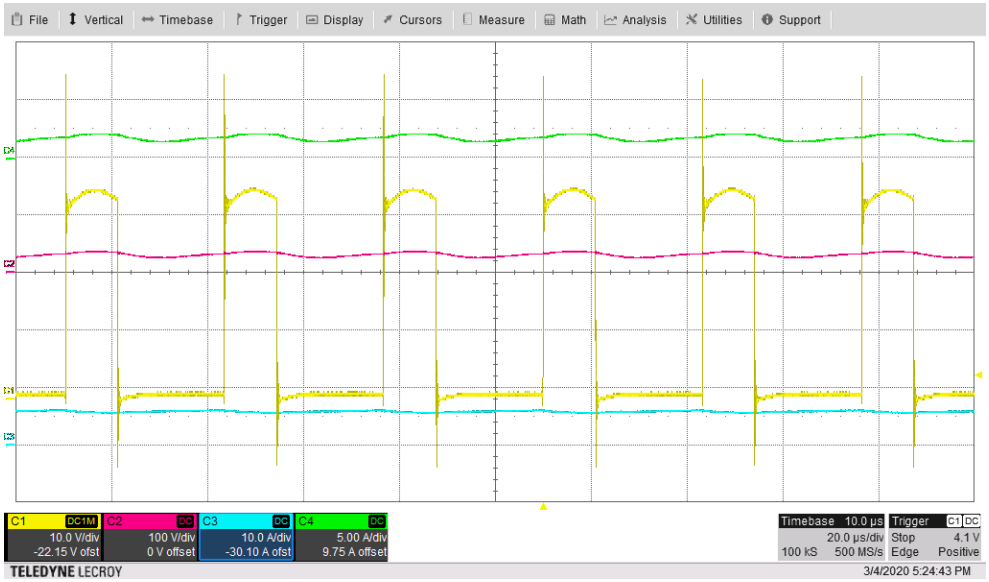


Figure 19. CCCI–BDC parameters in buck mode: The device parameters of upper switch (S_2) (yellow), load voltage (blue), load current(green) and input current (pink).

Table 6. Comparison of the various parameters during both transient and steady for the proposed and conventional converters in buck mode.

Ripples	Conventional		Proposed	
	Peak Value	Average Value	Peak Values	Average Values
Capacitor voltage	24.8 V	23.2 V	12.6 V	12.2 V
Input current	4.54 A	4.02 A	4.62 A	4.28 A
Load Current	8.54 A	8.34 A	8.48 A	8.36 A

Table 7 demonstrates the superior performance of the proposed converter in terms of capacitor voltage stress, during both steady state ripples. From Table 7, the ripple content can be compared in terms of input current, capacitor voltage, and load current, for the conventional and proposed converter, after observing a microscopic view of the same. The ripple content in capacitor voltage is 3.33% less in proposed converter vis–a-vis the conventional converter, for the same load current.

Table 7. Comparison of ripple values for the proposed and conventional converters in buck mode.

Ripples	Conventional	Proposed
Capacitor voltage	6.67%	3.33%
Input current	12.48%	8.16%
Load Current	2.4%	1.44%

Efficiency:

This paper considers the parasitic resistance of inductors and capacitors, as well as the diode forward conduction losses, to compute the efficiency analysis of the inverter. In all topologies, the parasitic resistances of the inductor and capacitor are r_L and r_C, respectively, and the forward conduction loss of the diode due to forward voltage (V_F) is assumed to be the same. This manuscript also considers the effect of parasitic resistances and the forward voltage drop of main power devices (MOSFETs).

The calculation of losses and efficiencies of CCCI-BDC and CI-BDC was carried out by considering the equivalent circuit with various parasitic components and the relevant formulas are shown in Table 8. Figure 20 depicts the losses incurred in various components

of the CCCI-BDC in relation to the duty ratio, which is calculated using the aforementioned formulas. According to these findings, at lower duty ratios, the diode is the main source of losses among all other components of the converter. MOSFETs, on the other hand, cause more losses at higher duty ratios. Capacitor losses are lower when compared to other components. The proposed converter's efficiency is 93.8% at the rated values, as shown in Table 3. In similar way, CI-BDC efficiency calculation is also carried out and found to be 93.2%. Hence, it can be understood that the proposed converter not only reduces ripples as well as the stresses on capacitors and devices, but also improves efficiency.

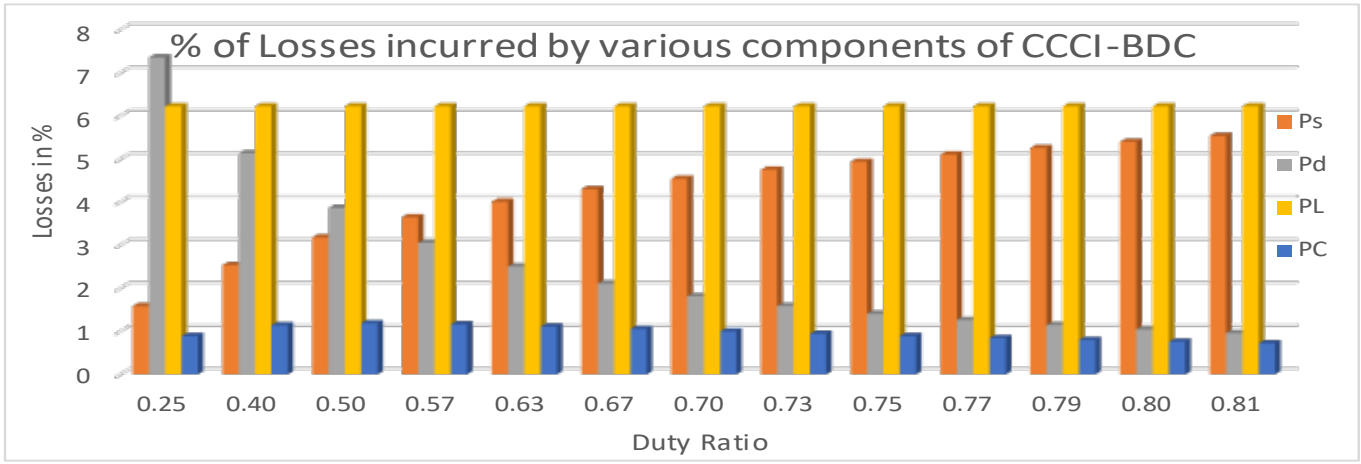


Figure 20. Losses incurred in various components of CCCI-BDC (Losses in MOSFETs, Diodes, Inductors and capacitors are P_S, P_d, P_L and P_c).

Table 8. Various variables (device, inductor and capacitor RMS currents (I_{rms}), overall losses (P_{LS}), efficiency (η), and non-ideal gain (M_{VDS})) of CCCI-BDC.

Variables	Switch	Diode	Inductor	Capacitor	Losses and Efficiency
I_{rms}	$\left(\frac{1+ND}{1-D}\right)\sqrt{D}I_o$	$\left(\frac{1+ND}{\sqrt{1-D}}\right)I_o$	$\left(\frac{1+ND}{1-D}\right)I_o$	$\sqrt{\frac{D(1+DN^2+2ND)}{1-D}}I_o$	$P_{LS}=\left\{\begin{array}{l}\left(\frac{1+ND}{1-D}\right)^2\frac{R_{ds}D}{R_L}+f_S{\cdot}c_oR_L+\left\{\frac{V_f}{V_o}+\frac{(1+ND)^2R_F}{(1-D)R_L}\right\}\\+\left(\frac{1+ND}{1-D}\right)^2\frac{r_L}{R_L}+\frac{D(1+DN^2+2ND)}{1-D}\frac{P_o}{R_L}r_c\end{array}\right\}P_o$
P_{rms}	$\left(\frac{1+ND}{1-D}\right)^2\frac{R_{ds}DP_o}{R_L}$	$\frac{(1+ND)^2}{1-D}\frac{R_fP_o}{R_L}$	$\left(\frac{1+ND}{1-D}\right)^2\frac{r_LP_o}{R_L}$	$\frac{D(1+DN^2+2ND)}{1-D}\frac{P_o}{R_L}r_c$	$\eta=\frac{1}{1+\left\{\begin{array}{l}\left(\frac{1+ND}{1-D}\right)^2\frac{R_{ds}D}{R_L}+f_S{\cdot}c_oR_L+\left\{\frac{V_f}{V_o}+\frac{(1+ND)^2R_F}{(1-D)R_L}\right\}\\+\left(\frac{1+ND}{1-D}\right)^2\frac{r_L}{R_L}+\frac{D(1+DN^2+2ND)}{1-D}\frac{P_o}{R_L}r_c\end{array}\right\}}$
P_{sw}	$f_S{\cdot}c_oR_LP_o$	$V_f{\cdot}\frac{P_o}{V_o}$			
P_{D_LS}	$\left\{\begin{array}{l}\left(\frac{1+ND}{1-D}\right)^2\frac{R_{ds}D}{R_L}\\+f_S{\cdot}c_oR_L\end{array}\right\}P_o$	$P_o\left\{\begin{array}{l}\frac{V_f}{V_o}+\\\frac{(1+ND)^2R_F}{(1-D)R_L}\end{array}\right\}$			$M_{VDS}=\frac{1+ND}{(1-D)\left\{\begin{array}{l}\left(\frac{1+ND}{1-D}\right)^2\frac{R_{ds}D}{R_L}+f_S{\cdot}c_oR_L+\left\{\frac{V_f}{V_o}+\frac{(1+ND)^2R_F}{(1-D)R_L}\right\}\\+\left(\frac{1+ND}{1-D}\right)^2\frac{r_L}{R_L}+\frac{D(1+DN^2+2ND)}{1-D}\frac{P_o}{R_L}r_c\end{array}\right\}}$

5. Conclusions

An improved version of the proposed non-ideal DC–DC converter is developed with the help of the capacitor clamping technique. A coupled inductor is adopted for this topology in the place of conventional inductors to achieve higher gain. Results have proven that there is reduction of 13.64% of capacitor voltage stresses. Moreover, under line varying conditions, converter responses prove that there is a 119% and 25.25% reduction of input current and output voltage transients, respectively, as well as a 25.25% and 76.5% reduction of input current transients observed for line and control parameter variations. A simplified single voltage clamped circuit is successfully developed to effectively recover leakage energy and thus mitigate voltage spikes caused by coupled inductors. Furthermore, clamping capacitors help to reduce voltage ripples, which reduces stress on the switch. From hardware investigations, one can observe that the estimation of a non-ideal model system plays a crucial role in understanding the effectiveness of any contemporary control strategy that one may wish to employ. Thus, the proposed non-ideal transfer function of the converter can be effectively used for designing controllers which are robust. The entire analytical part can also be used for various other categories of DC-DC converters, with relevant adjustments. In addition, this analysis can be carried out with motor load as output and with renewable sources as input for future work.

Author Contributions: Conceptualization: K.S.R.K. and D.R.; Methodology: K.S.R.K. and V.V.S.; Software: D.R., Validations: D.R.; formal analysis, D.R.; investigation, D.R. and K.S.R.K.; writing—original draft preparation, D.R. and K.S.R.K.; writing—review and editing, K.S.R.K., A.P. and V.V.S.; All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors hereby declare that they have no conflict of interest.

Abbreviations

PEV	Plug-in Electric Vehicle
BDC	Bidirectional DC-DC Converter
CI	Coupled Inductor
CC	Capacitor Clamping
VC	Voltage Clamping
L_1, L_2	Primary and Secondary inductances of Coupled Inductor
n_1, n_2	number of turns in primary and secondary inductors
N	Turns ratio of Coupled Inductor
k	Coupling Co-efficient
L_{m1} and L_{m2}	Magnetizing inductances of Coupled Inductor
L_{k1} and L_{k2}	Leakage inductances of Coupled Inductor

Appendix A

The list of coefficients for transfer functions used in Equations (30) and (31)

$$k_8 = L_1(V_{in}-v_d)(R+r_{c1}(N+1)) + I_{load}L_1R(R+r_{c1})(1-Nd) - (N-d)(v_d - I_{load}r_{c1})L_1R + L_1NRV_{in}(1+d) + (R+r_{c1})(v_d+NV_{in})L_1Nd + L_1NV_{in}dr_{c1} - I_{load}NRd^2r_{c1}(r_{L1}+r_{on})$$

$$k_9 = \begin{bmatrix} (r_{L1}+r_{on})\left(RV_{in}+V_{in}r_{c1}+\left(-Nr_{c1}v_d+I_{load}NR^2-NRv_d\right)\left(1-d^2\right)+N^2V_{in}d^2(R+r_{c1})+I_{load}NRr_{c1}\right)-R^2V_{in}(d-1)^2 \\ -Rv_d(2r_{L1}+r_{L2})-NR^2V_{in}(d-1)^2-r_{c1}v_d(2r_{L1}+r_{L2}+r_{on})+I_{load}R^2(2r_{L1}+r_{L2}+r_{c1}+r_{on})-I_{load}NRd^2r_{c1}(r_{L1}+r_{c1}) \\ +(r_{L1}+r_{L2})(2dr_{c1}v_d+2I_{load}Rr_{c1}(1-d)+2NV_{in}dr_{c1})+(r_{L1}+r_{L2}+r_{c1})\left(-2I_{load}R^2d+2Rdv_d+2NRV_{in}d\right)-I_{load}L_1NRdr_{c1} \\ +(r_{L2}+r_{c1}-r_{on})\left(-R^2d^2v_d+I_{load}R^2d^2-NRV_{in}\left(1+d^2\right)\right)+I_{load}Rr_{c1}r_{on}-Rv_d(r_{c1}+r_{on})+(r_{L2}-r_{on})\left(-d^2r_{c1}v_d-NV_{in}r_{c1}\left(1+d^2\right)+I_{load}Rd^2r_{c1}\right) \end{bmatrix}$$

$$k_{10} = R(r_{L1}+r_{L2})+r_{c1}(r_{L1}+r_{L2}+R)+R^2(d-1)^2-Rd(r_{L2}+r_{c1}-r_{on})-dr_{c1}(r_{L2}-r_{on})+Nd(r_{L1}+r_{on})(R+r_{c1})$$

$$k_{11} = \begin{bmatrix} L_1(R+r_{c1})(1+N)+C_1R^2(r_{L1}+r_{L2}+r_{c1})+C_1Rr_{c1}^2(1-d) \\ +(r_{L1}+r_{L2})\left(C_1r_{c1}^2+2C_1Rr_{c1}\right)-C_1R^2d(r_{L2}+r_{c1}-r_{on}) \\ -(r_{L2}-r_{on})\left(C_1dr_{c1}^2+2C_1Rdr_{c1}\right)+(r_{L1}+r_{on})\left(C_1NR^2d+C_1Ndr_{c1}^2+2C_1NRdr_{c1}\right) \end{bmatrix}$$

$$k_{12} = \begin{bmatrix} R(r_{L1}+r_{L2})+r_{c1}(r_{L1}+r_{L2}+R)+R^2(d-1)^2 \\ -Rd(r_{L2}+r_{c1}-r_{on})-dr_{c1}(r_{L2}-r_{on})+Nd(r_{L1}+r_{on})(R+r_{c1}) \end{bmatrix}$$

$$k_{13} = (1+N)\left[C_1L_1\left(R^2+r_{c1}^2\right)+2C_1L_1Rr_{c1}\right]$$

$$k_{14} = \begin{bmatrix} C_1R^3V_{in}(1+N-d)+(r_{L1}+r_{on})\left(-C_1I_{load}R^3(1+N)+C_1v_d\left(R^2+r_{c1}^2\right)+2C_1Rr_{c1}v_d\right) \\ -C_1I_{load}Rr_{c1}^2-2C_1I_{load}R^2r_{c1}(1+N)+C_1Nv_d\left(R^2+r_{c1}^2\right)+2C_1NRr_{c1}v_d+\left(C_1R^2V_{in}\right)(r_{L2}+2r_{c1})(1+N) \\ +(r_{L2}-r_{on})\left(C_1V_{in}r_{c1}^2+2C_1RV_{in}r_{c1}\right)(1+N)-C_1NR^2V_{in}d(R+r_{c1})+C_1NRV_{in}r_{c1}^2-C_1R^2V_{in}(Nr_{on}+dr_{c1})-C_1I_{load}NRr_{c1}^2(r_{L1}+r_{c1}) \end{bmatrix}$$

$$k_{15} = \begin{bmatrix} I_{load}R^3(d-1)^2+R^2V_{in}\left(2+N-2d-Nd^2\right)-R^2v_d(1+d)^2 \\ -R^2d^2(v_d+NV_{in})+(RV_{in}(r_{L2}+r_{c1}-r_{on})+(r_{L2}-r_{on})V_{in}r_{c1})(1+N) \\ (r_{L1}+r_{on})\left(Rv_d+r_{c1}v_d(1+N)-I_{load}R^2(1+N)-I_{load}Rr_{c1}(1+N)+NRv_d\right) \end{bmatrix}$$

$$k_{16} = \begin{bmatrix} R(r_{L1}+r_{L2})+r_{c1}(r_{L1}+r_{L2}+R)+R^2(d-1)^2 \\ -Rd(r_{L2}+r_{c1}-r_{on})-dr_{c1}(r_{L2}-r_{on})+Nd(r_{L1}+r_{on})(R+r_{c1}) \end{bmatrix}$$

$$k_{17} = \begin{bmatrix} L_1(R+r_{c1})(1+N)+C_1R^2(r_{L1}+r_{L2}+r_{c1})+C_1Rr_{c1}^2(1-d) \\ +(r_{L1}+r_{L2})\left(C_1r_{c1}^2+2C_1Rr_{c1}\right)-C_1R^2d(r_{L2}+r_{c1}-r_{on}) \\ -(r_{L2}-r_{on})\left(C_1dr_{c1}^2+2C_1Rdr_{c1}\right)+(r_{L1}+r_{on})\left(C_1NR^2d+C_1Ndr_{c1}^2+2C_1NRdr_{c1}\right) \end{bmatrix}$$

$$k_{18} = \begin{bmatrix} R(r_{L1}+r_{L2})+r_{c1}(r_{L1}+r_{L2}+R)+R^2(d-1)^2 \\ -Rd(r_{L2}+r_{c1}-r_{on})-dr_{c1}(r_{L2}-r_{on})+Nd(r_{L1}+r_{on})(R+r_{c1}) \end{bmatrix}$$

$$k_{19} = (1+N)\left[C_1L_1\left(R^2+r_{c1}^2\right)+2C_1L_1Rr_{c1}\right]$$

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