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Baseline for Split DC Link Design in Three-Phase Three-Level Converters Operating with Unity Power Factor Based on Low-Frequency Partial Voltage Oscillations

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Abstract: The study sets a baseline for split DC link capacitance values and voltage set points in three-phase three-level AC/DC (or DC/AC) converters operating with unity power factor. In order to equalize the average values of partial DC link voltages, the controller generates a zero-sequence containing DC components only while employing neither dedicated DC link capacitance balancing hardware nor high-order zero-sequence component injection. Such a baseline is required in order to evaluate the effectiveness of different DC link capacitance reduction methods proposed in the literature. Unlike most previous works, utilizing neutral point current based on cumbersome analytical expressions to determine neutral point potential oscillations, the instantaneous power balance-based approach is employed in this paper, resulting in greatly simplified and more intuitive expressions. It is demonstrated that while the total DC link voltage is low-frequency ripple-free under unity power factor balanced AC-side operation, split DC link capacitors absorb triple-fundamental frequency power components with one-sixth load power magnitude. This yields significant opposite phase partial voltage ripples. In such a case, selection of DC link capacitances and voltage set points must take into account the expected values of AC-side phase voltage magnitude and split DC link capacitor voltage and current ratings. Simulation and experimental results validate the proposed methodology by application to a 10 kVA T-type converter prototype.

Keywords: three-phase three-level converters; split DC link; capacitance; voltage set point

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1. Introduction

Due to ever-increasing power demand of modern energy systems, the use of controlled high-power AC/DC and DC/AC converters has become more widespread [1]. Multilevel converters possess several important advantages over classical two-level converters such as better efficiency, lower dv/dt stress and better lower total harmonic distortion of the output voltage [2]. The most common topologies of multilevel converters are cascaded H-bridge, flying capacitor and neutral point clamped [3].

Multilevel converters are widely used in dual-stage power conversion systems with intermediate DC voltage link [4–9]. The DC link is typically realized by a single capacitor in the case of two-level conversion or multiple split capacitors in the case of multilevel conversion [10,11], providing power decoupling between the stages so that both converters can be controlled independently by various PWM methods [12–18]. Size, weight and price of DC link capacitors vary according to DC link voltage and power conversion system rating [19]. Furthermore, the lifetime of the capacitors is limited and it influences the reliability of the whole system [20]. Therefore, DC link voltages and capacitance values should be minimized [21–23].

Three-level three-phase AC/DC and DC/AC converters have been identified as the most viable topology for power ratings from 10–100 kVA and are widely used in indus-

try [24]. Efficiency, reliability and output waveform quality of three-level converters are strongly dependent on the employed PWM method [25]. In case carrier-based PWM is applied, the main difference between the PWM methods is related to the zero-sequence voltage injection aimed to balance the split DC link capacitance voltages [26]. It should be emphasized that split capacitance balancing may be accomplished utilizing additional dedicated hardware [27,28], however, such a solution would increase system cost and physical size. On the other hand, different zero-sequence injection methods have been proposed over the years, allowing balancing of either average values of split DC link voltages in case of pure DC zero-sequence signal or instantaneous values of split DC link voltages in case the zero-sequence signal contains both DC and higher-order components [29–33]. Pure DC zero-sequence injection is the minimum required to sustain the DC link energy balance and is considered as the baseline in this paper. However, low-frequency neutral point voltage oscillations would appear under such an operation, requiring careful selection of both DC link capacitance values and corresponding voltage set points. Previous works evaluated the low-frequency neutral point voltage oscillations utilizing neutral point expression, which is quite cumbersome and cannot obtain an explicit analytical form [34,35]. Consequently, this paper proposes a methodology based on instantaneous split DC link powers rather than on neutral point current, allowing quantifying corresponding voltage oscillations analytically and intuitively. As a result, clear design guidelines are provided for split DC link capacitances and voltage set point values.

Since the paper focuses on low-frequency oscillations, switching frequency-related components are ignored for brevity in the presented discussion and may be adopted if needed from [35,36]. It is revealed that while the DC link voltage is low-frequency oscillation-free under unity power factor balanced AC-side operation, split DC link capacitors absorb triple-fundamental frequency one-sixth load magnitude powers, yielding opposite phase voltage oscillations. Consequently, selection of DC link capacitances and voltage set points must take into account the expected values of AC-side phase voltage magnitude and split DC link capacitor voltage and current ratings.

The outcomes of the proposed methodology may be used as a baseline for evaluation of advanced high-order zero-sequence injection algorithms, aimed to decrease low-frequency neutral point voltage oscillations and reduce the values of utilized split DC link capacitances. The presented findings' validity is well-supported by simulations and experiments.

2. Materials and Methods

A typical three-phase power conversion system is depicted in Figure 1. The system consists of an AC/DC (or DC/AC) converter, DC link and DC/DC converter. It should be emphasized that the energy flow direction may be either from the AC- to DC-side or vice versa (i.e., "Load" in Figure 1 denotes a power source if the energy flows from the DC- to AC-side). Moreover, the DC link may be formed either by two terminals (X, Y) in case of two-level conversion or three terminals (X, O, Y) in case of three-level conversion. Upon balanced unity power factor operation, steady-state AC-side quantities (all the signals in the subsequent discussion are switching-cycle averaged) are given by

$$\begin{aligned} \vec{v}_{RST}(t) &= \begin{pmatrix} v_{RN}(t) \\ v_{SN}(t) \\ v_{TN}(t) \end{pmatrix} = V_M \begin{pmatrix} \sin(\omega t) \\ \sin(\omega t - \varphi) \\ \sin(\omega t + \varphi) \end{pmatrix} \\ \vec{i}_{RST}(t) &= \begin{pmatrix} i_R(t) \\ i_S(t) \\ i_T(t) \end{pmatrix} = I_M \begin{pmatrix} \sin(\omega t) \\ \sin(\omega t - \varphi) \\ \sin(\omega t + \varphi) \end{pmatrix} \end{aligned} \quad (1)$$

with $\varphi = 2\pi/3$, attained by applying pulse-width modulation signals of the form [29]

$$\vec{m}_{RST}(t) = \begin{pmatrix} m_R(t) \\ m_S(t) \\ m_T(t) \end{pmatrix} \approx M(t) \begin{pmatrix} \sin(\omega t) \\ \sin(\omega t - \varphi) \\ \sin(\omega t + \varphi) \end{pmatrix} + M_0(t). \tag{2}$$

The latter are created by the controller shown in Figure 1 with

$$\vec{v}_{DC}(t) = \begin{cases} v_{XY}(t), & 2-level\ converter \\ \begin{pmatrix} v_{XO}(t) \\ v_{YO}(t) \end{pmatrix} & 3-level\ converter \end{cases} \tag{3}$$

and $M(t)$, $M_0(t)$ denoting the modulation index and zero-sequence component, respectively. In case of two-level conversion, $M_0(t)$ in (2) is zero [33]. On the other hand, in the three-level conversion case, $M_0(t)$ contains the DC component only in the baseline design considered in this paper (allowing equalization of split DC link voltage average values), while in advanced designs it may contain both DC and high-order AC components (allowing equalization of split DC link voltage instantaneous values). It should be emphasized that $M_0(t)$ may also be supplied by an additional hardware-based equalization circuit [27,28].

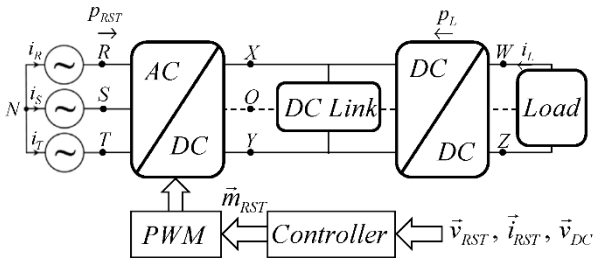

Figure 1. Generalized dual-stage power conversion system.

Considering (1), the instantaneous AC-side phase power vector is given by

$$\vec{p}_{RST}(t) = \begin{pmatrix} p_R(t) \\ p_S(t) \\ p_T(t) \end{pmatrix} = \begin{pmatrix} v_{RN}(t) i_R(t) \\ v_{SN}(t) i_S(t) \\ v_{TN}(t) i_T(t) \end{pmatrix} = \frac{V_M I_M}{2} \begin{pmatrix} 1 - \cos 2(\omega t) \\ 1 - \cos 2(\omega t - \varphi) \\ 1 - \cos 2(\omega t + \varphi) \end{pmatrix}, \tag{4}$$

hence the total AC-side power is ripple free, given by

$$p_{RST}(t) = p_R(t) + p_S(t) + p_S(t) = \frac{3}{2} V_M I_M = P_{RST}. \tag{5}$$

On the other hand, assuming DC-side voltage and current are governed by

$$v_{WZ}(t) = V_L, \quad i_L(t) = I_L, \tag{6}$$

The corresponding steady-state instantaneous power is also constant, given by

$$p_L(t) = v_{WZ}(t) i_L(t) = V_L I_L = P_L. \tag{7}$$

Consequently, the instantaneous system power balance (neglecting conversion losses and energy stored in AC-side L-, LC- or LCL-type filters [37]) is given by

$$P_{RST} = \frac{3}{2} V_M I_M = V_L I_L = P_L, \tag{8}$$

indicating that the instantaneous low-frequency DC link power is zero. In case a converter belongs to the generalized two-level three-phase topology in Figure 2a, its DC link is formed by a single capacitor C_{DC}. Since $M_0(t) = 0$, total switching cycle averaged power at the

converter AC-side $p_{ABC}(t)$ is equal to $p_{RST}(t)$. Hence, $p_C(t) = 0$ (cf. Figure 2b) and $v_{DC}(t)$ is low-frequency ripple free and regulated to a predefined DC link voltage set point V_{DC}^*. On the other hand, in case of a converter belonging to the generalized three-level three-phase topology in Figure 3a, split capacitor pair C_{DC1}, C_{DC2} forms the DC link. According to the above, $p_C(t) = p_{C1}(t) + p_{C2}(t) = 0$ and hence $v_{DC}(t)$ is still low-frequency ripple free, yet without implying zero $p_{C1}(t)$, $p_{C2}(t)$ and low-frequency ripple free $v_{DC1}(t)$, $v_{DC2}(t)$, as shown next. Note that the line connecting the middle point of the DC link with the load middle point is virtual and may be nonexistent in reality. It is only used to demonstrate that the power element p_L may be split into two halves [38].

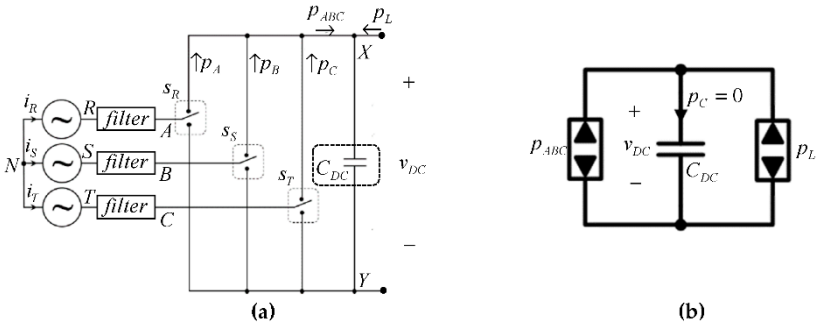

Figure 2. Two-level three-phase power conversion topology. (**a**) Generalized circuitry. (**b**) Power-level equivalent circuit of the DC link.

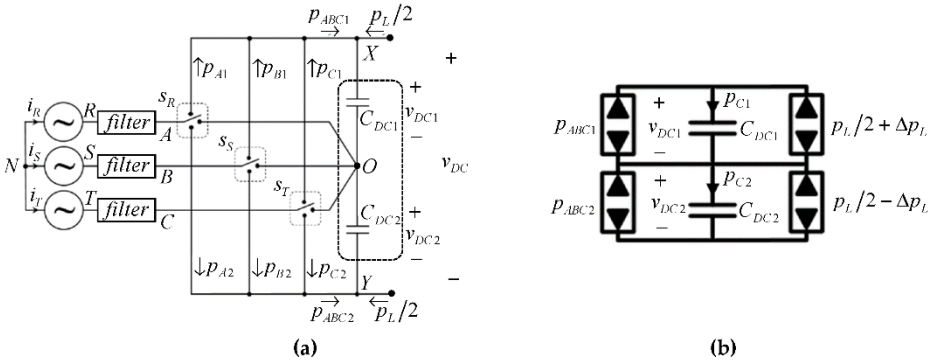

Figure 3. Three-level three-phase power conversion topology. (**a**) Generalized circuitry. (**b**) Power-level equivalent circuit of the DC link.

Since AC-side voltages $\vec{v}_{RST}(t)$ and currents $\vec{i}_{RST}(t)$ in Figure 3 cannot contain zero-sequence components (even for nonzero $M_0(t)$), corresponding power vectors are still given by (4). On the other hand, converter AC-side voltages $\vec{v}_{ABC}(t) = \begin{pmatrix} v_{AN}(t) & v_{BN}(t) & v_{CN}(t) \end{pmatrix}^T$ would contain DC components in case corresponding modulation signals are DC-shifted, yielding (cf. Figure 3b)

$$\vec{p}_{A1B1C1}(t) = \begin{cases} \begin{pmatrix} v_{AN}(t)i_R(t) \\ v_{BN}(t)i_S(t) \\ v_{CN}(t)i_T(t) \end{pmatrix}, & \vec{i}_{ABC}(t) > 0 \\ 0, & \vec{i}_{ABC} < 0 \end{cases} = \begin{pmatrix} p_{A1}(t) + \frac{P_0}{3} \\ p_{B1}(t) + \frac{P_0}{3} \\ p_{C1}(t) + \frac{P_0}{3} \end{pmatrix}$$

$$\vec{p}_{A2B2C2}(t) = \begin{cases} 0, & \vec{i}_{ABC}(t) > 0 \\ \begin{pmatrix} v_{AN}(t)i_R(t) \\ v_{BN}(t)i_S(t) \\ v_{CN}(t)i_T(t) \end{pmatrix}, & \vec{i}_{ABC} < 0 \end{cases} = \begin{pmatrix} p_{A2}(t) - \frac{P_0}{3} \\ p_{B2}(t) - \frac{P_0}{3} \\ p_{C2}(t) - \frac{P_0}{3} \end{pmatrix} \quad (9)$$

with $P_0/3$ denoting the DC power component imposed by M_0. Hence, partial converter AC-side low-frequency powers exchanged with the DC link (neglecting conversion losses and energy stored in AC-side filters) are given by

$$\begin{aligned} p_{ABC1}(t) &= p_{A1}(t) + p_{B1}(t) + p_{C1}(t) \approx \frac{P_L}{2} + P_0 + \frac{P_L}{6}\sin(3\omega t) \\ p_{ABC2}(t) &= p_{A2}(t) + p_{B2}(t) + p_{C2}(t) \approx \frac{P_L}{2} - P_0 - \frac{P_L}{6}\sin(3\omega t) \end{aligned}. \tag{10}$$

Note that P_0 may be either positive or negative, allowing compensating instantaneous energy shortage of any split DC link capacitors. In case of load power mismatch Δp_L (cf. Figure 3b), instantaneous system power balance (8) is sustained with $P_0 = \Delta p_L$ and partial low-frequency DC link powers are given in steady state by

$$\begin{aligned} p_{C1}(t) &= v_{DC1}(t) C_{DC1} \frac{dv_{DC1}(t)}{dt} \approx \frac{P_L}{6}\sin(3\omega t) \\ p_{C2}(t) &= v_{DC2}(t) C_{DC2} \frac{dv_{DC2}(t)}{dt} \approx -\frac{P_L}{6}\sin(3\omega t) \end{aligned}. \tag{11}$$

According to (11), each of the split DC link capacitors absorbs triple-fundamental frequency power component with one-sixth load power magnitude. In case partial capacitor voltages are regulated to set points given by V^*_{DC1} and V^*_{DC2}, respectively, corresponding instantaneous low-frequency energies and steady-state voltages would be

$$\begin{aligned} e_{DC1}(t) &\approx \frac{C_{DC1}}{2}\left(V^*_{DC1}\right)^2 - \frac{P_L}{18\omega}\cos(3\omega t) = \frac{C_{DC1}}{2} v^2_{DC1}(t) \\ e_{DC2}(t) &\approx \frac{C_{DC2}}{2}\left(V^*_{DC2}\right)^2 + \frac{P_L}{18\omega}\cos(3\omega t) = \frac{C_{DC2}}{2} v^2_{DC2}(t) \\ &\Downarrow \\ v_{DC1}(t) &= V^*_{DC1}\sqrt{1 - \frac{P_L}{9\omega\left(V^*_{DC1}\right)^2 C_{DC1}}\cos(3\omega t)} \\ v_{DC2}(t) &= V^*_{DC2}\sqrt{1 + \frac{P_L}{9\omega\left(V^*_{DC2}\right)^2 C_{DC2}}\cos(3\omega t)}, \end{aligned} \tag{12}$$

respectively. Typically,

$$V^*_{DC1} = V^*_{DC2} = 0.5V^*_{DC}, \quad C_{DC1} = C_{DC2} = C_{DC} \tag{13}$$

are employed, therefore (12) reduces to

$$v_{DC1,2}(t) = 0.5V^*_{DC}\sqrt{1 \pm \frac{P_L}{9\omega\left(0.5V^*_{DC}\right)^2 C_{DC}}\cos(3\omega t)} \approx 0.5V^*_{DC} \pm \underbrace{\frac{P_L}{9\omega V^*_{DC} C_{DC}}}_{\Delta V_{DC1,2}}\cos(3\omega t). \tag{14}$$

i.e., split capacitor voltages contain DC components as well as nonzero opposite phase triple-fundamental frequency ripples. The approximation in (14) is valid in practical systems where the low-frequency DC link voltage ripple magnitude $\Delta V_{DC1,2}$ is much lower than the corresponding voltage set point V^*_{DC1}, V^*_{DC2} [39]. Low-frequency split capacitor currents and corresponding RMS values are then obtained as

$$i^{3\omega}_{DC1,2}(t) = C_{DC}\frac{dv_{DC1,2}(t)}{dt} = \mp\frac{P_L}{3V^*_{DC}}\sin(3\omega t) \Rightarrow RMS\left(i^{3\omega}_{DC1,2}\right) = \frac{P_L}{3\sqrt{2}V^*_{DC}}. \tag{15}$$

If split DC link capacitors possess significant equivalent series resistance R_C, then (14) becomes

$$v_{DC1,2}(t) \approx 0.5V_{DC}^{*} \pm \frac{P_L}{9\omega V_{DC}^{*} C_{DC}} \cos(3\omega t) \mp R_C \frac{P_L}{3V_{DC}^{*}} \sin(3\omega t) \tag{16}$$

and the low-frequency DC link ripple magnitude is given by

$$\Delta V_{DC1,2} \approx \frac{P_L}{V_{DC}^{*}} \sqrt{\left(\frac{1}{9\omega C_{DC}}\right)^2 + \left(\frac{R_C}{3}\right)^2}. \tag{17}$$

Instantaneous partial DC link voltages are typically bounded as

$$V_{MIN} < v_{DC1,2}(t) < V_{MAX}, \tag{18}$$

where V_{MAX} is imposed by capacitor (or switching devices) voltage rating and V_{MIN} is dictated by the magnitude of AC-side phase voltages. Combining (18) with (16) yields the required capacitance value, given by

$$C_{DC} > \frac{1}{9\omega \cdot \min\left\{\sqrt{\left(\frac{V_{DC}^{*}}{P_L}\left(V_{MAX} - 0.5V_{DC}^{*}\right)\right)^2 - \left(\frac{R_C}{3}\right)^2},\ \sqrt{\left(\frac{V_{DC}^{*}}{P_L}\left(0.5V_{DC}^{*} - V_{MIN}\right)\right)^2 - \left(\frac{R_C}{3}\right)^2}\right\}}. \tag{19}$$

In order to decrease the DC link capacitance values by utilizing the whole allowable DC link voltage span, DC link voltage set point should be set to [40]

$$V_{DC}^{*} = \sqrt{2\left(V_{MAX}^2 + V_{MIN}^2\right)}, \tag{20}$$

yielding

$$C_{DC} > \frac{1}{9\omega \sqrt{\left(\frac{V_{DC}^{*}}{P_L}\left(V_{MAX} - \sqrt{\frac{V_{MAX}^2 + V_{MIN}^2}{2}}\right)\right)^2 - \left(\frac{R_C}{3}\right)^2}}. \tag{21}$$

Nevertheless, one must recall that according to (15), increasing the DC link voltage set point decreases the RMS value of low-frequency split capacitor currents, and vice versa. If the allowed RMS value of low-frequency split capacitor current is bounded by $I_{RMS,MAX}$, DC link voltage set point must obey

$$V_{DC}^{*} \geq \frac{P_L}{3\sqrt{2} I_{RMS,MAX}}. \tag{22}$$

3. Validation

In order to validate the revealed methodology, consider a 10 kVA LCL filter-based three-phase three-level T-type converter, depicted in Figure 4a. The corresponding experimental prototype is shown in Figure 4b, constructed according to design guidelines given in [41]. The converter was operated at 50 kHz switching frequency by Texas Instruments TMS320F28335 DSP. The power stage was fed by a DC power supply and terminated by a three-phase balanced resistive load, drawing nominal power for phase voltage magnitude of $V_M = 230\sqrt{2}$ V $\approx$ 325 V. The power stage was operated semi-open loop by applying pulse-width modulation signals (2) with $M(t) = 325/(0.5 \cdot V_{DC}^{*})$ (open loop) and $M_0(t)$ determined as shown in Figure 5 with NF_{150} representing a 150 Hz centered notch filter aimed to remove the triple-mains-frequency ripple so that the zero-sequence component contains DC constituent only, as desired, and K_0 denoting a constant gain (closed loop). Simulated (PSIM software) and experimental AC-side variables are depicted in Figure 6 (only one phase current is shown experimentally due to 4-channel oscilloscope usage). It is well-evident that the system operates with unity power factor under rated loading.

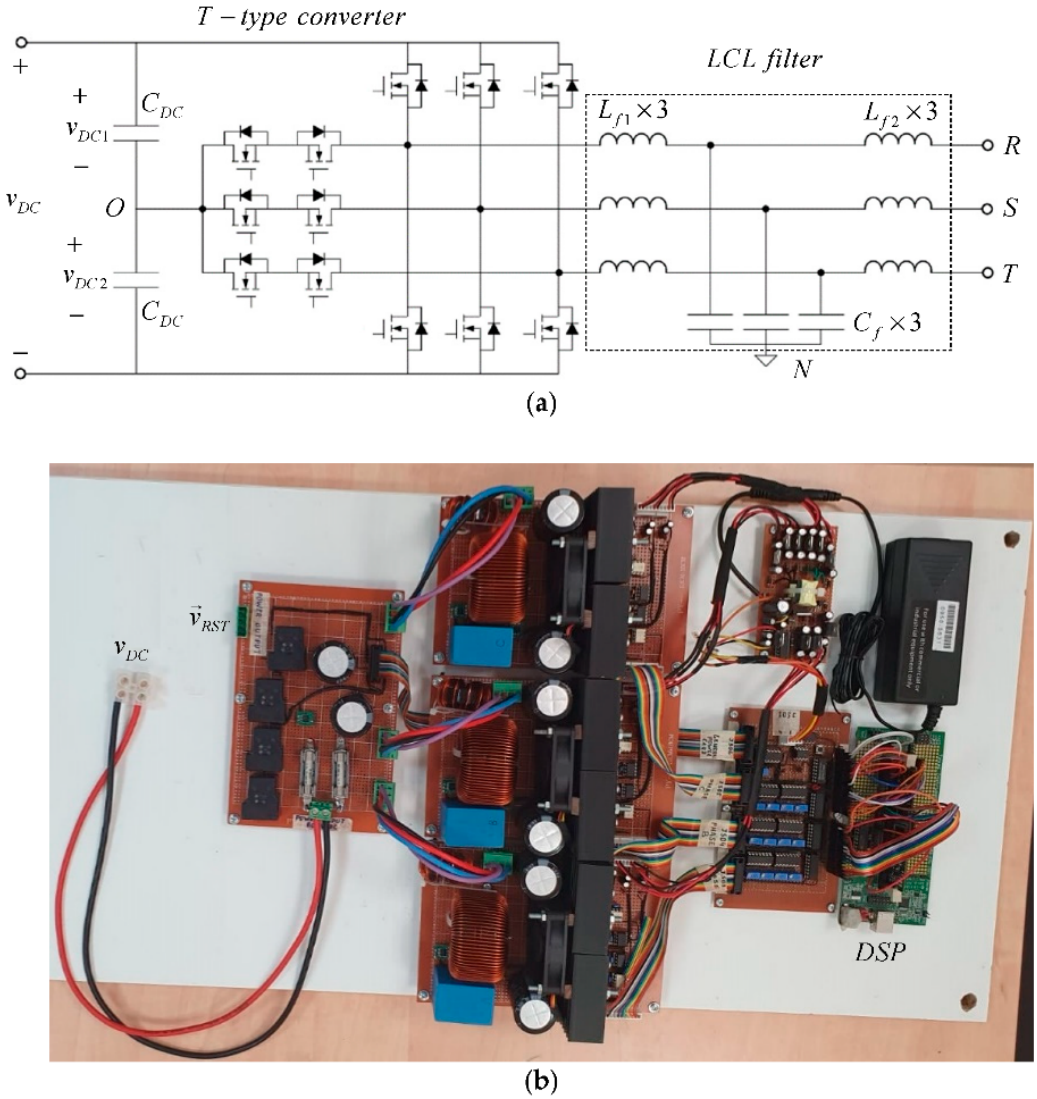

Figure 4. T-type three-phase three-level power converter. (**a**) Power stage circuitry. (**b**) The 10 KVA experimental prototype.

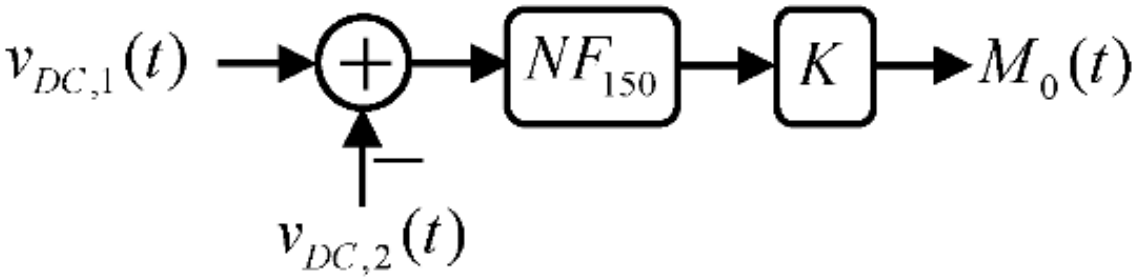

Figure 5. Generation of zero-sequence component $M_0(t)$.

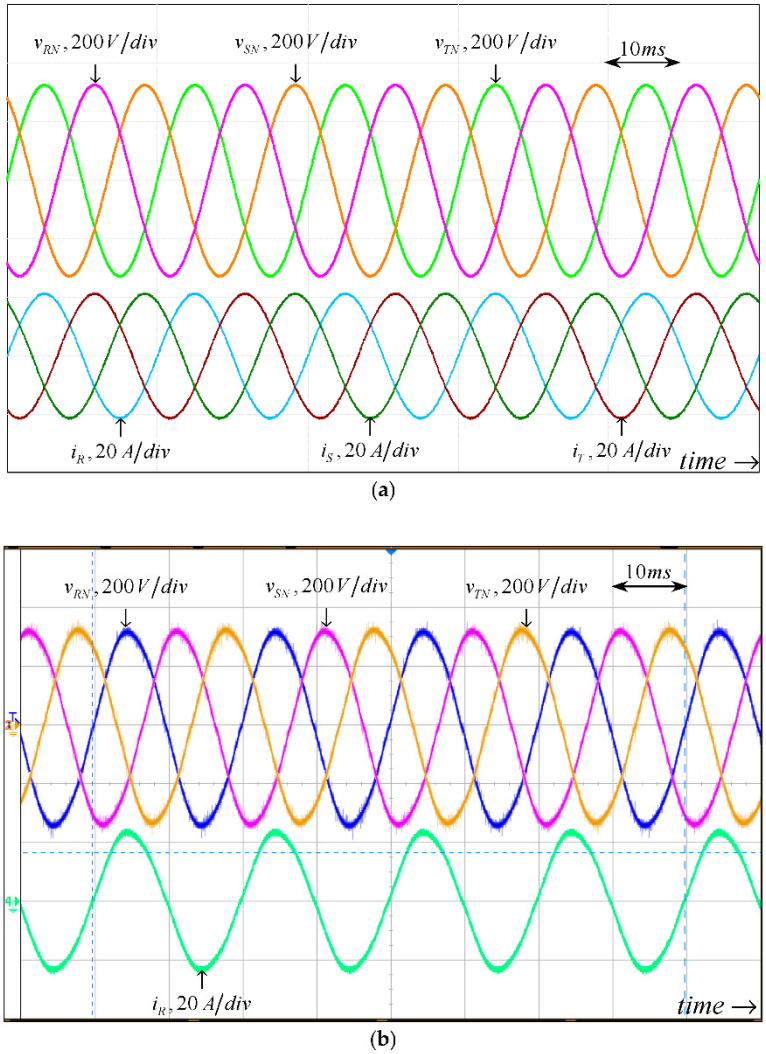

Figure 6. AC-side nominal loaded converter voltages and currents. (**a**) Simulation. (**b**) Experiment.

A. Capacitor low-frequency current rating imposed design

Consider DC link capacitors with low-frequency current rating of 3 A_{RMS}. Then, according to (22),

$$V_{DC}^{*} > \frac{P_L}{9\sqrt{2}} = 786\,V \Rightarrow V_{DC1,2}^{*} > 393\,V \tag{23}$$

must be selected. In case the capacitors are 450 V rated, the corresponding maximum value of the DC link voltage should remain below 410 V (i.e., keeping a 10% margin) to prolong the capacitors' lifetime [42]. Setting V_{DC}^{*} to 790 V (i.e., V_{DC1}^{*} and V_{DC2}^{*} to 395 V) and assuming R_C = 0.5 Ω (cf. (19)), the required DC link capacitance of C_{DC} > 458 μF is imposed. Four parallel connected 110 μF capacitors were employed for validation. The corresponding results are shown in Figure 7. It is well-evident that the maximum value of partial DC link voltages corresponds well to the upper bound constraint. On the other hand, the minimum value of partial DC link voltages is much higher than AC-side voltage magnitude. Experimental results possess a slightly higher switching ripple due to inductive component of practical capacitors, yet the average value of the partial low-frequency DC link voltage ripple magnitude (both simulated and experimental) is about ~10 V, matching analytical prediction in (17) well.

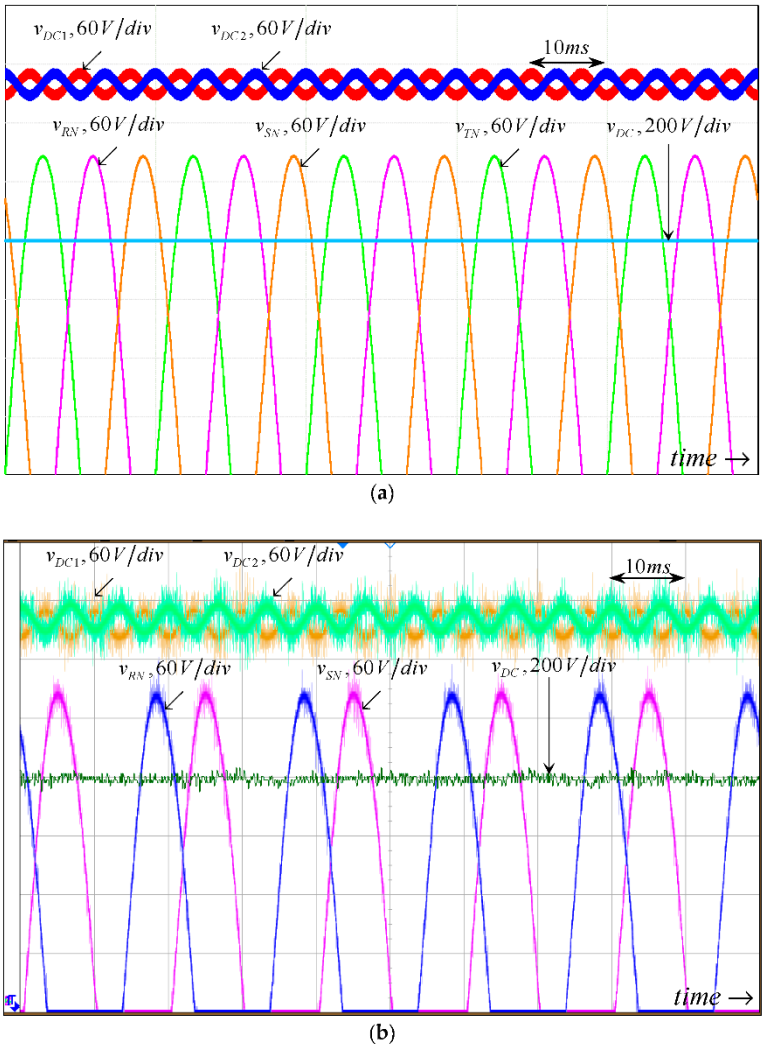

Figure 7. Results of capacitor low-frequency current rating imposed design. (**a**) Simulation. (**b**) Experiment.

B. Capacitor voltage rating imposed design

Next, consider the availability of DC link capacitors with voltage rating of 400 V. Then, the corresponding maximum value of the DC link voltage should remain below 360 V (again, considering a 10% margin for capacitor lifetime elongation). On the other hand, the minimum DC link voltage value should remain above V_M (330 V is selected to allow a safety margin of 5 V). According to (20), in order to utilize the whole allowable DC link voltage span, DC link voltage set point V^*_{DC} should be selected as 695 V (i.e., V^*_{DC1} and V^*_{DC2} set to 347.5 V). Assuming R_C = 0.5 Ω, DC link capacitance of C_{DC} > 433 μF is required according to (21). Again, four parallel connected 110 μF capacitors were employed for validation. The corresponding results are shown in Figure 8. It is well-evident that both the maximum and minimum values of partial DC link voltages correspond well to the upper and lower bound constraints. Once more, experimental results possess a slightly higher switching ripple due to nonideal capacitor usage, yet the average value of the partial low-frequency DC link voltage ripple magnitude (both simulated and experimental) is about ~12 V, matching analytical prediction in (17) well. Compared to the previous experiment, it may be concluded that the ripple has increased due to decreased V^*_{DC}, as expected.

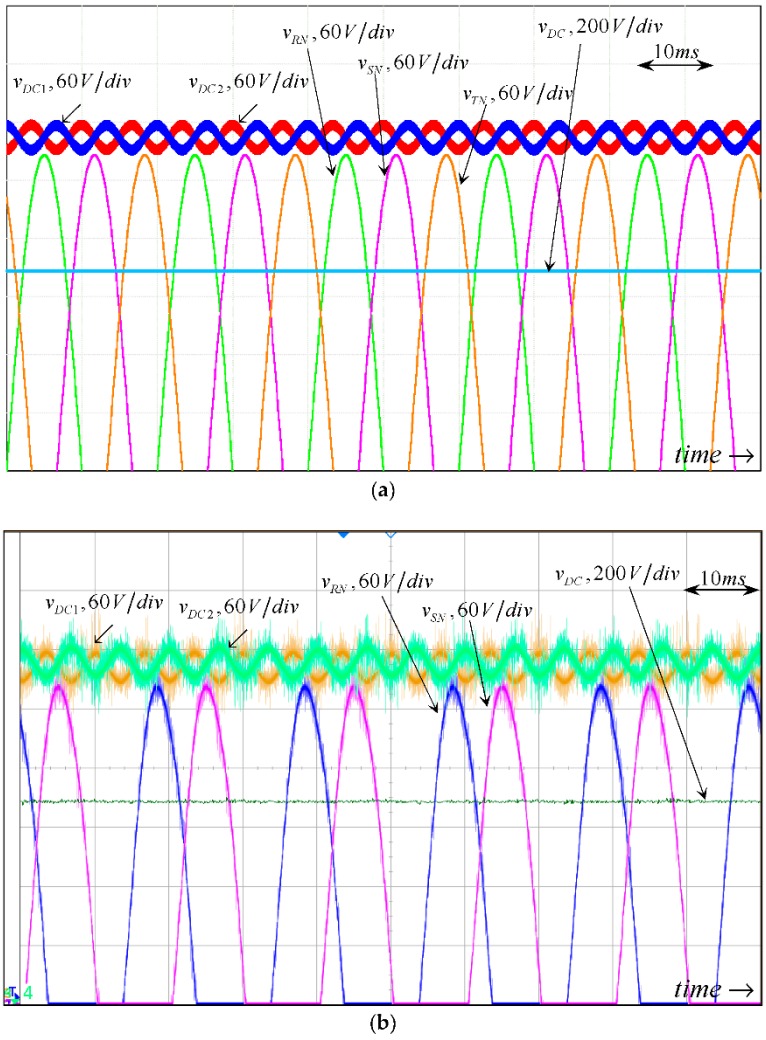

Figure 8. Results of capacitor voltage rating imposed design. (**a**) Simulation. (**b**) Experiment.

4. Conclusions

Design guidelines for split DC link capacitors and corresponding voltage set point value selection for three-phase three-level converters were established in the paper for the baseline case in which only average values of partial DC link voltages are equalized. It was shown that operational restrictions are imposed by the fact that even though the DC link voltage is low-frequency ripple free, partial voltages possess significant anti-phase triple-fundamental-frequency ripples. The proposed methodology utilized instantaneous power balance expressions to obtain simple and intuitive analytical expressions for partial DC link voltage oscillation quantification. Simulations and experiments carried out by applying the proposed methodology to a 10 kVA T-type converter successfully validated the revealed findings.

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