



Article

# Hardware-in-the-Loop Implementation of ROMatrix, a Smart Transformer for Future Power Grids

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**Abstract:** The evolution of power generation brings about extensive changes in other parts of the grid, especially in the transmission and distribution components. Within the scope of the Internet of Energy (IoE), electric power flows more flexibly between different parts of the grid. DC power will play an essential role in IoE. Decentralized photovoltaic panels, energy storage, electric vehicle charging stations, and data centers are some of the significant components of future grids dealing with DC power. As a result, power transformers must be appropriately modified to manage power among the different parts of the grid. A power electronic transformer (PET), also known as a solid-state transformer (SST) or smart transformer (ST), is a solution enabling a power grid to deal with this growing complexity. ROMatrix, as a matrix-converter-based ST, is a developing project targeting future power grids. ROMatrix realizes the application of a medium voltage (MV) transformer using commercially available power electronic semiconductors. Due to the distinctive features of ROMatrix and a high number of switches, the implementation of the control system using a single control board is highly demanding. This paper aims to illustrate the implementation, on a field-programmable gate array (FPGA), of pulse width modulation (SVMPWM) applied to the ROMatrix, considering specific switching patterns. The proposed switching procedure was simulated with PLECS and validated with the hardware-in-the-loop using the OPAL-RT solver.

**Keywords:** hardware-in-the-loop (HIL); LabVIEW; matrix converter (MC); ROMatrix; smart transformer (ST); solid-state transformer (SST); space vector modulation (SVM)



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## 1. Introduction

The growing trend towards distributed generation is transforming electric power systems. The advantages provided by distributed renewable energy, such as reduction of losses in the transmission lines, lower greenhouse effect, cost-effective performance, improved power quality, and increased reliability, are some of the motivations for shifting the pattern from centralized generation to micro-grids, which are based on distributed generators and local loads [1,2]. However, the implementation of these advanced grids is associated with various challenges. Microgrid protection is the most crucial factor to take into consideration. Due to the presence of distributed energy resources (DERs) in microgrids, the direction of the power flow and the magnitude of fault current vary, resulting in a more complicated protection scheme than in traditional grids [3]. The presence of DC grids, both on the generation and the consumer sides, is the other challenge of modern microgrids. Due to the intermittent nature of renewable resources, energy storage systems (ESS), such as DC components, are considered in the grid design. The presence of ESS requires the feasibility of bidirectional energy flow in the grid. In addition, resources such as photovoltaic (PV) systems and fuel cells inherently generate DC power. On the load side, LED lighting, electric vehicle charging stations, data centers, and electronic loads are the major consumer of DC power. Traditional transformers have proved to be entirely inadequate in the face of the ongoing changes to power grids.

The power electronic-based concept named smart transformers (ST), otherwise known as solid-state transformers (SST) or power electronic transformers (PET), are promising

solutions that can process any form of power. STs are able to fulfill the requirements of various generators and loads in the power grids [4]. In addition to enhanced flexibility and controllability, STs facilitate ancillary services in the grid [5,6]. The most common ST strategy is multistage DC/AC conversion and vice versa [7,8].

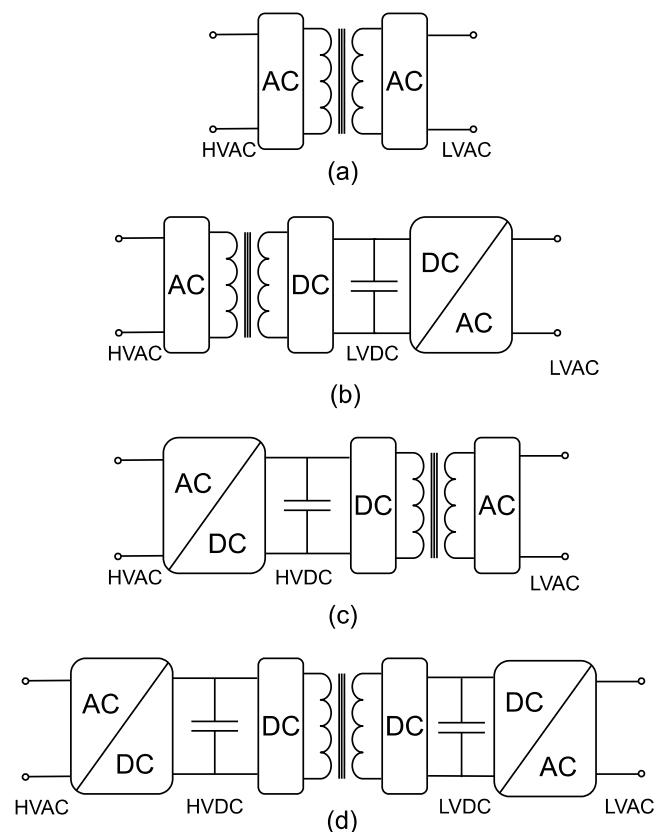
The traditional line frequency transformers have some undeniably remarkable features, such as low production costs, relatively high efficiency, and high reliability. However, they can only perform AC/AC conversion, whilst the need for DC source availability in future grids is a decisive factor [9]. According to [10], by 2030, renewable energies will account for 36% of the world's energy share. This high penetration of the DC grid requires more flexible power management. The advantages of traditional transformers have motivated some researchers to use them with STs, to obtain the benefits of both transformers and cope with the grid growth [11]. In these so-called hybrid transformers, a major part of the power flows through the traditional transformers and only a small fraction flows through the ST. Although traditional transformers offer higher reliability, in the case of any unplanned outages, it can take up to 24 months to receive a replacement transformer [12,13]. In [14], it is mentioned that with an EV penetration of 50%, traditional transformers' life is reduced by 200–300% relative to nonpenetration with uncontrolled charging. That is why STs were reported as one of the top ten emerging technologies by the Massachusetts Institute of Technology (MIT) Technology Review [15]. According to [16], in a grid with AC and DC players, ST is only 30% more expensive than a traditional transformer and its associated power electronic equipment. However, STs' advantages justify this additional cost. In addition to the extra flexibility and functionality, the smaller footprint of ST can lead to financial advantages. In Ref. [17], it is mentioned that ST could be a much better option in crowded city centers, where space is lacking and expensive. In transportation such as planes, trains, and ships, smaller volumes and lighter weights are crucial. In addition, [18] mentions that the modularity of ST would enable moving them with a truck as an emergency replacement for traditional transformers. In contrast to traditional transformers, SSTs do not use oil in their structure, making them environmentally friendly and safer in terms of fires or explosion. Finally, a drastic reduction in SiC devices is expected [19,20], which could change the status quo in favor of STs.

Smart grid (SG) technology optimizes a grid's performance by combining power systems and information and communication technology (ICT). That is, SG makes the power grid more flexible, efficient, and economical [21].

Having evolved from the smart grid, the internet of energy (IoE), also known as energy internet (EI), is another promising topic in power systems [22,23]. IoE eliminates the limits and shortcomings of the smart grids and integrates further infrastructure such as transportation systems and natural gas networks into power systems [24]. Renewable energy resources play a more dominant role in IoE than smart grids [25]. In addition, in grids based on the IoE, bidirectional energy transmission enables users to complete peer-to-peer transactions [26]. Taking these accelerating changes into account, future power transformers must process energy in a complex manner, while assuring a flexible and reliable power flow. As mentioned before, conventional power transformers will be unable to handle these forthcoming changes.

Different classifications for STs have been proposed in the literature [27,28]. Figure 1 presents different topologies of ST based on the number of AC/DC or DC/AC conversion stages [29], namely single-stage, two-stage, and three-stage ST transformers. Terminals for high-voltage alternating current (HVAC), high-voltage direct current (HVDC), low-voltage alternating current (LVAC), and low-voltage direct current (LVDC) are also indicated in Figure 1. Each topology has its pros and cons [30]; for example, a lower weight, smaller footprint, lower price, and fewer semiconductors give the single-stage topology (Figure 1a) distinct advantages over two and three-stage topologies. Nevertheless, due to the lack of a DC-link, disturbances of one side can easily be transferred to the other side. A lack of interaction with local DC components of the grid, such as DC loads, transmissions, renewables, and battery storage is another shortcoming of these topologies. Two single-

stage topologies based on a full-bridge converter and flyback converter are presented in [31]. Depending on the location of the isolation transformer, the two-stage ST has two different structures. In the first structure, shown in Figure 1b, high-voltage AC is converted into low-voltage DC and then into low-voltage AC [32]. Meanwhile, in the second structure, illustrated in Figure 1c, high-voltage AC is converted into high-voltage DC and then inverted into low-voltage AC. Two-stage topologies offer more functionality in comparison to single-stage topologies, such as interacting with DC components of the grid, decoupling the input and the output of the converter, and compensating for reactive power. Two-stage topologies, however, have a more complex control in comparison to single-stage topologies. In addition, obtaining zero voltage switching in these topologies is challenging, resulting in a reduced efficiency.



**Figure 1.** Classification of STs based on conversion stages, (a) single-stage ST, (b,c) two-stage ST, and (d) three-stage ST.

Three-stage STs, as presented in Figure 1d, comprise an AC/DC conversion followed by DC/DC and DC/AC conversion. There is an isolation transformer in the DC/DC stage. This topology has two DC links, one on the high-voltage side and the other on the low-voltage side, giving the transformer a higher degree of flexibility. All features of the previous topologies are achievable with this topology, making it the most favorable ST topology for the grid. Needless to say, the presence of three stages in this topology gives rise to higher costs and losses.

Due to the limited availability of commercially available power electronic switches and magnetic components, building an ST adaptable to high voltage (HV) and medium voltage (MV) grids requires a series of connections of several modules. Modular multilevel converters (MMC) and cascaded H-bridge converters (CHB) are the two common methods used to cope with higher voltage levels [33]. However, these two topologies suffer from serious disadvantages [34]. Both topologies require too many components, which is responsible for their lower reliability, higher cost, and complex control. CHB requires many isolated resources, provided by transformers and power electronic devices. Compared to

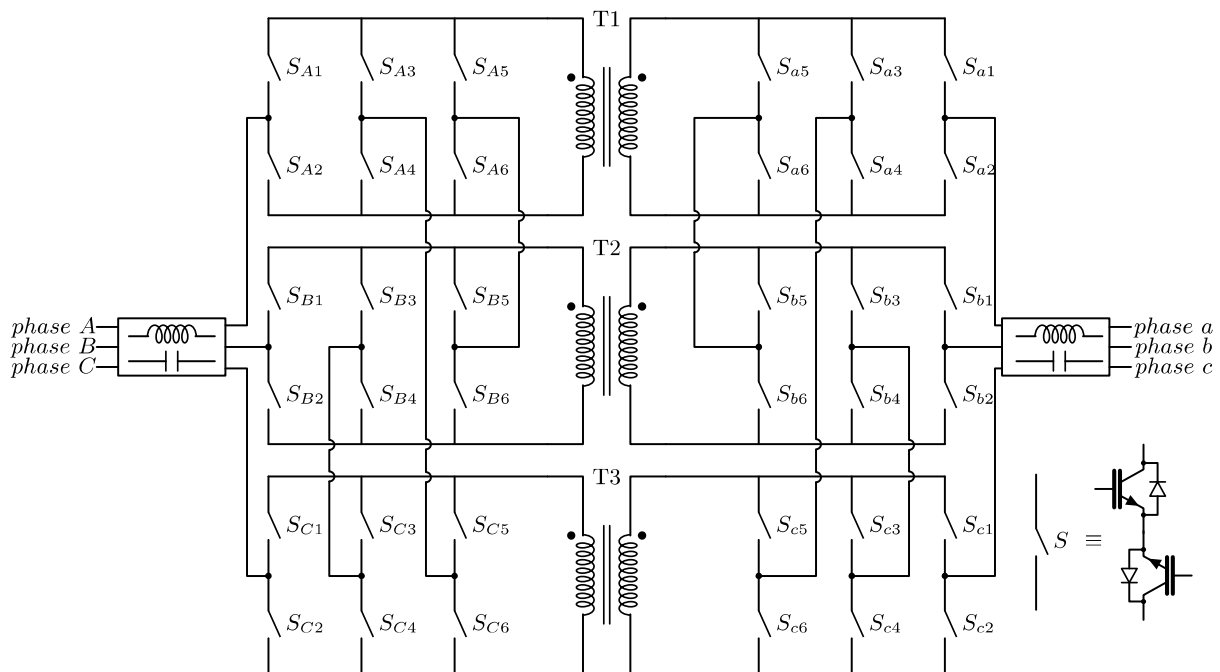
conventional inverters, an MMC requires large capacitance values. In addition, unbalanced capacitor voltages directly affect the output voltages' quality. Thus, it is essential to devise a strategy to ensure an equal voltage level in capacitors, which brings extra complexity and cost [35,36].

Due to their lack of capacitors, matrix converters do not deal with the control challenges of CHB and MMC. Eliminating the capacitors and their related components (such as pre-charge resistors in parallel with a thyristor) leads to a smaller footprint, affordable price, and enhanced reliability. Matrix converters can also control the input power factor without using a power factor correction (PFC) stage, which is an inevitable part of conventional converters. Several ST topologies based on matrix converters have been proposed in the literature. The topology proposed in [37] uses 144 semiconductor switches and nine transformers to convert MV to LV. The high number of elements in this topology is its main disadvantage, which results in a higher cost and complicated control. Moreover, the switches must tolerate phase-to-neutral voltage when they are turned off. The topology studied in [38] and [39] is not designed for a MV grid and the switches cannot tolerate higher voltage levels. The ST introduced in [40] is a modular multilevel matrix converter and was designed for high-voltage AC substations. However, in contrast to the nature of matrix converters, it utilizes numerous cell capacitors in its structure. The same problem is seen in the matrix converter presented in [41], and this converter requires a capacitor in its structure.

ROMatrix, an ongoing ST project, was first introduced in [42] and aims to remove ST's limitations in medium voltage grids. Due to the lack of capacitors in the structure, it does not suffer from the problems associated with capacitors. To comply with the perspective of the IoE, in future works, ROMatrix will be developed into a multi-port converter with an extra port, to include DC grids in its design. However, the multi-port design of ROMatrix is beyond the scope of this paper. The main focus of this paper is implementing space vector modulation pulse width modulation (SVMPWM) control of ROMatrix on a control board, which utilizes the field-programmable gate array (FPGA). Due to the unique characteristics of the ROMatrix, its switching pattern differs from other matrix converters. The switching procedure is validated through a real-time hardware-in-the-loop (HIL) system. The rest of the current manuscript is organized as follows: the second section briefly reviews the performance principles of ROMatrix. The switching procedure of the converter is presented in the third section. The simulation results, SVMPWM implementation on FPGA, and HIL validation are illustrated in the fourth and fifth sections. Finally, the sixth section concludes the paper.

## 2. Performance Principles of ROMatrix

The ROMatrix topology, which consists of three identical modules, is demonstrated in Figure 2. The modules are indirect matrix converters (IMC) isolated by a medium frequency transformer (MFT). Each module belongs to one of the phases in the input/output. There are three legs on each side of the modules. One of the legs connects the module to the input/output phases; the other two legs connect the module to other modules. Every leg used in the modules is made up of two bidirectional switches, which means four semiconductor switches exist in each leg. A detailed scheme of the switches is shown in Figure 2. Using bidirectional switches enables ROMatrix to guarantee complete control over the bidirectional power flow. The proposed topology would handle MV in the grid utilizing commercially available power electronics semiconductors. Therefore, switching arrangements that apply voltage values beyond the maximum rating of the semiconductors and transformers must be avoided.



**Figure 2.** ROMatrix topology.

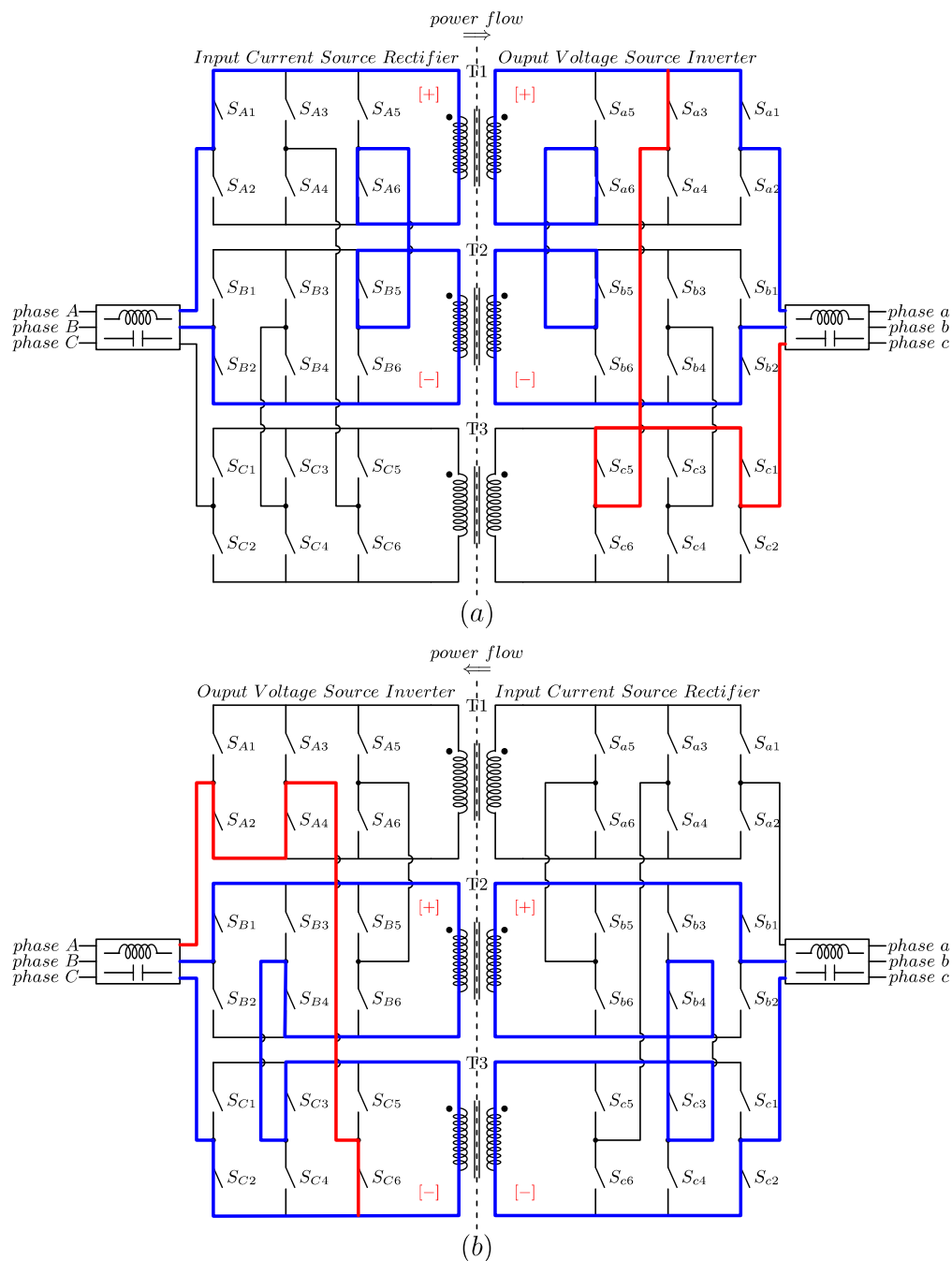
Given that the left side of the transformer is the MV side, in each instant, the phase-to-phase input voltage must be tolerated by two transformers in series. Similarly, the voltage applied to an open switch must be shared with another switch in series. In addition, there are some other common rules for the inverters that are taken into consideration. More specifically, in conventional two-stage converters, the input side is a rectifier, in which just two out of three phases conduct in a specific time interval, while the third phase is disconnected. Similarly, in the ROMatrix, the converter's input side behaves as a current rectifier (CSR); thus, in any interval, only two of the phases are responsible for transferring power from the input to the output. Furthermore, short-circuiting between phases must be avoided on the input side. In conventional voltage source inverters (VSI), a DC-link capacitor interconnects the input and output. Thus, switching states that make short circuits across the capacitor must be avoided. Due to the inductive nature of generic loads, switching states leading to an open circuit at the output should also be avoided.

In matrix converters, there is no DC-link capacitor, so by appropriate switching of the input phases, an instantaneous DC-link is created between the input and the output. This DC-link is called a virtual DC-link, implying the lack of a physical capacitor in the system. Here, the output-side converter acts as a VSI, and the same rules must be observed. Despite the high number of switches, these constraints limit switching states and facilitate control of the converter. Figure 3 depicts the two permissible switching states of the ROMatrix. In the first state, Figure 3a, since the power flow is from the left to the right of the converter, input phase A and phase B create a virtual DC-link. The polarity of this DC-link is indicated by [+] and [−]. In addition, on the output side, such as in a conventional VSI, the phases are connected either to the positive or negative pole of this DC-link.

However, in Figure 3b, due to the direction of the power flow, the converter's right side, grid "abc", transfers power to its left side, grid "ABC." As a result, in this case, the right side of the converter acts as CSR, and the left side acts as a VSI.

A qualitative comparison among three grid-scale converters, namely solid-state power substation (SSPS) [43], universal and flexible power management (UNIFLEX PM) [44,45], and ROMatrix is provided in Table 1. The superiority of the ROMatrix over the two other converters is the lower number of switches used in its structure. In addition, unlike UNIFLEX PM, ROMatrix does not have numerous DC-link stages containing electrolyte

capacitors in its topology. The only shortcoming of the ROMatrix in comparison to the two other topologies is that it is not scalable.



**Figure 3.** Examples of the permissible switching states: (a) power flow from grid “ABC” to “abc” and (b) power flow from grid “abc” to “ABC”.

**Table 1.** Comparing the general characteristics of the three grid-scale converters.

	SSPS	UNIFLEX PM	ROMatrix
Number of switches	96	96	72
Number of intermediate DC-link stages	0	24	0
Modular topology	Yes	Yes	Yes, not scalable

### 3. Switching Strategy

In the current work, to control ROMatrix, space vector modulation (SVM) is utilized. Assuming that the power flow is from left to right, as in Figure 3a, the converters on the left side will act as a current rectifier and are responsible for creating a virtual DC link in the circuit. Instead, the converters on the VSI side, generate the desired three-phase voltage at the output.

The space vector modulation of the input side of ROMatrix is shown in Figure 4, in which  $I_1$  [A, B] means phase A is connected to the positive pole of the virtual DC-link and phase B is connected to the negative pole of the DC-link. The arrangements of the switches in Figure 3a represent  $I_1$ . In addition to the six active vectors, there are three zero vectors, in which positive and negative poles are connected to the same phase. Supposing that the reference input current,  $I_{ref}$ , is located in the first sector (the vector  $I'_{ref}$  will be described a little further on), it will be synthesized with the two adjacent vectors, here  $I_1$  and  $I_2$ , together with one of the zero vectors. The equation for transferring  $I_{ref}$  to  $\alpha\beta$ -frame is as follows [46]:

$$\bar{I}_{ref} = i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{-j\frac{2\pi}{3}} = \frac{3}{2} I_i e^{j\omega_i t} \tag{1}$$

where  $I_i$  is the magnitude of the phase currents;  $\omega_i$  is the angular frequency of the input current; and  $i_a, i_b,$  and  $i_c$  are the instant values of the phases. Then:

$$\begin{aligned} d_\alpha &= \frac{T_\alpha}{T_s} = m_c \cdot \sin(60 - \theta_i) \\ d_\beta &= \frac{T_\beta}{T_s} = m_c \cdot \sin(\theta_i) \\ d_{0i} &= 1 - d_\alpha - d_\beta \end{aligned} \tag{2}$$

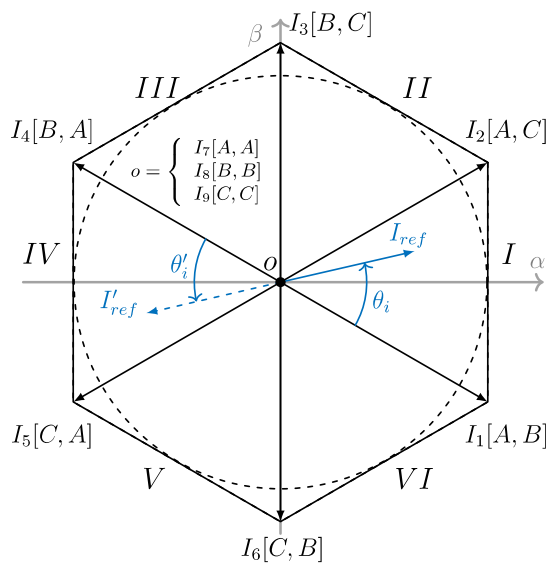


Figure 4. Space vectors of the input current rectifier.

Here,  $d_\alpha$  and  $d_\beta$  are the duty cycles of the sector’s first and second vectors. The rest of the switching period is covered by one of the zero vectors, indicated by  $d_{0i}$ . In addition,  $m_c$  is the modulation index of the current source rectifier and is equal to

$$0 \leq m_c = \frac{I_{ref}}{I_{dc}} \leq 1 \tag{3}$$

in which  $I_{ref}$  is the amplitude of the desired input phase current and  $I_{dc}$  is the current synthesized in the dc link. It is worth bearing in mind that, generally, there is no predefined value for  $I_{ref}$  and the only important parameter is  $\theta_i$ , which determines the power factor. Since the input CSR must supply  $I_{dc}$ , which is assigned by the output load,  $I_{ref}$  is set as equal to  $I_{dc}$  leading to  $m_c = 1$ . In this design, a phase-locked loop (PLL) measures the angle of the

three-phase input line voltages. This algorithm applies the appropriate  $\theta_i$  with reference to the angle of the input line voltages, considering the desired power factor.

For the output VSI, the space vectors are demonstrated in Figure 5, formed by six active vectors and two zero vectors. It should be noted that in this paper, the SVM PWM is implemented using line voltages, so the magnitudes of vectors are proportional to line values. The state of the converter on the output side of Figure 3a corresponds to the  $V_1$  in Figure 5.

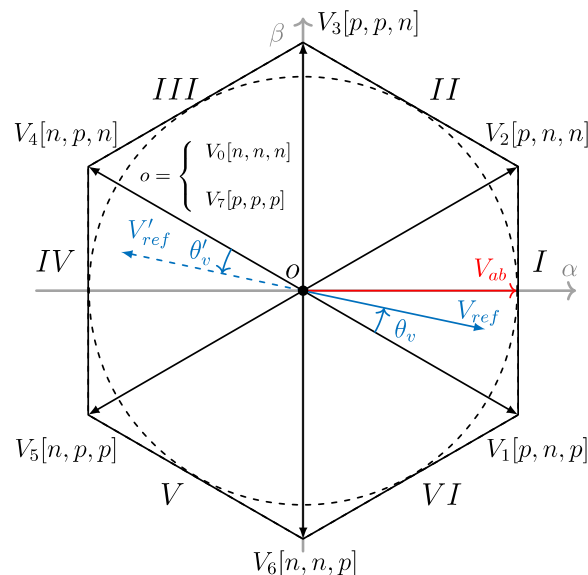


Figure 5. Space vectors for the output voltage source inverter.

During one switching period, the reference voltage vector  $V_{ref}$  is synthesized by two neighboring vectors and an appropriate combination of the zero vectors. Again,  $V'_{ref}$  will be explained later in this section. For instance, in Figure 5, the reference vector is inside sector 1, then by switching  $V_1$  and  $V_2$ , the reference voltage can be built. Depending on the magnitude of the reference vector, zero vectors may be required to cover the whole range of the switching period. The equations for the SVM modulation of the output converter are represented as follows:

$$\begin{aligned}
 d_\gamma &= \frac{T_\gamma}{T_s} = m_v \cdot \sin(60 - \theta_v) \\
 d_\delta &= \frac{T_\delta}{T_s} = m_v \cdot \sin(\theta_v) \\
 d_{0v} &= 1 - d_\gamma - d_\delta
 \end{aligned}
 \tag{4}$$

where  $d_\gamma$  and  $d_\delta$  are the duty cycle of the first and the second vectors in the sectors, respectively. Moreover,  $d_{0v}$  represents the duty cycles of the zero vectors. Finally,  $m_v$  is the modulation index of the VSI, which is defined as:

$$0 \leq m_v = \frac{V_{ref}}{V_{dc}} \leq 1
 \tag{5}$$

In contrast to the SVM PWM of the regular VSI with a fixed voltage in the DC link, the output voltage of the matrix converter directly correlates with the behavior of the input converter. Since CSR employs two different vectors during one switching period, two voltage levels will appear in the virtual DC link. Then, the switching pattern in Figure 6 is considered to fulfill the switching scheme in the input and the output. In this switching pattern, it is assumed that both reference vectors are in the first sector. Then:

$$\begin{aligned}
 d_\alpha &= dI_1 \\
 d_\beta &= dI_2 \\
 d_\gamma &= dV_1 \\
 d_\delta &= dV_2
 \end{aligned}$$



To simplify the representations, the following parameters are defined:

$$\begin{aligned}
 d_\alpha d_\gamma &= d_{\alpha\gamma} \\
 d_\alpha d_\delta &= d_{\alpha\delta} \\
 d_\beta d_\gamma &= d_{\beta\gamma} \\
 d_\beta d_\delta &= d_{\beta\delta}
 \end{aligned} \tag{6}$$

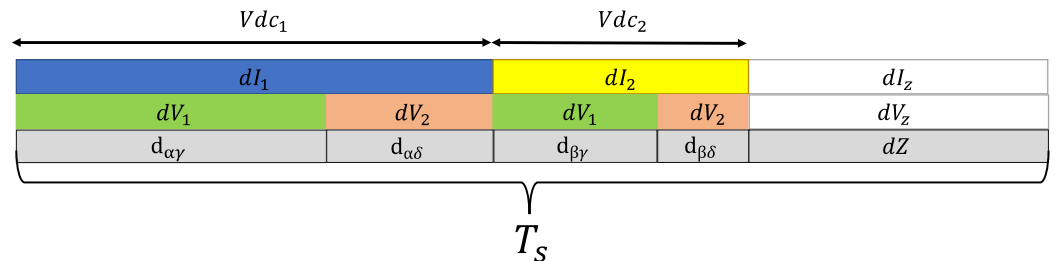


Figure 6. Switching pattern during one period.

The authors in [46] proved that the averaged voltage in the virtual DC-link is constant and equal to

$$V_{dc} = \frac{3}{2} V_i \cdot \cos(\varphi_i) \tag{7}$$

in which  $V_i$  is the amplitude of the input phase voltage and  $\varphi_i$  is the displacement angle of the input current regarding the input voltage. Taking all variations of the input and the output into account gives the following equations:

$$\begin{aligned}
 d_{\alpha\gamma} &= m_v \cdot \sin(60 - \theta_v) \cdot \sin(60 - \theta_i) \\
 d_{\alpha\delta} &= m_v \cdot \sin(\theta_v) \cdot \sin(60 - \theta_i) \\
 d_{\beta\gamma} &= m_v \cdot \sin(60 - \theta_v) \cdot \sin(\theta_i) \\
 d_{\beta\delta} &= m_v \cdot \sin(\theta_v) \cdot \sin(\theta_i)
 \end{aligned} \tag{8}$$

ROMatrix uses transformers in its structure, which are subject to magnetic saturation. The flux balance technique guarantees correct performance of the matrix converter, without being affected by saturation [39]. That is, in the following switching period, the so-called  $T'_s$ , both current and voltage reference vectors are rotated by as much as  $180^\circ$ . The vectors  $I'_{ref}$  in Figure 4 and  $V'_{ref}$  in Figure 5 represent the reversed reference vectors to realize the flux balance. Then, although different vectors are applied to the system, the power flow remains the same. If the flux balance technique is applied for the  $T_s$  (switching pattern in Figure 6), the result will be the  $T'_s$  in Figure 7. As a result, the performance of the ROMatrix has one extensive switching period, equal to  $T_s + T'_s$ .

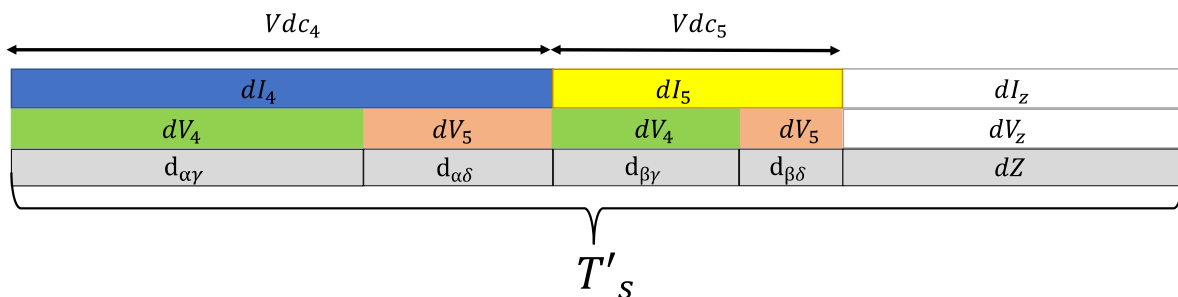


Figure 7. Switching pattern during flux balance period,  $T'_s$ .

#### 4. Simulation

In this section, the performance of ROMatrix was simulated using PLECS. The CSR side of the converter was connected to a  $400V_{LL}$ , 50 Hz three-phase source via an LC filter. The output VSI was directly connected to a  $5\Omega$  three-phase load. It was assumed that

the medium frequency transformers were used in the design, so the switching frequency was set to 5 kHz. In addition, the turn ratio of the transformers was equal to 1. In these tests, creating a 200 V line voltage in the output was expected. At the beginning of the process, the algorithm received the reference voltage and current. As mentioned before, the amplitude of the reference current depends on the load, so only the angle of the input current was used to control the power factor on the grid side. Using the Clark transform, the reference vectors were transferred to the  $\alpha\beta$ -frame, as shown in Figures 4 and 5. Then, the angles of vectors were adjusted to angles in the sectors, to calculate duty cycles using (8). In addition, the switching pattern was modified in this stage, to achieve soft switching on the CSR side. The new switching pattern is depicted in Figure 8. As shown, the current vectors were extended over the whole switching period, and zero vectors were distributed over the switching period of the VSI. In the new pattern, the duty cycles of CSR were modified as follows [47]:

$$\begin{aligned} d_{\alpha}^{\text{new}} &= \frac{d_{\alpha}}{d_{\alpha}+d_{\beta}} \\ d_{\beta}^{\text{new}} &= \frac{d_{\beta}}{d_{\alpha}+d_{\beta}} \end{aligned} \tag{9}$$

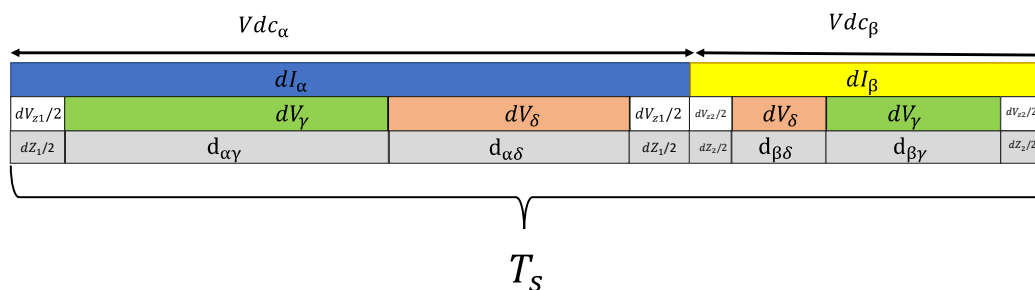


Figure 8. Modified switching pattern.

This change in the length of the current vectors affected the voltage that appeared in the virtual DC-link:

$$V_{dc} = d_{\alpha}^{\text{new}} V_{\alpha} + d_{\beta}^{\text{new}} V_{\beta} \tag{10}$$

in which  $V_{\alpha}$  and  $V_{\beta}$  are the voltages applied to the virtual DC-link when  $I_{\alpha}$  and  $I_{\beta}$  are active. To execute the flux balance technique, a parameter, namely  $S$ , was defined, which took 0 and 1, consecutively. When  $S = 0$ , the reference vectors were in their original sectors, while when  $S = 1$ , the reference vectors were transferred to the opposite sectors. This converter consisted of six input and output phases, each with six switch pairs. Then, taking into account the six sectors of the SVM plane and eight steps of the switching pattern, the control design required 1728 states in total. The unfiltered and filtered results of the simulation are shown in Figures 9 and 10, respectively.

An additional test was performed to verify the effect of unbalanced grid voltages on the output voltages and input currents. Although based on different standards, the unbalanced voltage should be less than 5% of the nominal peak value [48]; to verify the effectiveness of the proposed conversion system, an overstated unbalanced voltage was applied to the system. This means the input voltage amplitude of phase B was equal to 80% of phases A and C. The simulation results under such a situation are presented in Figure 11. As shown in the figure, the unbalanced voltage source directly affected the output voltages; similarly to other topologies, a specific control strategy was required to compensate for the effect of unbalanced voltage conditions.

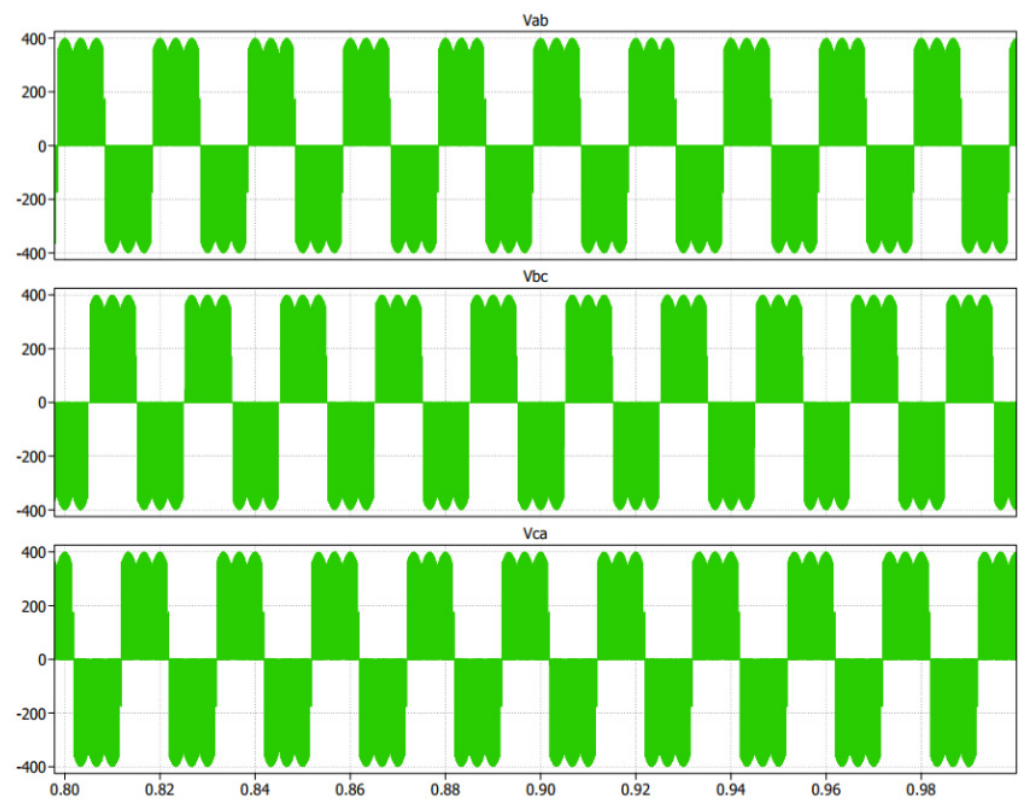


Figure 9. Output line voltage of ROMatrix, without filter from the simulation.

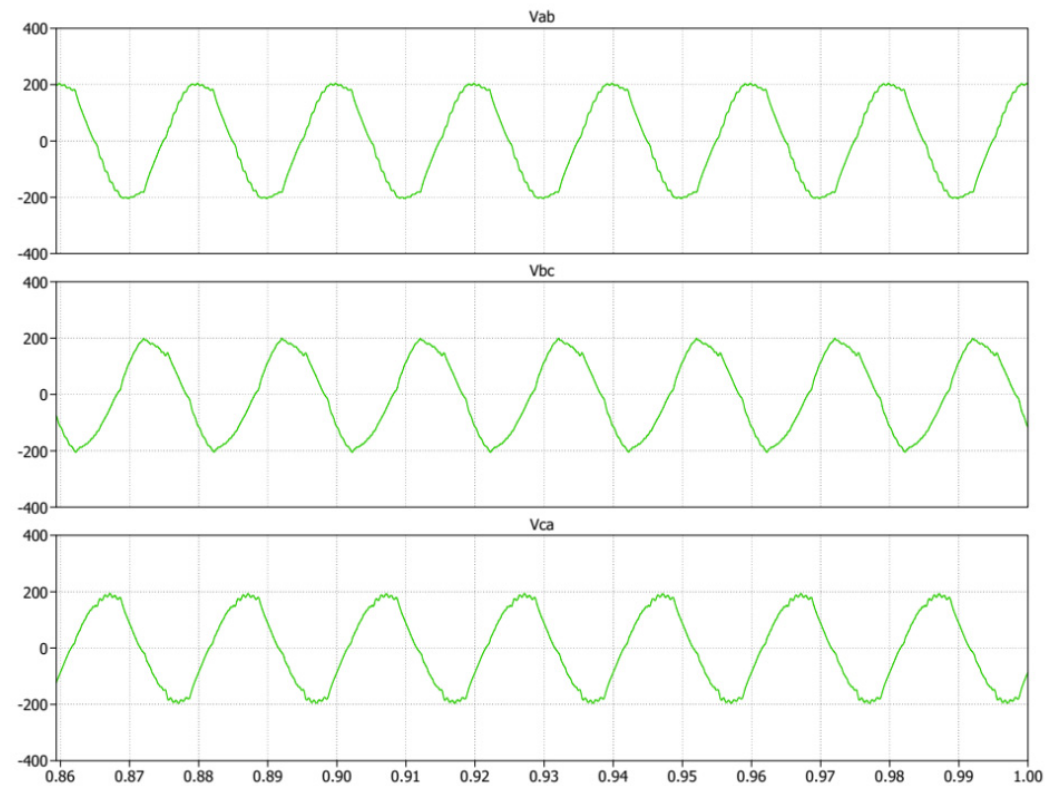
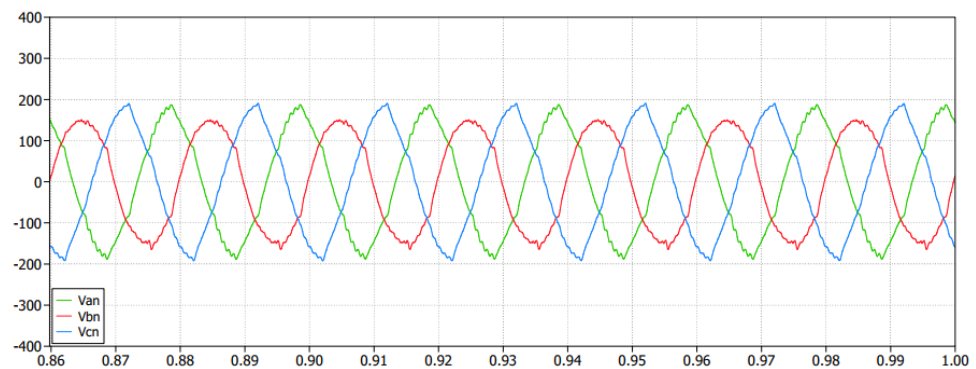


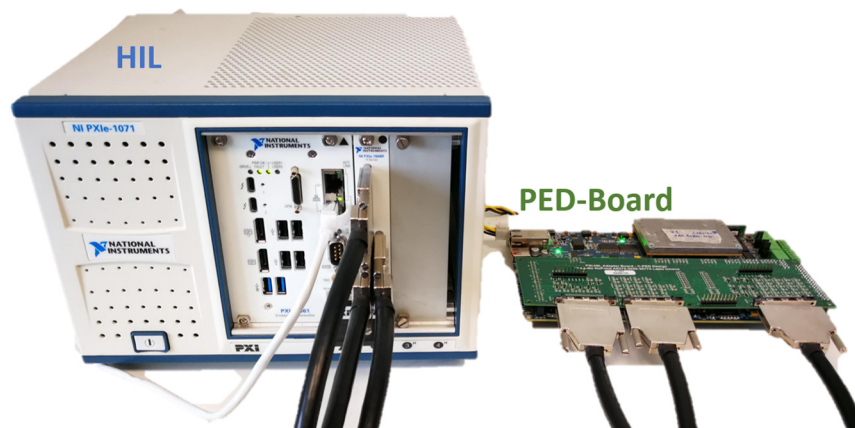
Figure 10. Filtered output line voltage of ROMatrix from the simulation.



**Figure 11.** Output line voltages under unbalanced grid voltages, simulation results.

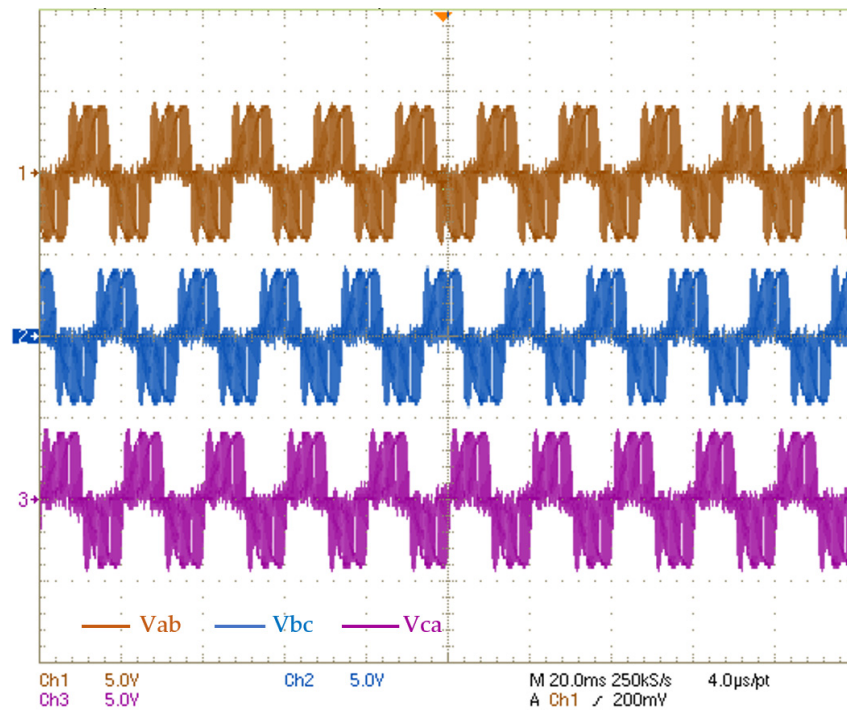
### 5. FPGA Implementation and HIL Validation

In this section, performance of ROMatrix was validated using HIL. The setup for the HIL implementation is shown in Figure 12, in which the PED-Board was an exclusively designed board for a wide variety of power electronic applications [49]. Using a National Instruments (NI) sbRIO-9651, the PED-board provides peripherals such as scalable PWM channels, fast analog to digital converters (ADC), various communication interfaces, and versatile I/Os, to name but a few. On the other hand, the HIL utilized the OPAL-RT eHS-64 solver, which was installed on the NI-PXIe 7868R module. The control of the ROMatrix was implemented on PED-board, while ROMatrix's MATLAB model was loaded on the HIL. The PED-board took advantage of NI LabVIEW FPGA, as an interfacing software with users, which permitted avoiding the use of VHDL, while maintaining high efficiency for the hardware resources used on the FPGA.

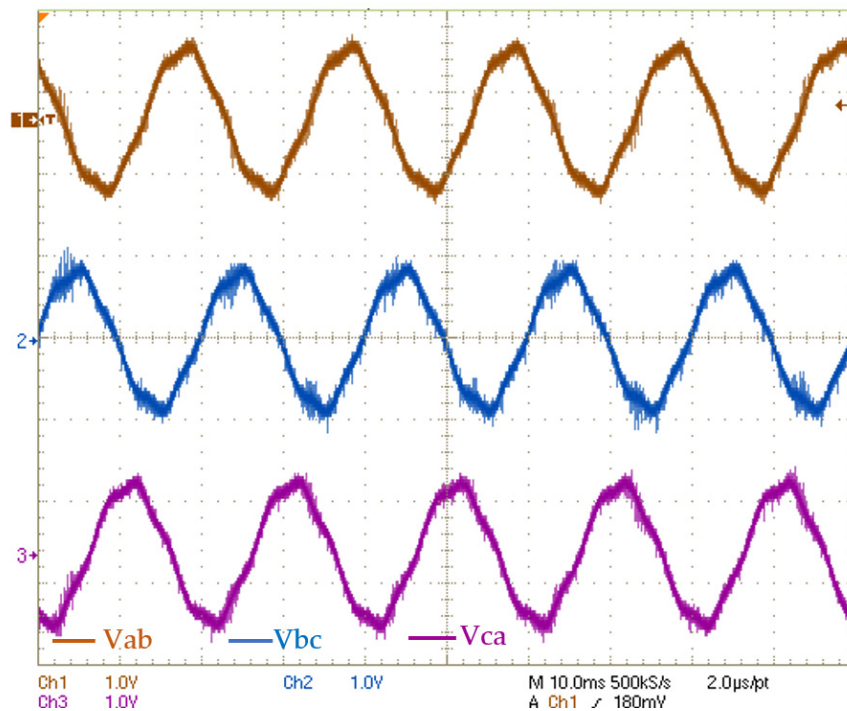


**Figure 12.** Setup for the HIL implementation.

The voltage source and the load for the HIL implementation were the same as in the simulation. The HIL implementation results, with unfiltered and filtered shapes, are illustrated in Figures 13 and 14, respectively. The maximum analog output of the PXIe 7868R is 10 V, so an appropriate scale should be applied, in order to read the voltage using an oscilloscope. Here, each unit of the oscilloscope represents 200 V. The measured voltages of the simulation and HIL were compatible with each other. Both implementations could achieve the desired values. The slight discrepancy between the two figures was due to the filters used in the HIL measurements. The output waveform contained low-frequency harmonics, which were due to the common-mode voltage. As a matter of fact, in the ROMatrix, in each switching sector, different phases play the role of the positive and negative poles of the DC-link, which results in a significant common-mode voltage (CMV). It is the task of future works to eliminate these undesired phenomena from the output waveforms.

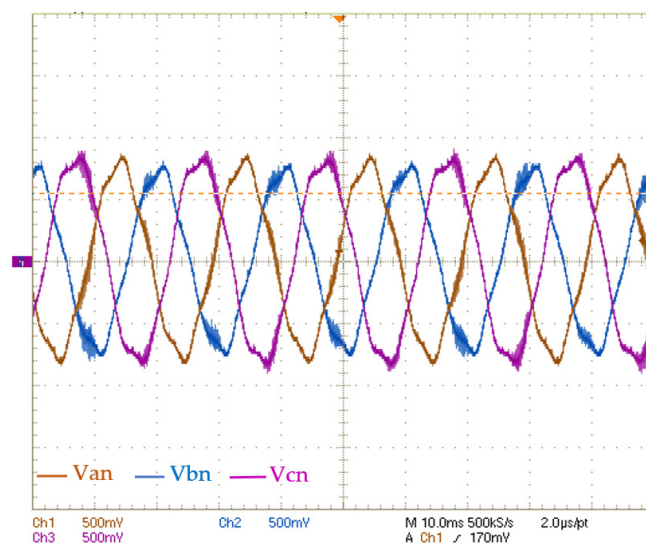


**Figure 13.** Output line voltage of the ROMatrix, without filtering, from HIL [scale 500 V/div].



**Figure 14.** Output line voltage of the ROMatrix, from HIL (scale 200 V/div).

The effect of an unbalanced voltage was also tested in the HIL and is shown in Figure 15. Similarly, to the simulation case, the unbalanced input affected all three phases, while it affected phase C more than the two other phases.



**Figure 15.** Line voltages under unbalanced input grid voltages, the HIL results (scale 100 V/div).

## 6. Conclusions

This paper presented the implementation of an FPGA-based control board for space vector modulation pulse width modulation, using specific switching patterns for the ROMatrix, a smart transformer. This ST has a special design, making it adaptable to medium voltage grids. As a matrix converter, ROMatrix provides several advantages, such as a smaller footprint and lower cost. First, ROMatrix and its working principle were reviewed. Then, the switching strategy used in this research work was described thoroughly. Finally, the simulation and the HIL implementation of the converter were presented in detail. The control of the ROMatrix was designed with an exclusive power electronic board, the so-called PED-Board, and its HIL model was implemented in NI-PXIe 7868R. Different tests were presented. In the first, the converter operated in the normal situation of the grid, whilst, in the second test, the capability of the converter under a grid voltage unbalance was successfully evaluated. The results acquired from the simulation and the HIL validated each other. The unbalanced voltage source directly affected the output waveforms. Future works will pursue several objectives. First, the origin of the CMV in the output waveforms will be investigated, to improve the system performance. After the implementation of the proposed topology on a laboratory prototype, the inclusion of an additional port, which will enable connecting battery storage to the converter, will be investigated.

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