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A Common DC Bus Circulating Current Suppression Method for Motor Emulators of New Energy Vehicles

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Abstract: In contrast to the conventional topology, wherein the Device Under Test (DUT) controller and the electric motor emulator (EME) are powered by the DC (Direct Current) voltage source independently, the common DC bus topology necessitates a single power supply. This reduces the cost and complexity of the motor emulator system, making it more favorable for large-scale industrial applications. However, this topology introduces significant circulating current issues in the system. A common DC bus circulating current suppression method is proposed in this paper for the motor emulator. First, the mechanism of zero-sequence circulating current generation in the common DC bus topology is analyzed and the expression for the system's zero-sequence voltage difference is derived. Then, a control method based on a Hybrid PWM (Pulse Width Modulation) strategy that unifies SPWM (SIN Pulse Width Modulation) and SVPWM (Space Vector Pulse Width Modulation) is proposed, which has been shown to be effective in suppressing the zero-sequence circulating current in a motor emulator system with a common DC bus topology. The proposed control method has been experimentally validated using a motor emulator system.

Keywords: motor emulator; common DC bus topology; circulating current suppression; modulation algorithm

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1. Introduction

With the development of the new energy vehicle industry, the testing processes for its core power motor have become increasingly stringent. Unlike the early practices where bench testing was conducted immediately after signal-level HIL (hardware-in-the-loop) testing of the motor controller signal board, an additional power-level HIL (PHIL) testing step is now incorporated to assess the entire MCU's (motor control unit) functionality and safety. This testing employs an electric motor emulator (EME), which can replace the real motor to emulate the electrical port characteristics of an automotive motor, fully testing the MCU functionality while eliminating the safety risk of a runaway motor. It achieves high-speed bidirectional emulation of the motor, supports four-quadrant operation, and is extensively used in various scenarios, including motor controller functionality testing, fault testing, and lifespan testing.

Both the MCU and the EME inverters require power supply during operation. Commonly, dual power supply involves equipping each inverter with a separate DC power source, ensuring complete decoupling of the DC circuits on both sides to avoid mutual interference. In 2016, Chowdhury et al. designed a floating bridge topology for dual active bridge inverters, removing the requirement for isolation transformers in dual inverter systems and reducing system size and weight [1,2]. Based on the dual power supply topology,

Chen et al. designed a novel Space Vector Pulse Width Modulation (SVPWM) algorithm that does not require sector judgment, reducing the overall system switching frequency to one-third of that in traditional modulation schemes [3]. The majority of research conducted on motor emulators is based on the dual power independent supply topology [4–7], a trend that is similarly evident in the development of motors. The mass-produced EME products developed through collaborations between KIT University and AVL, as well as Paderborn University and ScienLab, both employ dual power supply topologies [8,9]. However, the dual power supply method increases system size, leading to higher costs and complexity of the emulator.

To address the various drawbacks associated with dual power supply topologies, a few scholars have attempted to explore the common DC bus topology based on a single power supply. This approach eliminates a power source, supplying both inverters with a single power source, which increases DC bus voltage utilization and reduces system cost and complexity. However, it also results in less flexibility in adjusting the number of voltage levels and introduces the issue of circulating currents on the DC side, which require additional hardware or software algorithms for control [10]. Additionally, the circulating current will also increase the energy loss of system and reduce the lifetime of device; in severe cases, this can damage the device [11].

Therefore, many works have focused on voltage source converters' (VSCs') modulations to reduce or eliminate the zero-sequence component of the voltage supplied to the machine. In [12], a novel switching sequence of space vector modulation in the over-modulation region for the five-phase open-end winding topology is proposed to address this issue but it increases the switching band harmonics. In [13], a design method for the common-mode inductors for the common DC bus topology is proposed to suppress the circulating current. There are also many researchers making efforts to eliminate the circulating current by improving modulation methods to directly eliminate the common-mode voltage [14–18]. However, a zero-sequence loop current cannot be completely eliminated by PWM-based modulation alone, as both dead time and zero-sequence reverse potential can cause zero-sequence loop current fluctuations at the hardware level [19]. With this in mind, one study [20] designed a PR controller based on the pulsation frequency of circulating current to improve its control effectiveness, but this method needs to adjust the gain online to match the system fundamental frequency, which is not applicable to the wide frequency requirements of EME.

Two studies [21,22] considered the effect of two zero vectors on the common-mode voltage in classic SVPWM, and designed a controller to reasonably allocate the duration of the zero vectors. This method effectively suppresses the circulating current, but it will increase the complexity of the modulation algorithm. Specifically, it will make the SVPWM algorithm, which already takes up a large amount of computation, even more complex, further limiting the controller's maximum control frequency. Therefore, this paper proposes a relatively simple control method to suppress the zero-sequence circulating current in the common DC bus topology, in which the Hybrid PWM method will be used to in place of classic SVPWM, which can achieve the same voltage utilization as SVPWM by injecting a zero-sequence voltage to SPWM, and can save lots of calculations. The suppression effects of the proposed method are demonstrated in Section 5.

2. Principles of Zero-Sequence Current

The principle of a PHIL test platform based on the Electric Machine Emulator (EME) is illustrated in Figure 1. The system primarily consists of a bidirectional power supply, an under-test MCU, a filter coupling network, a load EME, and its internal components, including the motor control strategy, load mathematical model, current tracking control unit,

and motor mathematical model. Based on the voltage and current signals output from the MCU side of the acquisition, combined with the current load and the simulated rotational speed, the EME calculates the target current to be emulated in the motor model, then the current tracking control module will track the target current to achieve the emulation of the feedback of the real motor. In order to make the emulation result closer to the real motor, the EME-side controller needs to take care of the current tracking task, but also needs to make the zero-sequence current of the system close to zero, which makes the design of the EME-side controller more difficult.

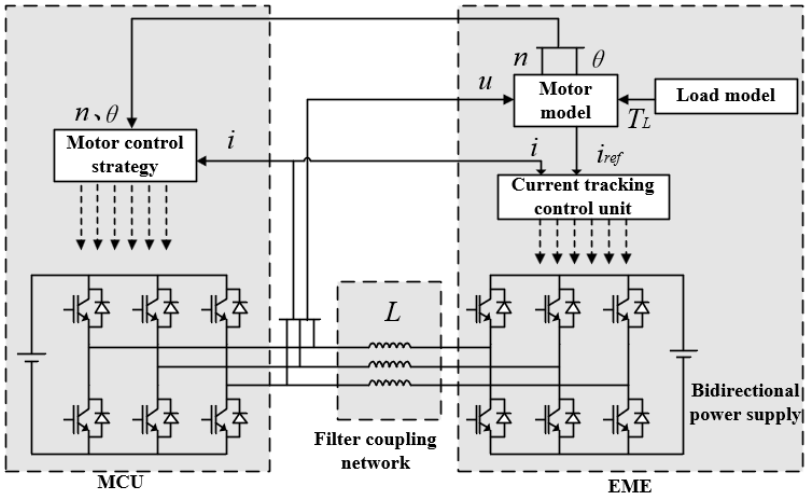

Figure 1. Simplified dual power supply independent motor emulator system.

2.1. Zero-Sequence Voltage Mathematical Model

Common-mode voltage exists in all voltage-source PWM inverter systems, and its magnitude is influenced by factors such as system circuit structure and control strategy. For traditional three-phase two-level inverters, differential-mode voltage is the component present between any two output lines of the three-phase two-level inverter, with electrical energy transferred in the form of differential-mode voltage. Common-mode voltage between the lines, on the other hand, exists between the inverter output and the reference ground and is the potential difference between the neutral point and the ground, shared by all three-phase windings. In engineering practice, common-mode voltage is often calculated by dividing the sum of the system's three-phase voltages by the number of phases:

$$U_{CMV}^{\mathrm{mcu}} = (U_A + U_B + U_C)/3 \tag{1}$$

where U_{CMV}^{mcu} represents the common-mode voltage of the MCU invertor; U_x represents the phase voltage of x phase. This common-mode voltage is the direct cause of a zero-sequence circulating current in motors with a neutral point connection. Similarly, the zero-sequence circulating current in common DC bus topology motor emulator systems also originates from this common-mode voltage. For ease of analysis, the battery emulator in the traditional motor emulator testing system is simplified, using the inverter's DC output as the system power supply to provide a relatively constant battery voltage and achieve power isolation. This simplified system topology is shown in Figure 2, without considering battery emulator voltage fluctuations or non-ideal characteristics of power devices such as dead time and conduction voltage drops.

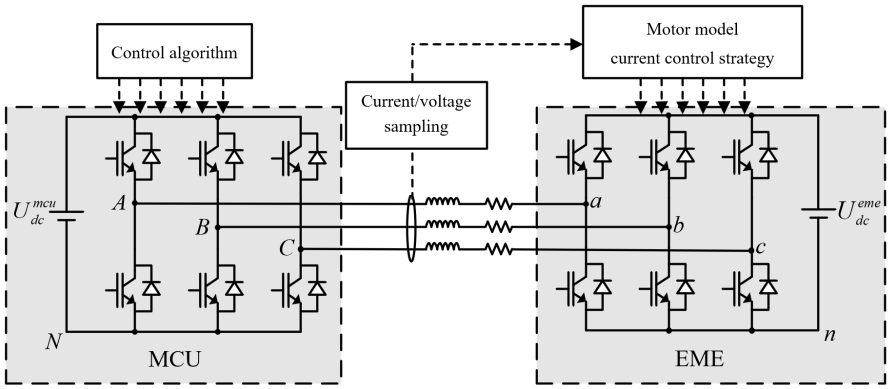

Figure 2. Simplified dual power supply independent motor emulator system.

In the common dual power supply EME topology shown in Figure 2, the bus voltage of the motor controller is denoted as U_{dc}^{mcu}, with the voltage zero reference point as N; the bus voltage of the motor emulator is denoted as U_{dc}^{eme}, with the voltage zero reference point as n.

Define $S_x^y (x \in \{A,B,C\}; y \in \{\mathrm{mcu},\mathrm{eme}\})$ to represent the switching state of each phase power device of the inverter on both sides of the motor controller and motor emulator. When $S_x^y = 1$, the upper bridge power device of phase x is conducting; when $S_x^y = 0$, the lower bridge power device of phase x is conducting. Define U_{dc}^{mcu} and U_{dc}^{eme} to represent the DC bus voltage of MCU and EME, respectively. The system voltage can be expressed by Equation (2):

$$\begin{bmatrix} S_A^{\mathrm{mcu}} \\ S_B^{\mathrm{mcu}} \\ S_C^{\mathrm{mcu}} \end{bmatrix} U_{dc}^{\mathrm{mcu}} = L \begin{bmatrix} \frac{\mathrm{d}i_a}{\mathrm{d}t} \\ \frac{\mathrm{d}i_b}{\mathrm{d}t} \\ \frac{\mathrm{d}i_c}{\mathrm{d}t} \end{bmatrix} + R_L \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} S_A^{\mathrm{eme}} \\ S_B^{\mathrm{eme}} \\ S_C^{\mathrm{eme}} \end{bmatrix} U_{dc}^{\mathrm{eme}} + \begin{bmatrix} U_{nN} \\ U_{nN} \\ U_{nN} \end{bmatrix} \tag{2}$$

where U_{nN} means the voltage difference between point n and point N. Although there is a voltage difference between the reference points of the two power supplies, a zero-sequence circulating current will not be generated, because the two power supplies are isolated from each other and do not form a closed loop. Since most existing automotive permanent magnet synchronous motors are three-phase star-connected, the sum of the phase current (i_a, i_b and i_b) will be 0 according to Kirchhoff's Current Law.

By the sum of the phase current in Equation (2), the voltage difference between point n and point N can be obtained as follows:

$$U_{nN} = \frac{U_{dc}^{\mathrm{mcu}}}{3}(S_A^{\mathrm{mcu}} + S_B^{\mathrm{mcu}} + S_C^{\mathrm{mcu}}) - \frac{U_{dc}^{\mathrm{eme}}}{3}(S_A^{\mathrm{eme}} + S_B^{\mathrm{eme}} + S_C^{\mathrm{eme}}) \tag{3}$$

However, for the common DC bus topology motor emulator system shown in Figure 3, U_{dc} is the output voltage of the battery emulator, providing a constant DC voltage to both the motor controller and the motor emulator. The common DC bus topology results in a parallel connection between the two inverters, with both inverters sharing a common ground, thereby forming a zero-sequence voltage loop.

The voltage difference U_{nN} acts on the supply bus to generate a current. According to Kirchhoff's Current Law, this will also cause a zero-sequence circulating current to be produced in the three-phase lines:

$$i_a + i_b + i_c = i^+ + i^- \tag{4}$$

where i^+ and i^- present the current flowing through the common-mode inductor from the positive and negative point in DC bus, respectively. Since the three-phase common-

mode voltages are equal and the sum of the three-phase currents is zero in the absence of common-mode voltage, the magnitude of the zero-sequence current i_0 (a DC current between same phase in MCU and EME caused by the voltage difference U_{nN}) is the average of the three-phase currents, which can be expressed as follows:

$$i_0 = \frac{i_a + i_b + i_c}{3} \tag{5}$$

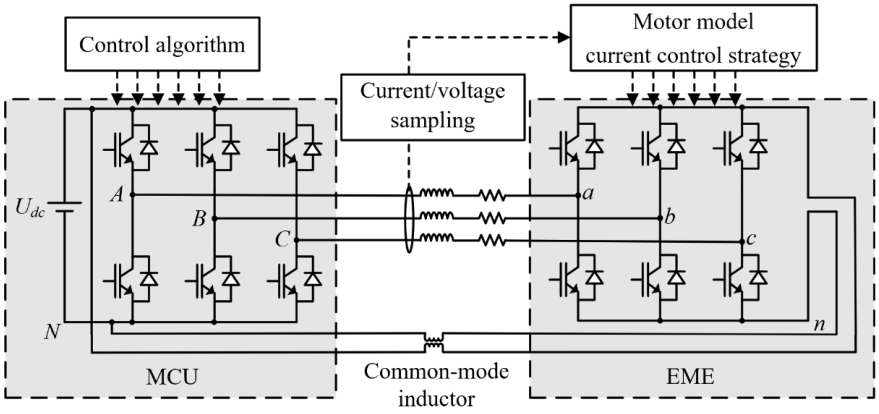

Figure 3. Simplified single power supply independent motor emulator system.

From Equations (1) and (3), the common-mode voltages on both sides of the motor emulator system can be obtained as follows:

$$\begin{cases} U_{CMV}^{\text{mcu}} = \frac{S_A^{\text{mcu}} + S_B^{\text{mcu}} + S_C^{\text{mcu}}}{3} U_{dc} \\ U_{CMV}^{\text{eme}} = \frac{S_A^{\text{eme}} + S_B^{\text{eme}} + S_C^{\text{eme}}}{3} U_{dc} \end{cases} \tag{6}$$

In Figure 3, it is easy to find that the circulation loop for a zero-sequence current i_0 is as follows: N → transistor (MCU) → phase A (or B and C) → leakage inductor and resistor of the filter network → phase a (or b and c) → transistor (EME) → n → common-mode inductors →N. Considering U_{CMV}^{mcu} and U_{CMV}^{eme} as two voltage sources, we can derive the zero-sequence equivalent circuit between the EME and MCU (Figure 4).

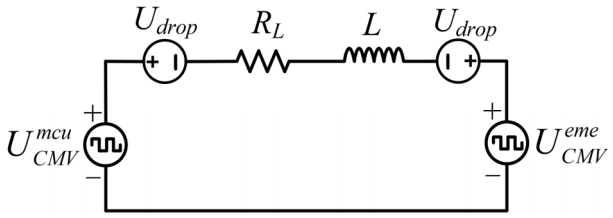

Figure 4. Simplified zero-sequence equivalent circuit.

In this circuit, U_{drop} represents the voltage drops throughout transistor branches, R_L is the equivalent resistance of the zero-sequence current loop, and L is the equivalent inductance of the zero-sequence current loop, which includes the leakage inductance of the filter network and the common-mode inductance between the DC sides of the two inverters. The voltage difference that generates the zero-sequence circulating current is given by U_{nN}, thus we have the following:

$$U_{nN} = U_{CMV}^{\text{eme}} - U_{CMV}^{\text{mcu}} = L\frac{\mathrm{d}i_0}{\mathrm{d}t} + R_L i_0 + 2U_{drop} \tag{7}$$

2.2. Zero-Sequence Voltage in SVPWM

Considering the voltage utilization factor, traditional three-phase two-level motor controllers commonly employ the SVPWM strategy to generate PWM waves for motor control. Therefore, this section analyzes the common-mode voltage on the MCU side based on the traditional SVPWM modulation strategy.

In a three-phase two-level inverter using traditional SVPWM modulation, only two zero voltage vectors, V_0 and V_7, and six non-zero voltage vectors, V_1 to V_6, with fixed amplitudes and 60° intervals, participate in synthesizing the target voltage. Based on the volt-second balance principle, the equivalent average voltage corresponding to the target voltage can be obtained through different time combinations of the basic voltage vectors within a single cycle, as shown in Figure 5. Taking Section IV as example, the action times of the two adjacent non-zero voltage vectors (U_α,U_β) can be calculated as follows based on the target voltage vector U_{out}:

$$\begin{cases} T_1 = -\sqrt{3}\frac{T_s}{U_{dc}}U_\beta \\ T_2 = \frac{\sqrt{3}}{2}\frac{T_s}{U_{dc}}\left(-\sqrt{3}U_\alpha + U_\beta\right) \end{cases} \tag{8}$$

where T_1 and T_2 represent the duration of the first and second non-zero vectors appearing in the seven-segment vector sequence, respectively; U_{dc} represents the voltage of the DC bus.

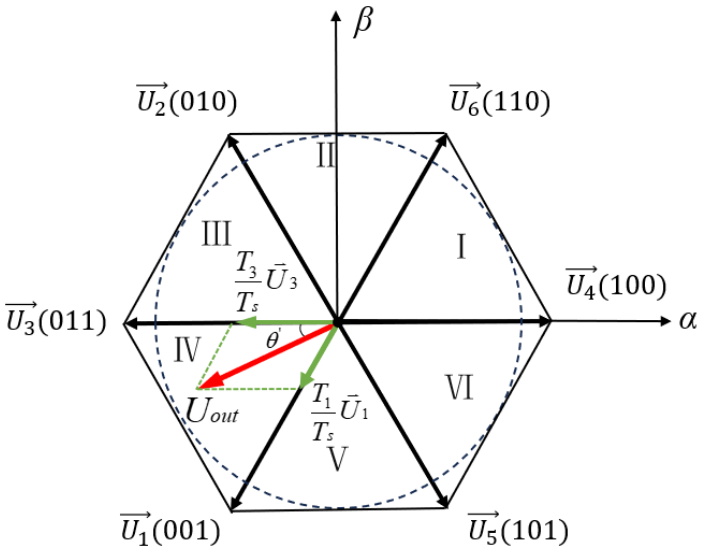

Figure 5. Illustration of the volt-second balance principle.

Further analysis of the MCU common-mode voltage for each switching state, based on Equation (6), results in Table 1:

Table 1. Distribution of voltage vectors for the eight switching states of a three-phase two-level inverter.

Vector Type	Vector	Switching State	U_{CMV}/U_{dc}
Zero vector	V_0	[0 0 0]	−1/2
	V_7	[1 1 1]	1/2
Non-zero vector	V_4	[1 0 0]	−1/6
	V_6	[1 1 0]	1/6
	V_2	[0 1 0]	−1/6
	V_3	[0 1 1]	1/6
	V_1	[0 0 1]	−1/6
	V_5	[1 0 1]	1/6

Combining the classical seven-segment vector sequence allocation method with Table 1, we can observe that regardless of which sector the target vector is in, the two non-zero vectors involved in the synthesis will inevitably result in $\pm 1/6 U_{dc}$. By combining this with Equation (1), we obtain the following:

$$U_{CMV}^{mcu} = -\frac{1}{6} T_1^{\mathrm{mcu}} U_{dc} + \frac{1}{6} T_2^{\mathrm{mcu}} U_{dc} \tag{9}$$

where T_1^{mcu} and T_2^{mcu} represent the duration of the first and second non-zero vectors appearing in the seven-segment vector sequence, respectively. No matter which section the target vector is in, T_1^{mcu} and T_2^{mcu} will satisfy the above equation.

If the SVPWM modulation strategy is also employed in the EME-side inverter, and the time interval of the two non-zero vectors and two zero vectors are equally distributed within each switching cycle on both sides, then the zero-sequence voltage $U_{nN} = 0$, and zero-sequence circulating current would not exist. However, in practice, only the time interval of the two zero vectors is equally distributed within each switching cycle for the MCU-side inverter, while the time interval of the two non-zero vectors is typically not equal and they are unevenly distributed. This uneven distribution of non-zero vectors result in common-mode voltages from the two inverters that cannot completely cancel each other out. Consequently, the varying common-mode voltage on each inverter side leads to a non-zero zero-sequence voltage. This discrepancy in common-mode voltage between the MCU and EME sides creates zero-sequence current in the zero-sequence equivalent circuit shown in Figure 4.

A simulation model was established based on the single power supply system in Figure 3 with the SVPWM modulation algorithm on both the MCU side and EME side. Figure 6 is a simulation result that illustrates the duty cycle of phase A and the duty cycles of the two non-zero vectors under the SVPWM modulation algorithm on the MCU side. After modulation, the duty cycle of phase A takes on a standard saddle wave form. The duty cycles of the two non-zero vectors are not equal outside the crossing points, indicating that, within any switching cycle, the inverter on this side generates a common-mode voltage due to the uneven distribution of non-zero vectors. Since the time interval for generating the target voltage vector cannot be adjusted, the generation of common-mode voltage is unavoidable. Furthermore, the circulation current (zero-sequence current i_0, obtained based on Equation (5)) and common-mode voltage difference (zero-sequence voltage U_{nN}) are shown in Figure 7. Although there is a phase difference caused by inductance between the common-mode voltage difference and the common bus DC circulating current, there is still a positive correlation, which confirms the validity of the circulating current mechanism analyzed in Equation (7).

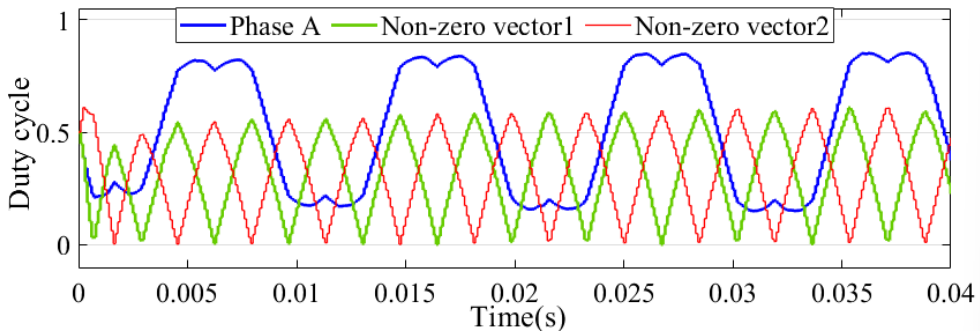

Figure 6. The duty cycle of phase A and the duty cycles of the two non-zero vectors in simulation.

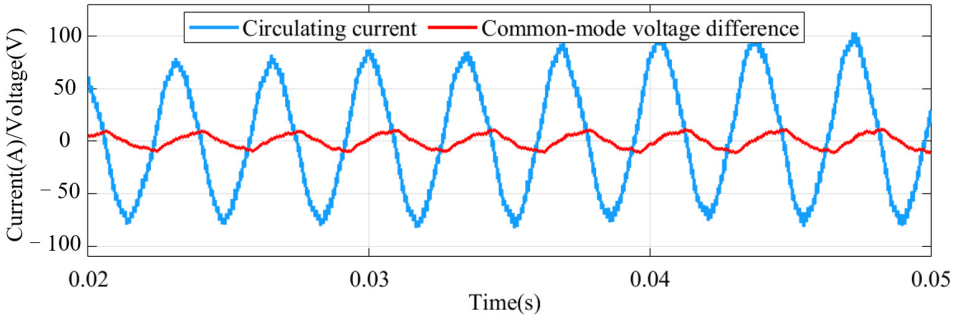

Figure 7. Common-mode voltage difference and circulating current in simulation.

3. Zero-Sequence Circulating Current Suppression Method

3.1. Hybrid PWM Strategy

The Hybrid PWM Strategy [23] unifies the SVPWM and SPWM modulation algorithms by injecting a zero-sequence voltage into the SPWM modulation. This allows the control system to maintain the same voltage utilization as the SVPWM algorithm while adjusting the system's zero-sequence voltage. Additionally, since the modulation is achieved through zero-sequence voltage injection, there is no need for SVPWM sector determination and vector sorting, significantly saving computational resources. This method reallocates the zero vector action time in SVPWM, assigning the action times of the two zero vectors, V_0 and V_7, to kT_{zero} and $(1-k)T_{\text{zero}}$, respectively, $k \in [0, 1]$. Taking Sector VI as an example, the switching times for each phase are as follows:

$$\begin{cases} T_a = kT_{zero} \\ T_b = T_3 + kT_{zero} \\ T_c = T_1 + T_3 + kT_{zero} \end{cases} \tag{10}$$

where T_x represents the duration of x phase PWM height time, $x = a, b, c$; T_i represents the duration of the non-zero vector V_i, i =1, 2, 3, 4, 5, 6; T_{zero} represents the duration of all zero vectors, V_0 and V_7. Based on this formula, the three-phase modulation waveforms for SVPWM (Hybrid PWM) after the reallocation of zero vector action times were derived Equation (11) and compared with the SPWM modulation waveforms Equation (12) [23], where V_{tp} represents the carrier amplitude:

$$\begin{cases} U^*_{a\text{SVPWM}} = \frac{2V_{tp}}{U_{dc}}U_a + (2k-1)V_{tp} - k\frac{2V_{tp}}{U_{dc}}U_c + (k-1)\frac{2V_{tp}}{U_{dc}}U_a \\ U^*_{b\text{SVPWM}} = \frac{2V_{tp}}{U_{dc}}U_b + (2k-1)V_{tp} - k\frac{2V_{tp}}{U_{dc}}U_c + (k-1)\frac{2V_{tp}}{U_{dc}}U_a \\ U^*_{c\text{SVPWM}} = \frac{2V_{tp}}{U_{dc}}U_c + (2k-1)V_{tp} - k\frac{2V_{tp}}{U_{dc}}U_c + (k-1)\frac{2V_{tp}}{U_{dc}}U_a \end{cases} \tag{11}$$

$$\begin{cases} U^*_{a\text{SPWM}} = \frac{2V_{tp}}{U_{dc}}U_a \\ U^*_{b\text{SPWM}} = \frac{2V_{tp}}{U_{dc}}U_b \\ U^*_{c\text{SPWM}} = \frac{2V_{tp}}{U_{dc}}U_c \end{cases} \tag{12}$$

where U^*_{xSVPWM} and U^*_{xSPWM} represent the modulation waves of the x phase in SVPWM and SPWM modulation algorithms, respectively; k represents the modulation factor to adjust the duration of two non-zero vectors, $k \in [0, 1]$. By comparing the two equations, it can be observed that the Hybrid PWM modulation wave is essentially the SPWM modulation wave with an added zero-sequence voltage U^*_0.

$$s = \frac{2V_{tp}}{U_{dc}} \tag{13}$$

$$U_0^* = (k-1)sU_a - ksU_c + (2k-1)V_{tp} \tag{14}$$

$$U_{\text{SVPWM}}^* = \begin{bmatrix} U_{\text{aSVPWM}}^* \\ U_{\text{bSVPWM}}^* \\ U_{\text{cSVPWM}}^* \end{bmatrix} = \begin{bmatrix} U_{\text{aSPWM}}^* \\ U_{\text{bSPWM}}^* \\ U_{\text{cSPWM}}^* \end{bmatrix} + U_0^* = U_{\text{SPWM}}^* + U_0^* \tag{15}$$

where U_{SVPWM}^* and U_{SPWM}^* represent the matrix of the modulation wave of three phases in the SVPWM and SPWM modulation algorithms, respectively. After summarizing the Hybrid PWM modulation wave formulas for all sectors, it was found that the phase voltage with a coefficient of k corresponds to the maximum phase voltage U_{max} among the three phases, while the phase voltage with a coefficient of $(k-1)$ corresponds to the minimum phase voltage U_{min}. Therefore, the zero-sequence component shown in Equation (14) can be uniformly expressed as follows:

$$U_0^* = (k-1)sU_{\text{min}} - ksU_{\text{max}} + (2k-1)V_{tp} \tag{16}$$

Under the traditional SVPWM modulation algorithm, the two zero vectors V_0 and V_7 are evenly distributed, corresponding to $k = 1/2$. In this case, the three-phase modulation wave generated by SVPWM can be expressed as follows:

$$U_{\text{SVPWM}}^* = U_{\text{SPWM}} - \frac{1}{2}s(U_{\text{max}} + U_{\text{min}}) \tag{17}$$

3.2. Current Suppression Method

Based on the aforementioned Hybrid PWM Strategy, this paper proposes a comprehensive control method, as illustrated in Figure 8, to suppress system circulating currents. The design approach for the circulating current suppression algorithm focuses on the zero vector action times. The aim is to actively generate common-mode voltage on the motor emulator side power inverter unit. The design goal is to compensate for the common-mode voltage difference between the motor controller and motor emulator power inverter units, ensuring that the zero-sequence voltage across the three-phase inductors is maintained at 0 V.

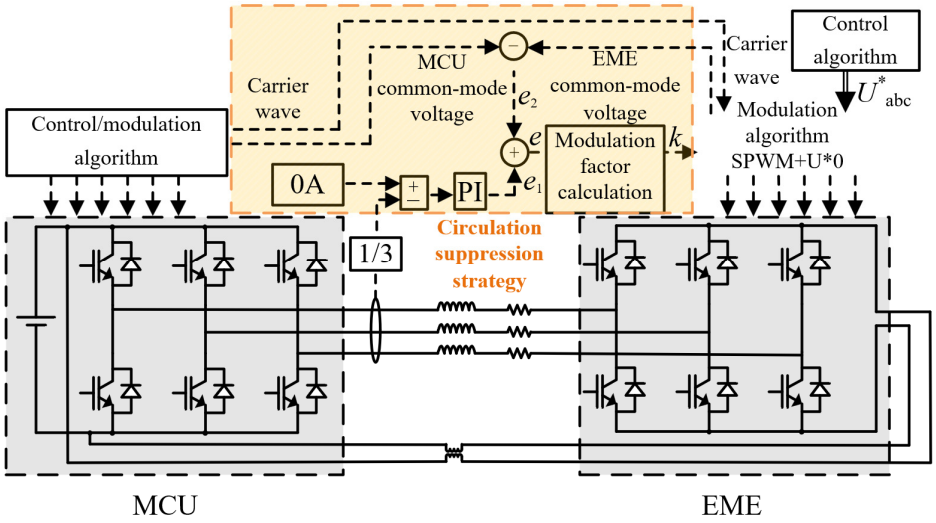

Figure 8. Common DC bus circulating current suppression method based on Hybrid PWM Strategy.

As shown in Figure 8, the proposed control method calculates the circulating current by sampling the three-phase currents and determines the compensation input term e_1 through a PI controller. Simultaneously, the PWM signals from the controllers at both the MCU and EME sides, respectively, are sampled to calculate the common-mode voltage. The common-mode voltage difference between the MCU and EME sides is then used to

derive the compensation input term e_2. Finally, based on e_1 and e_2, a modulation factor k is calculated to adjust the output common-mode voltage at the EME side. This modulation factor k is inputted into the Hybrid PWM Strategy module to generate PWM signals for controlling the EME, thereby suppressing the circulating current within the system.

In each switching cycle, the common-mode voltage produced by the two non-zero vectors in the traditional SVPWM modulation algorithm has been thoroughly derived in Section 2. To maintain the system's zero-sequence circulating currents within a lower range, it is necessary to control the zero-sequence voltage of the system in each switching cycle. Therefore, the target common-mode voltage difference across the three-phase inductors in each switching cycle should be 0 V, satisfying the following equation:

$$\begin{cases} U_{nN} = U_{CMV}^{\text{mcu}} - U_{CMV}^{\text{eme}} = 0 \\ U_{CMV}^{\text{mcu}} = -\frac{1}{6}T_1^{\text{mcu}}U_{dc} + \frac{1}{6}T_2^{\text{mcu}}U_{dc} \\ U_{CMV}^{\text{eme}} = -\frac{1}{6}T_1^{\text{eme}}U_{dc} + \frac{1}{6}T_2^{\text{eme}}U_{dc} \end{cases} \tag{18}$$

In the equation, T_1^{mcu} and T_2^{mcu} represent the action times of the two non-zero vectors for the MCU, while T_1^{eme} and T_2^{eme} represent the action times of the two non-zero vectors for the EME. In traditional SVPWM, the zero vector duration is usually equally distributed between the two zero states V_0 and V_7. To compensate for the common-mode voltage, the modulation algorithm on the motor emulator side is modified based on the seven-segment vector sequence shown in Figure 9. This adjustment actively generates common-mode voltage to suppress the common-mode voltage difference of the system, thereby reducing the low-frequency components of the circulating current.

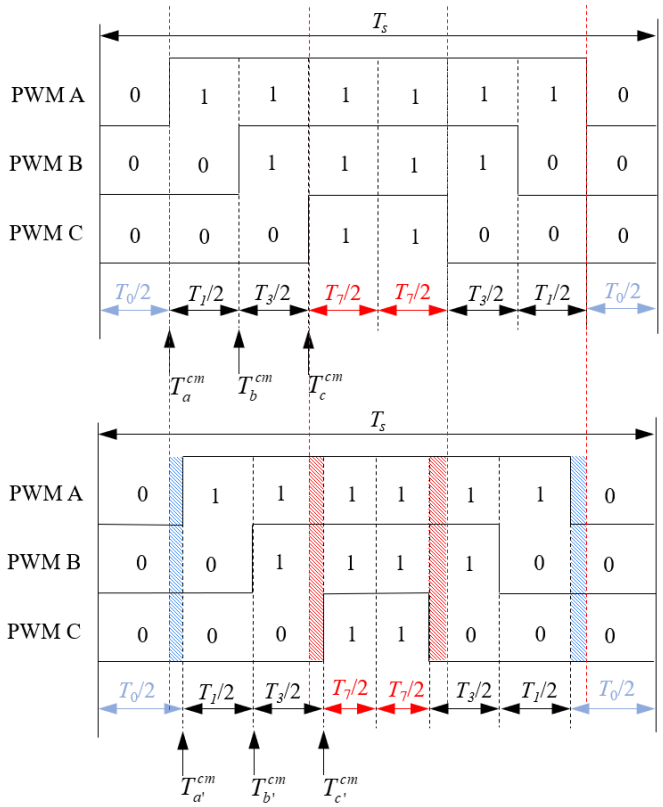

Figure 9. Zero vector redistribution strategy based on the seven-segment switching sequence.

In the proposed control method, a PI controller is being used to allocate the zero vector durations T_0 and T_7, outputting the common-mode voltage compensation value $u_{0\text{PI}}$ to compensate for steady-state common-mode voltage errors in real time. However,

the PI controller can only suppress the DC component of the zero-sequence circulating current and cannot completely eliminate the third harmonic component. Therefore, a new compensation input term e_2 is introduced, as shown in Equation (20). This term is used to calculate the difference in common-mode voltage produced by the non-zero voltage vectors on both sides during each switching cycle in real time. Combined with the PI-based compensation input term e_1, shown in Equation (19), the complete common-mode voltage modulation factor e can be represented as shown in Equation (21). By redistributing the zero vector durations, the common-mode voltage compensation is achieved.

$$e_1 = T^*_{0\mathrm{PI}} \tag{19}$$

$$e_2 = -\frac{1}{6}T_1^{\mathrm{mcu}} + \frac{1}{6}T_2^{\mathrm{mcu}} + \frac{1}{6}T_1^{\mathrm{eme}} - \frac{1}{6}T_2^{\mathrm{eme}} \tag{20}$$

$$e = e_1 - e_2, e \in [-T_s, T_s] \tag{21}$$

where T^*_{0PI} represents the output of the PI controller in Figure 8. The modulation factor e means the zero vector duration that needs to be redistributed. Taking Sector IV as an example, after introducing the common-mode voltage modulation factor e, the switching instants of the three-phase bridge power devices change from Equations (10)–(22):

$$\begin{cases} T_{a'}^{cm} = \frac{T_s - T_1 - T_3}{4} + \frac{e}{2} \\ T_{b'}^{cm} = T_{a'}^{cm} + \frac{T_1}{2} \\ T_{c'}^{cm} = T_{b'}^{cm} + \frac{T_3}{2} \end{cases} \tag{22}$$

where T_x^{cm} represents the switch time of x phase in a classical SVPWM modulation algorithm; $T_{x'}^{cm}$ represents the switch time of x phase after compensation in the proposed modulation algorithm (Figure 9). The aforementioned algorithm modifies the switching instants of the three-phase bridge based on SVPWM modulation and a seven-segment vector sequence. For $e > 0$, the effect of Equation (22) is to extend the zero vector duration T_0 by e seconds, while the zero vector duration T_7 is correspondingly shortened by e seconds. Conversely, for $e < 0$, the zero vector duration T_0 is shortened by e seconds, and the zero vector duration T_7 is correspondingly extended by e seconds.

When $e = 0$, the modulation strategy reverts to the traditional SVPWM, where $k = 1/2$. Therefore, we can easily derive the following:

$$k = \frac{1}{2} - \frac{e}{T_s} \tag{23}$$

$$U_0^* = -\frac{e}{T_s}V_{tp} - (\frac{1}{2} - \frac{e}{T_s})sU_{\max} - (\frac{1}{2} + \frac{e}{T_s})sU_{\min} \tag{24}$$

It should be noted that the method only changes the duration of the two zero vectors without altering the durations of the non-zero vectors involved in synthesizing the target voltage. The zero vectors do not generate effective α-β axis fundamental frequency voltage. Therefore, the proposed modulation algorithm does not affect the synthesis of the system's target voltage vector, nor does it impact the output capability of the motor emulator.

4. Simulation Results

Under the conditions specified in Table 2, a co-simulation test between the MCU and EME was conducted. This simulation aimed to replicate the DC bus circulating current occurring in the operation of a real power-level hardware-in-the-loop (PHIL) testing system. Subsequently, the circulating current suppression algorithm was activated to validate its effectiveness.

Table 2. Simulation parameters.

Parameter	Value	Symbol
DC voltage	800	V
Switch time	10	kHz
Dead time	3	μs
Pole pairs	4	-
Stator resistance	0.0125	Ω
Permanent magnet flux linkage	0.366	Wb
d-axis inductance	0.238	mH
q-axis inductance	0.238	mH
Electrical angular velocity	150	rad/s
d-axis target current	0	A
q-axis target current	100	A

As shown in Figure 10, the red waveform represents the modulation wave output by the motor emulator when the improved modulation algorithm is not enabled. The blue waveform represents the modulation wave output by the motor emulator after enabling the circulating current suppression algorithm. It can be observed that, before the activation of the circulating current suppression algorithm, the output modulation waveform of the motor emulator exhibits a standard saddle shape. After enabling the circulating current suppression algorithm, the system modulation waveform deviates from the standard saddle shape, with a significant height difference between the two peaks. This indicates that the proposed algorithm adjusts the shape of the injected zero-sequence component in real time, as illustrated in Figure 11, by modifying the time interval of the two zero vectors.

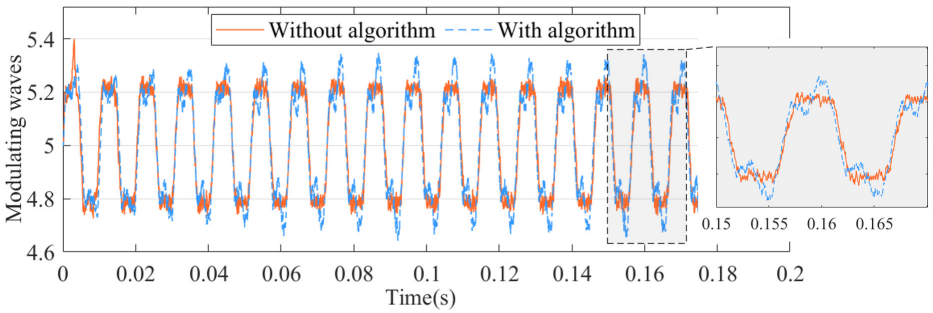

Figure 10. Modulation waveforms of phase a before and after the activation of the circulating current suppression strategy.

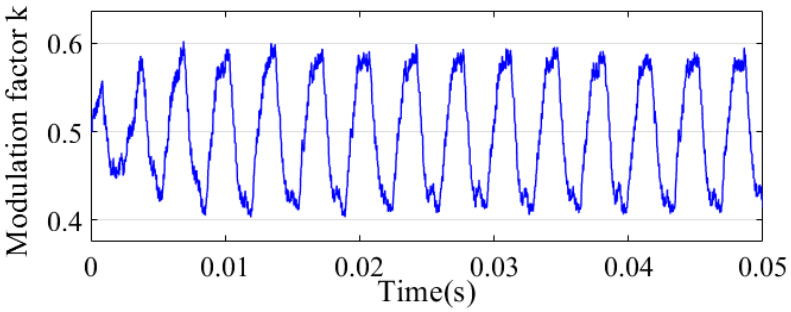

Figure 11. Zero-sequence component modulation factor *k*.

From Figure 11, it can be seen that the modulation factor *k* varies continuously over time, adjusting the system's zero-sequence voltage in real time. In this case, the system's circulating current, represented by the orange curve in Figure 12, shows significant suppression, with a noticeable reduction in amplitude compared with the blue curve.

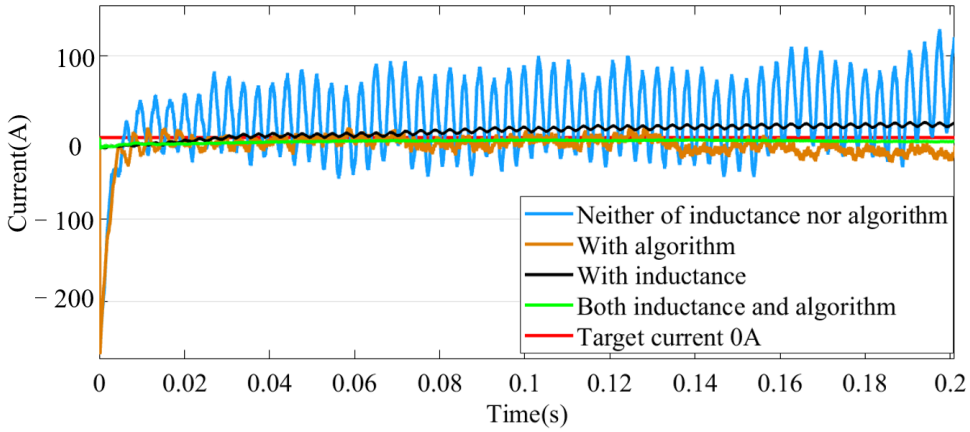

Figure 12. Comparison of DC bus circulating currents under four conditions.

To validate the effectiveness of the modulation algorithm proposed in this paper, the simulation conditions shown in Table 2 were used to obtain the DC bus circulating current under four different scenarios: without a common-mode inductor and without the algorithm, without a common-mode inductor but with the algorithm, with a common-mode inductor but without the algorithm, and with both a common-mode inductor and the algorithm, as shown in Figure 12.

The self-resistance, self-inductance, mutual resistance, and mutual inductance of the common-mode inductor between the busbars on both sides of the inverter in the motor emulator system shown in Figure 3 were set to 0.01 Ω, 0.002 H, 0.009 Ω, and 0.0019 H, respectively.

When the circulating current suppression method is not enabled, the amplitude of the circulating current is 91% of the phase current. Without taking the relevant method to suppress it, it will seriously affect the emulation accuracy of the system. In the absence of common-mode inductance, after enabling the modulation algorithm, the steady-state absolute mean value of the DC bus circulating current in the system decreased from 29.75 A to 16.11 A, a reduction of 45.8%; meanwhile, the amplitude of the circulating current decreased from 182.6 A to 48.75 A, a reduction of 73.3%. This proves the effectiveness of the proposed algorithm for low-frequency circulating current suppression, which can control the low-frequency component of the circulating current within a reasonable range.

When using the modulation algorithm in conjunction with common-mode inductance, the steady-state absolute mean value of the DC bus circulating current in the system decreased from 10.27 A to 5.05 A, a reduction of 50.8%; the amplitude of the circulating current decreased from 28.58 A to 8.31 A, a reduction of 70.9%, down to 4.2% of the phase current. This proves the effectiveness of the proposed method, which, when used in conjunction with common-mode inductance, achieves better DC bus circulating current suppression effects. Additionally, the performance and volume requirements for common-mode inductors can be lower with the algorithm, thereby maintaining system performance and reducing system cost and structural complexity.

5. Experiment Results

To verify the effectiveness of the circulating current suppression method for the single power supply topology, a minimal system of the MCU and EME test experimental platform was built. Both the motor controller and the motor emulator were designed as three-phase two-level structures, composed of six groups of SiC MOSFET power devices connected in parallel to reduce platform cost and increase expandability. Moreover, in order to simplify the experiment, a single chip was used to simultaneously control the MCU and the EME, thereby avoiding the high-frequency circulating current problem caused by the carrier

wave being out-of-sync. The experimental platform is shown in Figure 13. The system experiment parameters are listed in Table 3, the system speed was kept constant, with the d-axis target current set to 0 A and the q-axis target current set to 2 A.

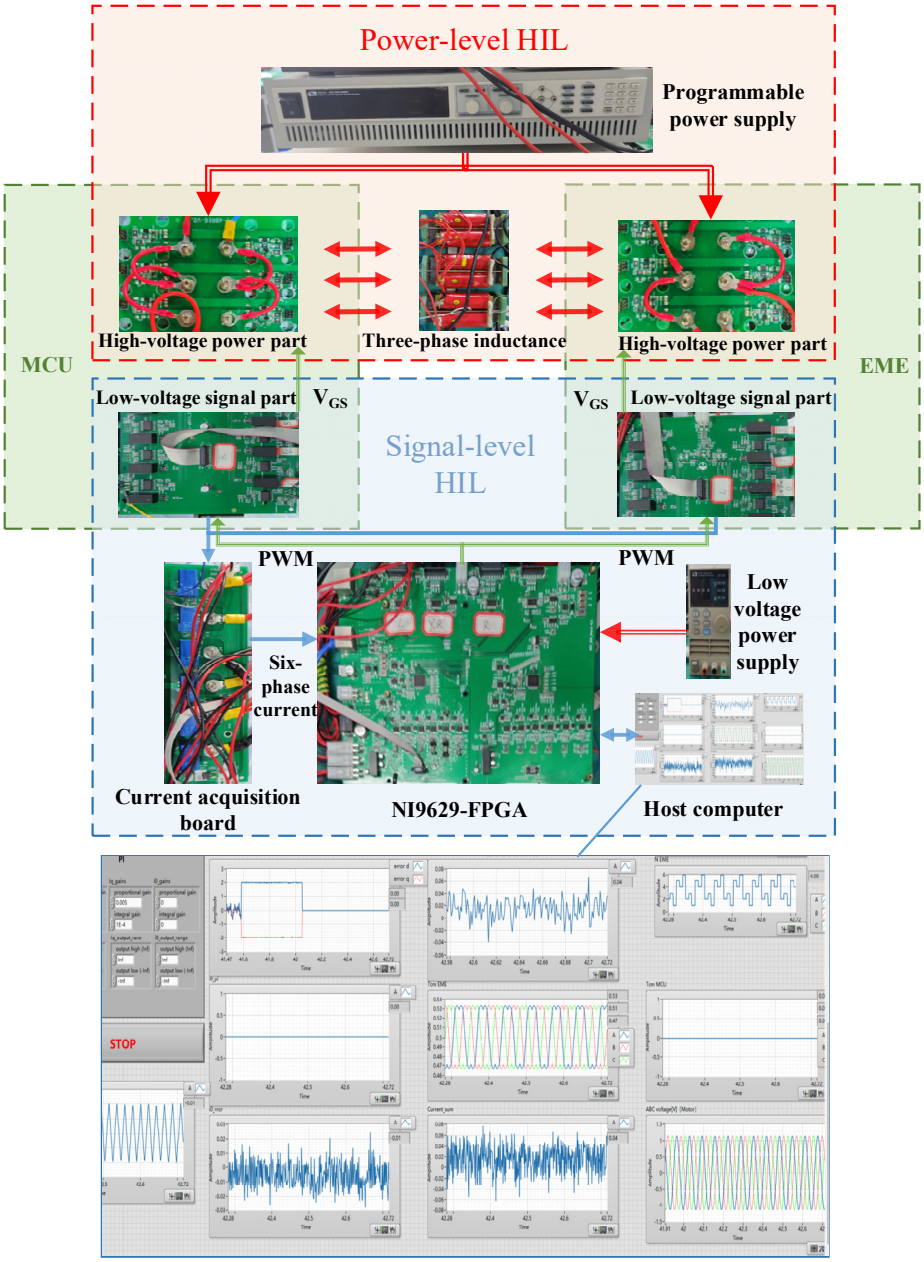

Figure 13. Motor emulator and motor controller common DC bus experimental platform.

Table 3. Experiment parameters.

Parameter	Value	Symbol
DC voltage	30	V
Switch time	10	kHz
Dead time	3	μs
Pole pairs	4	-
Stator resistance	0.08	Ω
Permanent magnet flux linkage	0.366	Wb
d-axis inductance	0.25	mH
q-axis inductance	0.25	mH

A comparison experiment between the dual power supply system (Figure 2) and the single power supply system (Figure 3) is firstly made. In this experiment, both systems used the classical SVPWM modulation algorithm without common-mode inductors. As shown in Figure 14, the circulating current in the dual power supply system is approximately zero, and the peak-to-peak circulating current in the single power supply system exceeds 2 A even under 30 V DC voltage, which validates the above-mentioned analysis.

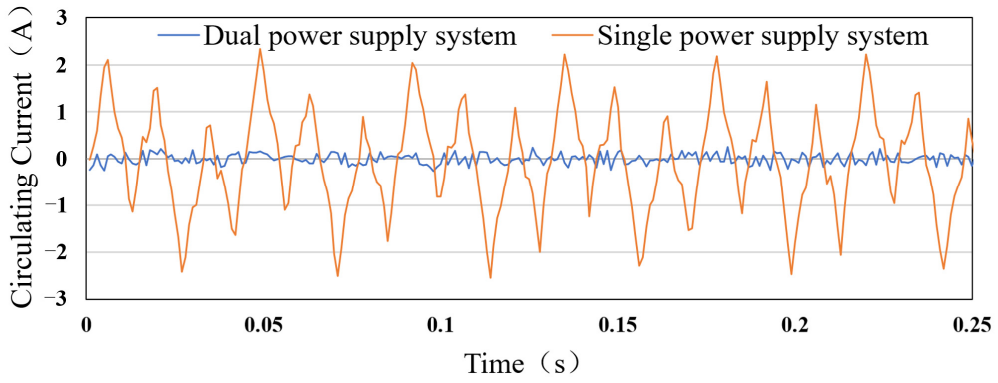

Figure 14. System circulating current in different power supply systems.

With the circulating current suppression algorithm not enabled, the system's circulating current and three-phase current are shown in Figures 15 and 16, respectively. At this point, the system lacks any hardware filtering structures such as common-mode inductors. Figure 15 illustrates that, in the absence of the circulating current suppression algorithm, the maximum absolute value of the circulating current is 1.99 A, which has a markedly detrimental impact on the sinusoidal quality of the three-phase current. Consequently, the three-phase current of the system (Figure 16) deviates from the standard sinusoidal waveform.

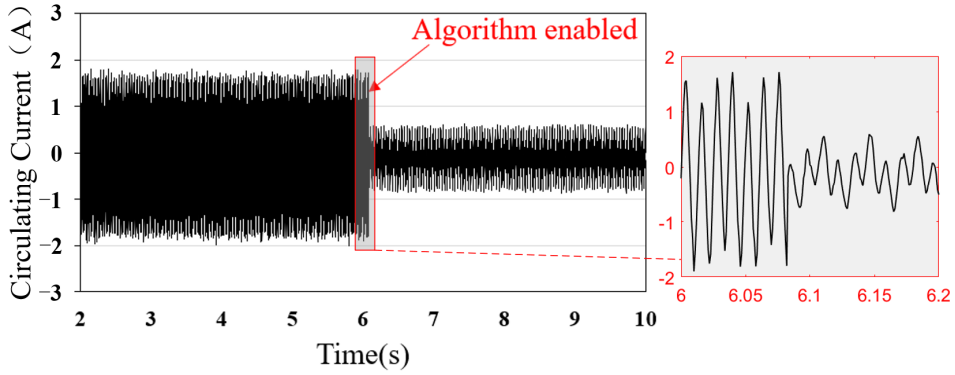

Figure 15. System circulating current without common-mode inductors.

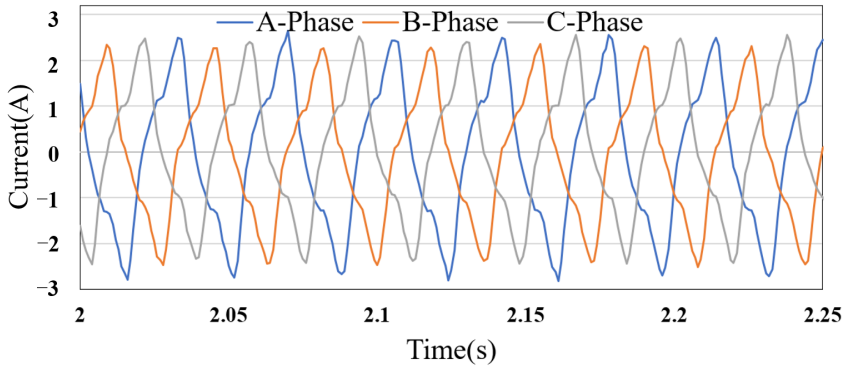

Figure 16. Three-phase current with neither common-mode inductors nor algorithm.

At 6.1 s, the circulating current suppression algorithm was initiated. At this juncture, the maximum value of the system's circulating current decreased to 0.58 A, representing a 70.9% reduction compared with the value observed prior to the activation of the algorithm. The amplitude of the circulating current was 26.4% of the phase current, representing a 59.6% reduction compared with the pre-algorithm current, and thus exerting a less impactful influence on the phase current. As illustrated in Figure 17, the system's actual three-phase current, in comparison to Figure 16, exhibited a notable enhancement in sinusoidal waveform quality. This suggests that the suppression algorithm facilitated the EME in generating higher-quality steady-state signals, thereby enabling more precise emulation of the characteristics of permanent magnet synchronous motors.

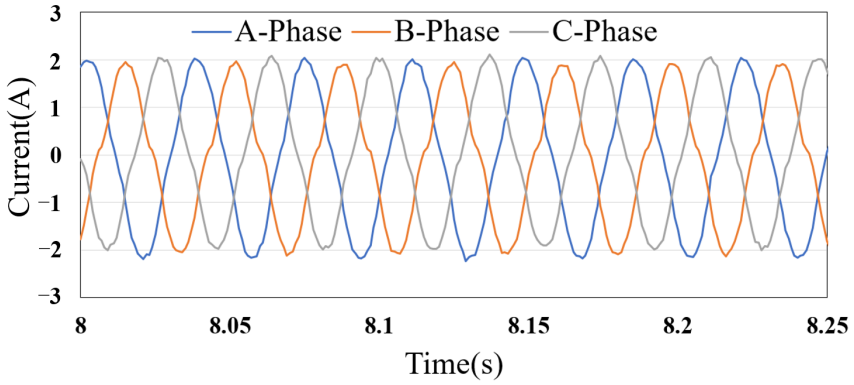

Figure 17. Three-phase current without common-mode inductors but with algorithm.

Figure 18 illustrates that prior to and subsequent to the activation of the algorithm, the system's d-axis current remains in close proximity to the target command of 0 A, while the q-axis current remains in close proximity to the target command of 2 A. This indicates that the actual d-q axis currents align well with the target currents.

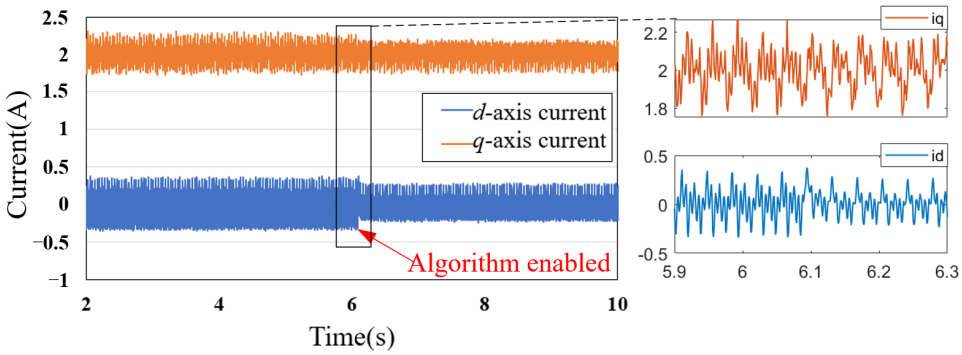

Figure 18. Difference of *d-q* axis current before and after algorithm enabled.

Before the algorithm was activated, the maximum absolute value of the d-axis current tracking error was 0.38 A, while the maximum absolute value of the q-axis current tracking error was 0.32 A. After activating the algorithm, the fluctuations in the d-q axis currents become smaller due to the improvement in the sinusoidal quality of the actual three-phase current. The maximum absolute value of the d-axis current tracking error decreased to 0.29 A and the maximum absolute value of the q-axis current tracking error decreased to 0.21 A. This represents reductions of 23.68% and 34.38%, respectively, compared with the current before the algorithm was activated, resulting in more accurate emulation performance.

Furthermore, a comparison was made of the circulating current in the system with the common-mode inductor (self-inductance is 200 uH) (Figure 19). After activating the circu-

lating current suppression algorithm, the amplitude of the circulating current decreased to 0.42 A, a reduction of 78.9% compared with the previous value. This demonstrates the effectiveness of the proposed suppression method for low-frequency components of the circulating current. It also indicates that when the proposed algorithm is used in conjunction with the common-mode inductor, better circulating current suppression can be achieved. The specific results are shown in Table 4.

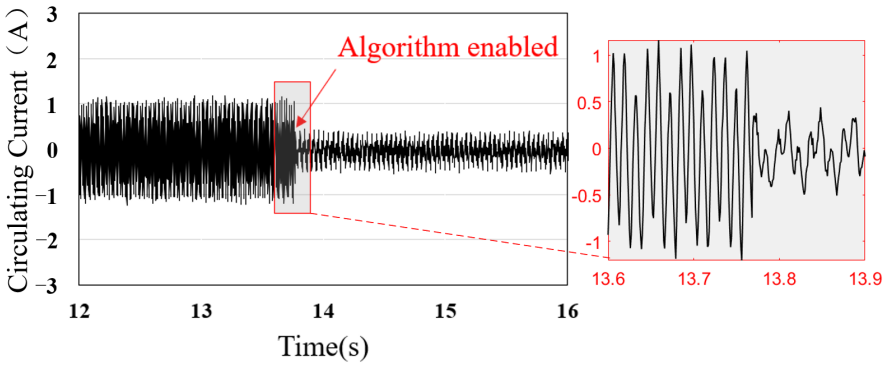

Figure 19. System circulating current with common-mode inductors.

Table 4. Comparison of system circulating current amplitude.

Inductor	Algorithm	Circulating Current	Amplitude	Phase Current THD
Without	Without	1.99 A	-	25.68%
Without	With	0.58 A	−70.9%	6.79%
With	Without	1.21 A	−39.2%	15.37%
With	With	0.42 A	−78.9%	4.89%

6. Conclusions

This study primarily investigates methods for suppressing circulating currents in a motor controller and motor emulator with a common DC bus topology. The low-frequency zero-sequence circulating current generation mechanism of the system is analyzed, and expressions for common-mode voltage (zero-sequence voltage) and circulating current are derived. A control method based on the Hybrid PWM Strategy is proposed, and effective suppression of zero-sequence circulating currents is achieved, which significantly improves the sinusoidal quality of the three-phase current output by the EME in the common DC bus topology. Effective suppression of zero-sequence circulating currents can also reduce system loss and improve the lifetime and reliability of equipment.

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