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Gradually Tunable Conductance in TiO_2/Al_2O_3 Bilayer Resistors for Synaptic Device

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Abstract: In this work, resistive switching and synaptic behaviors of a TiO_2/Al_2O_3 bilayer device were studied. The deposition of $Pt/Ti/TiO_2/Al_2O_3/TiN$ stack was confirmed by transmission electron microscopy (TEM) and energy X-ray dispersive spectroscopy (EDS). The initial state before the forming process followed Fowler-Nordheim (FN) tunneling. A strong electric field was applied to Al_2O_3 with a large energy bandgap for FN tunneling, which was confirmed by the I-V fitting process. Bipolar resistive switching was conducted by the set process in a positive bias and the reset process in a negative bias. High-resistance state (HRS) followed the trap-assisted tunneling (TAT) model while low-resistance state (LRS) followed the Ohmic conduction model. Set and reset operations were verified by pulse. Moreover, potentiation and depression in the biological synapse were verified by repetitive set pulses and reset pulses. Finally, the device showed good pattern recognition accuracy (~88.8%) for a Modified National Institute of Standards and Technology (MNIST) handwritten digit database in a single layer neural network including the conductance update of the device.

Keywords: neuromorphic system; synaptic device; resistive switching; metal oxides; bilayer

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1. Introduction

Resistive switching (memristive effect) was observed from an SiO_x layer in the 1960s. Resistance-based memory is considered a computing element and a storage element. Resistance-based memories are largely classified into three types, with each memory type having its advantages and disadvantages. Spin-transfer torque (STT)-magnetic random-access memory (MRAM) [1] has fast switching speed and long endurance. However, its on/off ratio is small and its scalability is inferior to others. Phase-change random-access-memory (PcRAM) [2] has an intermediate character between dynamic random-access memory (DRAM) and NAND flash in terms of latency and memory density. It is used for storage class memory (SCM). Resistive random-access memory (RRAM) [3–10], in which many materials can be used, has various properties. Interface type RRAM has good variability with multi-level cell (MLC). However, it has a slow switching speed [7]. Filamentary type RRAM has fast switching speed and good endurance. Unfortunately, its variation of resistance state is not good [11]. Among a lot of resistive switching materials, such as oxides [12–17], nitrides [18–20], organic materials [21] and 2D materials [22], oxides such as HfO_2, TaO_x, TiO_2, and Al_2O_3 are good candidates in terms of the endurance, stability, repeatability and reproducibility. The bilayer structure of oxide can enhance resistive switching performances. For example, HfO_2/Al_2O_3 dielectric stack on silicon can reduce operation current level [23]. The uniformity of cell-to-cell and device-to-device is improved in a TiO_x/Al_2O_3 bilayer dielectric stack [24]. HfO_2/Al_2O_3 bilayer device on TiN electrode can increase the nonlinearity of an I-V curve in the low-resistance state for high-density memory [25]. The stabilization is improved in a ZrO2(Y)/Ta_2O_5 bilayer device due to the electric field concentration of Ta nanocrystals [26]. TiO_2 is one of the important resistive switching materials showing unipolar and bipolar resistive switching behaviors [27]. A lot of resistive switching behaviors including gradual and abrupt switching have been

reported in various stacks. Al_2O_3 with large band gap can be used as a tunnel barrier layer as well as a resistive switching material [24,25].

RRAM devices show long-term and short-term plasticity to realize biological synapse for a neuromorphic system [28–31]. Many conductance states of memristor devices should be accurately and gradually controlled with the applied voltage bias. The state changed by the pulse can be maintained for a long time for off-chip learning in a neuromorphic system. To meet MLC with fine tuning, gradual set and reset switching in an RRAM device is essential. Many studies have been conducted on MLC improvement at the device level. Especially, optimizing a bilayer device is a powerful way to improve the gradual switching to achieve MLC. For example, synaptic properties are enhanced in a Ta_2O_5/HfO_2 device by controlling the conductance gradually [32]. Recently, similar results have been found for TiO_x/Al_2O_3 [33] and ZrO_2/ZTO bilayer devices [34]. An additional insulating layer can act as series resistance so that gradual resistive switching behavior can be obtained during conductance transition.

In this work, a TiO_2/Al_2O_3 bilayer device was fabricated for synaptic device application. Chemical and material compositions were verified by transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS). We investigated resistive switching characteristics and conduction mechanisms, including initial state before forming low-resistance state (LRS) and high-resistance state (HRS). Gradual increase and decrease of conductivity were demonstrated by set pulse and reset pulse. Finally, MNIST pattern recognition accuracy was calculated by neuromorphic simulation composed of a single layer neural network by applying conductance of the device into weight of the network.

2. Materials and Methods

The Ti/TiO_2/Al_2O_3/TiN memory device was prepared as follows—a 100-nm thick TiN bottom was deposited by DC sputtering. The Ti target was reacted with nitrogen (N_2: 3 sccm and Ar: 20 sccm) to deposit TiN film in which the pressure was 1 mTorr and the power was 500 W.

A 2-nm thick Al_2O_3 layer was deposited with an atomic layer deposition (ALD) system. $Al(CH_3)_3$ (TMA) and H_2O were used as precursors for Al_2O_3 deposition at a chamber temperature of 200 °C. A 16 nm thick TiO_2 layer was then deposited by pulsed sputtering at room temperature. The Ti target was reacted with oxygen in plasma conditions. Flow rates of argon and oxygen were 12 and 8 sccm, respectively. Ti top electrode and Pt capping layer were deposited by DC sputtering and e-bema evaporator after the shadow mask was attached on the TiO_2 layer. Each cell was separated by removing the mask.

The electrical properties of basic I-V curves were characterized in DC mode using a Keithley 4200-SCS semiconductor parameter analyzer (SPA, Keithley Instrumnets, Cleveland, OH, USA). Transient characteristics, potentiation, and depression curves were measured in pulse mode using a 4225-PMU ultrafast module. During measurements, a bias voltage and a pulse were applied to the Pt capping layer while maintaining the ground on the TiN bottom electrode.

3. Results and Discussion

Figure 1a shows a high-resolution TEM image of the Pt/Ti/TiO_2/Al_2O_3/TiN memory device. The layer between TiO_2 and TiN was thicker than the 2 nm target thickness of Al_2O_3, indicating that the TiON layer was created as an interfacial layer by reacting Al_2O_3 and TiN layers during Al_2O_3 deposition. A TiO_2 layer about 16 nm thick as the main switching material, a Ti electrode, and a Pt electrode were clearly observed in the TEM image. Figure 1b shows the EDS line scan to detect elements as a function of the location, confirming the deposition of each layer.

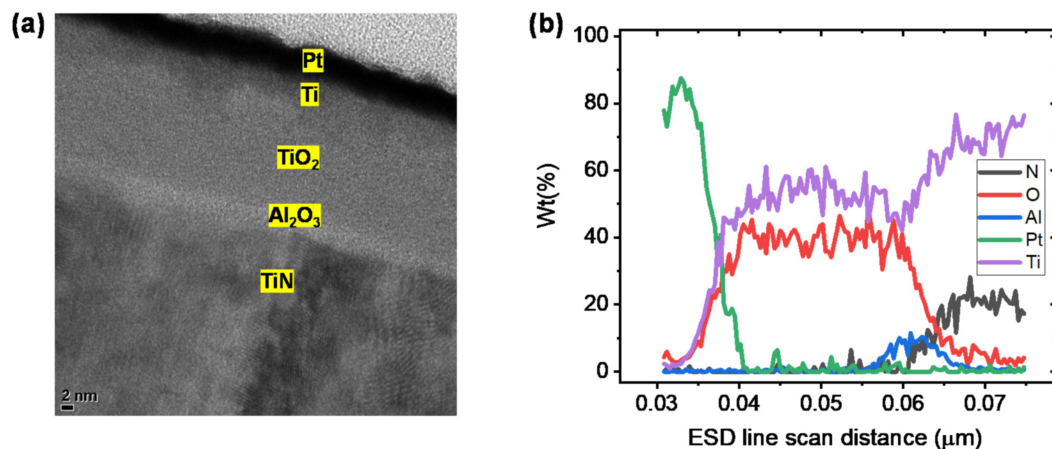

Figure 1. (**a**) High resolution transmission electron microscopy (TEM) image and (**b**) Energy-dispersive spectroscopy (EDS) line scan of a $Pt/Ti/TiO_2/Al_2O_3/TiN$ device.

Figure 2a shows the I-V curve of the forming process, which can activate the device before the set and reset processes. The Al_2O_3 layer has an important role in the conduction mechanism of the $Pt/Ti/TiO_2/Al_2O_3/TiN$ memory device before breakdown of the device. The Al_2O_3 layer in the initial state can act as a tunnel barrier. In a high field region (>2 V), FN tunneling can be a dominant mechanism in which electrons can tunnel more easily through the triangular barrier induced by a high electric field (Figure 2b). The FN tunneling equation is shown below [35]:

$$J = \frac{q^3E^2}{8\pi hq\phi_B} \exp\left[-\frac{8\pi(2qm^*)}{3hE}\right]{\phi_B}^{3/2} \quad (1)$$

where h is plank constant, q is electronic charge, m^* is the effective electron mass, and E is the electric field. Thus, the straight line in $\ln(I/V^2)$ versus $1/V$ at more than 2 V means this region follows FN tunneling as shown in Figure 2c.

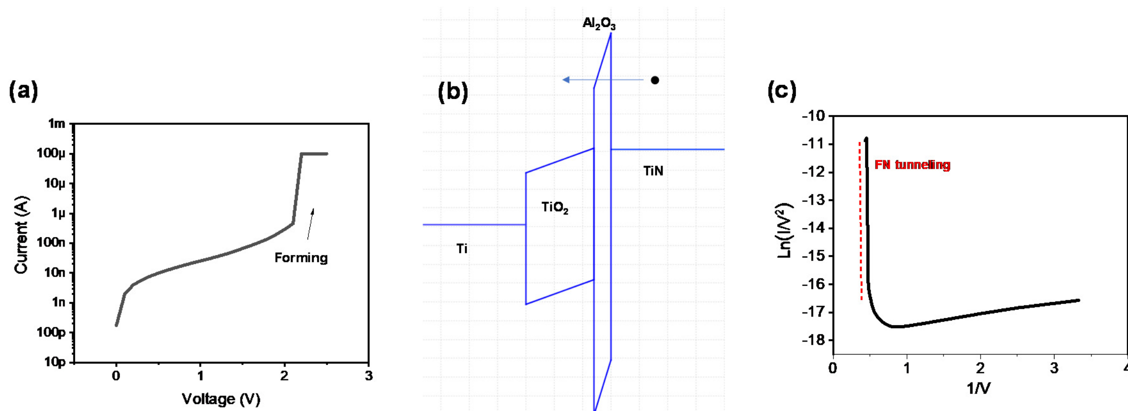

Figure 2. (**a**) Forming I-V characteristics, (**b**) Fowler-Nordheim (FN) tunneling illustration in energy band structure, (**c**) $Ln(I/V^2)$ versus $1/V$.

Figure 3a shows set and reset processes of the $Ti/TiO_2/Al_2O_3/TiN$ memory device after electroforming process. The set process occurred under a positive bias in which the conducting defect (oxygen vacancies) was induced in both layers. Here, the device did not need a specific compliance current for the set process due to self-compliance. The self-compliance occurred with series resistance. In this device, TiON and Al_2O_3 layers could act as the series resistance. The set process was progressively completed. The oxygen ions with a negative charge moved toward a Ti top electrode with a positive bias. Oxygen

vacancies were increased in the TiO_2 layer, leading to an increase in the conductance of the $Ti/TiO_2/Al_2O_3/TiN$ system. On the other hand, the reset process happened in a negative bias. The reset process induced a decrease in the conductance gradually. When a negative bias was applied, oxygen vacancies recombined with oxygen ions from the top electrode. To reveal conduction mechanisms of LRS and HRS, I-V fitting processes were conducted. Firstly, we checked FN tunneling for LRS and HRS. However, the fitting accuracy was very low (now shown here). It indicated that large conducting defects existed at both insulating layers after the forming process. Thus, the Al_2O_3 layer no longer served as a strong tunnel barrier. The possible conduction model of HRS was trap-assisted tunneling (TAT). The TAT model equation is shown below [36]:

$$J \propto \exp\left[\frac{-4\sqrt{2qm)}}{3hE}\right]{\phi_t}^{3/2} \tag{2}$$

where m is the effective mass in the insulator and ϕ_t is the energy level of the defect state. The conduction of the electron is strongly dependent on the trap concentration that can be induced by the applied bias. In other words, traps induced in the thin films by the electroforming process can affect this TAT. Figure 3b shows Ln(I) versus 1/V for TAT fitting. It can be seen that the HRS curve fits the TAT well within a voltage range greater than 1.2 V. Figure 3c shows a log–log fitting of I-V in the LRS. Linear fitting means that LRS follows Ohmic conduction and conducting defects could be connected to top and bottom electrodes via two insulators.

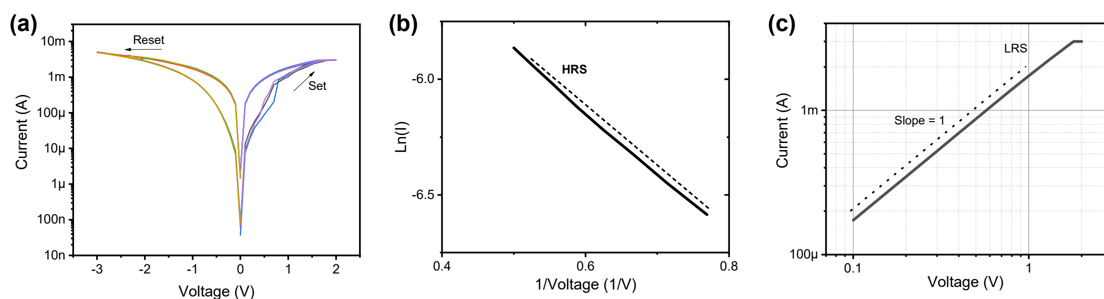

Figure 3. (**a**) Set and reset I-V characteristics, (**b**) Ln(I) versus 1/V fitting for high-resistance state (HRS), (**c**) Log-log scale for Ohmic conduction in the low-resistance state (LRS).

Figure 4a shows the transient characteristics of $Ti/TiO_2/Al_2O_3/TiN$ memory device by set and reset pulses. Set and reset pulse voltages were 3 V and −2 V, respectively. The set process occurred during the rising time when the pulse voltage was raised and the reset process was completed after the voltage reached −2 V. Read pulses were added before and after the main switching pulses to check whether a set or reset had occurred. A read voltage of 0.3 V was used so that it would not impact set or reset switching ranges. Increase and decrease of the current were clearly observed after applying set and reset pulses.

Multiple conductances are needed to mimic biological synapses and implement a hardware-based neuromorphic system. Figure 4b shows conductance modulation by pulse inputs to emulate the potentiation and depression of a biological synapse. As the same pulse with a voltage of 4 V was repeatedly applied to the device 49 times, the conductance gradually increased from the HRS to the LRS. Although it tended to decrease after applying the set pulse at a few points, the conductance generally increased and potentiation was successfully emulated. On the other hand, multiple pulse inputs with a voltage of −1.35 V decreased the conductance gradually for the potentiation.

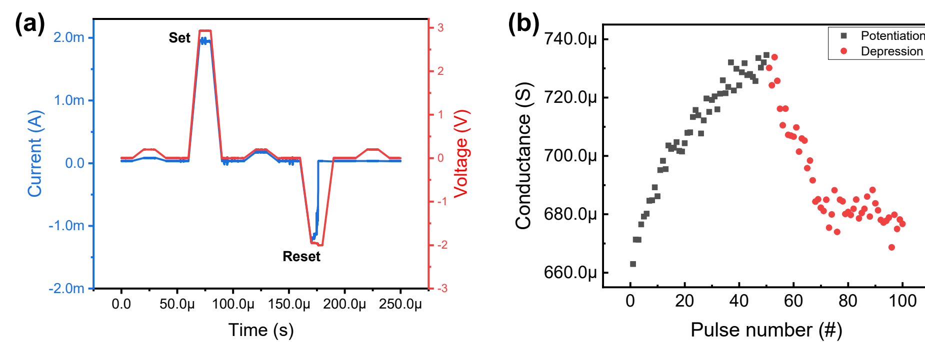

Figure 4. (**a**) Set and reset transient characteristics including set pulse, reset pulse, and read pulses; (**b**) Potentiation and depression curve as a synaptic device.

Next, MNIST pattern recognition accuracy was determined when the device's conductance was used as the weight of the synapse in the neuromorphic system. Figure 5a shows a neural network composed of a single layer network (784 × 10) for the neuromorphic simulation. This neuromorphic simulation was based on off-chip learning. The input neuron was the MINST binary dataset with 28 × 28 pixel images and 10 output neurons to classify 10 classes. Two neuron nodes were fully connected to the synapse. Conductance values from a single cell device were used as weights of synapse including exhibitory and inhibitory ones. Here, it was assumed that all cells in the array had the same characteristics as the measured single cell. The recognition rate might decrease due to variation when an actual array was configured. The weight update of the device was conducted with a vector-matrix multiplication operation. Figure 5b shows the pattern recognition accuracy as a function of the number of training images. As training continued, the overall recognition rate improved. The maximum recognition rate was about 88.8%. The weight of synapse can be optimized in the neural network with training. Thus, an incomplete conductance update will eventually adversely affect the recognition rate.

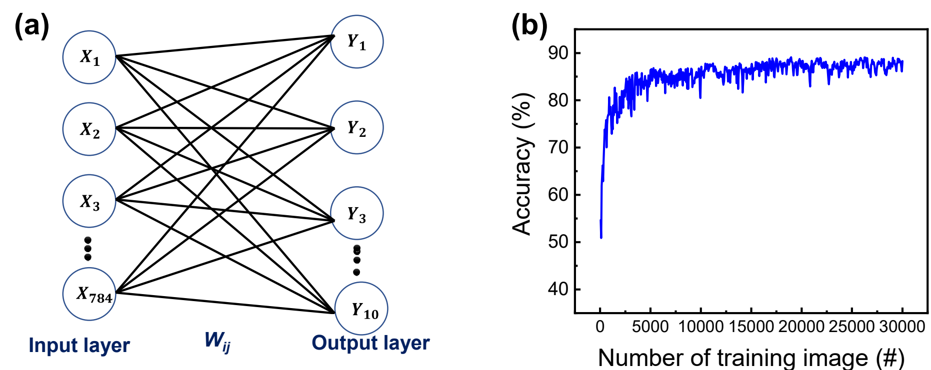

Figure 5. (**a**) Single layer neural network including input neuron, synapse, and output layer, (**b**) accuracy as a function of training epoch.

4. Conclusions

In summary, a TiO_2-based RRAM device with a thin Al_2O_3 layer was fabricated for neuromorphic application. $Pt/Ti/TiO_2/Al_2O_3/TiN$ stack was verified by TEM and EDS analyses. The conduction mechanism of an initial state can be explained by FN tunneling in the high voltage regime. Gradual set and reset switching were obtained under a DC sweep mode. HRS and LRS followed the TAT model and Ohmic conduction. Transient characteristics were well observed by applying set pulse and reset pulse. The conductance is tunable by applying set pulse and reset pulse, which can act as a synaptic device in a hardware based neuromorphic system. Finally, we evaluated the pattern recognition accuracy by constructing a single layer neural network including the measured conductance as synaptic weight. An accuracy of 88.8% was achieved due to a multi-level conductance.

Author Contributions: H.R. conducted electrical measurements and wrote the manuscript; S.K. designed the experiment and supervised the study. All authors have read and agreed to the published version of the manuscript.

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