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Improvement in Electrical Stability of a-IGZO TFTs Using Thinner Dual-Layer Dielectric Film

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Abstract: This study investigates the effect of gate insulators on thin-film transistors (TFTs) using an amorphous $InGaZnO_4$ (a-IGZO) channel layer. TFTs with single-layer Ta_2O_5 and dual-layer Ta_2O_5/SiO_2 gate insulators were fabricated on a glass substrate. An evaluation of the insulating film using the MIM (Metal-Insulator-Metal) structure confirmed its electrical characteristics. Microscopic imaging showed that the dual-layer Ta_2O_5/SiO_2 dielectric significantly improved surface characteristics. A reduction in the leakage current, better on/off ratios, and a decreased subthreshold swing (SS) compared to a single-layer Ta_2O_5 dielectric were reported. The dual-layer insulator composed of SiO_2/Ta_2O_5 was highly effective in improving device characteristics.

Keywords: a-IGZO; dual-layer dielectric; high-*K*; oxide TFT

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1. Introduction

Oxide semiconductor materials have emerged as novel candidates for large-area silicon devices. In particular, amorphous $InGaZnO_4$ (a-IGZO), a transparent amorphous oxide semiconductor, has attracted considerable attention because of its high electron mobility [1–4]. In addition, Nomura et al. and Yabuta et al. demonstrated the fabrication of high-performance amorphous *a*-IGZO thin-film transistors (TFTs) using pulsed laser deposition [1] and RF sputtering [3]. a-IGZO has a carrier mobility of 10 $cm^2/(Vs)$ or more and can control the carrier concentration even in the amorphous phase [5]. This mobility value is much higher than organic or other amorphous oxide semiconductors. This high mobility is due to the overlap of the ns-orbital of the metal cation, being larger than the 2p-orbital of the oxygen anion; a-IGZO exhibits high mobility while having an amorphous structure.

The utilization of a-IGZO TFTs as switching elements in flat-panel displays, such as liquid-crystal displays (LCDs), organic light-emitting diode displays, and electronic paper, is of particular interest [6–8]. Currently, hydrogenated amorphous silicon (a-Si:H) TFTs are commonly used as switching elements in the display industry. Although both *a*-IGZO and a-Si:H are amorphous semiconductors, they differ in their material properties; including the carrier generation mechanisms and the chemical bonding structures. Understanding the key features of a-IGZO TFT, which are different from the existing a-Si:H TFT, is important for commercial use of a-IGZO [9–11]. However, the carrier movement of semiconductor materials greatly affects device performance. It is essential to remove these defects [12]; in addition, electrical contact between the channel and source/drain also determines the electrical performance of the device. For this purpose, an additional heat treatment process is required [13].

In consideration of this, research on various gate dielectric film materials (HfO_2 [14], Al_2O_3 [15,16], Ta_2O_5 [17,18], Y_2O_3 [19], and ZrO_2 [20]) has been conducted in order to improve the performance of the transistor.

SiO_2 has long been the gate dielectric material selected for silicon device applications due to its excellent materials and interfacial properties, including: (i) device-quality films that can be grown directly on silicon; (ii) a large energy band gap (~9 eV) [21]; (iii) relatively large conduction and valence band offset energies with respect to Si (~3.2 eV and 4.5 eV, respectively); (iv) high effective electrical resistivity (10^{15}–10^{17} Ωcm); (v) excellent dielectric breakdown strength (>10^7 V/cm); (vi) low bulk and interface defect densities (<10^{16} cm^{-3} and <10^{11} cm^{-2}, respectively); and (vii) excellent thermal stability in contact with crystalline Si [22]. These studies show that device performance is limited by the tunneling leakage current through ultrathin (< 2 nm) SiO_2 dielectrics, which are required in the devices with aggressively scaled gate lengths. Recently, high-*K* oxides containing transition metals or rare earth elements (including ternary silicate and aluminate phases) have attracted attention as alternatives to conventional gate dielectrics [23]. High-*K* gate dielectrics can potentially provide comparable device performance with a much thicker dielectric layer, thereby significantly reducing tunneling leakage currents. A comprehensive study of all known elemental and multi-component oxides using a thermodynamic approach identified several high-*K* gate dielectric candidates with excellent silicon compatibility [24,25]. Among high-k gate dielectric materials, Ta_2O_5 is one of the most promising materials due to its high dielectric constant (22~60), low leakage current, excellent dielectric breakdown strength, thermal and chemical stability, and other properties. Moreover, in order to be applied to a flexible substrate of a transistor device, the factor of temperature cannot be ignored. Conventional chemically deposited organic dielectrics give good results for transistor properties; however, they require slow and high temperatures in growth and curing processes to form organic thin films [26,27]. In order to solve these factors, attempts have been made to manufacture a dielectric capable of low-temperature processing using rf magnetron sputtering. However, in the case of a thin film prepared in this way, it affects the growing film and its interface [28–32]. In the electrical characteristics of IGZO TFT, reduction of leakage current, improvement of surface roughness, and reduction of charge trapping density are essential factors. In order to solve these factors, considering the physical and low-temperature processes, the interface quality of the high-temperature process, SiO_2, is excellent. In addition, most high dielectric constants exhibit polycrystalline structures and rough surfaces; which can contribute to reduced reliability and degraded interfacial properties. Furthermore, high-k dielectrics typically exhibit a lower bandgap and smaller band offset (by semiconductors) than conventional SiO_2; this results in lower breakdown voltages and higher leakage currents.

The overall performance of the transistor is very dependent on the gate insulating film; and it is necessary to apply a high-k, high-k thin film to drive the transistor at a low voltage. The conventional gate insulating film mainly uses a SiO_2 thin film through a high-temperature process. However, for application to devices requiring a lower process temperature, an alternative insulating film or process technology is essential. However, when using a high-k gate insulating film, there may be disadvantages in that the leakage current is high and the breakdown voltage is lowered in terms of electrical performance due to the relatively lower band gap and band offset than that of SiO_2; as well as the polycrystalline structure and surface roughness. Due to these factors, studies on double stacking [17,18], multi-layer [33], and multi-component structures [34] using high-k gate materials and conventional SiO_2 materials have recently been conducted. Therefore, instead of using one type of high-k gate insulating film, it is necessary to secure an oxide TFT with high mobility and stable characteristics by using the existing SiO_2 and SiNx insulating film, and a study on the stacked structure of the high-k insulating film. In order to secure transistor characteristics even in low-temperature processes and thin thicknesses, we developed an oxide transistor with a dual structure of gate insulating film of low-temperature process SiO_2 and room temperature process high dielectric constant Ta_2O_5 thin film.

2. Materials and Methods

The oxide transistor constructed for this study had a bottom-gate structure. A glass plate (5 cm × 5 cm) was used as the substrate. Molybdenum (Mo) was used to construct the gate, source, and drain electrodes. For the deposition of Mo thin films, a Mo target (4-inch diameter) was sputtered with argon (Ar) at room temperature using a DC sputtering system. The base and working pressures of the sputtering chamber were 4.3 x 10^{-5} Torr and 6.7 mTorr, respectively. The applied DC power was 100 W, and the thickness of all the Mo thin films was controlled at 150 nm. The Mo thin films were carefully deposited as the source and drain electrodes after the deposition of the a-IGZO films. Mo thin films provide ohmic contact with the a-IGZO semiconductor layer and have negligible contact resistance [35].

An a-IGZO thin film, which forms the semiconductor layer, was deposited via RF magnetron sputtering. A ceramic $InGaZnO_4$ target (2-inch diameter) was sputtered using Ar plasma at room temperature. The thickness of the a-IGZO layer was controlled at 30 nm. The substrate and the target were 7 cm apart; and the substrate holder rotated at 1 rpm to ensure the uniformity of the deposited thin films. During sputtering, the RF power, chamber pressure, O_2 flow rate, and Ar flow rate were maintained at 100 W, 10 mTorr, 6 sccm, and 54 sccm, respectively.

A Ta_2O_5 film (30 nm thick) was deposited on the substrate using RF magnetron sputtering. During the deposition process, the O_2 ratio was maintained at 30%; and the deposition rate was 3 nm/min. The RF power, chamber pressure, O_2 flow rate, and Ar flow rate were maintained at 100 W, 2 mTorr, 6 sccm, and 14 sccm, respectively.

SiO_2 film (30 nm thick) was deposited on the substrate using a plasma-enhanced chemical vapor deposition (PECVD) system. During sputtering, the RF power, SiH_4 and N_2O flow rates, and temperature were maintained at 140 W, 4 sccm, 2000 sccm, and 300 °C, respectively.

All the patterning processes, except for defining the source and the drain, were performed using photolithography. The gate length and width of the fabricated a-IGZO TFT were 7 µm and 100 µm, respectively. Post-heat treatment of some transistors was performed in conventional thermal treatment equipment (tube furnace, OTF-1200X, MTI, Richmond, CA, USA) at 300 °C for 2 h in the state of continuously injecting oxygen.

The thickness and microstructures of the a-IGZO thin films were observed using a field emission scanning electron microscope (FE-SEM, Nova Nano SEM 200, FEI, Hillsboro, OR, USA). X-ray diffraction (XRD, Dmax2500/PC) analysis was conducted to obtain information on the structure of the crystalline material. The leakage current densities and electrical properties of the TFTs were measured using a Keithley 4200A-SCS source measure unit. All the electrical properties were measured in the dark.

Figure 1a gives a schematic description of a dual-layer gate insulator in the a-IGZO transistor. The optical microscope results, as shown in Figure 1b, confirmed that the width and the length of the channel are 100 µm and 7 µm, respectively.

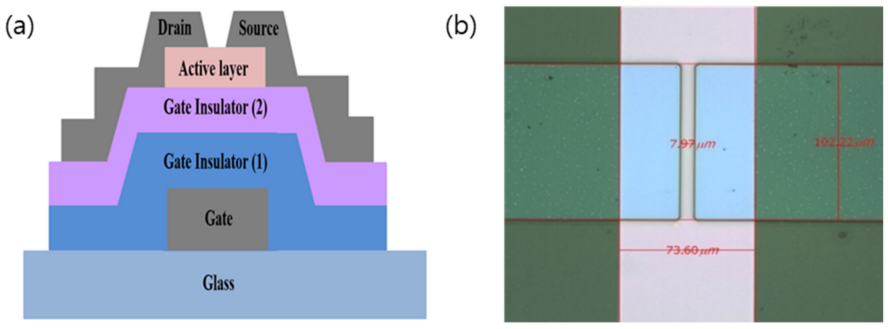

Figure 1. (**a**) Schematic structure of a-IGZO TFT with a dual-layer gate insulator. (**b**) Top view of the channel using an optical microscope.

3. Results

The a-IGZO/Si/SiO_2 and Ta_2O_5/Mo/SiO_2/Si structures were confirmed by SEM. FE-SEM imaging (Figure 2a,b) confirmed that the a-IGZO film of the channel layer and the Ta_2O_5 film of the gate insulator layer were 30 nm thick and the electrode Mo was 150 nm thick. Figure 2c shows the XRD pattern of an a-IGZO layered structure grown on a Si/SiO_2 substrate. In order to confirm the change of the IGZO film before and after the heat treatment, the samples that were not heat treated and the samples that were heat treated at 300 °C for 2 h in an oxygen atmosphere were analyzed. Two halo peaks were observed at around 22° and 34°.

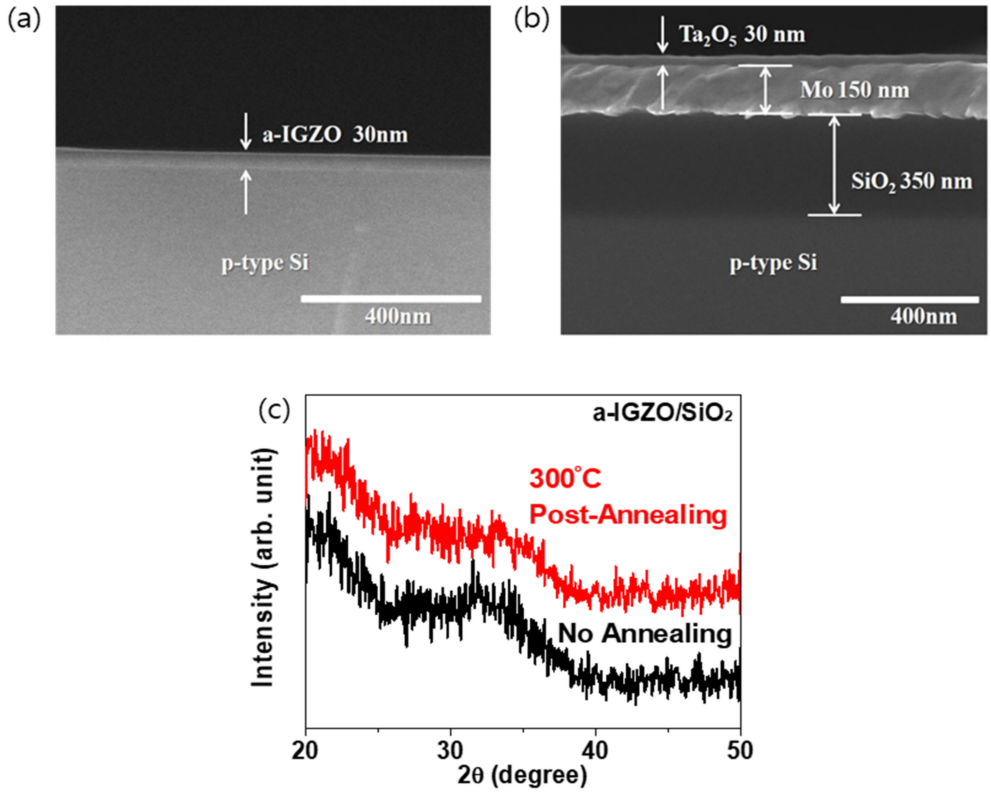

Figure 2. (**a**) The cross-sectional FE-SEM image of the a-IGZO/SiO_2/Si structure; (**b**) the Ta_2O_5/Mo/SiO_2/Si structure; and (**c**) an XRD pattern of the a-IGZO/SiO_2 layered structure grown on a Si substrate by sputtering.

Figure 3a,b show the surface characteristics of Ta_2O_5 (60 nm) and SiO_2/Ta_2O_5 (30 nm/30 nm). We can see that the surface properties were improved by depositing SiO_2 at the bottom and Ta_2O_5 at the top. The dual-structure SiO_2/Ta_2O_5 (30 nm/30 nm) thin-film had an RMS characteristic of 0.385 nm, which was reduced by about 21% compared to the surface characteristic of the Ta_2O_5 single layer of 0.487 nm.

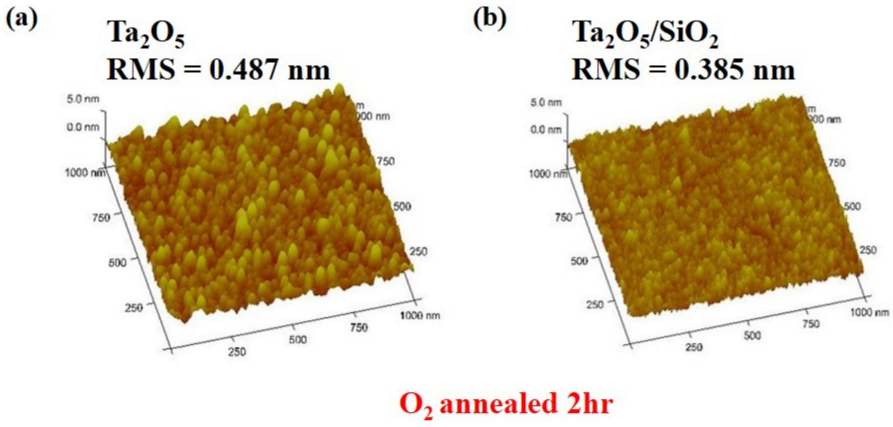

Figure 3. AFM image of: (**a**) the Ta_2O_5 film and (**b**) the SiO_2/Ta_2O_5 film grown on a Si substrate.

Because the electric field-induced carrier is confined to a narrow region close to the interface between the gate-insulating film and the channel layer, the characteristics of the interface have a significant influence on the TFT characteristics. The surface of a rough gate-insulating film may result in more grain boundaries [36] or in an increased number of trap states [37]; which may cause surface scattering [38] and reduce the mobility of the carrier.

The leakage current densities of the SiO_2 (60 nm), Ta_2O_5 (60 nm), and SiO_2/Ta_2O_5 (30 nm/30 nm) dielectric films are shown in Figure 4. As can be seen, the leakage current density is clearly improved by depositing the SiO_2 thin film before the Ta_2O_5 thin film deposition.

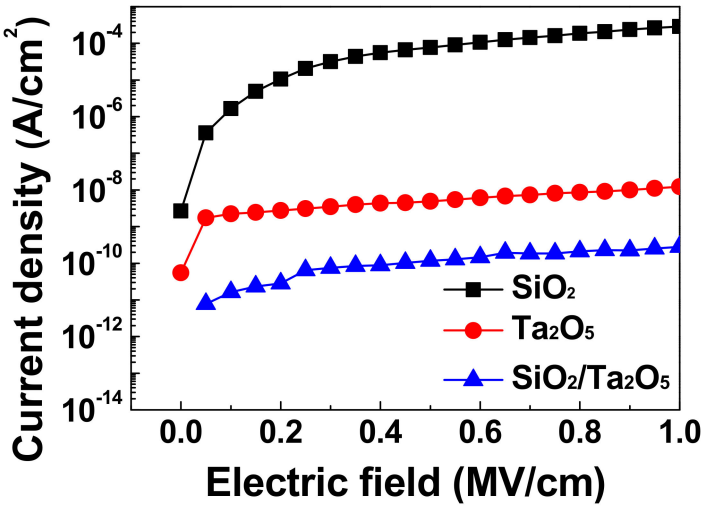

Figure 4. Leakage current densities of the SiO_2 (60 nm), Ta_2O_5 (60 nm), and SiO_2/Ta_2O_5 (30 nm/30 nm) dielectric films.

Figure 5 shows the electrical characteristics before heat treatment of a-IGZO transistor to which the gate insulating film SiO_2 (60 nm), Ta_2O_5 (60 nm), and SiO_2/Ta_2O_5 (30 nm/30 nm) are applied.

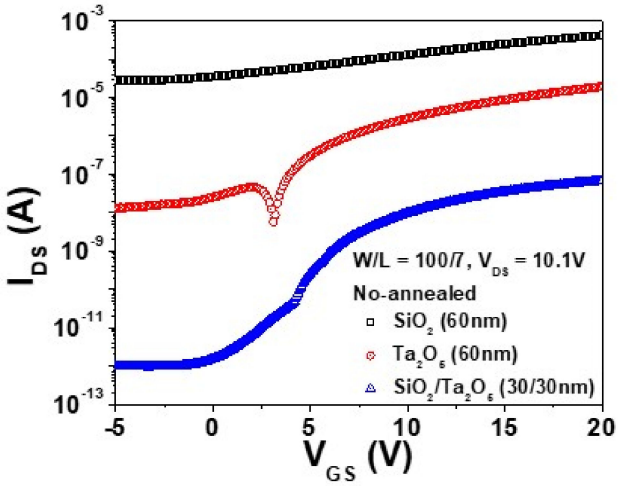

Figure 5. Transfer characteristics of a-IGZO transistors according to the gate insulating (SiO_2 (60 nm), Ta_2O_5 (60 nm), and SiO_2/Ta_2O_5 (30 nm/30 nm)) films. The device is not annealed.

In the case of a SiO_2 (60 nm) and Ta_2O_5 (60 nm) single gate insulating layer, the driving characteristics of the transistor are not exhibited. However, in the case of a device to which a double structure SiO_2/Ta_2O_5 (30 nm/30 nm) is applied, the driving characteristics are visible; but the characteristics are deteriorated.

Figure 6 specifies the electrical characteristics of the Ta_2O_5, SiO_2/Ta_2O_5 TFT, and SiO_2 TFT devices. In the case of Figure 6a,b, compared to the SiO_2 TFT device in (c), the on-current increased; indicating that the mobility was improved. In addition, when the device is turned on, the steep curvature of the SiO_2/Ta_2O_5 TFT appears; which means that the sub-threshold slope is smaller. We believe that this significant improvement in the transfer characteristics is because of the reduction in the density of the tail states below the conduction band in a-IGZO or the increased mobility in a-IGZO.

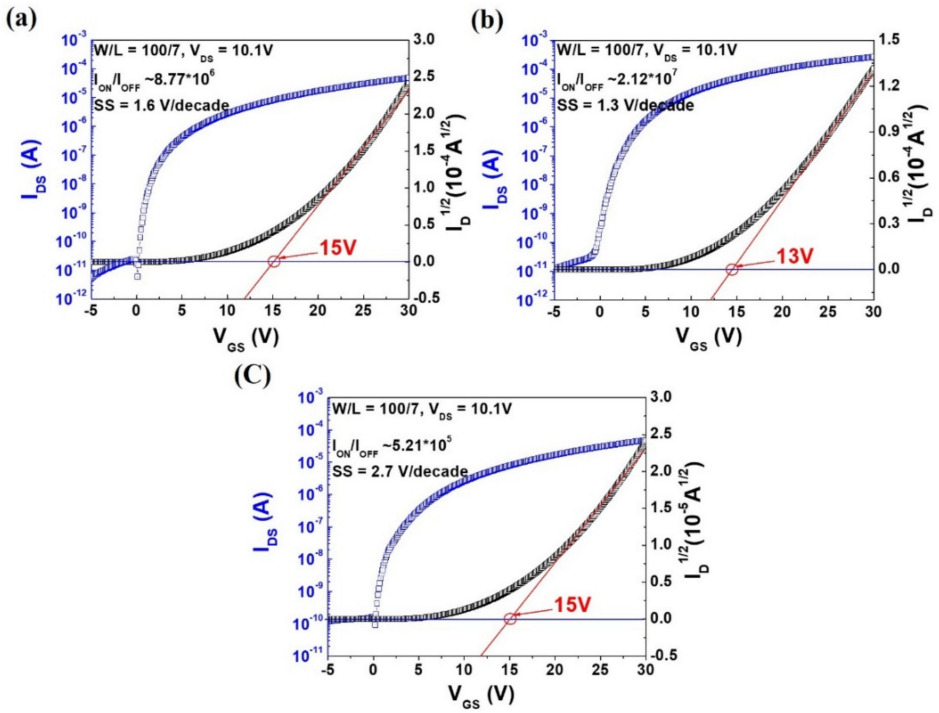

Figure 6. Transfer curves of the (**a**) Ta_2O_5 (60 nm), (**b**) SiO_2/Ta_2O_5 (30 nm/30 nm), and (**c**) SiO_2/a-IGZO TFTs. Heat treatment was carried out for 2 h in an oxygen atmosphere at 300 °C.

We confirmed that post heat treatment had a significant effect on the improvement of the transfer properties of IGZO TFTs. In the a-IGZO thin film transistor, problems such as defects in the thin film and contact resistance between metal channels must be solved. In particular, since carrier movement in semiconductor materials greatly affects device performance, removal of defects through additional heat treatment is essential in oxide semiconductor devices [12]. In addition, the electrical contact between the channel and the source/drain in transistor fabrication is also an important factor in determining the electrical performance of the device [13]. It is possible to significantly reduce the switching speed of the transistor device. In order to improve this phenomenon, an additional heat treatment process is required.

The channel mobility and threshold voltage were calculated by linearly fitting the square root of the drain to source current (I_D) vs. gate voltage (V_G) curve of the transistor operating in the saturation region.

The expression for the operation of a field-effect transistor in the saturation region is as follows:

$$I_D = \left(\frac{C_i \mu_{sat} W}{2L}\right)(V_G - V_{th})^2 \quad for \quad V_D > V_G - V_{th} \tag{1}$$

where W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate insulator, and V_{th} is the threshold voltage of the TFT.

The sub-threshold slope (SS) can be determined from Ids–Vgs curves through Equation (2):

$$SS = \frac{\partial V_{gs}}{\partial (log I_{ds})} I_{max} \quad for \quad V_D > V_G - V_{th} \tag{2}$$

Table 1 shows a comparison of the characteristics of Ta_2O_5, SiO_2/Ta_2O_5, and SiO_2 TFT devices. The mobility of the SiO_2/Ta_2O_5 TFT device is 11.3 $cm^2/V{\cdot}s$ and that of the SiO_2 TFT is only 0.6 $cm^2/V{\cdot}s$; in addition, the mobility is increased by almost 19 times. The on–off current ratio of the SiO_2 TFT device was 10^5; however, the on–off current ratio of the SiO_2/Ta_2O_5 TFT device was 10^7, which increased more than 10 times. Moreover, the SS value of the SiO_2 TFT device was 2.7 V/dec; however, in the case of the SiO_2/Ta_2O_5 TFT device, it dropped to 1.6 V/dec. The reduction in SS value means a faster switching speed and greater gate control capability of the SiO_2/Ta_2O_5 TFT device. Of course, the Ta_2O_5 TFT device also has superior characteristics compared to the SiO_2 TFT device.

Table 1. Transistor parameters of the Ta_2O_5/a-IGZO and Ta_2O_5/SiO_2/a-IGZO TFTs.

Gate Insulator	On/Off Ratio	SS (V/Decade)	μ_{sat} (cm^2/Vs)
Ta_2O_5	8.77×10^6	1.6	8.4
SiO_2/Ta_2O_5	2.12×10^7	1.3	11.3
SiO_2	5.21×10^5	2.7	0.6

4. Conclusions

In this study, we investigated SiO_2 and Ta_2O_5 with a single structure and SiO_2/Ta_2O_5 with a double structure for the gate insulating film to improve transistor performance. In TFTs with a dual structure SiO_2/Ta_2O_5, characteristics such as an on/off ratio, subthreshold swing (SS), and saturation mobility (μ_{sat}) are significantly improved compared to a single structure SiO_2 and Ta_2O_5. By applying the double-structured gate insulating film, the surface roughness was reduced to 0.385 nm through interface control of the formed thin film. In addition, TFT driving characteristics, such as the on/off ratio, SS, and μ_{sat}, were greatly improved to 2.12×10^7, 1.3 V/dec, and 11.3 cm^2/Vs, respectively. The improvement mechanism was reduced charge trapping density through improved surface roughness and interfacial control. Moreover, through the post heat treatment process, the contact resistance between the channel layer and the source/drain electrodes was improved. In this study, we developed a thin film high dielectric constant gate insulating film necessary for

the development of a low-temperature process oxide TFT applicable to flexible substrates. The double-structured high-k gate insulating film is a promising tool that can be applied to next-generation flexible transistors.

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Conflicts of Interest: The authors declare no conflict of interest.

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