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A Modified Step-Up Converter with Small Signal Analysis-Based Controller for Renewable Resource Applications

Davood Ghaderi [1,*], Pandav Kiran Maroti [2], P. Sanjeevikumar [2,*], Jens Bo Holm-Nielsen [2], Eklas Hossain [3] and Anand Nayyar [4]

1 Electrical and Electronics Engineering Department, Bursa Technical University, 16310 Bursa, Turkey
2 Center for Bioenergy and Green Engineering, Department of Energy Technology, Aalborg University, 6700 Esbjerg, Denmark; kiranpandav88@yahoo.co.in (P.K.M.); jhn@et.aau.dk (J.B.H.-N.)
3 Oregon Renewable Energy Center (OREC), Department of Electrical Engineering and Renewable Energy, Oregon Tech, Klamath Falls, OR 97601, USA; eklas.hossain@oit.edu
4 Graduate School, Duy Tan University, 254 Nguyen Van Linh, Danang 550000, Vietnam; anandnayyar@duytan.edu.vn
* Correspondence: davood.ghaderi@btu.edu.tr (D.G.); san@et.aau.dk (P.S.)

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Abstract: Solar energy is one of the most important renewable sources due to its advantages such as simple structure, convenient installation, diverse applications, and low maintenance costs. Low power generation is the main concern with solar panels, so the maximum transmission of this power is a prime priority. The design of boost converters with the ability to generate high voltage gain, efficient structure, and stable and low-cost control circuits is the first step after installing these panels. This study presents a simple and high-gain design of a step-up converter, which uses only one power switch. The significance of this issue is when it will be apparent to know that each switch needs a separate control circuit and complex systems require more control topologies. In comparison with the conventional converter, the gain of the proposed converter, with the use of two additional diodes, a capacitor, and an inductor, was five times greater than the gain of a classical converter with 80% of the duty cycle. The proposed converter can solve the narrow turn-off period problem for the power semiconductor components in order to achieve higher DC voltages that are possible at higher duty cycles in classical converters. Small signal analysis of the proposed converter is presented and a controller based on steady-space matrixes is presented. The reaction of the proposed controller is considerable since a deep mathematical analysis supports this controller. The principal operations of the proposed converter and the projected controller were analyzed mathematically and verified with the help of MATLAB/SIMULINK. Additionally, hardware implementation of the proposed converter was done on a laboratory-scale around 100 W.

Keywords: step-up converter; renewable energy sources; high voltage gain converter

1. Introduction

The optimal use of diverse renewable energy sources is one of the main challenges in terms of power and energy. In order to connect renewable energy sources (RESs) to the network, the use of electronic power interfaces is essential. Solar cell systems are one of the most desirable renewable energy sources due to the availability of solar radiation and flexibility in installing panels. It is preferable to use modular photovoltaic systems to increase the efficiency of these panels and to overcome problems such as shadowing on panels and mismatches between them [1,2]. In these systems, a high-efficiency DC–DC converter is used to increase the output voltage of the photovoltaic cells and connect them

into the high-voltage bus [3–6]. Additionally, these batches are used in many applications including emergency electrical systems, fuel cells, server power supplies, and high-intensity discharge lamps [7].

Boost converters can be divided into isolated and non-isolated categories. Isolated converters can usually present low amounts of efficiency. In these types of choppers, the high voltage gain is obtained through adjustment of the correct transformer ratio. Non-isolated converters are highly applicable structures due to their high efficiency, high power density, and low cost in medium and low power systems [8]. In [9], a three-level boost converter was introduced. This converter can reduce the voltage stress of semiconductor components when compared to a conventional boost converter, which is suitable for high voltage applications. As a result, switching losses and electromagnetic interference (EMI) are improved due to low voltage stress in this configuration. Nevertheless, semiconductor parts act under hard switching conditions and the problem of recovering the output diode is one of the most serious problems in this type of converter.

In [10,11], a highly addictive coupled-inductor single-switch converter was introduced. In [10], the leakage energy of the coupled-inductors was reclaimed by the clamp circuit, which reduces the voltage stress on the switch and diodes. As a result, the switch can be used with a low light-up time resistance, which results in improved efficiency. However, it should be noted that this converter has a complex structure. In [12], an interleaved based configuration by coupled-inductors was introduced. Due to the use of a voltage multiplier and coupled-inductors, a high voltage gain was achieved for the proposed structure. In this converter, due to the use of cross-linked inductors, the input current ripple decreased. Additionally, by using active clamping circuits, the leakage energy of the inductor's spools and soft-switching conditions were created for the main switches. One of the disadvantages of topologies by coupled-inductor is the high voltage stresses on output diodes that make use of high voltage diode applications and clamper structures. In [13], a high-gain nonsymmetrical interleaved converter was presented. In this structure, two ferrite cores were used for two inductors. Due to the use of two switches, in addition to reducing the current stress of the switches, the ripple of the input current will be limited. One of the disadvantages of this converter is the creation of hard switching conditions, which increases the number of magnetic elements and the total volume of the circuit.

In [14], a boost converter integrated with a fly-back topology was introduced to obtain the high voltage gain. In this structure, the boost converter acts like a passive clamp circuit and recycles the leakage energy. In [15], a similar boost converter was introduced. In this converter, the clamper capacitor is located in the direction of charging the output capacitor, and in addition to absorbing the self-leakage energy, it also increases the voltage gain of the converter. To reduce the number of components, single switch fly-back boost converters are commonly integrated. Different designs of this converter are presented in [16]. One of the main concerns is the voltage and current spikes on the switching devices in a power module. Zero voltage switching (ZVS), zero current switching (ZCS), zero voltage transition (ZVT), and zero current transition (ZCT) are different approaches that can reduce these stresses and decrease the switching losses on power diodes and power switches [17,18]. In these ways, to obtain higher efficiency, applying an additional switch is often inevitable and can need more control topologies and enhance the complexity and cost of the converter.

Cascade structures can be employed for high step-up requirements. The authors in [19,20] proposed sample topologies for this kind of converter. Higher DC gains can be achieved by applying more serial blocks of converters, but by increasing the number of blocks, the number of components will increase, especially extra power switches that have been applied, and the dynamic and frequency losses will increase, which will seriously affect the efficiency. Furthermore, the control process will be difficult for more power switches and the total cost will increase. Our study introduces a topology that can provide a pre-amplifier block containing an inductor, two power diodes, and a capacitor. This configuration can increase the input voltage, and according to the duty ratio, this amount can be greater. Next, it acts as a boost converter and increases the voltage to higher values. For high efficiency purposes, the diodes on the pre-amplifier part act in a complementary manner and when one of them is in ON mode, another is in OFF mode and vice versa. So, in comparison with a classical

cascaded boost converter, the proposed configuration is more efficient. All mathematical analysis of the projected converter, calculations of the voltage gain, and the controller design and small signal analysis based on steady space matrixes are presented in Section 2. Section 3 presents the simulation results and the implemented prototype and the performance assessment of the proposed simple controller is presented in Section 4.

2. Modified Boost Converter (MBC)

Figure 1a–c shows the conventional, cascaded, and proposed boost converters, respectively. As can be seen in Figure 1c, a boosting structure is located between the entrance inductor and the power switch. Based on switch ON or OFF working modes, only one of the D_1 and D_2 diodes will be active in the structure and in this way, it makes a preamplifier layer for boosting purposes. All working principles and mathematical analyses have been stipulated for both ON and OFF states of the power switch.

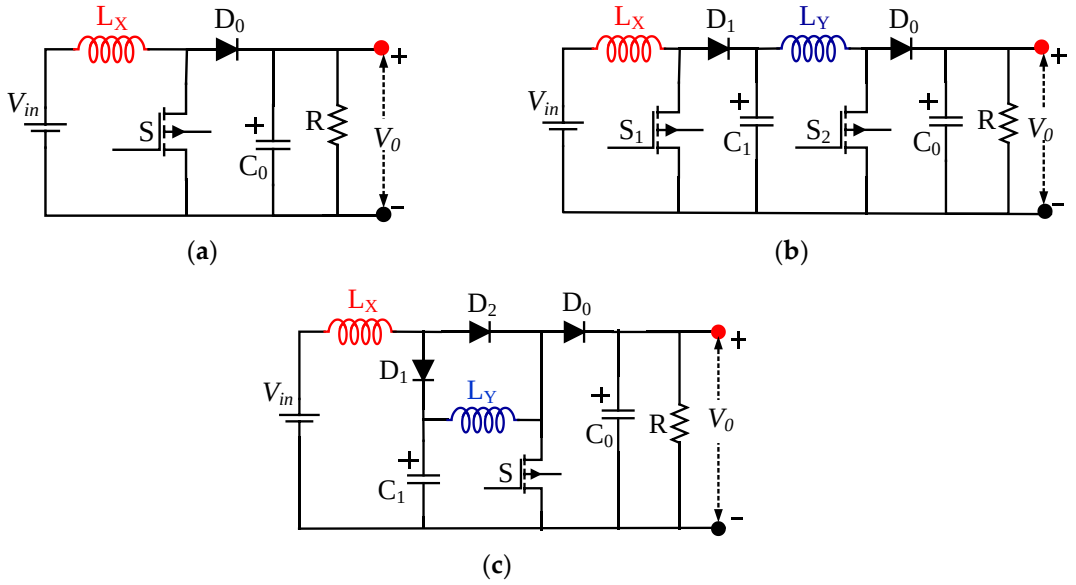


Figure 1. (**a**) Conventional; (**b**) cascaded; and (**c**) modified boost structures.

Figure 2 presents the Pulse Width Modulation (PWM) wave applied to the power switch in the boost converter. In this figure for the [0, t_1] and [t_1, T_S] time intervals switch S_1 is in ON and OFF modes, respectively. So, if we consider [0, t_1] interval as DT_S, the [t_1, T_S] interval will be (1-D) T_S. In other words, D is the duty cycle of power switch S_1.

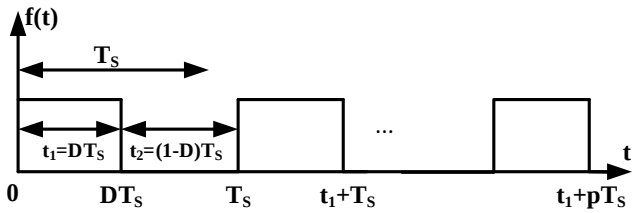


Figure 2. Pulse width modulation (PWM), which is applied to the power switch. Per period (T) contains two (0, t_1) and (t_1, T) intervals.

2.1. Converter Analysis

This part presents the converter's reactions for the ON and OFF time intervals.

2.1.1. Mode-I

For a time-interval that the power switch receives the pulse and is in the short circuit state, both L_X and L_Y are magnetizing. This is done by inputting the voltage through diode D_2 and the power switch for L_X and from C_1 and switch for L_Y. As can be seen in this mode, D_1 is in mode-I. Based on this statement, currents of inductors are rising in the ON state. As predicted, the voltage value on capacitor C_1 is discharging on L_Y through the power switch and decreases. Additionally, the voltage on the output capacitor is discharging on the output load in this mode. The current value of diode D_1 is zero and because of the conducting condition for diode D_2, its current will increase. Figure 3a shows the ON state of the power switch in the projected structure and Figure 3b illustrates the simplified form of Figure 3a.

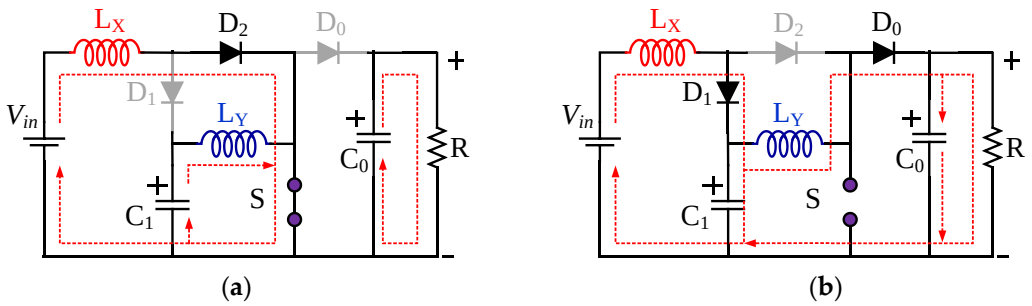


Figure 3. State of the proposed structure (**a**) when the power switch is ON and (**b**) when the power switch is OFF.

Based on these situations, the current waveform passing through inductor L_X can be written as below:

$$L_X \frac{di_{LX}}{dt} = V_{in} \Rightarrow \frac{di_{LX}}{dt} = \frac{V_{in}}{L_X} \tag{1}$$

The current of inductor L_Y is:

$$L_Y \frac{di_{LY}}{dt} = v_{C1} \Rightarrow \frac{di_{LY}}{dt} = \frac{v_{C1}}{L_Y} \tag{2}$$

The voltage waveform for capacitor C_1 can be gained as:

$$C_1 \frac{dv_{C1}}{dt} = -i_{LY} \Rightarrow \frac{dv_{C1}}{dt} = -\frac{i_{LY}}{C_1} \tag{3}$$

Finally, we can find the voltage for the output capacitor as Equation (4):

$$C_2 \frac{dv_0}{dt} = -\frac{v_o}{R} \Rightarrow \frac{dv_o}{dt} = -\frac{v_o}{C_2 R} \tag{4}$$

The steady-space matrix of the ON state for the proposed converter can be obtained by Equation (5)

$$\left\{ \begin{array}{l} L_X \frac{di_{LX}}{dt} = V_{in}(d) \Rightarrow \frac{di_{LX}}{dt} = \frac{V_{in}}{L_X}(d) \\ L_Y \frac{di_{LY}}{dt} = v_{C1}(d) \Rightarrow \frac{di_{LY}}{dt} = \frac{v_{C1}}{L_Y}(d) \\ C_1 \frac{dv_{C1}}{dt} = -i_{LY}(d) \Rightarrow \frac{dv_{C1}}{dt} = \frac{-i_{LY}}{C_1}(d) \\ C_2 \frac{dv_o}{dt} = -\frac{v_o}{R}(d) \Rightarrow \frac{dv_o}{dt} = -\frac{v_o}{RC_2}(d) \end{array} \right\} \Rightarrow \begin{bmatrix} \dot{i}_{LX} \\ \dot{i}_{LY} \\ \dot{v}_{C1} \\ \dot{v}_{01} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_Y} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{LX} \\ i_{LY} \\ v_{C1} \\ v_{01} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_X} \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}] \tag{5}$$

2.1.2. Mode-II

In this time interval, L_X is demagnetizing on capacitor C_1 through D_1 and D_2 is in OFF mode. Additionally, inductor L_Y is demagnetizing through diode D_0 on the output capacitor and load. In this

time interval, as above-mentioned, the voltage values on capacitors C_1 and C_2 will increase through L_X and L_Y, respectively. Figure 4 illustrates all of the components' conductions in both ON and OFF modes of power Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Small signal analysis for this state was also analyzed and written below. Inductor L_X can be calculated as:

$$L_X \frac{di_{LX}}{dt} = (V_{in} - V_{C1})(1-d) \Rightarrow \frac{di_{LX}}{dt} = \frac{V_{in} - V_{C1}}{L_X}(1-d) \tag{6}$$

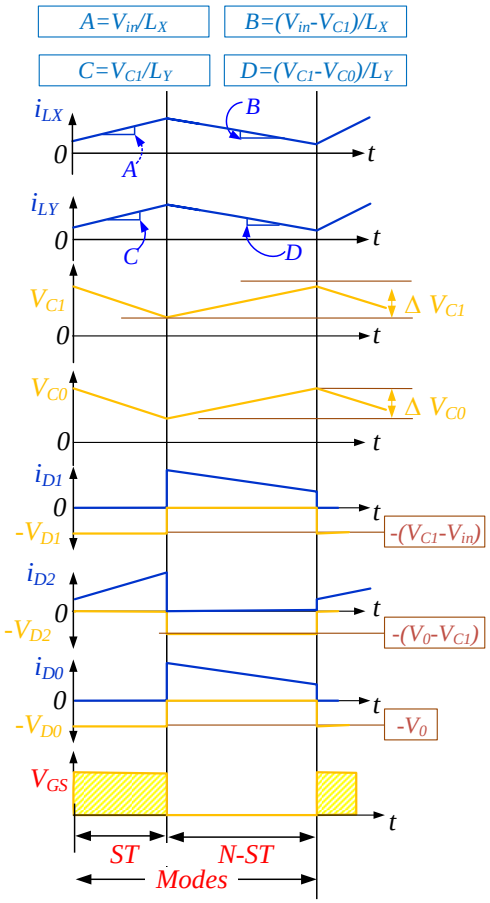


Figure 4. Mode of operation of the proposed structure.

Additionally, the current waveform of inductor L_Y is equal with:

$$L_Y \frac{di_{LY}}{dt} = (V_{C1} - V_0)(1-d) \Rightarrow \frac{di_{LY}}{dt} = \frac{V_{C1} - V_0}{L_Y}(1-d) \tag{7}$$

The voltage waveform for capacitor C_1 and C_0 are:

$$C_1 \frac{dv_{C1}}{dt} = (i_{LX} - i_{LY})(1-d) \Rightarrow \frac{dv_{C1}}{dt} = \frac{i_{LX} - i_{LY}}{C_1}(1-d) \tag{8}$$

$$C_0 \frac{dv_0}{dt} = (i_{LY} - \frac{V_0}{R})(1-d) \Rightarrow \frac{dv_0}{dt} = \frac{i_{LY} - \frac{V_0}{R}}{C_0}(1-d) \tag{9}$$

Term (1 − d) in the above equations guarantees work in the OFF state. Through the same method, we can obtain the below matrix for the OFF state of the power switch:

$$\left.\begin{array}{l} L_X\frac{di_{LX}}{dt} = (V_{in} - V_{C1})(1-d) \Rightarrow \frac{di_{LX}}{dt} = \frac{V_{in}-V_{C1}}{L_X}(1-d) \\ L_Y\frac{di_{LY}}{dt} = (V_{C1} - V_0)(1-d) \Rightarrow \frac{di_{LY}}{dt} = \frac{V_{C1}-V_0}{L_Y}(1-d) \\ C_1\frac{dv_{C1}}{dt} = (i_{LX} - i_{LY})(1-d) \Rightarrow \frac{dv_{C1}}{dt} = \frac{i_{LX}-i_{LY}}{C_1}(1-d) \\ C_2\frac{dv_0}{dt} = (i_{LY} - \frac{V_0}{R})(1-d) \Rightarrow \frac{dv_0}{dt} = \frac{i_{LY}-\frac{V_0}{R}}{C_2}(1-d) \end{array}\right\} \Rightarrow \begin{bmatrix} \dot{i}_{LX} \\ \dot{i}_{LY} \\ \dot{V}_{C1} \\ \dot{V}_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_X} & 0 \\ 0 & 0 & \frac{1}{L_Y} & -\frac{1}{L_Y} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{LX} \\ i_{LY} \\ V_{C1} \\ V_0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_X} \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}] \quad (10)$$

So, for both ON and OFF states of the switch, by adding Equations (5) and (10), we have:

$$\left.\begin{array}{l} \frac{di_{LX}}{dt} = -\frac{(1-d)}{L_1}V_{C1} + \frac{1}{L_X}V_{in} \\ \frac{di_{LY}}{dt} = \frac{1}{L_Y}V_{C1} - \frac{(1-d)}{L_Y}V_0 \\ \frac{dV_{C1}}{dt} = \frac{(1-d)}{C_1}i_{LX} - \frac{1}{C_1}i_{LY} \\ \frac{dV_0}{dt} = \frac{(1-d)}{C_2}i_{LY} - \frac{1}{RC_2}V_0 \end{array}\right\} \Rightarrow \begin{bmatrix} \dot{i}_{LX} \\ \dot{i}_{LY} \\ \dot{V}_{C1} \\ \dot{V}_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1-d}{L_X} & 0 \\ 0 & 0 & \frac{1}{L_Y} & -\frac{1-d}{L_Y} \\ \frac{1-d}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1-d}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{LX} \\ i_{LY} \\ V_{C1} \\ V_0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_X} \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}] \quad (11)$$

For the modeling process of a power circuit by the steady space method, we can find the relation between inputs, outputs, and the current and voltage derivations for the inductors and capacitors by Equation (12):

$$Y = CX + Du \quad (12)$$

where X is the inductor current or capacitor voltage derivate matrix and C is the coefficient matrix; u is the input sources matrix; and D is the coefficient matrix of u. While Y as the output wave, can be obtained as:

$$Y = V_0 = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{LX} \\ i_{LY} \\ V_{C1} \\ V_0 \end{bmatrix} \quad (13)$$

The general view in order to obtain the small signal for the proposed converter can be re-the organized by Equation (14), since A, B, C, and D can be introduced for the ON and OFF states of power switch:

$$\begin{array}{l} \hat{\dot{X}} = A\hat{X} + B\hat{u} + [(A_1 - A_2)X + (B_1 - B_2)u]\hat{d}; \\ \left\{\begin{array}{l} A = A_1 d + A_2(1-d) \\ B = B_1 d + B_2(1-d) \\ C = C_1 d + C_2(1-d) \\ D = D_1 d + D_2(1-d) \end{array}\right. \end{array} \quad (14)$$

If we want to introduce the general equation for both ON and OFF states of the power switch through Equation (14), we can obtain:

$$\begin{bmatrix} \hat{\dot{i}}_{LX} \\ \hat{\dot{i}}_{LY} \\ \hat{\dot{V}}_{C1} \\ \hat{\dot{V}}_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1-d}{L_X} & 0 \\ 0 & 0 & \frac{1}{L_Y} & -\frac{1-d}{L_Y} \\ \frac{1-d}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1-d}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} \hat{i}_{LX} \\ \hat{i}_{LY} \\ \hat{V}_{C1} \\ \hat{V}_0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_X} \\ 0 \\ 0 \\ 0 \end{bmatrix} \left[\hat{V}_{in}\right] + \begin{bmatrix} \frac{V_{C1}}{L_X} \\ \frac{V_0}{L_Y} \\ \frac{I_{LX}}{C_1} \\ \frac{I_{LY}}{C_2} \end{bmatrix} \hat{d} \quad (15)$$

So, in this condition, the output voltage of the structure can be gained by Equation (16):

$$Y = \hat{V_0} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i_{LX}} \\ \hat{i_{LY}} \\ \hat{V_{C1}} \\ \hat{V_0} \end{bmatrix} \tag{16}$$

The voltage gain of the converter can be found through Equation (17):

$$\frac{V_0}{V_{in}} = -\frac{\frac{(1-d)^2}{C_1C_0L_XL_Y}}{S^4 + S^3\left(\frac{1}{RC_2}\right) + S^2\left(\frac{(1-d)^2(C_1L_X+C_0L_Y)+L_XC_0}{C_1C_0L_XL_Y}\right) + S\left(\frac{L_Y(1-d)^2+L_X}{C_1C_0L_XL_Y}\right) + \frac{(1-d)^4}{C_1C_0L_XL_Y}} \tag{17}$$

2.2. Design of Closed-Loop Controller

By considering that the output voltage of a boost converter should be kept constant by the load or input voltage changes, the key point for controller design is finding an equation between the output voltage and one of the inductor currents or capacitor voltage derivatives and it can be obtained from Equation (9):

$$C_0\frac{dV_0}{dt} + \frac{1}{R}V_0 = (1-d)i_{LY} = u;\ C_2SV_0 + \frac{1}{R}V_0 = V_0\left(C_0S + \frac{1}{R}\right) = (1-d)i_{LY} = u \tag{18}$$

Other obtained equations cannot present a direct mathematical relation for the output voltage and Equation (9) is more suitable. Here, the final destination is generating a PWM signal for the power switch that will change according to these amendments to guarantee a fixed output voltage. In Equation (18), u is the PI controller output signal and d is the duty cycle of PWM, which will be implemented to power MOSFET. Equation (18) can be rewritten in a simpler way as:

$$d = 1 - \frac{u}{i_{LY}} \tag{19}$$

Figure 5 illustrates the closed-loop form of the PI controller based on Equation (18). Since the goal is receiving a fixed DC voltage at the endpoints of the converter on the load side, a sampling of this voltage was done and compared with a reference voltage in order to be applicable by a microcontroller. Therefore, the sampled voltage should be at a comparable level of the reference voltage. For example, for a 120 V as the fixed output voltage, if the reference voltage chosen is 4 V, the sampled voltage should be decreased through high resistors and be equal to 4 V. For other amounts of the output voltage above or under the 120 V, this sampled voltage will change between 3 to 5 V to be comparable with the reference voltage. After passing through the controller, the control signal u will be compared with the current of the second inductor i_{LY}, and as Equation (19) shows, the desired duty cycle is supplied for the power switch. Figure 6 presents the controller structure for the proposed converter.

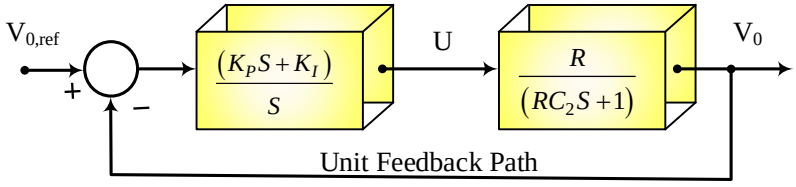


Figure 5. Closed-loop form of the Proportional-Integral (PI) controlled cascade boost structure.

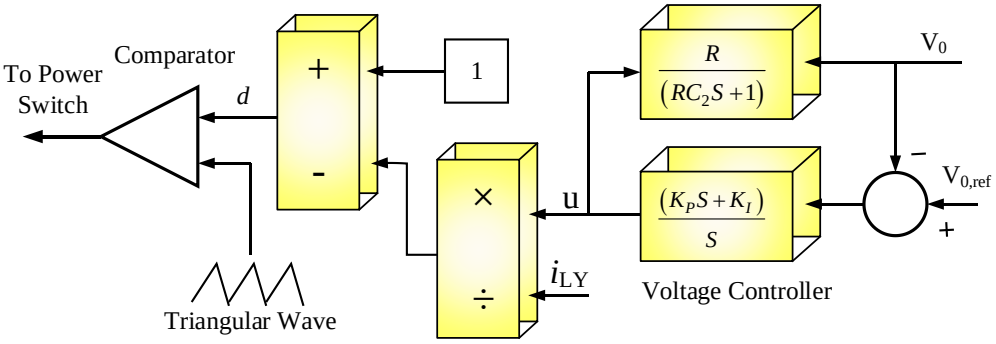


Figure 6. Voltage comparison, PI control, and PWM modulator blocks.

The general form of a PI controller comes from:

$$G(s) = k_p + \frac{k_i}{s} = \frac{k_p s + k_i}{s} \quad or \quad G(j\omega) = k_p + \frac{k_i}{j\omega} \tag{20}$$

where K_P and K_I are the proportional and integral gains of the PI controller. We can put Equation (20) in a feedback loop by a PI controller as presented in Figures 5 and 6 by considering Equation (19). The transfer function of closed-loop form of this feedback is equal with:

$$G_F = \frac{G_o}{1+G_o} = \frac{\frac{1}{C_2}\left(k_p + k_i\right)}{s^2 + \left(\frac{1+Rk_p}{RC_2}\right) + \frac{k_i}{C_2}} \Rightarrow G_F = \frac{\frac{1}{C_2}\left(k_p s + k_i\right)}{s^2 + 2\xi\omega_0 s + \omega_0^2} \tag{21}$$

K_P and K_I are the proportional and integral coefficients of the PI controller. It is easy to gain:

$$\begin{cases} \frac{1+Rk_p}{RC_2} = 2\xi\omega_0 \\ \frac{k_i}{C_2} = \omega_0^2 \end{cases} \Rightarrow \begin{cases} k_p = 2\xi\omega_0 C_2 - \frac{1}{R} \\ k_i = \omega_0^2 C_2 \end{cases} \tag{22}$$

The representation of the frequency domain in the kp and ki plane can be introduced by:

$$\begin{bmatrix} X_{Rp} & X_{Ri} \\ X_{Ip} & X_{Ii} \end{bmatrix} = \begin{bmatrix} k_p \\ k_i \end{bmatrix} = \begin{bmatrix} 0 \\ -\omega_0 \end{bmatrix} \tag{23}$$

By solving this equation for $\omega \neq 0$;

$$\begin{aligned} K_p(\omega, \theta_A, \xi) &= \frac{-Re(\omega) - \frac{1}{\xi}(A_A cos\theta_A - B_A sin\theta_A)}{X(\omega)} \\ K_I(\omega, \theta_A, \xi) &= \frac{\omega(Im(\omega) + \frac{1}{\xi}(A_A sin\theta_A + B_A cos\theta_A))}{X(\omega)} \end{aligned} \tag{24}$$

$$X(\omega) = \begin{pmatrix} \left|G_p(j\omega)\right|^2 + \frac{1}{\xi^2}\left|W_A(j\omega)\right|^2 + \frac{2}{\xi}(\mathrm{Re}(\omega)(A_A cos\theta_A - B_A sin\theta_A) \\ +Im(\omega)(A_A sin\theta_A + B_A cos\theta_A)) \end{pmatrix} \tag{25}$$

For $\omega 0 = 0$, Equation (24) will result in:

$$\begin{bmatrix} 0 & X_{Ri}(0) \\ 0 & X_{Ii}(0) \end{bmatrix} = \begin{bmatrix} k_p \\ k_i \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{26}$$

For this equation, it can be found that K_P is an arbitrary factor while K_I (0,θA,ξ) = 0, unless $X_{Ri(0)}$ = $X_{Ii(0)}$ = 0, which can be possible only under $\xi \to \infty$ and Rp(0) = Ip(0) = 0 conditions, which holds by a zero for Gp(S) at the origin. Therefore, damping factor ξ was selected as 0.707, which can present a

good response for the second order circuits [21]. Since ω_0 is a pulsation, it was chosen as less than the switching frequency ωs to get an appropriate response. Based on [21], this factor can be introduced as Equation (28):

$$\frac{f_{PWM}}{5\xi} \leq \omega n \leq \frac{f_{PWM}}{2\xi} \quad (27)$$

By decreasing the ω_n value, the bandwidth of the control system will reduce and will give the increased dither amplitude attenuation and longer set-up times, enhancing the ω_n value above the presented band, and resulting in the poor matching of the linearized model's response to the actual system. This is due to the effect of sampling on the frequency response of the system. In our calculations, the pulsation frequency was fixed to 230.63 rad/s with the consideration of the calculated K_p and K_I values based on Equation (22), and the switching frequency was adjusted to 50 kHz, so $\omega_s = 2\pi f_S$ is equal to 314 K rad/s.

2.3. Comparison of the Conventional Cascaded and Proposed Converters

The main purpose of this section was a comparison between the inductor currents and capacitor voltage ripples for a classical cascade and our proposed converters. Table 1 summarizes these equations. In this table, V_{C1} and V_{C0} are the steady state voltages of the C_1 and C_2 capacitors; D_1 and D_2 are the duty cycles of PWM signals for S_1 and S_2 power MOSFETs of the conventional cascaded boost converter; D is the duty cycle for the proposed converter's switch, respectively; T_S is the switching frequency; and Δi_{LX} and Δi_{LY} are the current ripples for the inductors L_X and L_Y, respectively. Additionally, I_0 is the output current and V_{in} is the input voltage of the structures.

Table 1. Capacitor voltage and inductor current ripples for both converters.

Classical Cascaded Converter	
First Block	**Second Block**
$\Delta i_{LX} = \frac{V_{in}}{L_X} D_1 T_s$	$\Delta i_{LY} = \frac{V_{C0} - V_{C1}}{L_Y}(1 - D_2)T_s$
$\Delta V_{C1} = \frac{I_{LY}}{C_1} D_1 T_s$	$\Delta V_{C0} = I_o D_2 T_s$
Proposed Converter	
$\Delta i_{LX} = \frac{V_{in}}{L_X} D T_s$	$\Delta i_{LY} = \frac{(V_{C0} - V_{C1}) - V_{in}}{L_Y}(1 - D)T_s$
$\Delta V_{C1} = \frac{I_{LX}}{C_1} D T_s$	$\Delta V_{C0} = I_o D T_s$

By considering the same duty cycle for all switches, the current ripples for inductors were the same for both configurations, while the proposed converter uses only one power switch and has a simpler structure and needs to simple with a one controller topology to guarantee a fixed output voltage at the output of the converter. Part of simulations is presented in Section 3, and can show the first inductor currents, output diode currents, power switch currents, and the average values of these converters. All results can easily confirm the equations presented in Table 1.

Table 2 illustrates all of the component conduction and switching losses for both conventional, cascaded, and proposed power boost converters comprehensively. This table was written according to [22]. In this table, the P_{con} and P_{sw} are the conductive and switching losses, respectively. For example, $P_{con,D1}$ is the conductive losses of the power diode D_1 and $P_{sw,D2}$ is the switching losses for the diode D_2. P_{LX} and P_{LY} are the conductive losses on inductors. Additionally, V_f is the forward voltage on diodes; f_S is the frequency switching value; and Q_{rr1}, Q_{rr2}, and Q_{rr3} are the electrical charges of the D_1, D_2, and D_0 diode forward capacitors. T_{ON} and T_{OFF} are presenting the transition times for the power switches for the ON and OFF states, respectively. The dissipated energy for the turn ON and OFF

momentary times are presented by W_{ON} and W_{OFF}. D' presents the time that the power switch is in OFF mode.

Table 2. Equations for both converters operating in continuous conduction mode (CCM).

Conventional Cascade Converter	Proposed Converter
$I_{LX} = \frac{1}{(1-d_1)\times(1-d_2)} \times \frac{V_0}{R}$	$I_{LX} = \frac{1}{(1-d)^2} \times \frac{V_o}{R}$
$I_{LX} = \frac{1}{(1-d_2)} \times \frac{V_0}{R}$	$I_{L2} = \frac{1}{(1-d)} * \frac{V_o}{R}$
$P_{LX} = R_{LX}\left(i_{LX}^2 + \frac{\Delta i_{LX}^2}{12}\right)$	$P_{LX} = R_{LX}\left(i_{LX}^2 + \frac{\Delta i_{LX}^2}{12}\right)$
$P_{LY} = R_{LY}\left(i_{LY}^2 + \frac{\Delta i_{LY}^2}{12}\right)$	$P_{LY} = R_{LY}\left(i_{LY}^2 + \frac{\Delta i_{LY}^2}{12}\right)$
$P_{conD1} = V_{f1}I_{LX}D_1' + R_{onD1}D_1'\left(I_{LX}^2 + \frac{\Delta i_{LX}^2}{12}\right)$	$P_{conD1} = V_{f1}(I_{LX}+I_{LY})D_1' + R_{onD1}D_1'\left((I_{LX}+I_{LY})^2 + \frac{\Delta i_{LX}^2}{12}\right)$
$P_{conD2} = V_{f2}I_{L2}D_2' + R_{onD2}D_2'\left(I_{L2}^2 + \frac{\Delta i_{L2}^2}{12}\right)$	$P_{conD2} = V_{f2}(I_{L1}+I_{L2})D_2' + R_{onD2}D_2'\left((I_{L1}+I_{L2})^2 + \frac{\Delta i_{L1}^2}{12}\right)$
$P_{conD0} = 0$	$P_{conD0} = V_{f3}(I_{LX}+I_{LY})D_2' + R_{onD3}D_2'\left((I_{LX}+I_{LY})^2 + \frac{\Delta i_{LX}^2}{12}\right)$
$P_{conM1} = R_{dsM1}D_1\left(I_{LX}^2 + \frac{\Delta i_{LX}^2}{12}\right)$	$P_{conM} = R_{dsM}D\left(I_{LX}^2 + \frac{\Delta i_{LX}^2}{12}\right)$
$P_{conM2} = R_{dsM2}D_1\left(I_{LY}^2 + \frac{\Delta i_{LY}^2}{12}\right)$	$P_{conM2} = 0$
$P_{swD1} = V_{c1}Q_{rr1}f_s$	$P_{swD1} = V_{c1}Q_{rr1}f_s$
$P_{swD2} = V_{c2}Q_{rr2}f_s$	$P_{swD2} = V_{c2}Q_{rr2}f_s$
$P_{swD0} = 0$	$P_{swD0} = V_{c3}Q_{rr3}f_s$
$P_{swM1} = (W_{ON1} + W_{OFF1})f_s$ $W_{ON1} = 0.5I_{LX}V_{C1}T_{on1}$ $W_{OFF1} = 0.5I_{LX}V_{C1}T_{OFF1}$	$P_{swM1} = (W_{ON1} + W_{OFF1})f_s$ $W_{ON1} = 0.5I_{LX}V_{C1}T_{ON1}$ $W_{OFF1} = 0.5I_{LX}V_{C1}T_{OFF1}$
$P_{swM2} = (W_{ON2} + W_{OFF2})f_s$ $W_{ON2} = 0.5I_{LY}V_{C2}T_{ON2}$ $W_{OFF2} = 0.5I_{LY}V_{C2}T_{OFF2}$	$P_{swM2} = 0$

The main advantage of the proposed converter is that it has only one power switch. Therefore, there are no conductive and switching losses for the second power switch. In addition, it should be considered that it has three power diodes compared with a conventional cascaded converter and the projected converter will have these losses for the third diode. This presents a preferable condition compared with conventional cascaded structures.

2.4. Comparison of the Conventional Cascaded and Proposed Converters

By considering the ideal conditions for all inductors, capacitors, power diodes, and power switches, the voltage gain of the proposed converter can be obtained. Based on the charging and discharging states of inductors, mathematical evaluation for the voltage gain will appear in two different modes.

State 1: Voltage across inductor L_X when the power switch is in ON and OFF modes:

The voltage across inductor L_X will be equal with:

$$V_{in}D + (V_{in} - V_{C1})(1-D) = 0 \Rightarrow V_{C1} = \frac{V_{in}}{1-D} \quad (28)$$

In the above equation, D is for a time interval where the switch is in ON mode and (1-D) is for the OFF state of MOSFET.

State 2: Voltage across inductor L_Y when the power switch is in ON and OFF modes:
The voltage drops can be calculated as Equation (29):

$$V_{C1}D + (V_{C1} - V_0)(1 - D) = 0 \Rightarrow V_0 = \frac{V_{C1}}{1 - D} \tag{29}$$

By replacing Equation (28) into Equation (29), the voltage gain of the proposed structure can be calculated:

$$V_0 = \frac{V_{in}}{(1 - D)^2} \tag{30}$$

Therefore, the voltage gain of the proposed structure can be obtained by Equation (32):

$$G = \frac{V_0}{V_{in}} = \frac{1}{(1 - D)^2} \tag{31}$$

Through a simple calculation, the relation between the input and output current values can be calculated as:

$$I_o = I_{in}(1 - D)^2 \tag{32}$$

For the proposed converter, we can find the values of the inductor currents from the below equations:

$$\left.\begin{array}{l} \Delta i_{LX} = \frac{V_{in}}{L_X} dT \\ I_{LX} = \frac{I_0}{(1-d)^2} \end{array}\right\} \tag{33}$$

$$\left.\begin{array}{l} \Delta i_{LY} = \frac{V_{C1}}{L_Y} dT \\ I_{LY} = \frac{I_0}{(1-d)^2} \end{array}\right\} \tag{34}$$

So, the oscillation of the current for these inductors can be presented by:

$$\xi_1 = \frac{\Delta i_{LX}/2}{I_{LX}} = \frac{d(1-d)^2 T V_{in}}{2 L_X I_o} = \frac{d(1-d)^4}{2} \frac{R}{f L_X} \tag{35}$$

$$\xi_2 = \frac{\Delta i_{LY}/2}{I_{LY}} = \frac{d(1-d) T V_{C1}}{2 L_Y I_o} = \frac{d(1-d)^2}{2} \frac{R}{f L_Y} \tag{36}$$

Additionally, the voltage fluctuation for the output capacitor can be presented by Equation (37):

$$\varepsilon = \frac{\Delta V_0/2}{V_0} = \frac{1-d}{2 R f C_0} \tag{37}$$

For the simulation and experimental analysis, considered one percent for these oscillations, the values of the inductors and capacitors can be calculated.

3. Simulation Results and Discussion

A group of simulations were performed in MATLAB SIMULINK R2017a for the evaluation and testing of the stability of the proposed circuit. The input voltage for the structure was adjusted between 25 and 45 V based on the panel's ability to generate voltage according to different temperature and irradiance values. The output load value was chosen between 50 and 200 ohms for an output power limit of around 288 W. Additionally, 50 kHz was considered as the switching frequency. Simulations were done for the duty cycle from 30% to 90% and the results are presented in this section. Table 3 presents all of the components and parameters that were used in the simulation.

For our tests, we assumed 0.1 Ω for inductors L_X and L_Y as their internal resistance. This value of the internal resistance was tested on a real 200 μH inductor in the laboratory. For that, a fixed 0.5 V

implemented on the inductor and serial ammeter showed around 5 A as the current. Figure 7a presents the I-V and P-V characteristics of the JIYANGYIN HR-200 W type of the PV array that was selected for hardware implementation. The level of the input voltage and power array were in a good domain of the desired issues presented in Table 3. Figure 7b illustrates the final diagram of the proposed converter and controller and as can be seen, a sampling was done based on Equation (9) for the controller design. This diagram is suitable for all kinds of renewable energy sources since these produce limited values of power. The controller loop was drawn based on Equations (18) and (19) and Figures 5 and 6. For the controller, PIC18f877 was selected to do the comparison between the reference and sampled voltages and a triangular wave with a 50 kHz frequency was implemented for duty cycle generation to drive the power switch.

Table 3. Particularization of the projected and conventional boost converters in the simulation and experimental steps.

Parameter	Proposed Structure	Conventional Cascade Structure
Power	288 W	288 W
Input voltage	20–45 V	20–45 V
L_X and L_Y	200 uH	200 uH
ESR of inductors	0.1 Ω	0.1 Ω
C_1	1 uF	47 uF
C_0	47 uF	47 uF
Duty cycle	30–90%	30–90%
Switching frequency	50 kHz	50 kHz

Figure 8 shows the efficiency diagram and was done with a comparison between the conventional cascaded and projected prototypes. The most important reason for the comparable efficiency value for the new converter is its components, especially the power diodes. As mentioned in Section 2.1, in any time interval of PWM, only one diode will be located in the current direction and will charge the inductors or output capacitor. Additionally, this structure has only one power switch and the same inductor and capacitor values when compared with conventional topologies. As expected, both the proposed and cascaded converters can present low efficiency for lower power based on some fixed losses on devices, and for higher values of power, both structures will be more efficient. By considering that in any time interval two diodes will be active for both topologies by the same number of inductors and since the average current of the proposed converter is approximately equal with the total currents of both MOSFETs of the cascaded converter, efficiency values were obtained close to each other. This figure has been presented for a fixed load with a 200 Ω value and different values of input voltages.

A low-pass filter can be a single-tuned or doubled-tuned filter. This is a technique of eliminating a particular current harmonic by tuning a low-pass filter to a specific frequency that uses low impedance such as 5th multiple or 7th multiple harmonics of the fundamental. High-pass filters on the other hand also consist of passive components with less impedance for harmonics at specific frequencies, thus filtering all harmonics present with higher frequencies [22]. These filters can be configured as the first order, second order, third order, and fourth-order high pass filters. The first order filters are the simplest form of high-pass filters, containing only one passive component. The order of the high-pass determines the number of component(s) contained in the filter and the higher-order provides better stability to the power system. In our study, we simply applied a capacitor between the PV panel and boost converter. Additionally, the MPPT algorithm of the boost converter helps to decrease the current harmonics of the topology and increase the efficiency.

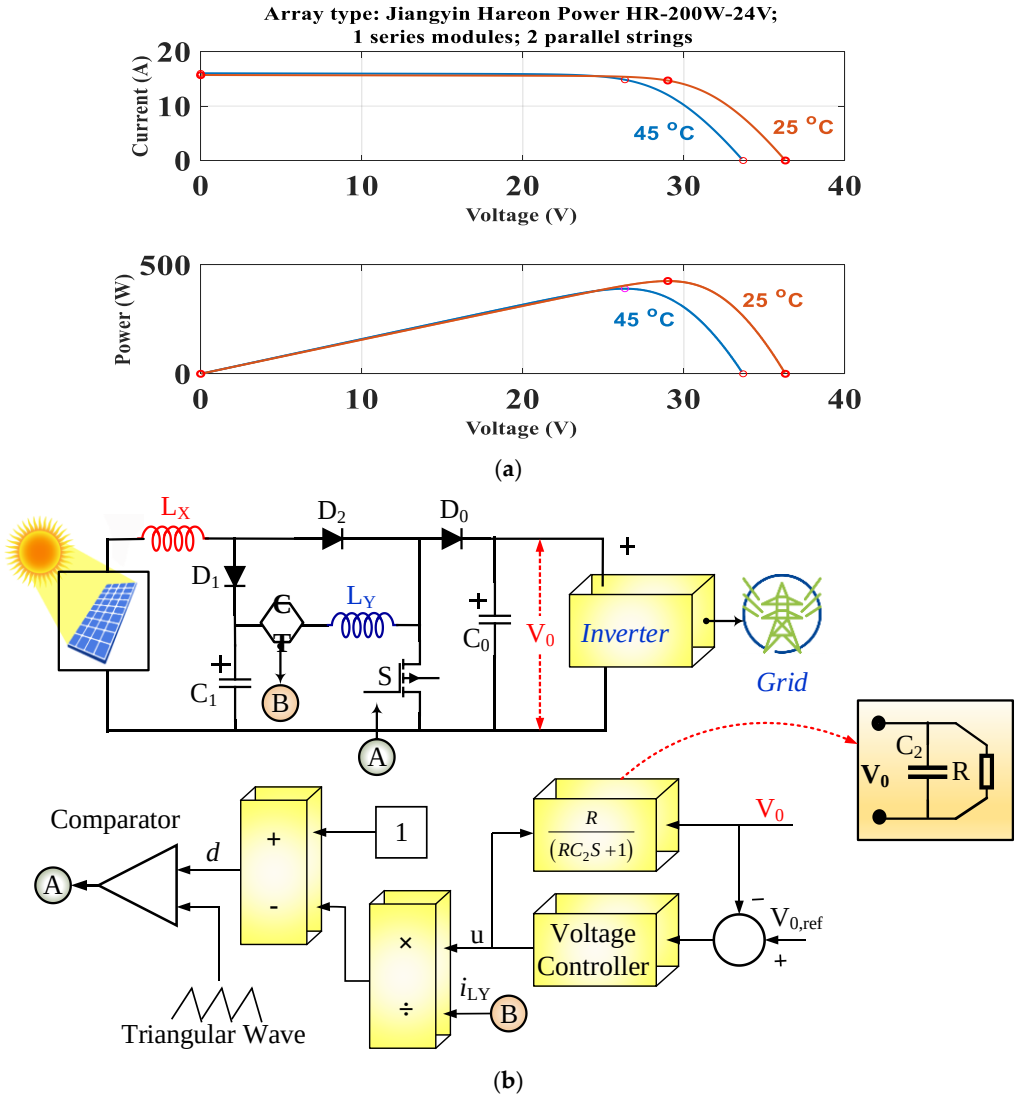


Figure 7. (**a**) Current-Voltage (I-V) and Power-Voltage (P-V) characteristics of the applied PV arrays and (**b**) the proposed structure with the designed controller block.

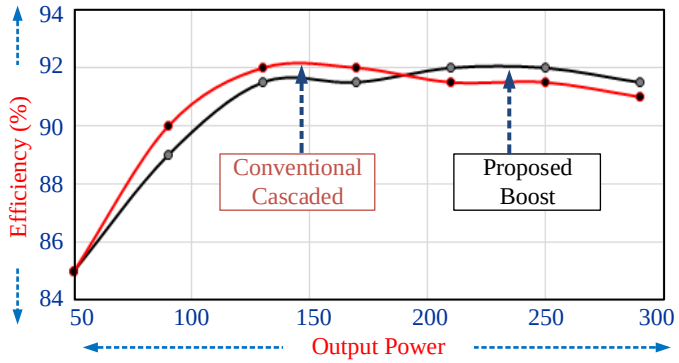


Figure 8. Efficiency diagram for the proposed and conventional cascaded structures.

Figure 9a shows the voltage gain for the proposed and conventional boost circuits in 50% of the duty cycle and 50 to 200 Ω as the load. One of the most important issues for a boost converter is the converter's ability to gain production since voltage transfer is preferred, rather than the current transition in all parts of fossil or renewable energy sources.

The simulation was conducted from 50 W to around 290 W of the output power and for all of this band, the proposed converter presented higher DC gain. Additionally, Figure 9b illustrates a comparison diagram between the classical cascade and proposed topologies voltage gain for this band of output power for different values of duty cycles from 30 to 90%. The same result is reported for this test.

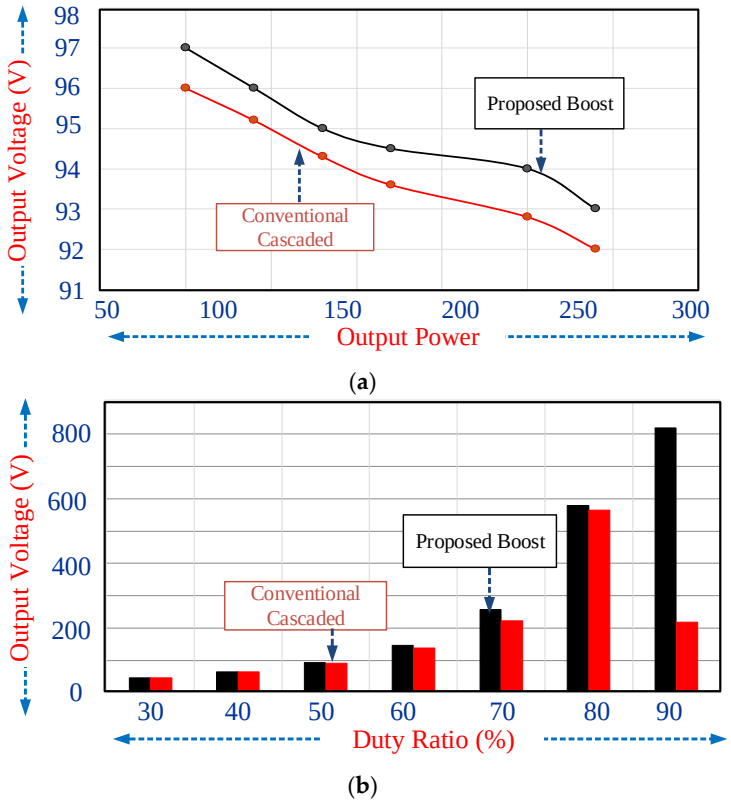


Figure 9. (**a**) Voltage gain diagram for the proposed and conventional cascaded structures in real and ideal states based on different (**a**) loads and (**b**) duty cycles.

Figure 10 illustrates the controller performance and stability in producing different voltages in output. For this simulation, the input supply was fixed to 24 V and the reference voltage was changed between 80 V, 100 V, and 120 V. For our tests, in order to carry out the PWM implementation to gate-source pins of the power semiconductor switch, the triangle waveform was considered with a 50 kHz frequency. By considering the damping factor for the proposed controller at the change points of the output voltage, a limited value of the overshoot was reported. These overshoot values can have smaller values with PI controller internal adjustments in MATLAB/SIMULINK for the upper and lower output limits, which is applicable for an embedded controller like the M9036A and M9037A or MEC1609 series.

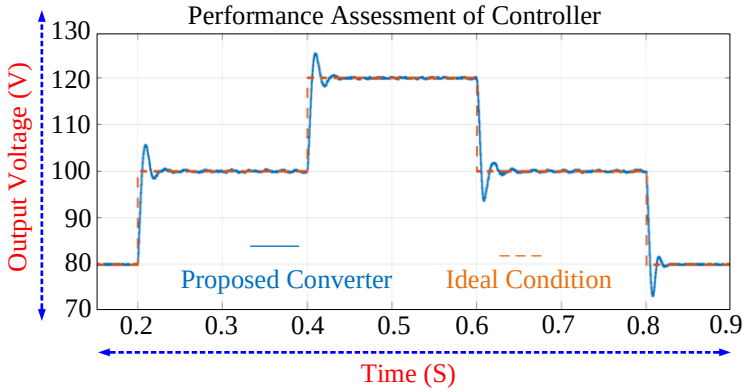
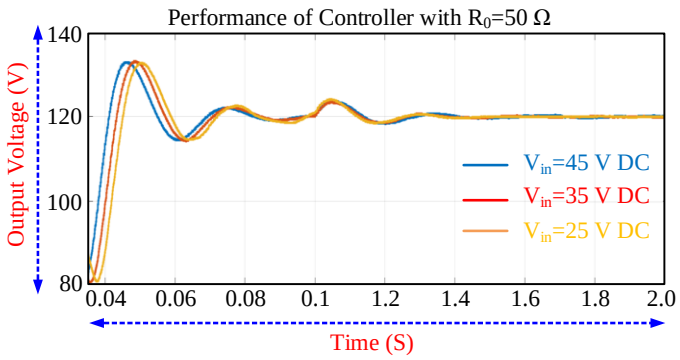


Figure 10. Tracking and ability to obtain different output voltages by the proposed controller.

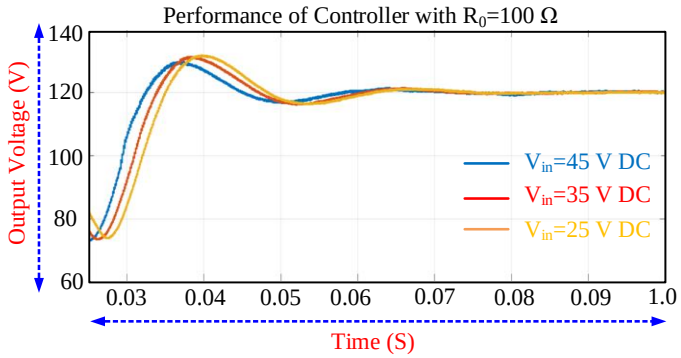
Figure 11 presents the performance of the controller to present the fixed voltage at the load side by changing the input voltage values. As known, PV panels based on different irradiance and temperatures present different values of voltages. Therefore, one of the specifications of a good converter and controller is the ability in obtaining a fixed DC voltage for load by different values of the input voltage. Therefore, in the worst condition, if both the input voltage and output load change, we should consider the performance of the controller for reliability analysis. Figure 11 presents the reaction of the controller for input voltages from 25 V to 45 V and load values from 50 Ω to 200 Ω. As reported in Figure 11a, and as expected, for higher loads where higher currents are needed, the overshoot is higher and the settling time is longer. For a higher amount of input voltages and lower amount of output currents, as Figure 11c presents, both overshoot value and settling time are less. In addition, it can be found that when the input voltage is higher for a fixed load, the overshoot is less and settling time is shorter.

Figure 12 illustrates the current values for the power MOSFETs, output diodes, and input inductors of around 50 W of output power. As can be seen from Figure 12a,b, approximately the average value of the current for the switch in the proposed converter was equal with the total currents of switches in the cascaded converter. In fact, we should make a trade-off between having two different power MOSFETs with two controller structures and only one power MOSFET with only one controller. Moreover, for the new SiC generation of power MOSFETs, we can present a quick and stable converter and resonant snubber structures can be used to decrease these stresses. Figure 12c,d show that the proposed converter can present a lower amount of currents for the input inductor and output diode. However, this difference was not impressive. In general, as the mathematical analysis shows, the total losses of the proposed converter are comparable with the cascaded converter and for higher amount of power, it is more efficient.

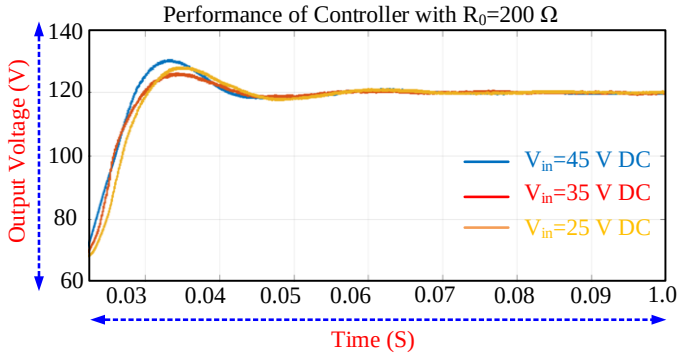


(**a**)

Figure 11. *Cont.*



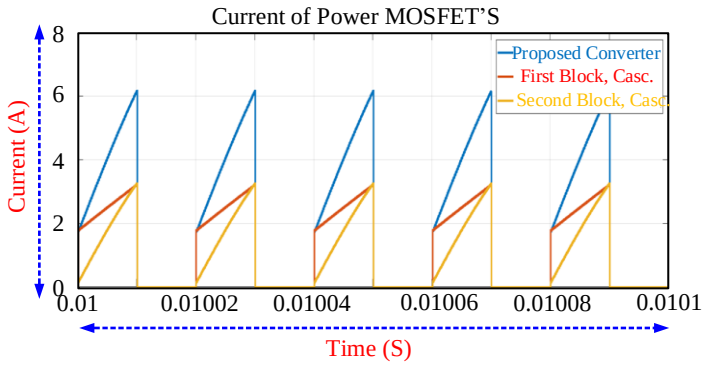
(**b**)



(**c**)

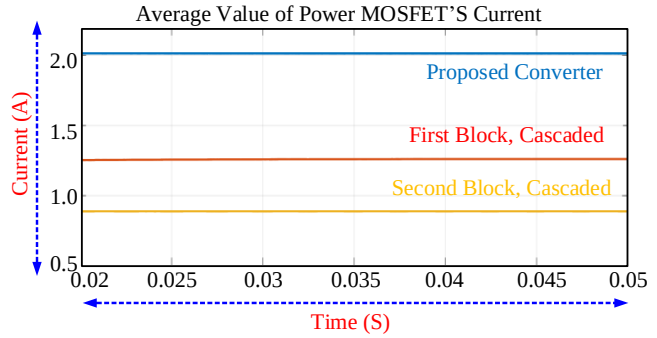
Figure 11. Tracking of the desired voltage in the proposed converter when the input voltage changes from 25 V to 45 V and the loads are (**a**) 50 Ω; (**b**) 100 Ω, and (**c**) 200 Ω.

Figure 13 illustrates the current wave form for the input side of the boost converter. As can be seen, the performance of the capacitor as the simple input passive filter was considerable and under the control procedure by the proposed PI controller, a very high quality current wave form could be obtained. This current guarantees a pure DC current for the load.

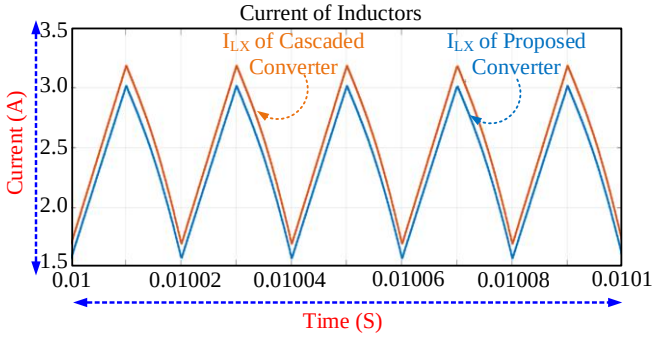


(**a**)

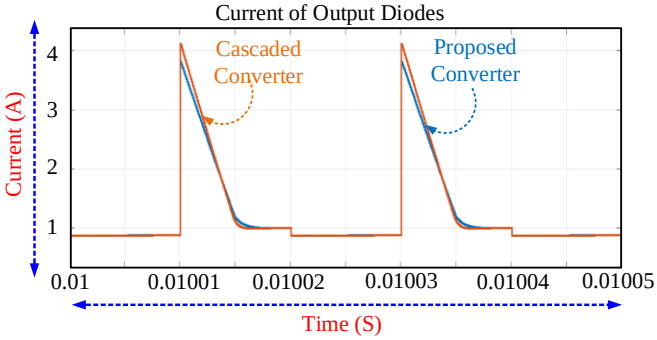
Figure 12. *Cont.*



(**b**)



(**c**)



(**d**)

Figure 12. (**a**) Current wave forms for the power MOSFETs and (**b**) average of these currents; currents for the (**c**) input inductors, and (**d**) output diode.

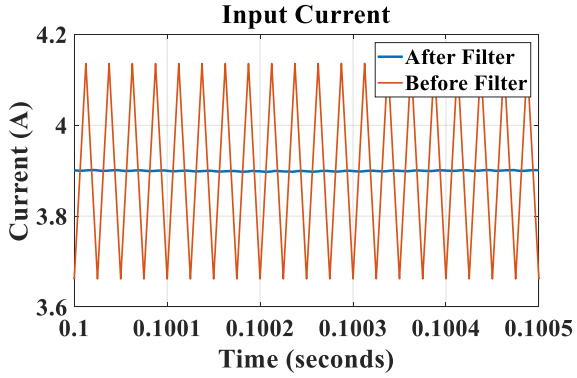


Figure 13. The reaction of the input current under performance of the passive filter and proposed controller.

4. Experimental Results and Discussion

A prototype with around 100 W was implemented and Figures 14–17 show the results. The switching frequency was set to 50 kHz. Inductors L_X and L_Y were fixed to 200 uH, the capacitor C_1 value was considered as 1 µF, and the output capacitor C2 as 47 uF. Figure 14 presents the hardware prototype. Figure 15 shows the gate source and drain source pulses of the structure in 50% and 75% of duty cycles and as we expected, different values of ON and OFF intervals of power MOSFET and as a result, different duty cycles for the voltages of drain-source pins were obtained. Figure 16 illustrates the voltage waveforms for the capacitors and currents of the inductors.

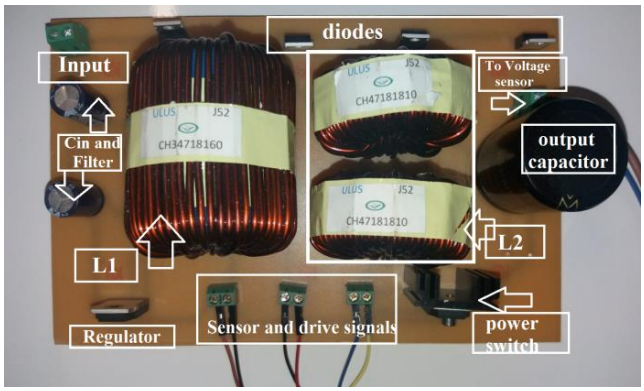
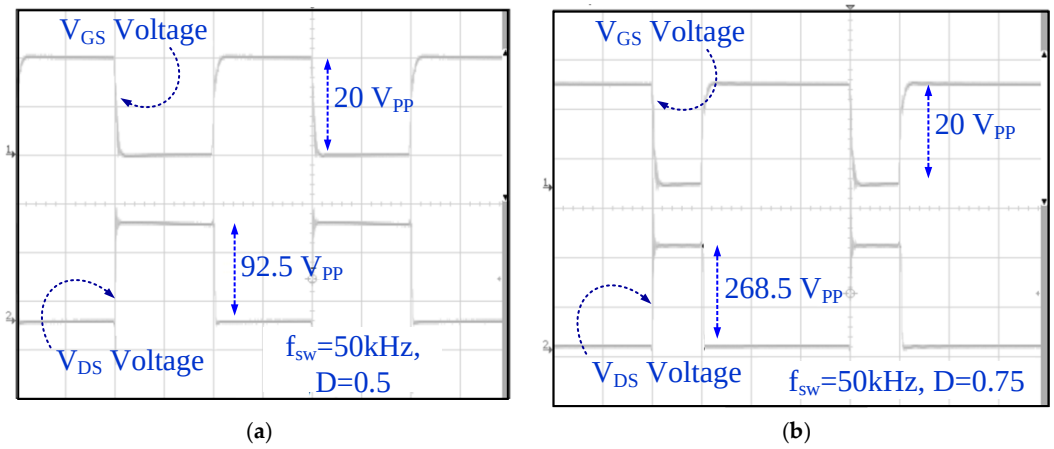
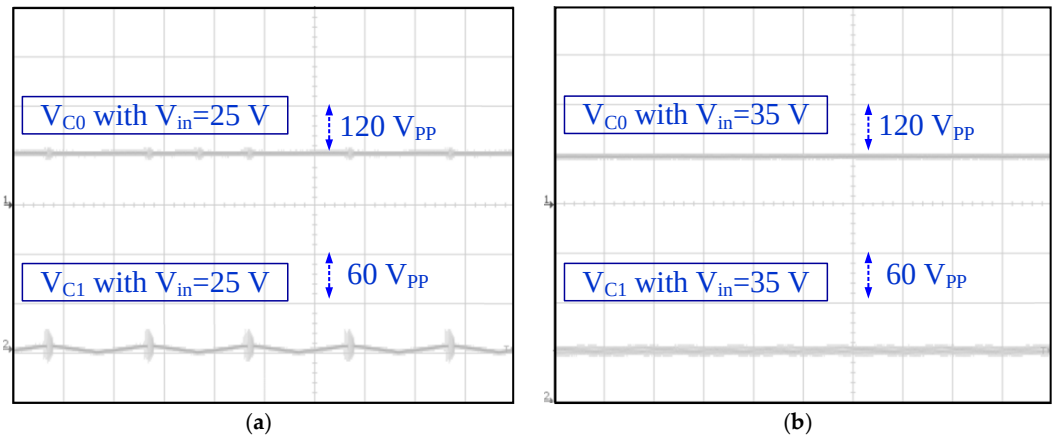


Figure 14. Hardware prototype.



(**a**) (**b**)

Figure 15. Gate source and drain-source voltages of the projected structure when the duty cycle is (**a**) 50% and (**b**) 75%.



(**a**) (**b**)

Figure 16. *Cont.*

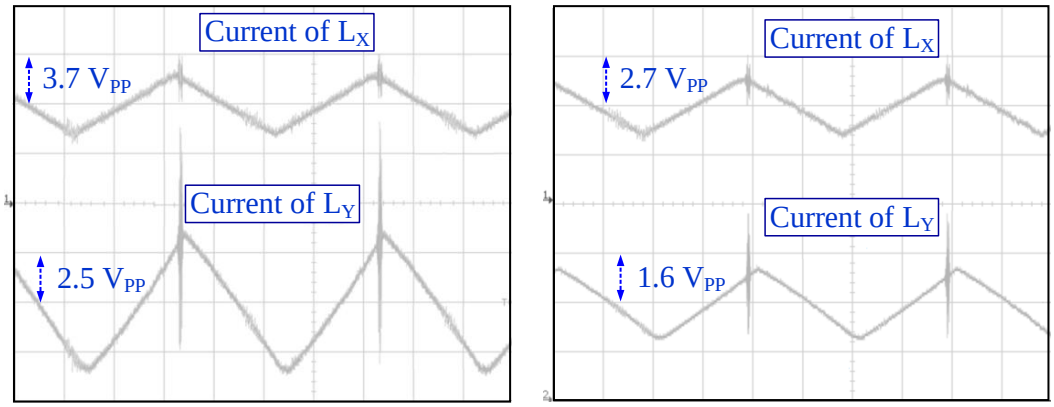


Figure 16. Voltage through capacitors C_1 and C_2 under (**a**) V_{in} = 25 V; (**b**) V_{in} = 3 5 V and currents of the inductors L_X and L_Y under (**c**) V_{in} = 25 V, R_0 = 150 Ω and (**d**) V_{in} = 35 V, R_0 = 250 Ω.

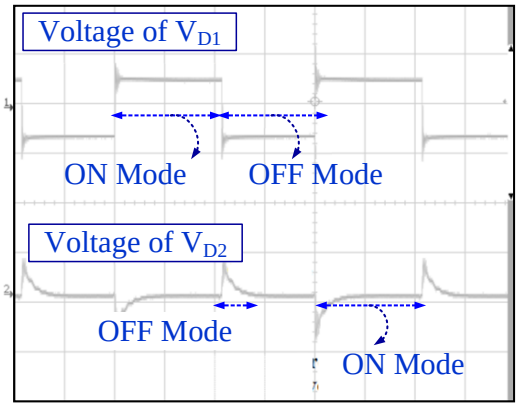


Figure 17. Oscillation domain of output DC voltage in the 50% duty cycle and switching frequency of 50 kHz.

In Figure 16a, under 25 V as the input voltage, by applying the proposed controller method, the output voltage was set to 120 V. So, as expected based on Equation (30), half of this value was measured on the first capacitor and the second half of the proposed converter doubled this value on capacitor C_0. This test was undertaken on a 120 Ω resistive load, so the voltages on the capacitors, especially the voltage on capacitor C_1, had fluctuations on switching times. The load value was set to 240 Ω and the input voltage was increased to 35 V for Figure 16b, and as shown, these sudden ripples decreased. This event is normal because not only was the input voltage increased, but the output current was also a lower level in comparison with the first test. Figure 16c presents the current waveforms of the inductors for a 150 Ω resistive load with 120 V and 25 V as the output and input voltages, respectively. As the results show, the current of the inductor L_Y was less and the result confirmed Equations (34) and (35). Additionally, ripple values were reported of around 1.3 and 1.8 A for L_X and L_Y, respectively, which is in agreement with the mathematical analysis presented in Table 1. Figure 16d reports the results of the same process with a 250 Ω resistive load, 35 V input, and 120 V output voltages. The obtained currents and ripple values confirmed the same equations mentioned for Figure 16c.

Figure 17 shows the status of the power diodes D_1 and D_2 and confirms the conductivity theory of these diodes in different work principles that was presented in Section 2.1 in 50% of the duty cycle. Based on this result, when the power diode D_1 is in ON mode, D_2 is in OFF mode and vice versa. A comparison was done in this part between the proposed PI controller and several other controllers in order to assess the performance of the projected structure. Different controllers have been investigated for DC–DC boost converters. The authors in [23] presented a fault tolerant-based DC–DC boost converter. This structure uses an extra Triode for Alternating Current (TRIAC) and an auxiliary power

switch with a DC gain closed to the conventional boost converter. The optimal switching frequency of this converter was adjusted to 20 kHz and the efficiency of the controller was calculated as around 87 percent for low power applications. In [24], a field-programmable gate array control technique was presented for non-isolated DC–DC converters. The basis of this controller was established on time and the current of the inductor and the robustness of the system was investigated. The controller worked in low switching frequencies around 15 kHz and is suitable for high power applications. The inductor value was comparatively high and at the same time, several internal controller blocks worked to fix the output voltage. The study in [25] suggested a model-based state estimator approach for the DC–DC converter where the mathematical complexity and specifications of this converter such as switching frequency and inductor value were similar to the method presented in [24].

A PV-connected DC–DC boost converter using a LUENBERGER observer-based fault detection controller was presented in [26]. A deep mathematical approach was investigated in this study and the converter block worked as a part of the PV-based maximum power point tracking system. The converter's disadvantage is not applicable in high switching frequencies and is also proper for high power applications. Therefore, the IGBT is suggested for application instead of the power MOSFET. The authors in [27] presented a time-domain analysis of the state-space observer residual controller technique for interleaved DC–DC converters. The switching frequency was adjusted to 25 kHz. The total cost of the prototype was categorized in the medium to high range. Table 4 presents the general specifications of these controllers.

Table 4. Comparison of different controllers for DC–DC boost converters.

Reference	Controller	Switching Frequency	Average Efficiency (500 W)	Complexity
[23]	Capacitor voltage	20 kHz	87	Medium
[24]	Inductor current	15 kHz	85	Medium
[25]	State estimation	10–20 kHz	87	Medium
[26]	LUENBERGER observer	10 kHz	85	High
[27]	Linear observer	25 kHz	90	High
Proposed	PI	50 kHz	91.5	Medium

Figure 18 presents the efficiency curves for the presented controllers in Table 4 versus the output power. As can be seen, the performance of the proposed PI controller is considerable, especially in low powers. It can be interpreted based on all facts presented in Table 2. Based on less power MOSFET numbers in the converter's structure and good performance of the proposed PI controller to 350 W, it had the highest efficiency. The performance of the linear observer acts in a similar way to the proposed controller for 350 to 500 power range.

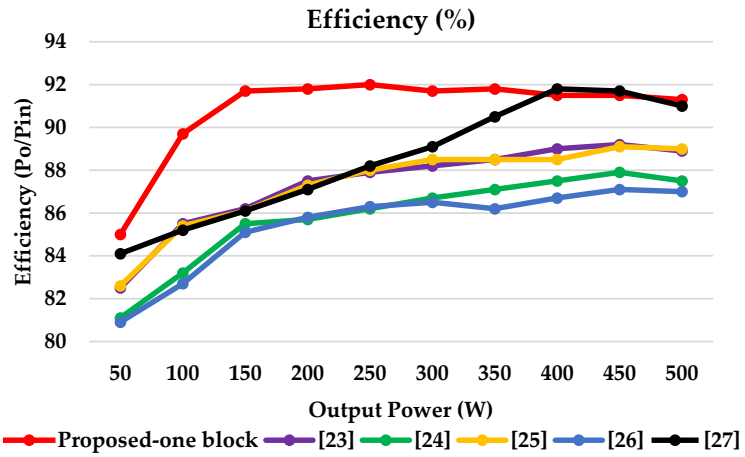


Figure 18. Efficiency comparison for different controllers for maximum power point tracking of DC–DC boost converter-based.

5. Conclusions

This study presents a high gain step-up converter with a simple and cheap controller based on small signal analysis and steady space matrixes. In comparison with the conventional boost converter, the proposed converter uses two additional power diodes, a capacitor, and an inductor. However, the voltage gain of the projected converter is considerable and acts as a cascaded step-up converter. Furthermore, by considering that the topology has only one power switch and in any time interval only two diodes will be in the structure, it presents the same values of the losses in comparison with the cascaded converter by considering the switching, dynamic, and frequency losses. For the controller design, the topology was examined in two ON and OFF states of the switch. So, among all of the equations, the optimal equation that can present a relation between the output voltage and current derivation of the second inductor was selected. The controller was investigated through this equation and the simulation and experimental results showed the robust and stable working conditions for the proposed controller.

A group of simulations was undertaken in MATLAB/SIMULINK 2017a and the results confirmed the theoretical and mathematical analysis. Simulations were done for different values of the input voltages and output loads to generate the different voltages by the PV panels based on the irradiance and temperature. Therefore, a good controller should present stable and fixed DC voltages for the different values of this input source. Additionally, the stability of the structure and controller is important when different values of loads are entered at the output side of the structure. The results showed that for 24 V and 50 Ω as the output load, the controller can reach the fixed desired 120 V with around 0.12 S, which is acceptable for a topology that will work for a long time. A laboratory scaled prototype was implemented. For a 24 V input source, since the simulation results give 93 V as the output voltage in 50% of duty cycles, the prototype can present around 92.5 V, which is acceptable and confirms the theoretical analysis and simulation results. Working in lower switching frequencies will help to decrease the voltage and current stresses on power switches where a high gain application is necessary. As a suggestion, soft switching and snubber sub-structures can be utilized to decrease these stresses.

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