Low-Noise Multimodal Reconfigurable Sensor Readout Circuit for Voltage/Current/Resistive/Capacitive Microsensors

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Abstract: This paper presents a low-noise reconfigurable sensor readout circuit with a multimodal sensing chain for voltage/current/resistive/capacitive microsensors such that it can interface with a voltage, current, resistive, or capacitive microsensor, and can be reconfigured for a specific sensor application. The multimodal sensor readout circuit consists of a reconfigurable amplifier, programmable gain amplifier (PGA), low-pass filter (LPF), and analog-to-digital converter (ADC). A chopper stabilization technique was implemented in a multi-path operational amplifier to mitigate 1/f noise and offsets. The 1/f noise and offsets were up-converted by a chopper circuit and caused an output ripple. An AC-coupled ripple rejection loop (RRL) was implemented to reduce the output ripple caused by the chopper. When the amplifier was operated in the discrete-time mode, for example, the capacitive-sensing mode, a correlated double sampling (CDS) scheme reduced the low-frequency noise. The readout circuit was designed to use the 0.18-μm complementary metal-oxide-semiconductor (CMOS) process with an active area of 9.61 mm^2. The total power consumption was 2.552 mW with a 1.8-V supply voltage. The measured input referred noise in the voltage-sensing mode was 5.25 μV$_{rms}$ from 1 Hz to 200 Hz.

Keywords: reconfigurable sensor readout circuit; multimode sensing; microsensors; correlated double sampling (CDS); multi-path operational amplifier; chopper stabilization

1. Introduction

The market for microsensors based on micro-electromechanical systems (MEMS) technology has grown rapidly in recent years, with many attempts using the Internet of Things (IoT) to integrate various microsensors into systems for safety, health, convenience, and industry [1].

Microsensors provide output signals based on changes in voltage, current, resistance, or capacitance by utilizing specific physical/chemical variations. Various analog front-end architectures that can convert and amplify the input signals from microsensors to an amplified voltage or digital output have been reported, for example, pressure, acceleration, humidity sensors, and so on [2–7]. In the recent IoT environment, which demands multi-functional sensing capability, a readout circuit for multimodal sensing is required. An example of IoT utilization with a range of microsensors is environmental monitoring [8]. As environmental pollution increases due to population growth and industrial development, monitoring technology using environmental sensors is becoming increasingly

important. Microsensors, such as fine dust sensors, water quality sensors, and temperature and humidity sensors, in an environmental monitoring system must use a suitable readout circuit for each sensor type to detect and respond appropriately to adverse effects on the human body and the air/water ecosystem. The conventional approach is for each type of microsensor to have individual readout circuits. Following this approach, the cost can be drastically increased as the required modality of sensors increases. To solve this problem, several research papers have presented a multimodal sensing system that shares a single reconfigurable readout circuit [9–13]. A combined system that provides accurate and precise performance with reconfigurable capability can reduce the system cost, the overall power consumption, and the size. To obtain an accurate multimodal sensing capability, a low-input referred noise in the readout circuit is essential. For example, a resistance or capacitance to voltage conversion through an instrumentation amplifier (IA) can have low, long-term output fluctuations caused by the effect of low-frequency noise in an amplifier. In addition, the low-frequency noise can be amplified by the IA and can limit the output dynamic range.

To solve this problem, dynamic offset cancellation techniques, including chopper stabilization or correlated double sampling (CDS), are widely used [14–16]. Among them, chopper stabilization is preferred because the low-frequency noise density can be lowered to near the thermal noise level by modulating the low-frequency noise components. However, the chopper stabilization technique restricts the bandwidth of the amplifier and generates a ripple caused by the up-modulation of the offset, and these disadvantages should be resolved.

This paper presents a low-noise multimodal reconfigurable sensor readout circuit for voltage/current/resistive/capacitive microsensors. The aim of the proposed circuit was to obtain multimodal characteristics and to achieve low noise for accurate sensing capability in IoT sensors, such as environmental sensors. For multimodal characteristics, we proposed a reconfigurable structure that can accommodate voltage/current/resistance/capacitive sensors.

Also, both low-noise and wide-bandwidth characteristics were achieved by adopting multiple dynamic offset cancellation (DOC) techniques. The amplifier was designed using a chopper-stabilized multi-path topology with an AC-coupled ripple reduction loop (RRL). Bandwidth limiting caused by the chopper stabilization technique was solved using a multi-path structure amplifier [17]. The front-end stage of this circuit could be operated in the continuous-time mode or discrete-time mode. In the discrete-time mode, to eliminate the residual offset and low-frequency noise components, the correlated double sampling technique was applied.

2. Proposed Multimodal Reconfigurable Sensor Readout Circuit

2.1. Top-Level Architecture

The block diagram of the proposed multimodal reconfigurable sensor readout circuit is shown in Figure 1. The proposed readout circuit uses a three-operational amplifier IA topology consisting of the reconfigurable structure, a programmable gain amplifier (PGA), and a low-pass filter (LPF). For digital processing, a 12-bit successive approximation register analog-to-digital converter (SAR ADC) was implemented.

2.2. Reconfigurable Structure

The reconfigurable structure of the first stage according to the sensor application is shown in Figures 2 and 3. Depending on the voltage/resistive-, current-, or capacitive-sensing modes, the chopper-stabilized, multi-path operational amplifiers, A_{1M} and A_{2M} can be reconfigured to three amplifier types: a voltage buffer, trans-impedance amplifier (TIA), and a CDS scheme. The reconfiguration of the amplifier is manually controlled by switches.

Figures 2 and 3 illustrate the configurations of the possible sensing modes. To describe the readout operation, the sensor in the voltage/resistive-, current-, and capacitive-sensing modes in Figures 2 and 3 is expressed by the resistive bridge, diode, and capacitive sensor, respectively.

The configuration of the voltage/resistive-sensing mode is shown in Figure 2a. The A_{1M} and A_{2M} amplifiers are converted to TIAs, which have a programmable feedback register R_1. R_{mid} is connected to the negative input of the TIAs by switches such that the output signal is amplified by the ratio of R_1 to R_{mid}. The output voltage of the voltage/resistive-sensing mode is expressed using the following equation:
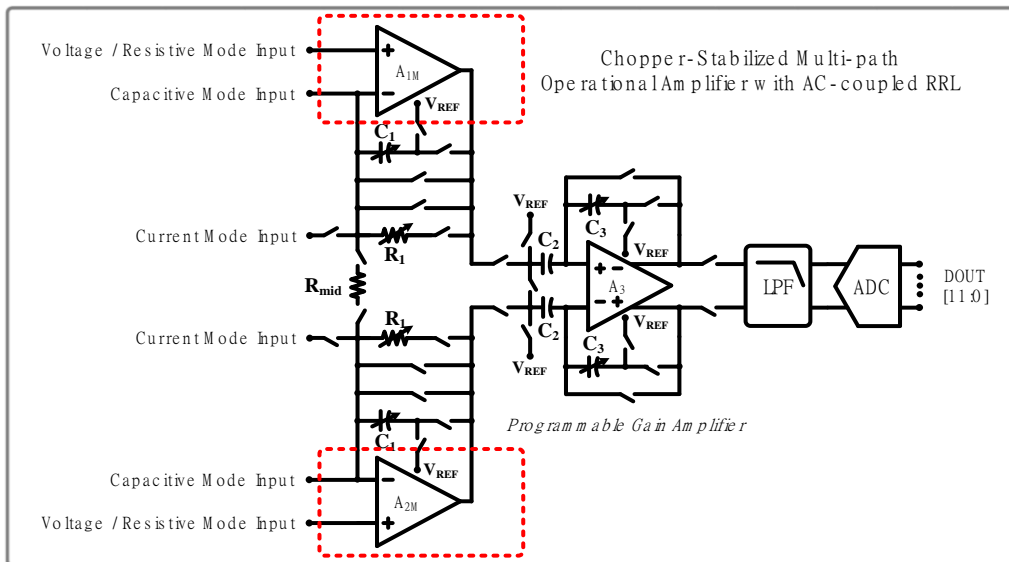
$$V_{ov1} = \left(1 + \frac{2R_1}{R_{mid}}\right) \times V_{idv} \tag{1}$$

Figure 1. Block diagram of the proposed multimodal reconfigurable sensor readout circuit. ADC: analog-to-digital converter, LPF: low-pass filter.
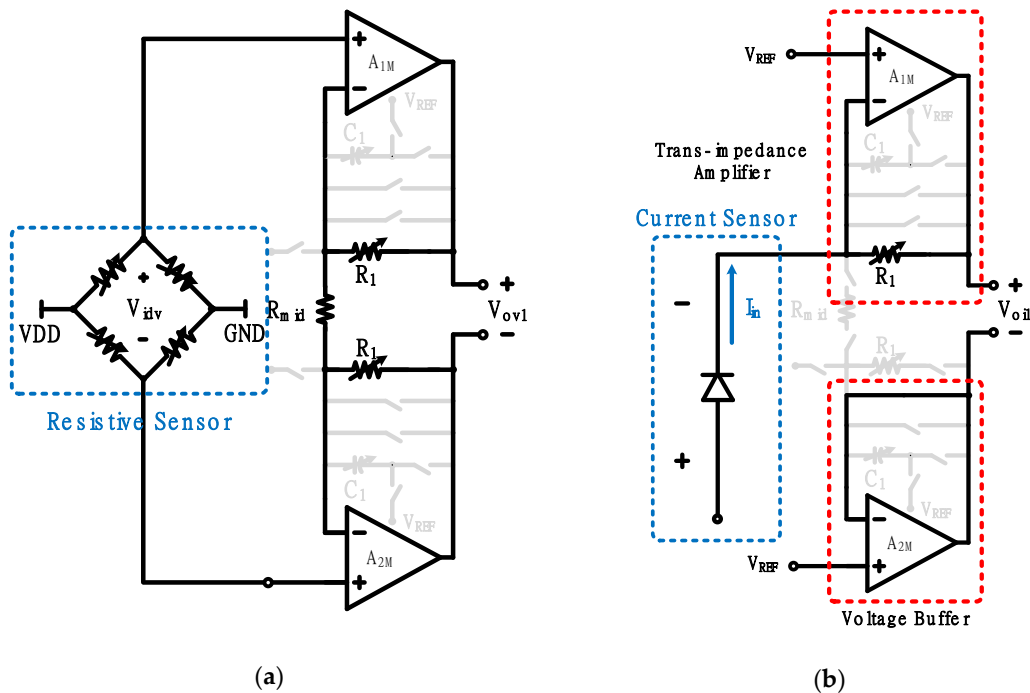

Figure 2. (**a**) Configuration of the voltage/resistive-sensing mode (**b**) Configuration of the current-sensing mode. GND: ground, VDD: dc supply voltage.

The configurations of the current-sensing and capacitive-sensing modes are shown in Figures 2b and 3 respectively. These configuration modes are available in both single-ended and differential modes. For simplicity, both modes are described using the single-ended mode. In the current-sensing mode configuration, the A_{1M} amplifier is converted to a TIA and the A_{2M} amplifier is converted to a voltage buffer. The output current of the sensor is converted into a voltage through the TIA. The ratio of the output voltage to the input current can be adjusted using programmable resistor R_1, and is expressed using the following equation:

$$V_{oi1} = R_1 \times I_{in} \tag{2}$$

In the capacitive-sensing mode configuration, the A_{1M} amplifier is converted to the CDS scheme and the A_{2M} amplifier reconfigures as a voltage buffer. In this mode, as the CDS scheme is operated by non-overlapping CDS clocks, P_{1CDS} and P_{2CDS}, the capacitive-sensing mode is driven under the discrete-time mode. If an offset exists in front of the A_{1M} amplifier input, the CDS scheme can reduce the offset by subtracting the offset charges stored in capacitor C_1 at the P_{1CDS} and P_{2CDS} clocks. Its output is amplified by the ratio of the input capacitance to a programmable capacitor C_1, such that the output voltage is expressed using the following equation:

$$V_{oc1} = V_{DD} \times \frac{2\Delta C}{C_1} \tag{3}$$

In this mode, resolution degradation can be caused by the parasitic capacitance of the capacitive sensor. The parasitic capacitance is an unwanted component due to a process mismatch and random variations. The parasitic capacitance can often be greater than the change of input capacitance, resulting in a poor resolution. In extreme cases, the output voltage of the readout circuit can be ground or DC supply voltage. Assuming the capacitive sensor in Figure 3 has a parasitic capacitance, the output voltage is expressed using the following equation:

$$V_{oc1} = V_{DD} \times \frac{\left(2\Delta C + C_{p1} - C_{p2}\right)}{C_1} \tag{4}$$

In the above equation, if C_{p1} and C_{p2} are ideally the same such that there is no effect on the output voltage. However, if C_{p1} and C_{p2} are different, and the difference of the value is large, V_{oc1} has an offset regardless of the input capacitance. To attenuate this difference, the 8-bit capacitive digital-to-analog converter (DAC) is applied. The C_{dac1} and C_{dac2}, the capacitance of 8-bit capacitive DAC, can be adjusted from 0.1 pF to 12 pF to compensate for the difference in parasitic capacitances C_{p1} and C_{p2}.

The CDS configuration of the PGA in the second stage is shown in Figure 4. The offset can be reduced by the CDS configuration of the second stage. If the amplifier operates in a capacitive-sensing mode, the offset can be reduced twice through two CDS configurations. The CDS operation of the PGA is driven by non-overlapping clocks, P_1 and P_2. In the P_2 clock, the input and offset are stored in C_2, and in the P_1 clock, the offset stored in C_2 is removed, such that a low offset can be achieved [18]. The input voltage of the PGA is amplified by the ratio of C_2 to C_3. The programmable capacitor C_3 enables adjustment of the gain. The gain is expressed using the following equation:

$$V_{oPGA} = \frac{C_2}{C_3} \times V_{ox1} \tag{5}$$

Consequently, the output voltages of the readout circuit according to the sensing mode (voltage/resistive-sensing mode, current-sensing mode, and capacitive-sensing mode) are respectively defined by the following equations:

$$V_{ovPGA} = \frac{C_2}{C_3} \times \left(1 + \frac{2R_1}{R_{mid}}\right) \times V_{idv} \tag{6}$$

$$V_{oiPGA} = \frac{C_2}{C_3} \times R_1 \times I_{in} \tag{7}$$

$$V_{ocPGA} = \frac{C_2}{C_3} \times \frac{2\Delta C}{C_1} \times V_{DD} \tag{8}$$
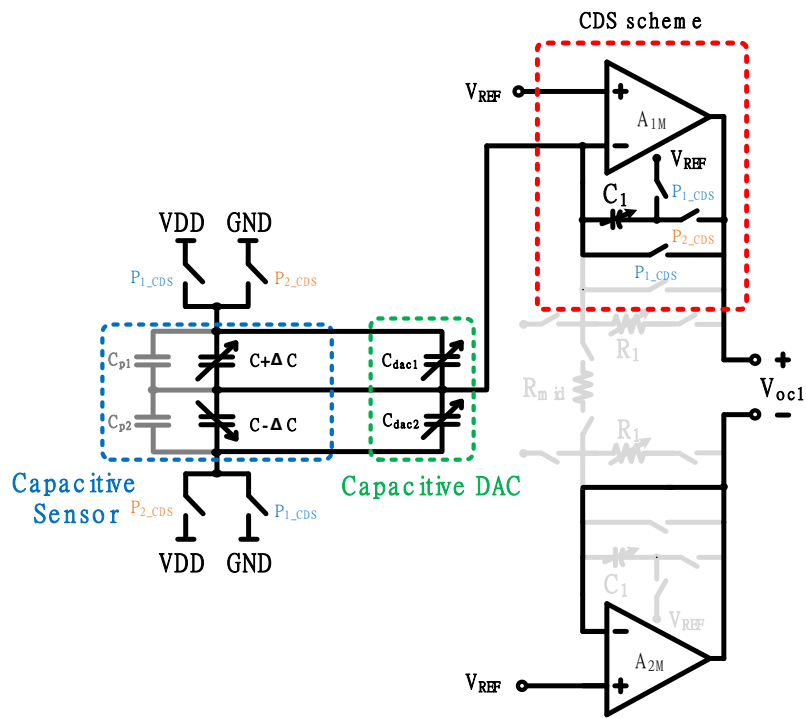

Figure 3. Configuration of the capacitive-sensing mode. CDS: correlated double sampling, DAC: digital-to-analog converter.
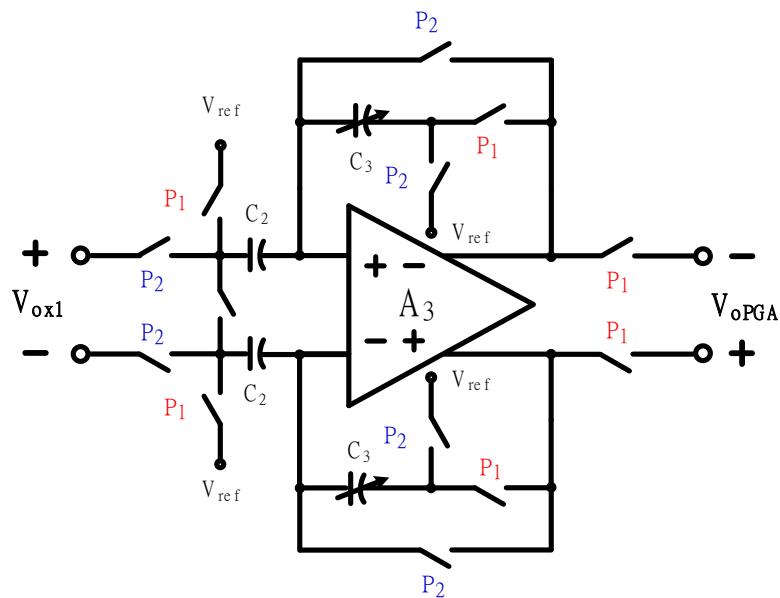

Figure 4. CDS configuration of the programmable gain amplifier (PGA) in the second stage.

2.3. Detailed Description of the Amplifiers

2.3.1. Chopper-Stabilized, Multi-Path Operational Amplifier with an AC-Coupled RRL

The block diagram of the chopper-stabilized, multi-path operational amplifier with an AC-coupled RRL is shown in Figure 5. This circuit has two main signal paths: a low-frequency path and a high-frequency path. The low-frequency path determines the gain and noise at low frequencies, while the high-frequency path determines the gain at high frequencies. This multi-path structure can compensate for the bandwidth limiting caused by chopper stabilization [17].
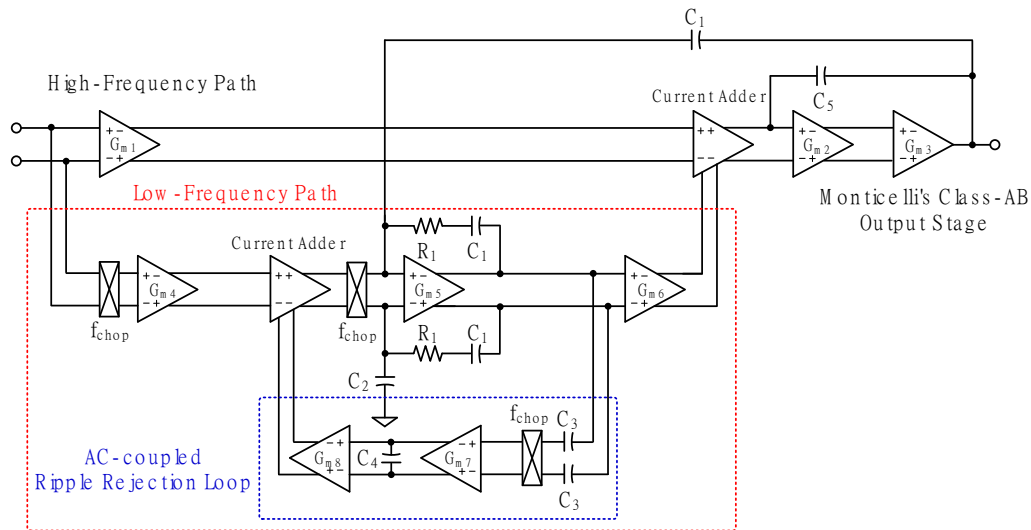

Figure 5. Block diagram of the chopper-stabilized, multi-path operational amplifier with an AC-coupled RRL.

In the high-frequency path, the folded cascade stage is used to provide a high gain. A nested Miller compensation through C_5 is applied for compensation in the high frequency path. To obtain a high power efficiency and slew rate, a Monticelli class-AB output stage was applied.

In the low-frequency path, the chopper stabilization technique was implemented to reduce the low-frequency noise. This technique modulates the low-frequency noise into the high-frequency band with low noise and then demodulates the input signal. It can reduce the low-frequency noise, but a ripple is generated, which can restrict the dynamic range of the amplifier. For a low supply voltage, the effects are more severe and should be reduced. To reduce the ripple, an AC-coupled RRL was applied. When the offset is at the input of the low-frequency path, the offset is up-modulated from DC to AC and amplified by G_{m4}. After entering the chopper circuit, the offset is demodulated from AC to DC and integrated in G_{m5}, causing a ripple approximated by the following equation:

$$V_{ripple} \approx \frac{V_{os}G_{m4}}{2f_{chop}C_2} \tag{9}$$

The ripple enters the AC-coupled RRL through the capacitor C_3 and the RRL reduces the ripple at G_{m5} according to the following equation:

$$V_{rip\_RRL} \approx \frac{V_{os}G_{m4}}{2G_{m7}G_{m8}} \tag{10}$$

By implementing the AC-coupled RRL, the ripple is reduced, but it causes a notch in the transfer function of the amplifier at the chopper frequency. This notch restricts the bandwidth of the amplifier. By combining the low-frequency path and high-frequency path signals in the current

adder, the chopper-stabilized, multi-path structure can compensate for the notch caused by the AC-coupled RRL.

2.3.2. Fully Differential Amplifier

The fully differential amplifier with a rail-to-rail input stage in the PGA is shown in Figure 6. The rail-to-rail input stage can receive the output of the first stage over a wide range of values. To achieve a high gain, this amplifier has two stages: the folded cascade and common source (CS) stages [19]. To ensure frequency stability, the RC compensation using R_{2f} and C_{1f} is applied between the two stages.

In the amplifying stage, matching the common mode signal at the differential output is essential to obtain high signal-to-noise ratios, which is an advantage when using a differential pair. If the common mode signals of the differential outputs do not match each other, unnecessary components, including noise in the outputs, cannot be removed. In addition, the output dynamic range can be limited if common mode signals cannot be matched by the reference voltage, 0.9 V, in the CS stage. To solve this problem, the two common mode feedback (CMFB) scheme was applied. In the folded cascade stage, the resistive divider CMFB was applied. The output common mode signal, which is detected by the resistive divider, adjusts the current source consisting of an n-channel metal-oxide-semiconductor(NMOS). As the gate and drain of the NMOS form a negative feedback loop, the output common mode signal can be matched. In the CS stage, the CMFB consists of a resistive/capacitive divider and an error amplifier. The resistive/capacitive divider detects the common mode signal of the differential output at high and low frequencies. The error amplifier accepts the reference voltage and the detected common mode signal as a differential input and produces an output voltage, V_{cmfb}. V_{cmfb} is connected to the gate of the p-channel metal-oxide-semiconductor (PMOS) device in the CS stage, and a negative feedback loop is formed. The output common mode signal is matched to the reference voltage of 0.9 V by the negative feedback loop.
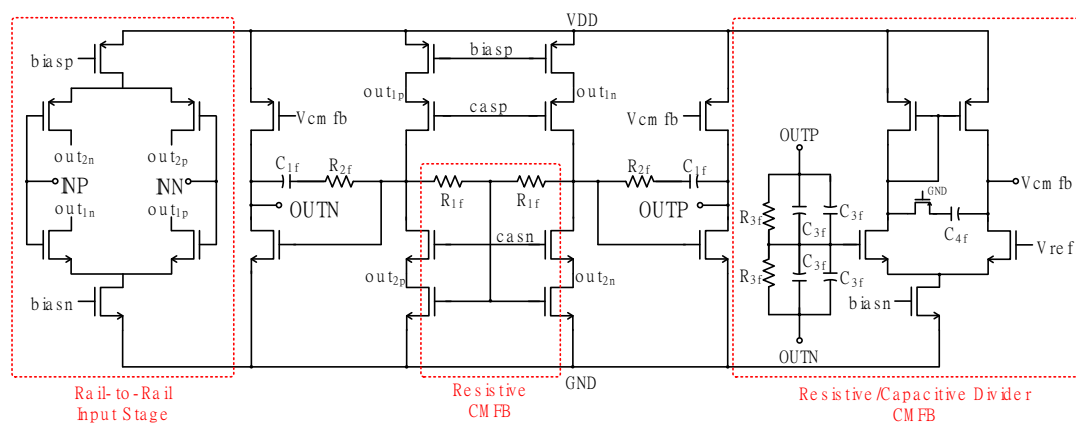

Figure 6. Fully differential amplifier with rail to rail input stage in the PGA. CMFB: common mode feedback, INN: negative input, INP: positive input, OUTN: negative output, OUTP: positive output.

3. Measurement Results

3.1. Measurement Results Using the Implemented Sensor on a Printed Circuit Board (PCB)

A photograph of the fabricated die is shown in Figure 7. The proposed readout circuit was fabricated using 0.18-μm complementary metal-oxide semiconductor (CMOS) technology. The active area of the fabricated die was 9.61 mm^2. The measurement setup is shown in Figure 8. For measurement devices, Keysight's 35670A was used for spectrum analysis, Rohde & Schwars's RTE 1032 was used for signal acquisition, and Keysight's 33500B was used for waveform generation. Arduino's Arduino Due microcontroller was mounted on a PCB for the digital processing of analog output signals and was directly connected to the digital output of the ADC. In the voltage-sensing mode, the gain

could be adjusted from 26 dB to 55 dB by fixing the PGA gain to 13.9 dB. The gain of the PGA was also adjustable from 13.9 dB to 44 dB. The output voltage in the voltage-sensing mode is shown in Figure 9a. The transfer function in the voltage-sensing mode is shown in Figure 9b. A DC gain of 37.4 dB was measured, and the cut-off frequency was 182 Hz. The measured input referred noise in the voltage-sensing mode is shown in Figure 10. The measured input referred noise at 1 Hz was 2.09 $\mu V/\sqrt{Hz}$. The RMS input referred noise was calculated to be 5.25 μV_{rms} over the bandwidth from 1 Hz to 200 Hz.
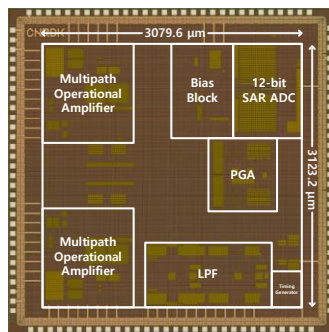
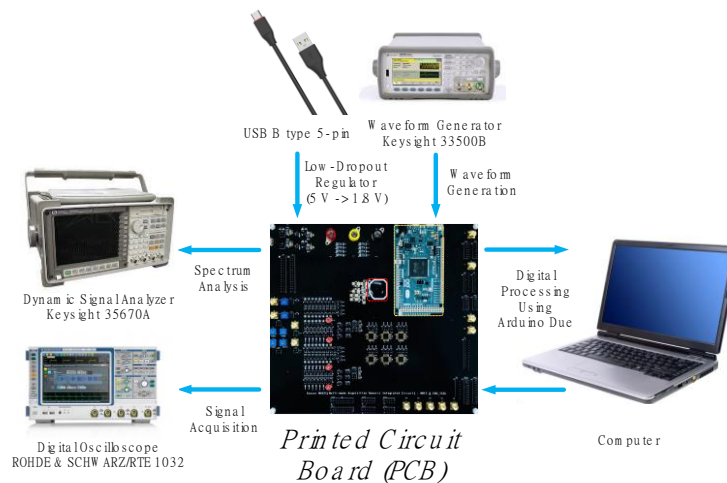**Figure 7.** Photograph of the fabricated die, SAR: successive approximation register.

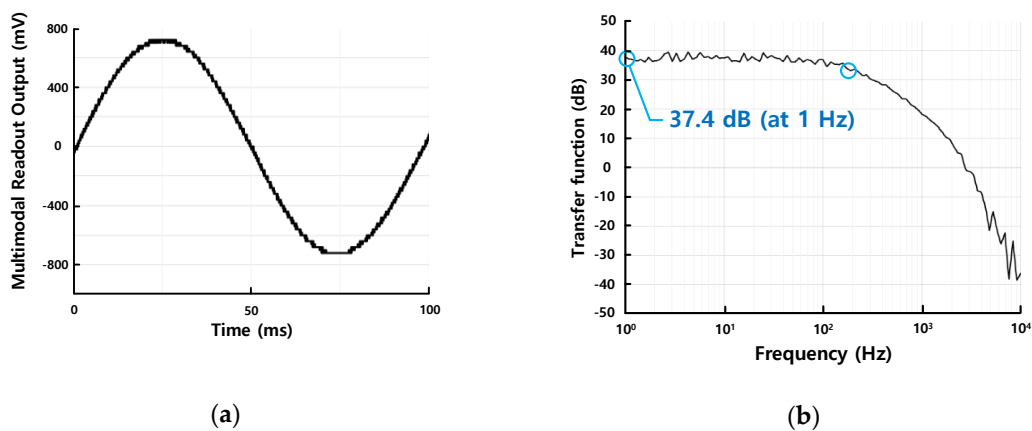**Figure 8.** Measurement setup for the proposed readout circuit.

Figure 9. (**a**) Output in the voltage-sensing mode. (**b**) Transfer function in the voltage-sensing mode.
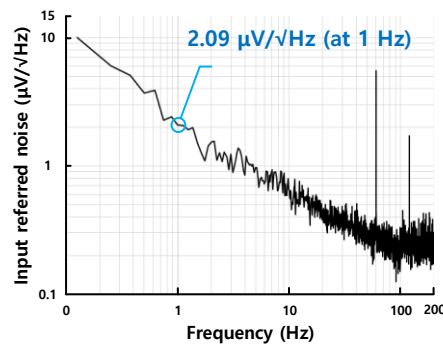
Figure 10. Measured input referred noise in the voltage-sensing mode.

In the resistive-sensing mode, the gain, which is the ratio of the output voltage to the input voltage, equals the gain of the voltage-sensing mode because the resistive-sensing mode shares the configuration of the voltage-sensing mode. The linearity expressed by the ratio of the digital output code to the input resistance is shown in Figure 11a. The coefficient of determination, R^2, was calculated to be 0.9991. The resistance noise floor is shown in Figure 11b. The resistance noise floor was calculated by dividing the input referred noise by 180 mV/kΩ, which was the ratio of the input voltage to the input resistance. This ratio was calculated using a bridge sensor consisting of four 10 kΩ resistors. The resistance noise floor at 1 Hz was 1.16 mΩ/$\sqrt{\text{Hz}}$. The RMS resistance noise floor was calculated to be 2.9 mΩ_{rms} over the bandwidth from 1 Hz to 200 Hz.
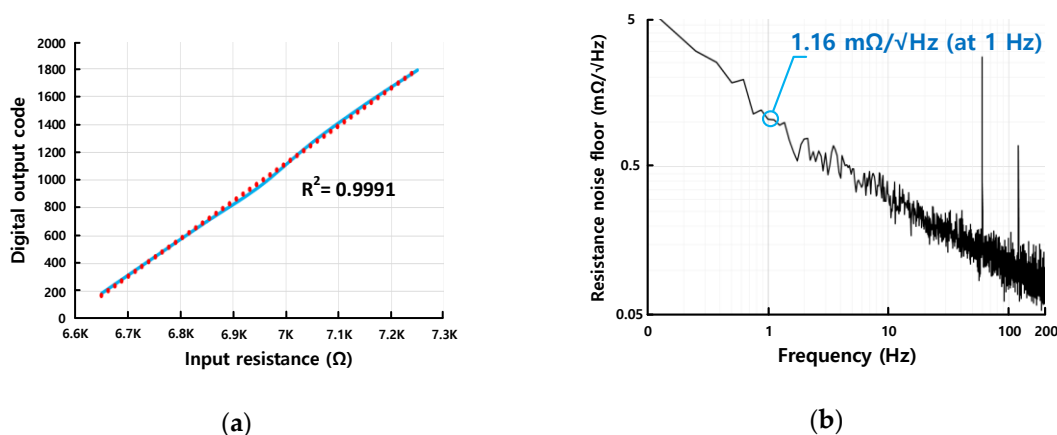

(a)

(b)

Figure 11. (**a**) Linearity expressed as the ratio of the digital output code to the input resistance. (**b**) Resistance noise floor.

In the current-sensing mode, the gain, which is the ratio of output voltage to the input current, could be adjusted from 0.544 MΩ to 11.5 MΩ by fixing the PGA gain to 13.9 dB. The output in the current-sensing mode is shown in Figure 12a. The transfer function of the current-sensing mode is shown in Figure 12b. The DC gain was measured to be 1.24 MΩ and the cut-off frequency was 244 Hz. The measured input referred current noise is shown in Figure 13. The measured input referred current noise at 1 Hz was 25.5 pA/$\sqrt{\text{Hz}}$. The RMS input current noise was 742 pA$_{\text{rms}}$ over the bandwidth from 1 Hz to 200 Hz. In the capacitive-sensing mode, the linearity expressed by the ratio of the digital output code to the input capacitance, is shown in Figure 14a. The coefficient of determination, R^2, was calculated to be 0.9949. The measured capacitance noise floor is shown in Figure 14b. The capacitance noise floor was measured by dividing the gain by the output noise density, which is the ratio of output

voltage to the input capacitance. The gain of the capacitive-sensing mode is expressed by the following equation:

$$\text{Gain} = \frac{V_{DD}}{C_1}(\text{1st stage gain}) \times (\text{2nd stage gain}) = \frac{1.8\ \text{V}}{1.84\ \text{pF}} \times \frac{36.8\ \text{pF}}{0.23\ \text{pF}} = 156\ \text{mV/fF} \qquad (11)$$
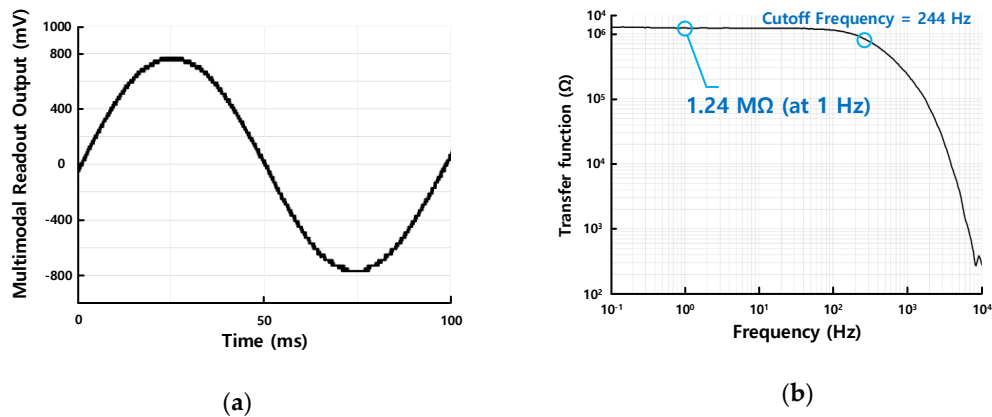

Figure 12. (**a**) Output in the current-sensing mode. (**b**) Transfer function of the current-sensing mode.
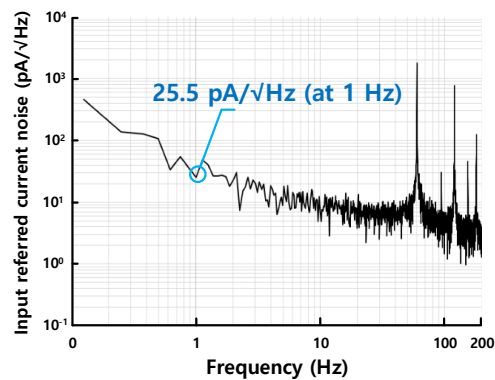

Figure 13. Measured input referred current noise in the current-sensing mode.

The gain could be adjusted from 250 mV/pF to 1250 mV/fF. The measured capacitance noise floor at 1 Hz was 0.142 aF/$\sqrt{\text{Hz}}$. The RMS capacitance noise floor was 0.313 aF$_{\text{rms}}$ over the bandwidth from 1 Hz to 200 Hz.
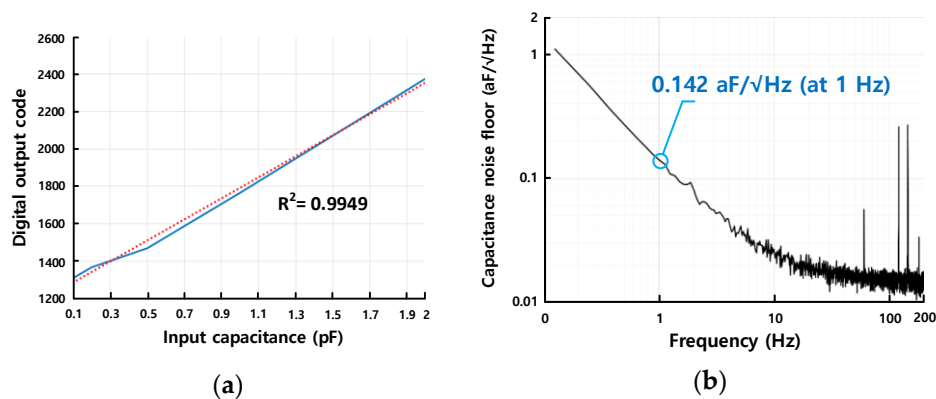

Figure 14. (**a**) Linearity expressed as the ratio of the digital output code to the input capacitance. (**b**) Capacitance noise floor.

In the capacitive-sensing-mode test, the capacitive DAC inside the chip was tuned to reduce the offset due to the parasitic capacitance. For the capacitive inputs, the difference due to the input parasitic capacitance had a value of 2.67 pF caused by the PCB and the capacitive sensor. After adjustment, the difference due to the input parasitic capacitance was 0.09 pF. The measured offset voltage of the capacitive-sensing mode after adjustment is shown in Figure 15.

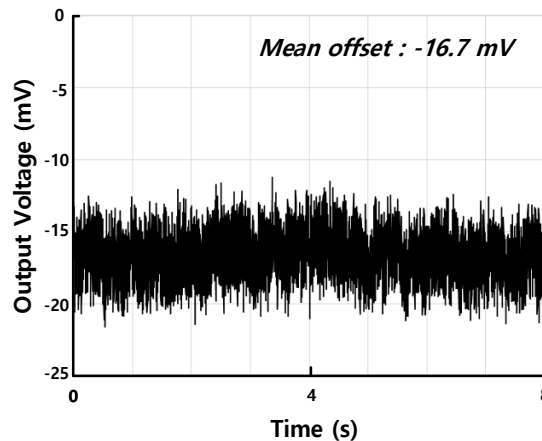The performance summary of proposed multimodal readout circuit is shown in Table 1.

Figure 15. The measured offset voltage of the capacitive-sensing mode after adjustment.

Table 1. Performance summary. CMOS: complementary metal-oxide semiconductor, UGBW: unit gain bandwidth.

Overall Performance of the Proposed Multimodal Readout Circuit						
Technology	**1P6M 0.18-μm CMOS Process**					
Supply Voltage	**1.8 V**					
Multimodal Readout Circuit					**Bias Block**	
Signal type	Voltage	Resistance	Current	Capacitance	Power	483.7 μW (sim)
					Low-Pass Filter	
Input range	70 mV (max)	0.4–400 Ω	1.65 μA (max)	±2 pF	Bandwidth	1 kHz (sim)
Total power	2.784 mW		2.552 mW	2.8 mW	Power	487.8 μW (sim)
Input noise (1–200 Hz)	5.25 μV$_{rms}$	2.9 mΩ$_{rms}$	742 pA$_{rms}$	0.313 aF$_{rms}$	**PGA**	
P$_{chop}$ P$_{cds}$	1 MHz (chopping frequency) 125 kHz (CDS frequency)				Gain Power	13.9–44 dB 608 μW (sim)
Multi-Path Operational Amplifier					**Clock Generator**	
Power UGBW Open loop gain	10.09 μW (sim) 4.81 MHz 98 dB				Power	138 μW (sim)
12-bit SAR ADC						
Power Sampling frequency	802.98 μW (sim) 1 MHz					

3.2. Measurement Results Using a Real Application

For a resistive/capacitive-sensing-mode test using a real application, a flexible bend sensor, which senses a bending force via a change of resistance and a capacitive *z*-axis accelerometer, were used. Each sensor specification is shown in Table 2.

Table 2. Sensor specification.

Flexible Bend Sensor		Capacitive Z-Axis Accelerometer	
Signal Type	R	Signal Type	C
Flat resistance	10 kΩ	Torque/g	2.03×10^{-10}
Resistance tolerance	±30%	Nominal capacitance	5.409 pF
		Δ C/g	0.125 pF/g
Bend resistance range	60–110 kΩ	Resolution	0.5 mg
		Δ degree/g	3.65×10^{-4} µm/g

The photography of sensors on the PCB are shown in Figure 16. The real-time measurement result using a flexible bend sensor and a z-axis accelerometer are shown in Figures 17 and 18, respectively. In Figure 17, in resistive-sensing mode, the resistive bridge sensor including a flexible bend sensor was applied. The resistive bridge sensor was constructed using three variable 10 kΩ resistors and a flexible bending sensor. Also, the gain of the readout circuit was adjusted to 26 dB. The degree of bending was adjusted in consideration of the bend resistance range of the sensor and the input resistance range of the designed readout circuit. The output amplitude of the readout circuit was measured up to 860 mV, which was approximately 400 Ω in terms of resistance.
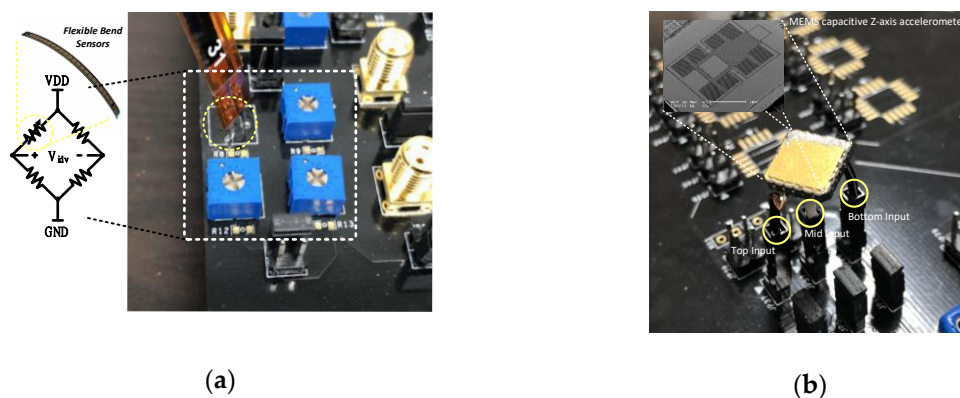

(**a**) (**b**)

Figure 16. (**a**) Photograph of the flexible bend sensor on a PCB. (**b**) Photograph of a z-axis accelerometer on a PCB.
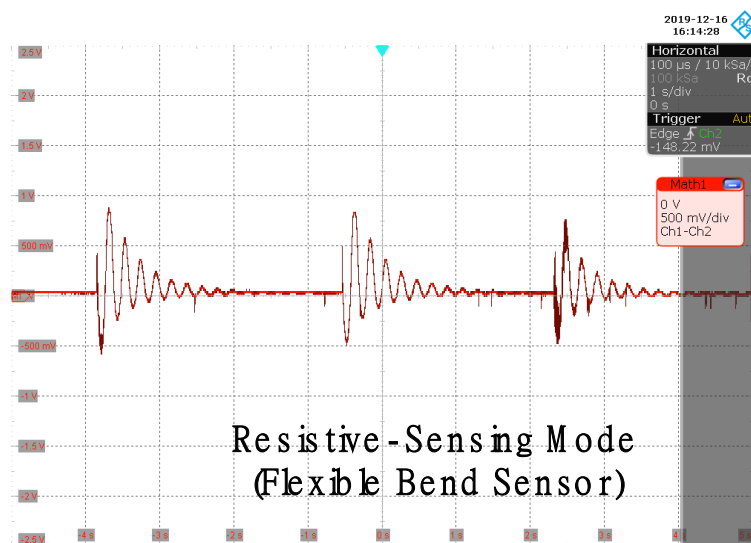

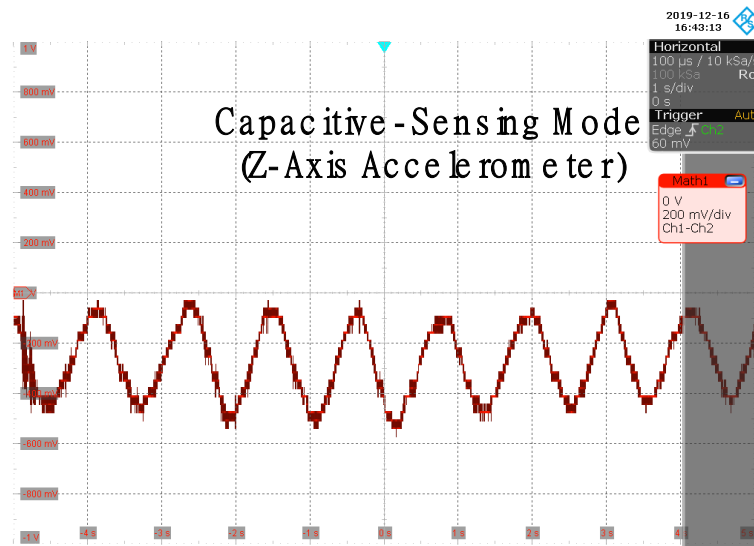**Figure 17.** The real-time measurement result using a flexible bend sensor.

Figure 18. The real-time measurement result using a capacitive z-axis accelerometer.

In Figure 18, in capacitive-sensing mode, the parasitic capacitance was reduced by using an 8-bit capacitive DAC inside the chip after considering the input parasitic capacitance inside the sensor. Also, the gain was adjusted to 4 mV/fF. The amplitude of the output of the readout was measured in the range of 400–450 mV, which was a variation of about from 0.1 pF to 0.12 pF. Considering the specification of the z-axis accelerometer sensor, the acceleration was about 0.8 g to 0.96 g.

The performance summary and comparison with references is shown in Table 3.

Table 3. Performance summary and comparison.

Parameter	This Work	Ref. [20]	Ref. [21]	Ref. [10]	Ref. [12]
Supply (V)	1.8	2.7	5	1.2	1.8
Technology (μm)	0.18	0.18	0.35	0.18	0.35
Power consumption (mW)	2.552	0.02765	189.3	0.058	0.942
Area (mm^2)	9.61	N/A	12.5	N/A	11.25
Signal type	V/I/R/C	R	C	V/R	V/I/R/C
Noise cancellation	Chopping, CDS	Chopping	CDS	Chopping	Chopping
Input noise	5.25 μV_{rms}	3.76 μV_{rms}	N/A	0.6 μV_{rms}	0.769 μV_{rms}
Resistance noise floor	2.9 $m\Omega_{rms}$	N/A	N/A	8.6 $m\Omega/\sqrt{Hz}$	N/A
Input current noise	742 pA_{rms}	N/A	N/A	N/A	N/A
Capacitance noise floor	0.313 aF_{rms}	N/A	0.41 aF_{rms}	N/A	N/A
Input range	V: 70 mV_{pp} R: 0.4–400 Ω I: 1.65 μA C: ±2 pF	V: 17.6 mV	C: ±2.9 pF	V: 30 mV_{pp} R: N/A	C: 10 pF

4. Conclusions

A low-noise multimodal reconfigurable sensor readout circuit for voltage/resistive/ current/capacitive microsensors has been presented. The proposed circuit has a reconfigurable structure that can provide a voltage/resistive-sensing mode, a current-sensing mode, or a capacitive-sensing mode. The reconfigurable characteristics of the proposed circuit can be applied in an environmental monitoring system using various sensors. A low noise and wide bandwidth were achieved by applying multiple DOC techniques, including chopper stabilization and the CDS technique. The chopper-stabilized, multipath operational amplifier with an AC-coupled RRL resolved the band-limiting issue and the ripple caused by the chopper. The measurement input noise values in the voltage/resistive/current/capacitive-sensing modes were 5.25 μV_{rms}, 2.9 $m\Omega_{rms}$, 742 pA_{rms}, and 0.313 aF_{rms}, respectively, from 1 Hz to 200 Hz. The proposed readout circuit was fabricated using

0.18-μm CMOS technology to fabricate a device with an active area of 9.61 mm^2. The total power consumption was 2.552 mW with a 1.8-V supply voltage.

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