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# DC Converter with Wide Soft Switching Operation, Wide Input Voltage and Low Current Ripple

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**Abstract:** A soft switching current-source resonant converter is presented and implemented for wide voltage applications such as fuel cells and solar power. An *LLC* (inductor–inductor–capacitor) converter is adopted to accomplish zero voltage (current) operation on active switches (diodes). Thus, the circuit efficiency is increased. The interleaved pulse-width modulation (PWM) converter is employed on the input side to accomplish low input ripple current. A hybrid *LLC* converter is adopted to achieve wide voltage operation from $V_{in,\,min}$ to $4V_{in,\,min}$ and to improve the weakness of a conventional *LLC* converter. Half-bridge diode rectification is employed on the output side to decrease power loss on the rectifier diode. To confirm the theoretical analysis and feasibility, experimental verifications with a 500-W prototype are demonstrated in this paper.

**Keywords:** DC converters; ZVS operation; variable frequency control; *LLC* converter

## 1. Introduction

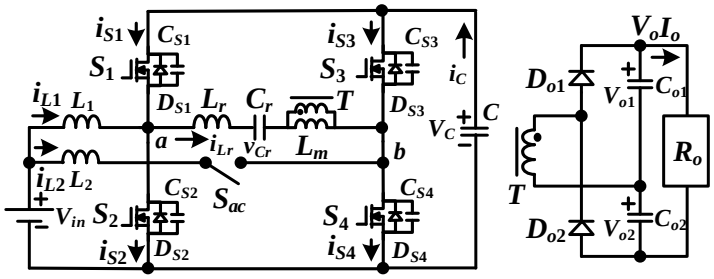
A fuel cell or solar cell is the clean renewable power energy to change chemical or photovoltaic energy to utility power by using a power electronic circuit, such as dc-dc or dc-ac power converters [1]. The output voltage of single solar cell stack is low and related to solar illuminance (or intensity). Therefore, the high-frequency-link power electronic converters with wide voltage operation are essentially demanded to produce an sTable 400 V on a dc bus between PV (photovoltaic)panels and ac (or dc) grids. However, the input voltage range of the conventional dc-dc converters or dc-ac converters for solar power conversion applications is limited. For dc-dc converters, the allowed maximum input voltage is less than three times of the minimum input voltage, i.e., $V_{in,\,max} < 3V_{in,\,min}$, due to the available duty cycle control. The high-frequency-link dc-dc converters have two types: current source converters [2,3] and voltage source converters [4,5]. Current source converters have less input current ripple compared to the voltage source converters. To increase converter efficiency, the zero-voltage switching dc-dc converters have developed to decrease the turn-on switching losses on power switches. Soft switching flyback with active clamped pulse-width modulation (PWM) [6] have been implemented for adaptor applications with low power rating. Asymmetric PWM converters have been studied in [7,8] to accomplish high-efficiency power converters. However, the problems of an asymmetric half-bridge converter are unbalance current rating on power switches and rectifier diodes. Full-bridge PWM converters have been presented and discussed in [9,10] for high-power applications and a wide range of zero-voltage switching operationa. However, the drawbacks of this circuit topology are the large circulating current on the primary side under freewheeling state and the serious switching losses at low load condition. To solve the above problems, *LLC* (inductor-inductor-capacitor) resonant converters have been implemented in [11–15] to accomplish soft switching operation over a wide load range. Half-bridge and full-bridge *LLC* converters are adopted for low and medium power application due to the fundamental ac input voltage of a half-bridge *LLC* converter is only one-half of a full-bridge

*LLC* converter. However, the input voltage operation of an *LLC* converter is limited. It is not easy for an *LLC* converter to be applied in fuel cells or solar power applications with wide input voltage variation.

A hybrid *LLC* circuit is proposed in this paper to implement wide voltage operation from $V_{in,\,min}$ to $4V_{in,\,min}$, zero-voltage switching for all power semiconductors and input current ripple-free. The interleaved PWM converter is used on the input side to realize current ripple reduction. The second-stage is a full-bridge (low voltage mode) or half-ridge (high voltage mode) *LLC* resonant circuit to realize wide input voltage capability and accomplish wide zero-voltage or zero-current switching operation on active devices or rectifier diodes. Due to the fundamental ac, the input voltage of the half-bridge *LLC* converter is only one-half of full-bridge *LLC* converter, half-bridge circuit topology is operated at a high input voltage range and full-bridge circuit topology is operated at a low input voltage range. The selection of a half-bridge or full-bridge converter is implemented with an additional switch to realize wide input voltage operation. The interleaved PWM circuits and full-bridge-type *LLC* converter share same power switches. Thus, the switch counts are reduced and the single-stage current source dc converter is implemented in the presented circuit. The voltage double rectification topology is adopted on the output side to decrease diode counts and voltage rating on diodes. Finally, experimental verifications based on a 500 W circuit are demonstrated to validate the performance of the studied single-stage dc-dc converter.

## 2. Circuit Diagram

The circuit configuration of the studied circuit is shown in Figure 1a with the abilities of wide voltage operation capability, wide zero-voltage switching load range and less input ripple current. In the presented circuit, $S_1$~$S_4$ are MOSFET devices, $S_{ac}$ is an ac switch. $L_r$ is resonant inductor, $C_r$ is resonant capacitor, $L_1$ and $L_2$ are input inductors, $T$ is the isolated transformer with the magnetizing inductance $L_m$, $D_{o1}$ and $D_{o2}$ are rectifier diodes, $C_{o1}$ and $C_{o2}$ are the output capacitors and $R_o$ is a load resistor. The circuits ($L_1$, $S_1$, $S_2$, $C$) and ($L_2$, $S_3$, $S_4$, $C$) are two boost converters. The gating signals of $S_2$ and $S_4$ are interleaved by half of switching cycle. Thus, the resultant input current ripple $\Delta i_{in}$ is reduced to zero. $S_1$~$S_4$ have the same duty cycle and equal to 0.5. Therefore, the boost voltage $V_C$ is equal to $2V_{in}$. In order to realize wide voltage input capability, there are two operated modes (Figure 1b,c) in the studied circuit. When input voltage is under a low input voltage mode $V_{in,\,min}$~$2V_{in,\,min}$, switch $S_{ac}$ is off, as shown in Figure 1b. Circuit components $C$, $S_1$~$S_4$, $C_r$, $L_r$, $T$, $D_{o1}$, $D_{o2}$, $C_{o1}$ and $C_{o2}$ are operated as a full-bridge structure *LLC* converter. The current ripple $\Delta i_{in}$ is equal to zero. When $2V_{in,\,min} < V_{in} < 4V_{in,\,min}$ (high voltage mode), active devices $S_{ac}$ and $S_3$ are turned off and $S_4$ is on (Figure 1c). Circuit components $C$, $S_1$, $S_2$, $S_4$, $C_r$, $L_r$, $T$, $D_{o1}$, $D_{o2}$, $C_{o1}$ and $C_{o2}$ are operated as a half-bridge structure *LLC* converter to obtain lower voltage gain. Therefore, a current-fed and wide input voltage *LLC* converter is achieved. Owing to resonant behavior of the *LLC* converter, power switches and rectifier diodes have soft switching operation capability.




(**a**)

**Figure 1.** *Cont.*

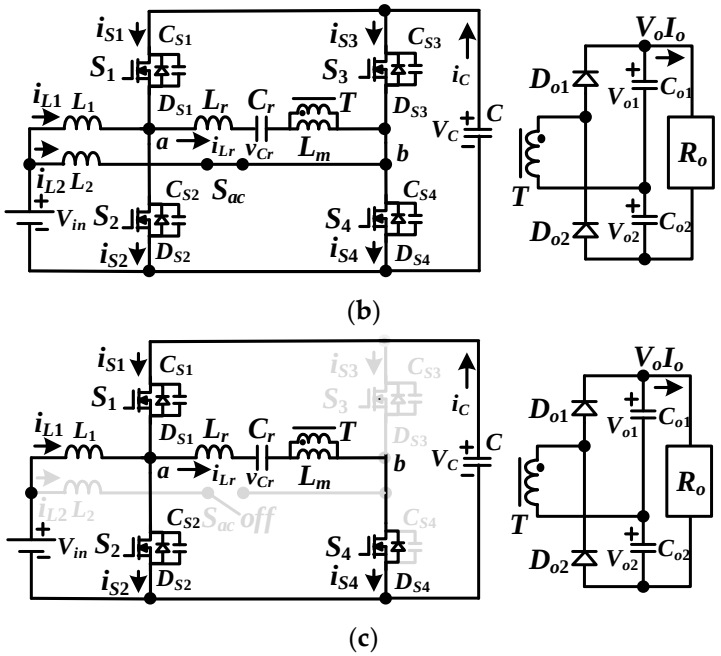



**Figure 1.** Proposed wide voltage range LLC (inductor–inductor–capacitor) converter with input current ripple-free (**a**) circuit diagram, (**b**) equivalent circuit under low input voltage mode, (**c**) equivalent circuit under high input voltage mode.

## 3. Principles of Operation

The variable switching frequency related to input voltage and load conditions is used to adjust load voltage. $S_{ac}$ is kept at on or off state according to the low ($V_{in,\,min}$~$2V_{in,\,min}$) or high ($2V_{in,\,min}$~$4V_{in,\,min}$) input voltage mode. Figures 2 and 3 illustrate the PWM signals for low and high input voltage modes. The studied *LLC* converter has six effective operating steps if the series resonant frequency ($f_r$) is greater than the switching frequency ($f_{sw}$). For low input voltage mode (Figure 1b), ac switch $S_{ac}$ is in the on-state. $L_1$, $L_2$, $S_1$~$S_4$ and $C$ are operated as two interleaved boost converters to accomplish input current ripple-free. The boost capacitor voltage $V_C = 2V_{in}$ due to the duty ratio $d_{S1} = d_{S2} = d_{S3} = d_{S4} = 0.5$. Components $S_1$~$S_4$, $L_r$, $C_r$, $T$, $D_{o1}$ and $D_{o2}$ are operated as a full-bridge structure *LLC* converter. Figure 2a gives the pulse-width modulation waveforms and Figure 2b–g show the circuits for six operating steps. Under the low input voltage mode, the voltage gain of the full-bridge structure *LLC* converter is $G_L = nV_o/V_{in,L}$, where $V_{in,L}$ denotes $V_{in,min} < V_{in} < 2V_{in,min}$ and $n$ denotes the transformer turns ratio.

**Step 1 [$t_0 \le t < t_1$]:** At $t_0$, $v_{CS2}$ and $v_{CS3}$ are decreased to zero voltage and $D_{S2}$ and $D_{S3}$ become on due to $i_{S2}(t_0) < 0$ and $i_{S3}(t_0) < 0$. Active semiconductors $S_2$ and $S_3$ are turned on after time $t_0$ to realize zero-voltage switching. The boost inductor voltages $V_{L1}$ equals $V_{in}$ and $V_{L2} = V_{in} - V_C \approx -V_{in}$. $i_{L1}$ is increasing and $i_{L2}$ is decreasing. Voltage $V_C$ connects to $L_r$, $C_r$ and $L_m$. Due to $D_{o2}$ is conducting, it can obtain $v_{Lm} = -nV_{o2} = -nV_o/2$. Components $C_r$ and $L_r$ are resonant with the resonant frequency $f_r = 1/2\pi\sqrt{L_rC_r}$.

**Step 2 [$t_1 \le t < t_2$]:** Because of $f_r > f_{sw}$, $i_{Lm}$ equals $i_{Lr}$ at time $t_1$. Therefore, $D_{o2}$ is reverse biased. $L_m$, $C_r$, $L_m$ and $L_r$ are resonant in step 2 with the other resonant frequency $f_p = 1/2\pi\sqrt{(L_m + L_r)C_r} < f_r$. $i_{L1}$ is still increasing and $i_{L2}$ is decreasing in step 2.

**Step 3 [$t_2 \le t < t_3$]:** At half of switching cycle ($t_2 = T_{sw}/2$), switches $S_2$ and $S_3$ turn off. Since $i_{L1}(t_2) - i_{Lr1}(t_2)$ is greater than zero current and $i_{Lr1}(t_2) + i_{L2}(t_2)$ is less than zero current, capacitors $C_{S1}$ and $C_{S4}$ will be discharged at time $t_2$. After time $t_2$, $i_{Lr} > i_{Lm}$, $D_{o1}$ is forward biased and $v_{Lm} = nV_{o1} = nV_o/2$.

**Step 4 [$t_3 \le t < t_4$]:** At $t_3$, the voltages $v_{CS1}$ and $v_{CS4}$ are decreased to zero voltage. Owing to the fact that $i_{S1}(t_3)$ and $i_{S4}(t_3)$ are both less than zero, $D_{S1}$ and $D_{S4}$ become on. After $t_3$, $S_1$ and $S_4$ turn on with

zero-voltage switching. In this step, $i_{Lr} > i_{Lm}$ so that $D_{o1}$ conducts and $v_{Lm} = nV_o/2$. $L_r$ and $C_r$ are resonant with resonant frequency $f_r$ in this step. Inductor voltages $v_{L1} = V_{in} - V_C \approx -V_{in}$ and $v_{L2} = V_{in}$. Thus, $i_{L1}$ and $i_{L2}$ are decreasing and increasing.

**Step 5 [$t_4 \le t < t_5$]:** Owing to $f_{sw} < f_r$, $i_{Lm}$ equals $i_{Lr}$ at time $t_4$ so that $D_{o1}$ is reverse biased. $i_{L1}$ and $i_{L2}$ decrease and increase, respectively.

**Step 6 [$t_5 \le t < T_{sw}+ t_0$]:** $S_1$ and $S_4$ turn off at $t_5$. Since $i_{Lr}(t_5) - i_{L1}(t_5) > 0$ and $i_{Lr}(t_5) + i_{L2}(t_5) > 0$, the capacitors $C_{S2}$ and $C_{S3}$ discharge at time $t > t_5$. Since $i_{Lr} < i_{Lm}$, $D_{o2}$ is forward biased and $v_{Lm} = -nV_o/2$. Step 6 ends at $t = T_{sw} + t_0$ and $v_{CS2} = v_{CS3} = 0$.

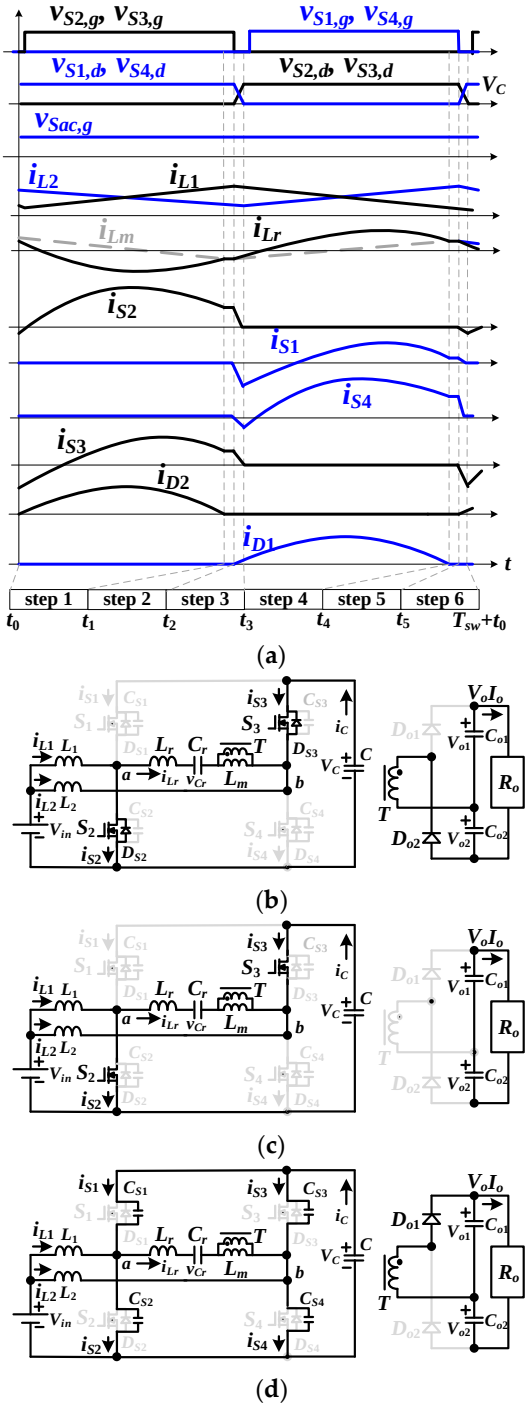



**Figure 2.** *Cont.*

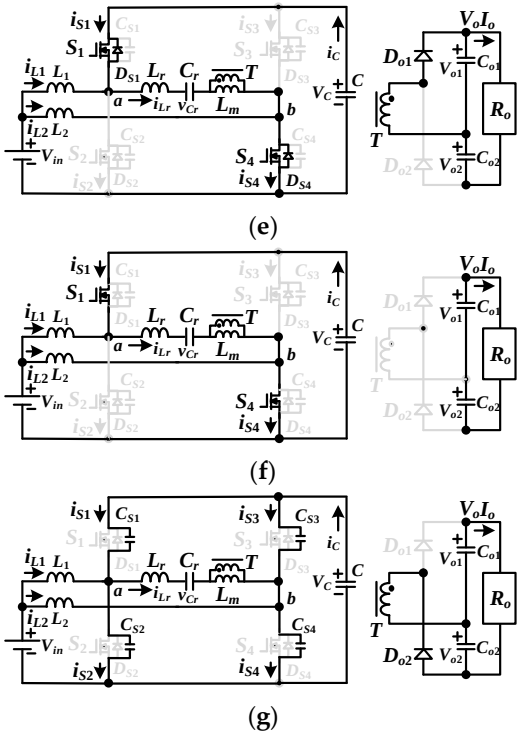



**Figure 2.** Converter operated at low input voltage mode (**a**) main pulse-width modulation (PWM) signals, (**b**) step 1, (**c**) step 2, (**d**) step 3, (**e**) step 4, (**f**) step 5, (**g**) step 6.

For high input voltage mode (Figure 1c), $S_{ac}$ and $S_3$ are off and $S_4$ is on. Only active devices $S_1$ and $S_2$ are gated to adjust load voltage. Therefore, only one boost converter by $L_1$, $S_1$, $S_2$ and $C$ and the half-bridge structure $LLC$ resonant converter by $C$, $S_1$, $S_2$, $L_r$, $C_r$, $T$ and $S_4$ are used to realize zero-voltage turn-on. In high input voltage mode, the $LLC$ converter has voltage gain $G_H = 2nV_o/V_{in,H}$, where $V_{in,H}$ denotes $2V_{in,min} < V_{in} < 4V_{in,min}$. Based on the dc voltage gains $G_L = nV_o/V_{in,L}$ (low input voltage mode) and $G_H = 2nV_o/V_{in,H}$ (high input voltage mode), it can obtain $G_H = G_L$ due to $V_{in,H} = 2V_{in,L}$. It means the proposed converter has the same circuit characteristics under low and high input voltage modes. Figure 3a gives the PWM signals and Figure 3b–g show the circuits for six operating steps.

**Step 1 [$t_0 \le t < t_1$]:** $v_{CS2} = 0$ at $t_0$. Owing to $i_{Lr}(t_0) - i_{L1}(t_0) < 0$, $D_{S2}$ is forward bias and $S_2$ turns on after $t > t_0$ to accomplish zero-voltage switching. $i_{L1}$ increases and $C_r$ and $L_r$ are resonant and $v_{Lm} = -nV_o/2$.

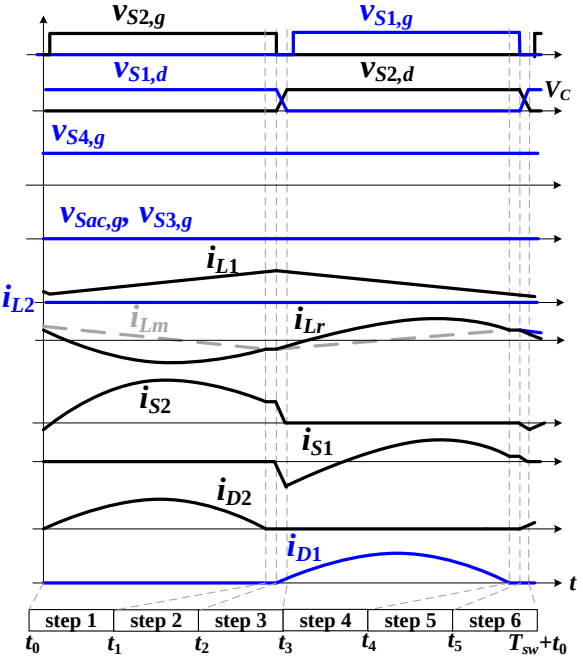
**Step 2 [$t_1 \le t < t_2$]:** $D_{o2}$ is reverse biased owing to $i_{Lr} = i_{Lm}$ at time $t_1$. Thus, $L_m$, $C_r$ and $L_r$ are resonant and $i_{L1}$ increases due to $V_{L1} = V_{in}$.

**Step 3 [t2 ≤ t < t3]:** Active device S2 is turned off at t = t2. Due to iL1(t2) − iLr(t2) > 0 and iLr(t2) > iLm(t2), CS1 will be discharged and Do1 becomes on.

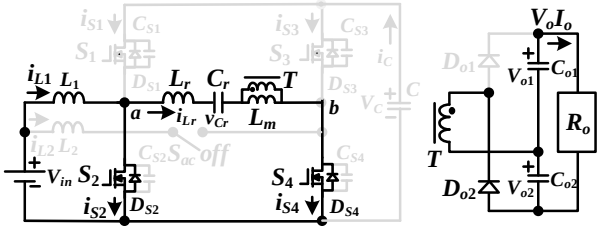
**Step 4 [$t_3 \le t < t_4$]:** $v_{CS1} = 0$ at time $t_3$. Owing to $i_{L1}(t_3) > i_{Lr}(t_3)$, the body diode $D_{S1}$ becomes on and $S_1$ can be turned on after $t > t_3$ to achieve soft switching turn-on. $i_{L1}$ is decreasing in step 4 and $D_{o1}$ conducts such that $v_{Lm} = nV_o/2$.

**Step 5 [$t_4 \le t < t_5$]:** At time $t_4$, $i_{Lm}$ equals $i_{Lr}$ and $D_{o1}$ becomes off. $L_m$, $C_r$ and $L_r$ are resonant and $i_{L1}$ decreases due to $V_{L1} = V_{in} - V_C < 0$.

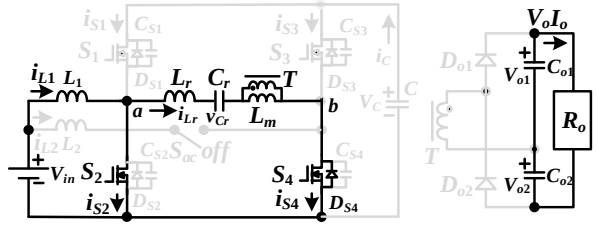
**Step 6 [$t_5 \le t < T_{sw} + t_0$]:** Switch $S_1$ turns off at time $t_5$. Since $i_{Lr}$ is less than $i_{Lm}$ and $i_{L1}$ is less than $i_{Lr}(t_5)$, diode $D_{o2}$ conducts and $C_{S2}$ is discharged. When the voltage of $C_{S2}$ is decreased to zero voltage at time $T_{sw} + t_0$.




(a)




(b)

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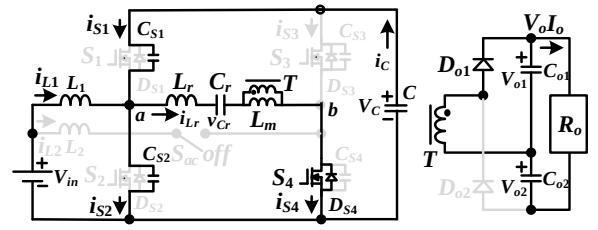
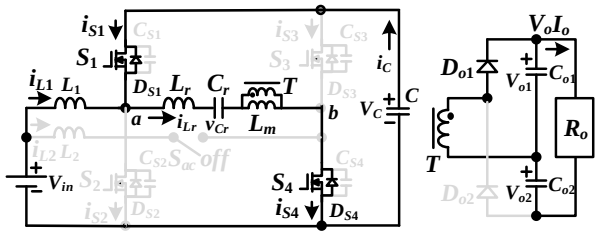



(d)




(e)

**Figure 3.** *Cont.*

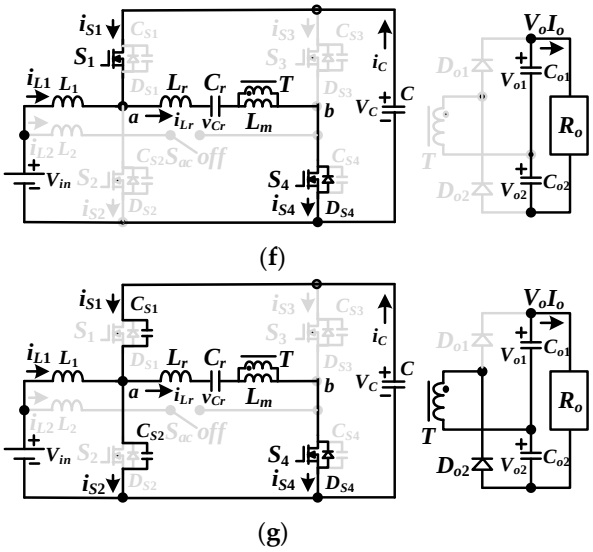



**Figure 3.** Converter operated at high input voltage mode (**a**) main PWM signals, (**b**) step 1, (**c**) step 2, (**d**) step 3, (**e**) step 4, (**f**) step 5, (**g**) step 6.

## 4. Circuit Analysis

For low input voltage mode ($V_{in} = V_{in,\,min}$~$2V_{in,\,min}$), two boost converters and one full-bridge structure *LLC* converter is used to reduce input ripple current and obtain soft switching turn-on operation. However, only one boost converter and a half-bridge structure *LLC* converter are adopted for high input voltage mode ($V_{in} = 2V_{in,\,min}$~$4V_{in,\,min}$). According to voltage-second balance on $L_1$ and $L_2$, the output voltage $V_C$ of the boost converter is obtained in Equation (1).

$$V_C = V_{in}/(1-d) = V_{in}/(1-0.5) = 2V_{in} \tag{1}$$

where $d = 0.5$ for $S_1$~$S_4$ under low voltage mode and for $S_1$ and $S_2$ under high voltage mode. Since the PWM signals of $S_1$ and $S_2$ are phase shifted with respective to the signals of $S_3$ and $S_4$ by half switching cycle, the inductor current ripples $\Delta i_{L1}$ and $\Delta i_{L2}$ can be eliminated by each other. Therefore, the resultant input current ripple $\Delta i_{in} = \Delta i_{L1} + \Delta i_{L2}$ is reduced to zero. The voltage rating on $S_1$~$S_4$ is equal to the boost voltage $V_C$ (=$2V_{in}$).

The frequency control scheme [16] is adopted to analysis the circuit features and voltage gain of the adopted *LLC* converter. To implement wide input voltage operation, two operating modes (low and high input voltage modes) are operated. The magnetizing inductor voltage at fundamental frequency is derived in (2).

$$V_{Lm,rms} = \sqrt{2}nV_o/\pi \tag{2}$$

Based on the full-bridge *LLC* converter (low voltage mode) and the half-bridge *LLC* converter (high voltage mode), the input voltage of the resonant converter at fundamental frequency $V_{ab,\,rms}$ is derived in (3).

$$V_{ab,rms} = \begin{cases} 2\sqrt{2}V_C/\pi = 4\sqrt{2}V_{in,L}/\pi, S_{ac}\ on \\ \sqrt{2}V_C/\pi = 2\sqrt{2}V_{in,H}/\pi,\ S_{ac}, S_3 : off, S_4 : on \end{cases} \tag{3}$$

The primary-side resistance of transformer $T$ at fundamental switching frequency is derived in Equation (4).

$$R_{ac} = \frac{v_{Lm,rms}}{i_{s,T}/n} = \frac{2n^2}{\pi^2}R_o \tag{4}$$

The voltage gain of the equivalent resonant tank ($C_r$, $L_r$, $L_m$ and $R_{ac}$) is derived in Equation (5).

$$|G| = \frac{V_{Lm,rms}}{V_{ab,rms}} = \left|\frac{\frac{R_{ac}\times j\omega_{sw}L_m}{R_{ac}+j\omega_{sw}L_m}}{j\omega_{sw}L_r+\frac{1}{j\omega_{sw}C_r}+\frac{R_{ac}\times j\omega_{sw}L_m}{R_{ac}+j\omega_{sw}L_m}}\right| = \frac{1}{\sqrt{\left[1+\frac{1}{L_n}\left(1-\frac{1}{F^2}\right)\right]^2+Q^2\left(F-\frac{1}{F}\right)^2}} = \begin{cases} \frac{nV_o}{4V_{in,L}}, S_{ac}: on \\ \frac{nV_o}{2V_{in,H}}, S_{ac}, S_3: off,\ S_4: on \end{cases} \quad (5)$$

where $Q = \sqrt{L_r/C_r}/R_{ac}$, $L_n = L_m/L_r$ and $F = f_{sw}/f_r$. The gain curves of $|G|$ related to $F$ and $Q$ are shown in Figure 4 for the adopted prototype circuit. From Equation (5), the output voltage $V_o$ can be obtained and expressed in Equation (6).

$$V_o = \begin{cases} \frac{4V_{in,L}}{n\sqrt{\left[1+\frac{1}{L_n}\left(1-\frac{1}{F^2}\right)\right]^2+Q^2\left(F-\frac{1}{F}\right)^2}}, S_{ac}: on \\ \frac{2V_{in,H}}{n\sqrt{\left[1+\frac{1}{L_n}\left(1-\frac{1}{F^2}\right)\right]^2+Q^2\left(F-\frac{1}{F}\right)^2}}, S_{ac}, S_3: off,\ S_4: on \end{cases} \quad (6)$$

It is clear that the output voltage is related to the frequency ration $F$, quality factor $Q$ and inductor ratio $L_n$. If $F$ equals unity, $V_o$ is independent to $l_n$ and $Q$. Owing to the fact that $V_{in,H}$ is designed as two times of $V_{in,L}$, two output voltage equations in (5) are identical. Therefore, the voltage gains $V_{Lm,rms}/V_{ab,rms}$ of the half-bridge and half-bridge *LLC* converter in the developed circuit are identical. As a result of this, the *LLC* resonant converter is operated at inductive load impedance (negative slope of voltage gain curve). Thus, all active semiconductors $S_1$~$S_4$ can be turned on at zero-voltage condition.

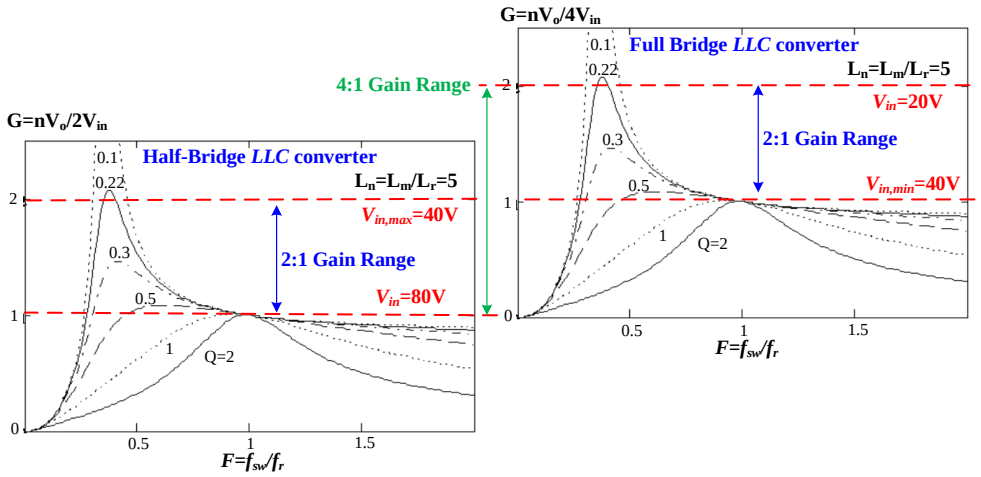



**Figure 4.** Gain curves of presented converter at $V_{in}$ = 20~80 V.

## 5. Design Steps and Experimental Verifications

The proposed circuit was created and experimented in a laboratory prototype with $V_{in}$ = 20~80 V (4:1 ratio), $V_o$ = 400 V, series resonant frequency $f_r$ = 100 kHz and the maximum output power $P_o$ = 500 W. Two boost circuits with interleaved PWM are employed on the input side to achieve a ripple-free input current. For low input voltage mode, the input voltage range $V_{in}$ is between 20 and 40 V. The full-bridge-type *LLC* converter is operated to control load voltage. When input voltage $V_{in}$ = 40 V~80 V, the proposed circuit is worked under the high voltage mode with the half-bridge-type *LLC* converter. Since the duty cycle $d_{S1} = d_{S2} = d_{S3} = d_{S4} = 0.5$, the inductances $L_1$ and $L_2$ are obtained in Equation (7) with the defined inductor ripple currents $\Delta i_{L1} = \Delta i_{L2}$ = 4 A at resonant frequency $f_{sw}$ = 100 kHz.

$$L_1 = L_2 = \frac{V_{in,\min}T_{sw}}{2\Delta i_{L1}} = \frac{80\times10^{-5}}{2\times4} \approx 100\mu H \quad (7)$$

To design the resonant converter, the inductor ratio $L_n$ = 5 is adopted at maximum power under the full-bridge converter. The curves of voltage gain at the presented converter are demonstrated in Figure 4 with the normalized gain $G_n = nV_o/4V_{in}$. The transient voltage between high and low input voltage modes is set at 40 V. The voltage comparator (schmitt trigger circuit) with ±2 V voltage tolerance is used at 40 V to achieve transient voltage detector. Therefore, the input voltage range at low voltage mode operation is from 20 to 42 V. Similarly, the input voltage range at high voltage mode operation is from 38 to 80 V. The transfer function of voltage gain $G$ for each voltage mode is expressed in (5). Since the input voltage range at high voltage mode is two times the input voltage range at low voltage mode $V_{in,H} = 2V_{in,L}$, it can obtain that voltage gain $G_H$ at high voltage mode is identical to the voltage gain $G_L$ at low voltage mode. Hence, the circuit design for two input voltage modes are identical. The full-bridge *LLC* converter is operated for low input voltage mode. $S_1$~$S_4$ are controlled to make $V_o$ = 400 V. It is assumed that the voltage gain at 40 V input is unity. The necessary turn ratio $n$ is calculated in Equation (8).

$$n = \frac{4GV_{in,L}}{V_o} = \frac{4 \times 1 \times 40}{400} = 0.4 \tag{8}$$

TDK (Tokyo Denki Kagaku) EER 42 core is used to implement transformer $T$ with $N_p$ = 14 and $N_s$ = 35. The maximum and minimum voltage gain under low voltage mode operation are expressed in Equations (9) and (10).

$$G_{\max} = \frac{nV_o}{4V_{in,L,\min}} = \frac{0.4 \times 400}{4 \times 20} = 2 \tag{9}$$

$$G_{\min} = \frac{nV_o}{4V_{in,L,\max}} = \frac{0.4 \times 400}{4 \times 42} \approx 0.95 \tag{10}$$

The fundamental resistance $R_{ac}$ in (4) is calculated as:

$$R_{ac} = \frac{2n^2}{\pi^2} R_o \approx 10.38\Omega \tag{11}$$

Based on voltage gain in Figure 4, the load voltage $V_o$ is controlled well under $Q < 0.22$. The circuit parameters $L_r$, $L_m$ and $C_r$ are obtained in (12)–(14) according to the selected values $f_r$ = 100 kHz, $L_n$ = 5 and $Q$ = 0.2.

$$L_r = \frac{QR_{ac}}{2\pi f_r} = \frac{0.2 \times 10.38}{2\pi \times 100,000} \approx 3.3\mu H \tag{12}$$

$$L_m = L_n L_r = 5 \times 3.3 = 16.5\mu H \tag{13}$$

$$C_r = \frac{1}{4\pi^2 L_r f_r^2} = \frac{1}{4\pi^2 \times 3.3 \times 10^{-6} \times (100,000)^2} \approx 768nF \tag{14}$$

Owing to the fact that voltage double rectifier topology is used on the output side, the voltage ratings of switches and diodes are obtained in Equations (15)–(17).

$$V_{S1,stress} = V_{S4,stress} = V_{C,\max} = 160V \tag{15}$$

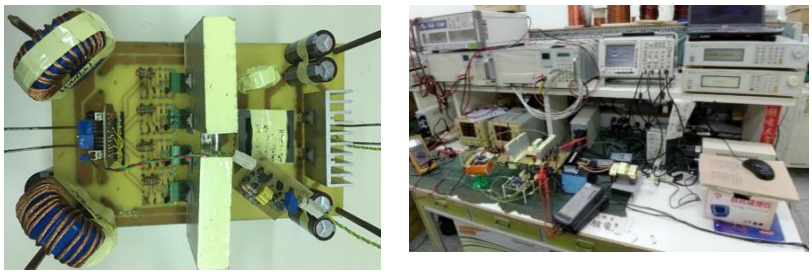
$$V_{Sac,stress} = V_{in,\max} = 80V \tag{16}$$

$$V_{D1,stress} = V_{D2,stress} = V_o = 400V \tag{17}$$

The selected output split capacitances are $C_{o1}$ = $C_{o2}$ = 300 μF and the dc bus capacitance $C$ = 2000 μF. Power MOSFETs n-channel IRFB4229 (250 V/46 A) are selected for switches $S_1$~$S_4$ and $S_{ac}$. Diodes BYC8-600 (600 V/8 A) are used for rectifier diodes $D_{o1}$ and $D_{o2}$. The frequency modulation is implemented by an integrated circuit UCC25600. The input voltage mode detection is implemented by using schmitt trigger comparator.

Figure 5 shows the photograph and the experimental setup of the prototype circuit. Figures 6–9 demonstrates the measured waveforms at low input voltage mode operation. Figures 6 and 7

demonstrate the test results at 20 V input voltage condition. Under low voltage mode operation, the switch $S_{ac}$ is turned on and the full-bridge-type *LLC* converter is worked to obtain high voltage gain. Two input boost converters are interleaved operation to achieve ripple-free input current. Figure 6a illustrates the gating signals of full bridge converter. Figure 6b provides the test results of $i_{L1}$, $i_{L2}$ and $i_{in}$. It can observe that the current ripples $\Delta i_{L1}$ and$\Delta i_{L2}$ cancelled each other. Thus, the input current ripple $\Delta i_{in}$ is close to zero. Figure 6c shows the measured results of resonant current $i_{Lr}$, resonant voltage $v_{Cr}$ and the dc bus current $i_C$. Since the switching frequency at 20 V input is less than the resonant frequency, the measured resonant current $i_{Lr}$ is a quasi-sinusoidal waveform. Figure 6d provides the diode currents and output capacitor voltages. It is clear that $D_{o1}$ and $D_{o2}$ are turned off at zero-current switching and $V_{o1} = V_{o2} = 200$ V. Figure 7a,b provides the test results of active device $S_1$ at 20% and 100% rated power, respectively. In the same way, the experimental results of active device $S_2$ at 20% and 100% rated power are demonstrated in Figure 7c,d. It can see that $S_1$ and $S_2$ turn on at zero voltage from 20% rated power. Figures 8 and 9 demonstrate the experimental results at 39 V input condition. Two input boost current ripples are cancelled so that the resultant input current ripple $\Delta i_{in} \approx 0$ as shown in Figure 8b. Since the switching frequency at 39 V input condition is very close to resonant frequency, the current $i_{Lr}$ is a sinusoidal waveform as shown in Figure 8c and diodes $D_{o1}$ and $D_{o2}$ turn off at zero current switching (Figure 8d). The voltages $V_{o1}$ and $V_{o2}$ are balanced each other and $V_{o1} = V_{o2} = 200$ V. Figure 9 shows the experimental waveforms of the switches $S_1$ and $S_2$ at 39 V of input and 20% and 100% load conditions. It is clear that $S_1$ and $S_2$ all turn on at zero-voltage switching from 20% rated power. Figures 10–13 provide the measured waveforms at high input voltage mode operation ($V_{in}$ = 40 V~80 V). Under the high input voltage mode, $S_{ac}$ and $S_3$ are off and $S_4$ is on. Figures 10 and 11 illustrate the experimental results at $V_{in}$ = 41 V input condition. At 41 V input condition, the resonant frequency is greater than the switching frequency. Figure 10a demonstrates the test waveforms of $v_{Cr}$, $i_{Lr}$, $v_{S1,g}$ and $v_{S2,g}$ at the rated power. Figure 10b gives the test results of $i_{L1}$, $i_{S1}$, $i_{S2}$ and $-i_{Lr}$. The experimental waveforms $i_{Do1}$, $i_{Do2}$, $V_{o1}$ and $V_{o2}$ are provided in Figure 10c. Diodes $D_{o1}$ and $D_{o2}$ are turned off at zero current. The test results of $S_1$ and $S_2$ at 20% and the rated power are provided in Figure 11. It is clear that $S_1$ and $S_2$ turn on at zero-voltage voltage from 20% rated power. Similarly, the test waveforms at 80 V input case are shown in Figures 12 and 13. The resonant current $i_{Lr}$ (Figure 12a is a sinusoidal waveform and $D_{o1}$ and $D_{o2}$ (Figure 12c) turn off at zero-current switching. From the measured results in Figure 13, both switches $S_1$ and $S_2$ can achieve soft switching operation from 20% rated power.



(**a**) (**b**)

**Figure 5.** Pictures of the proposed converter, (**a**) prototype circuit, (**b**) experimental setup.

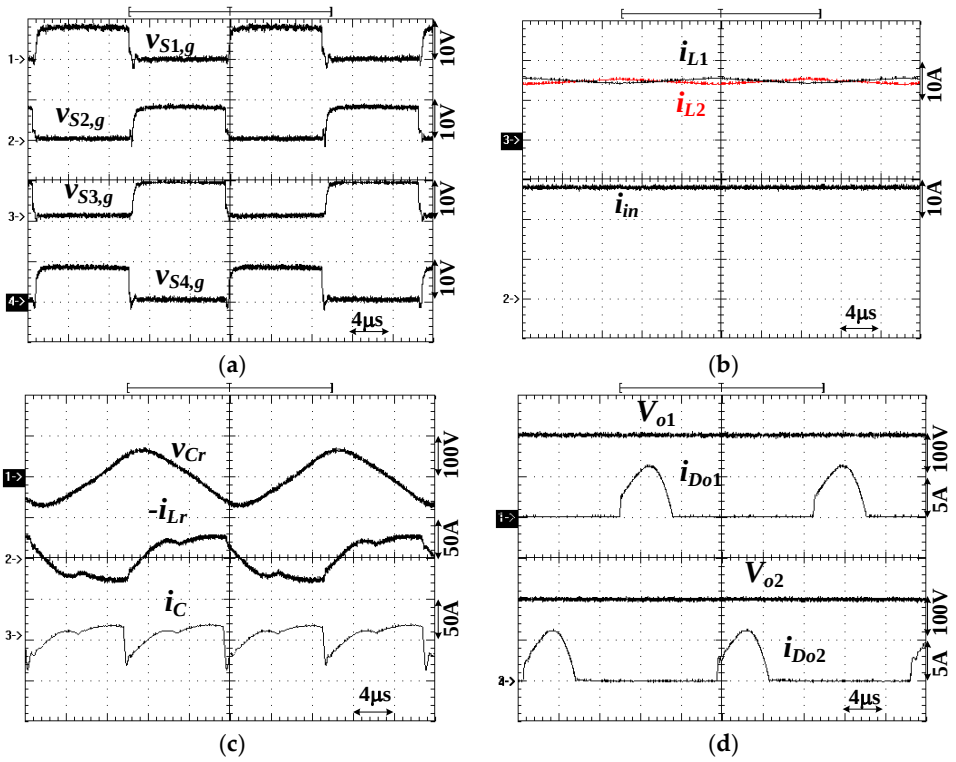



**Figure 6.** Test waveforms at $V_{in}$ = 20 V and rated power: (**a**) $v_{S1,g}$~$v_{S4,g}$; (**b**) $i_{L1}$, $i_{L2}$, $i_{in}$; (**c**) $v_{Cr}$, $-i_{Lr}$, $i_C$; (**d**) $i_{Do1}$, $i_{Do2}$, $V_{o1}$, $V_{o2}$.

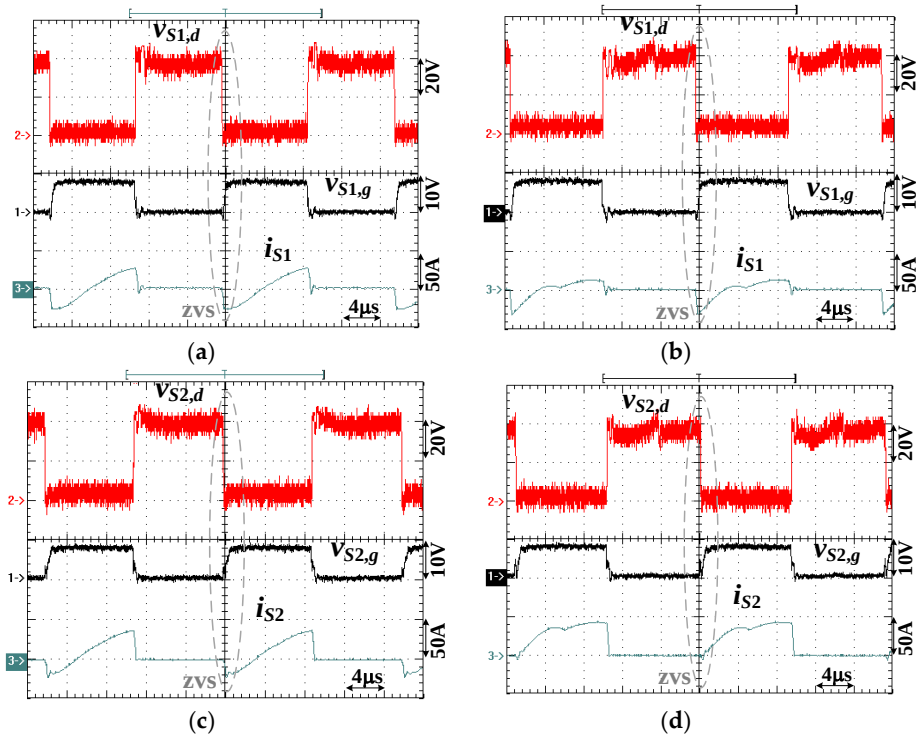



**Figure 7.** Experimental results of power switches $S_1$ and $S_2$ under low voltage mode operation and $V_{in}$ = 20 V: (**a**) $v_{S1,g}$, $v_{S1,d}$, $i_{S1}$ at 20% rated power; (**b**) $v_{S1,g}$, $v_{S1,d}$, $i_{S1}$ at 100% power; (**c**) $v_{S2,g}$, $v_{S2,d}$, $i_{S2}$ at 20% rated power; (**d**) $v_{S2,g}$, $v_{S2,d}$, $i_{S2}$ at 100% power.

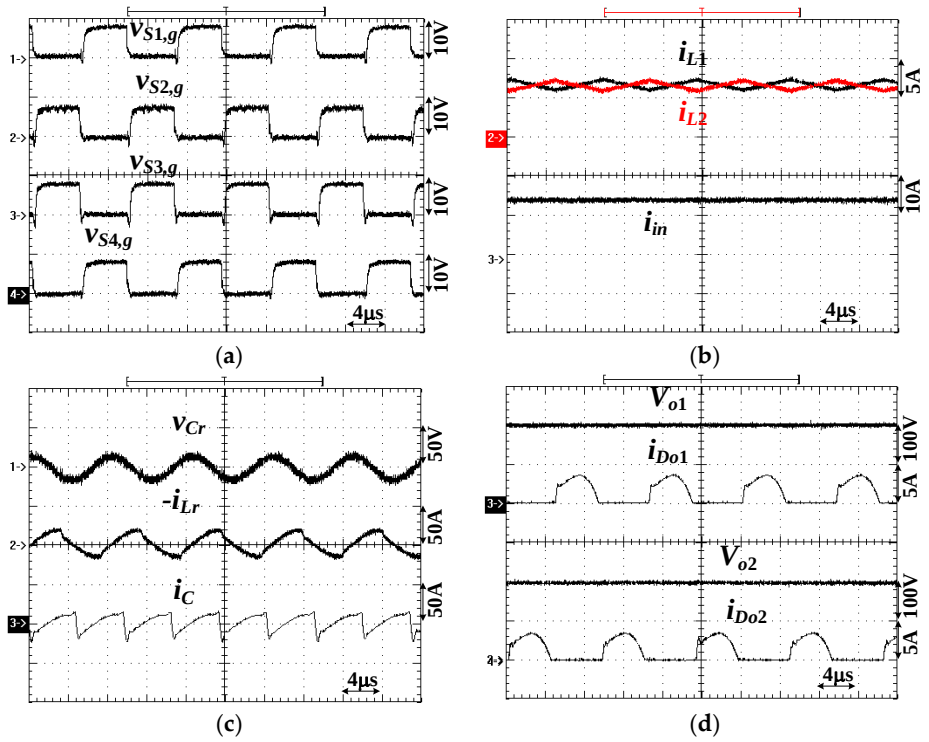



**Figure 8.** Test waveforms at $V_{in}$ = 39 V and rated power: (**a**) $v_{S1,g}$~$v_{S4,g}$; (**b**) $i_{L1}$, $i_{L2}$, $i_{in}$; (**c**) $v_{Cr}$, $-i_{Lr}$, $i_C$; (**d**) $i_{Do1}$, $i_{Do2}$, $V_{o1}$, $V_{o2}$.

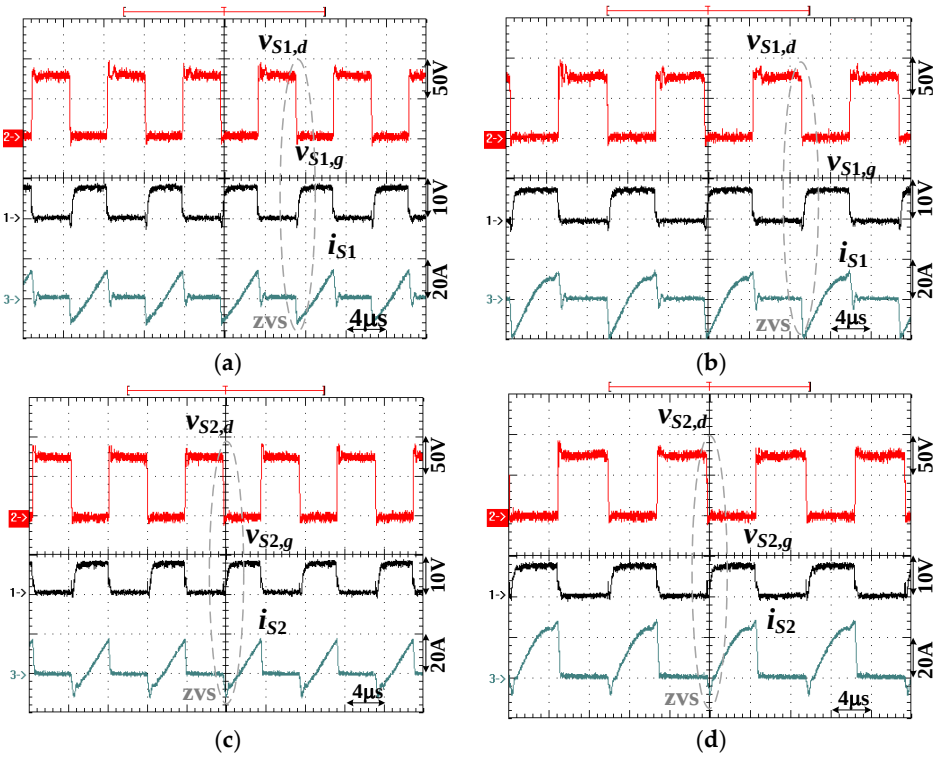



**Figure 9.** Experimental results of power switches $S_1$ and $S_2$ under low voltage mode operation and $V_{in}$ = 39 V: (**a**) $v_{S1,g}$, $v_{S1,d}$, $i_{S1}$ at 20% rated power; (**b**) $v_{S1,g}$, $v_{S1,d}$, $i_{S1}$ at 100% power; (**c**) $v_{S2,g}$, $v_{S2,d}$, $i_{S2}$ at 20% rated power; (**d**) $v_{S2,g}$, $v_{S2,d}$, $i_{S2}$ at 100% power.

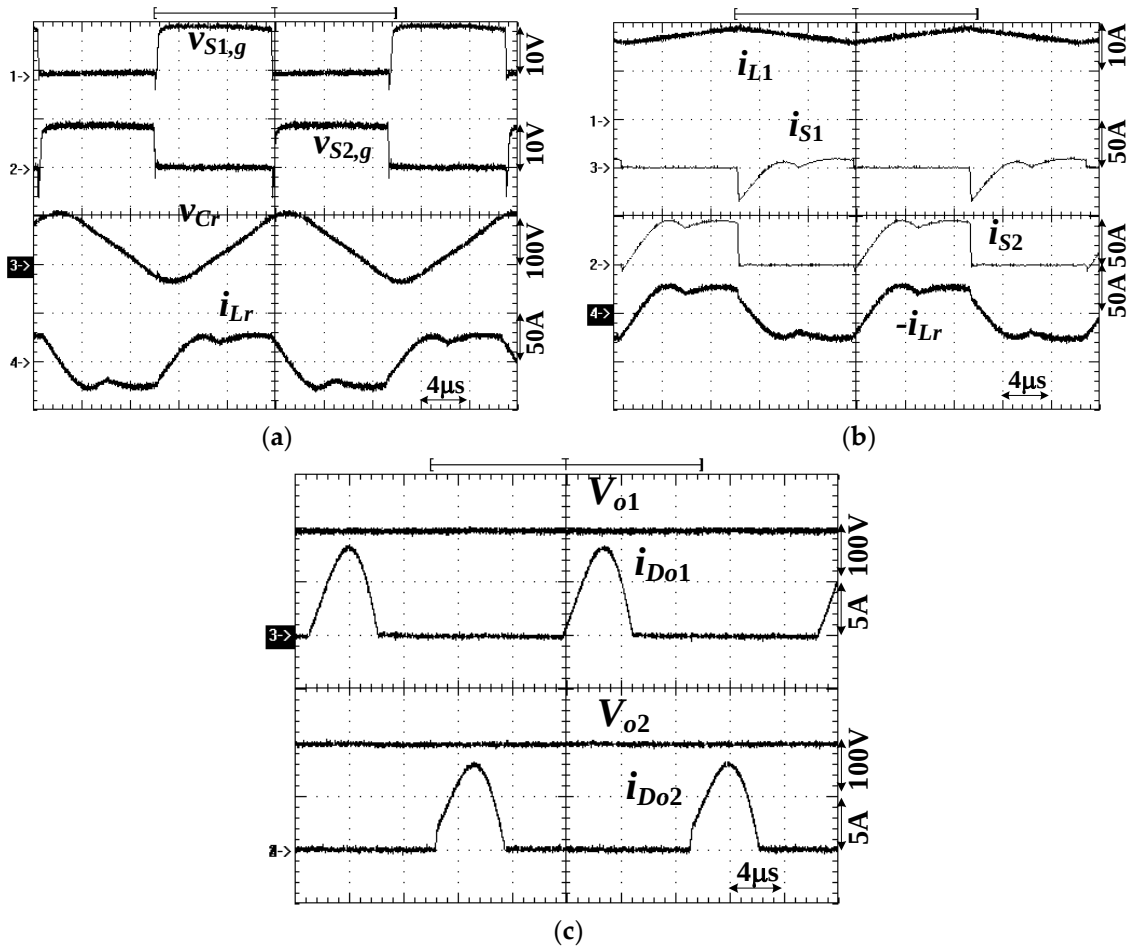



**Figure 10.** Test waveforms at $V_{in}$ = 41 V and rated power: (**a**) $v_{S1,g}$, $v_{S2,g}$, $v_{Cr}$, $i_{Lr}$; (**b**) $i_{L1}$, $i_{S1}$, $i_{S2}$, $-i_{Cr}$; (**c**) $i_{Do1}$, $i_{Do2}$, $V_{o1}$, $V_{o2}$.

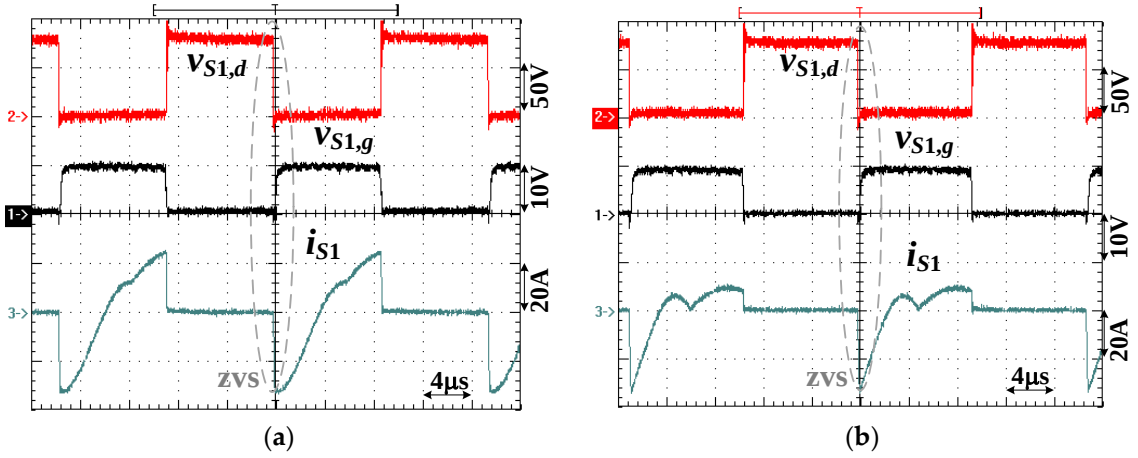



**Figure 11.** *Cont.*

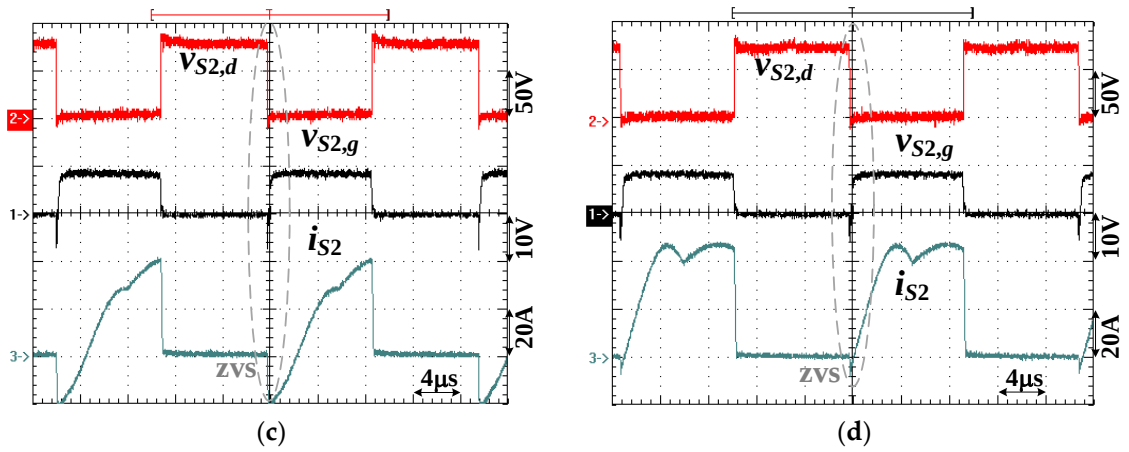



**Figure 11.** Experimental results of power switches $S_1$ and $S_2$ under high voltage mode operation and $V_{in}$ = 41 V: (**a**) $v_{S1,g}$, $v_{S1,d}$, $i_{S1}$ at 20% rated power; (**b**) $v_{S1,g}$, $v_{S1,d}$, $i_{S1}$ at 100% power; (**c**) $v_{S2,g}$, $v_{S2,d}$, $i_{S2}$ at 20% rated power; (**d**) $v_{S2,g}$, $v_{S2,d}$, $i_{S2}$ at 100% power.

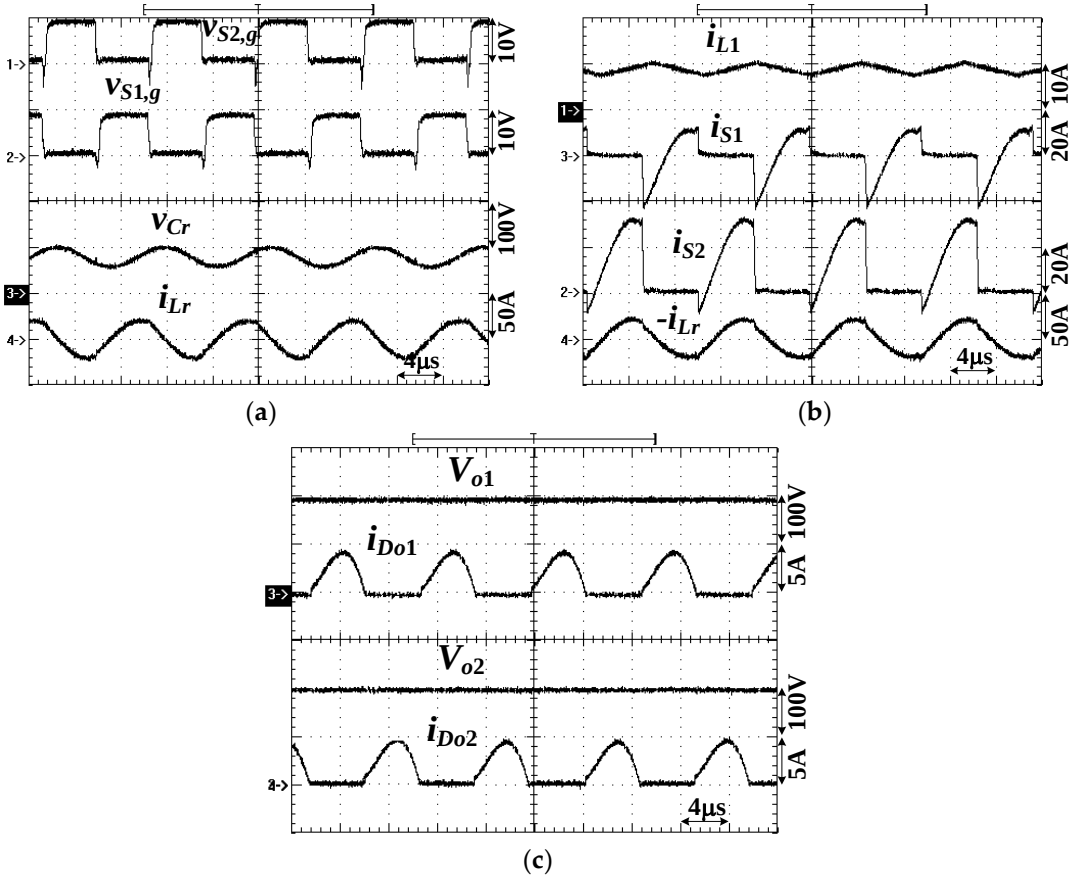



**Figure 12.** Test waveforms at $V_{in}$ = 80 V and rated power: (**a**) $v_{S1,g}$, $v_{S2,g}$, $v_{Cr}$, $i_{Lr}$; (**b**) $i_{L1}$, $i_{S1}$, $i_{S2}$, $-i_{Cr}$; (**c**) $i_{Do1}$, $i_{Do2}$, $V_{o1}$, $V_{o2}$.

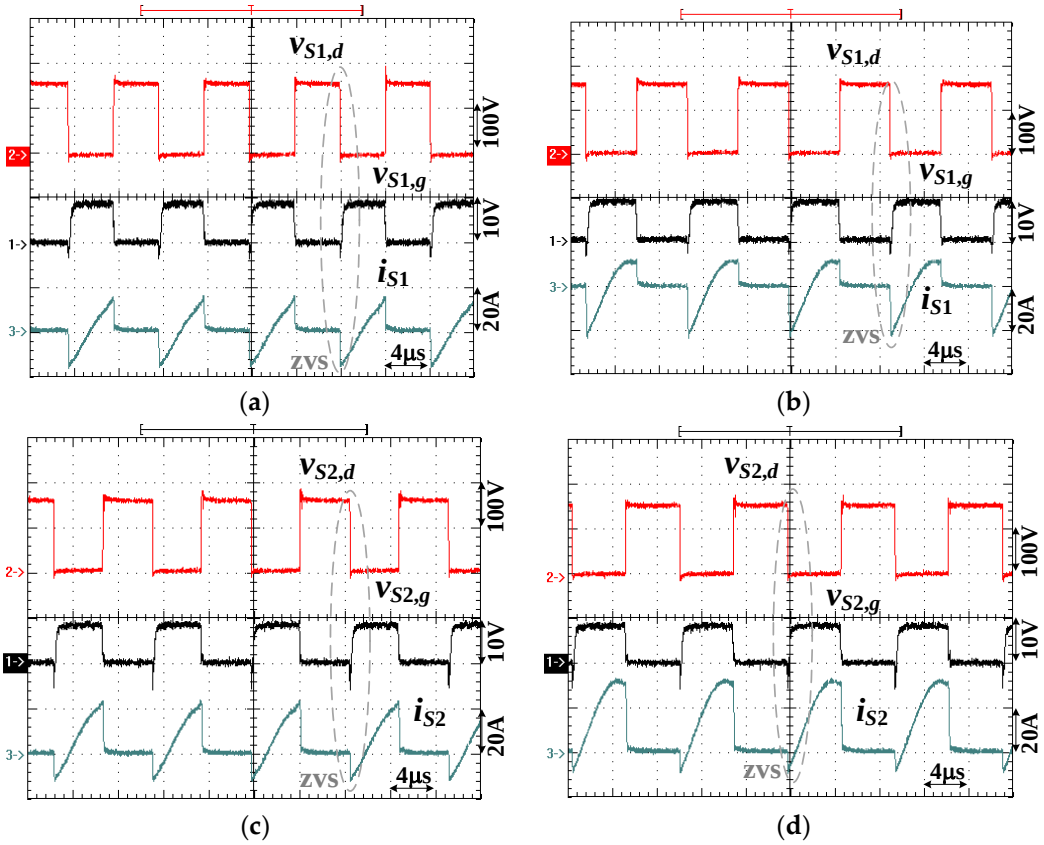



**Figure 13.** Experimental results of power switches $S_1$ and $S_2$ under high voltage mode operation and $V_{in}$ = 80 V: (**a**) $v_{S1,g}$, $v_{S1,d}$, $i_{S1}$ at 20% rated power; (**b**) $v_{S1,g}$, $v_{S1,d}$, $i_{S1}$ at 100% power; (**c**) $v_{S2,g}$, $v_{S2,d}$, $i_{S2}$ at 20% rated power; (**d**) $v_{S2,g}$, $v_{S2,d}$, $i_{S2}$ at 100% power.

## 6. Conclusions

A new wide voltage operation *LLC* converter with current-fed input is presented and experimented to realize soft switching operation and input current ripple reduction. A hybrid *LLC* resonant converter with a half-bridge-type or full-bridge-type structure is employed to realize wide input voltage operation. Owing to the fundamental leg voltage of the full-bridge-type resonant circuit being double the leg voltage of the half-bridge-type resonant circuit, a 4:1 input ($V_{in,\,max} = 4V_{\text{in, min}}$) *LLC* converter is achieved in the presented converter. Two interleaved boost circuits are used at the input side to reduce input current ripple. Owing to the circuit characteristics of the *LLC* converter, all switches can turn on at zero-voltage switching. The proposed single-stage current-fed hybrid *LLC* converter has less switch components. To verify the effectiveness of the presented circuit, a design procedure of the prototype circuit is presented first to obtain the circuit components. Finally, the experimental verifications are provided to show the circuit performance. Due to the wide input voltage operation, the converter at the low input voltage condition has the serious power losses compared to the high input voltage case. Therefore, the selection of power devices and the design of the magnetic components are very important to achieve a high efficiency converter. These issues will be analyzed and investigated in the future work for the studied converter.

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