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Light Load Efficient Silicon Power Converters Based on Wide Bandgap Circuit Extensions

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Abstract: A power electronics converter is generally designed for a specific load condition. However, depending on the applications and its mission profiles, the operating load conditions can be distinctly lower than the specified ones (PV cell under shading conditions, etc.). During this light load condition, the efficiency diminishes considerably, especially if Si–IGBT devices are considered within the power circuit. This study explains a light-load circuit extension based on wide-bandgap (WBG, silicon carbide and gallium nitride) material, which can improve the light-load efficiency and transient response of the conventional IGBT-based active rectifiers and inverter. Such an additional circuit extension is, in general, associated with additional cost. Numerous factors, such as the power electronics application itself, mission profiles, converter power rating and sizing of passive components, etc., can shift the break-even point of the upgraded power electronics system in terms of time. Therefore, a profound investigation of the relevant areas of interest is required in advance to ensure the most efficient amortization of the additional incurred costs of the applied circuitry. A 125 kW 3-phase six-switch inverter is discussed to highlight relevant effects in light-load operation that must be considered for final product design.

Keywords: efficiency; wide bandgap; power electronics; AC/DC; DC/AC

1. Introduction

1.1. Background

The share of power electronics in transmission and distribution grids has been growing now for decades and will continue to expand effectively also in the future. The reasons for this are the accelerated transition and migration towards renewable energy systems, primarily driven by compliance with climate targets and thus the reduction of GHG emissions. There are a vast number of applications covered by power electronic circuits and at least as many different implementations and strategies for the realization and provision of the required energy transfer from the generator to the corresponding load. In general, the efficiency curve of such a power electronics inverter, active rectifier or converter shows a nonlinear characteristic which is depending on its instantaneous load. It typically peaks in the region of around 40%–60% (partial load operation) of the system's nominal load. Under the nominal load, the efficiency of such an inverter slightly diminishes (approximately 1%–7% lower compared to its absolute maximum), if an inverter or active rectifier reaches no-load or light-load conditions, its performance in terms of efficiency is vastly decreasing as the switching losses of semiconductors dominate the operating mode. Due to, for example, capacitive charging/discharging effects, circulating currents caused by parallelization of several power systems and occurring input/output current ripple with switching frequency that still must be processed. Thus, the efficiency of the system ramps down expeditiously (Figure 1a—red area) if no loss compensating control strategy is employed. Energy efficiency has an important societal impact as it directly affects CO_2 emissions. Due to a higher

energy efficiency either less energy is required for a specific load (such as a motor drive) or a higher amount of generated energy can be fed to the grid and less additional power sources are required. Due to the environmental impact of energy efficiency international societies such as the International Energy Agency (IEA) are running several working groups which are elaborating on energy efficiency related topics.

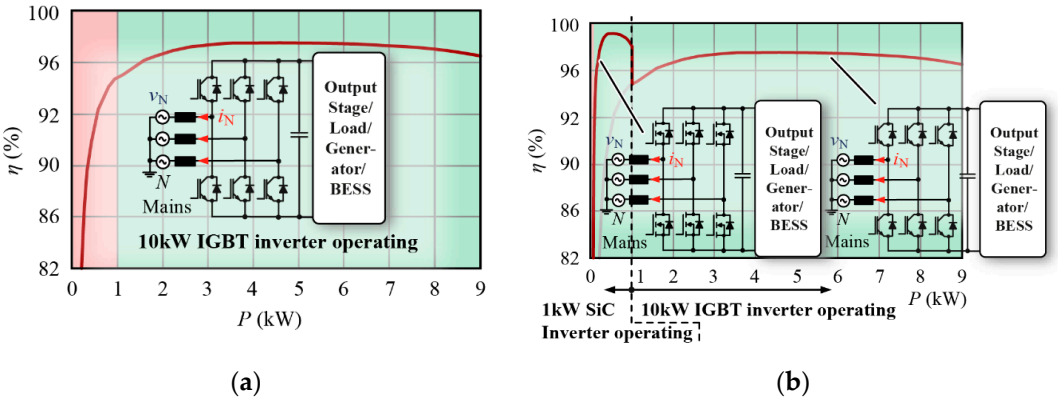


Figure 1. Example efficiency curves of (**a**) a standard 3-phase 10 kW IGBT inverter and (**b**) a combination of both, SiC and IGBT inverter where a 1 kW SiC inverter is operating during load conditions of 0 to 1 kW and the 10 kW Si–IGBT inverter for any mode >1 kW.

1.2. Relevant Contribution to This Field

There are different concepts already available in the literature (for example, [1–12]), which are addressing these partial load issues. The authors try to solve it using either sophisticated control strategies, modulation strategies, costly and high volume paralleled converter approaches or partial load converter topologies. Especially approaches from [1–10] show some lack in different areas, e.g., simplicity, cost-effectiveness, power density, flexibility, etc. Another example, is discussed in [13]. There, the authors describe a novel FFCS (flywheel fast-charging system) aiming to improve converter efficiency with a sophisticated control strategy.

This study proposes and discusses an optional light-load efficient circuit extension, which can be enabled during this inefficient light-, ultra-light or no-load conditions and still guarantees high performant power electronics operation for a more comprehensive load range while re-utilizing already existing parts of the high-power inverter such as input filter, commutation inductance, capacitive DC-link, etc. (Figure 1b). The proposed solutions would be of special interest for renewable energy systems such as PV, wind power BESS which are operating a significant amount of time under light-load conditions or for high power applications with space restrictions (such as transportation, aviation etc.). In this study, initial design guidelines are discussed, and the potential of this solution is highlight by two examples (high-power converter with and without light-load upgrade).

The rest of the study is organized as follows. Section 2 introduces different general examples on how such an upgrade box could be integrated into different power electronics topologies. Design parameters for a comparison between a 125 kW six converter with and without optional light-load converter are specified in Section 3. In Section 4 different switching and conduction losses of a high-power Si–IGBT converter and a low power SiC–MOSFET converter are compared to each other. Moreover, the potential of utilizing GaN transistors is discussed. Some conclusions and a short outlook is given in Section 5.

2. General Considerations

2.1. Topologies

As already mentioned, there are many different power electronic applications available that can benefit from such a light/no-load WBG operating upgrade. The study at hand deals primarily with

three-phase systems, which can be implemented as either 2-level or multilevel topology. In terms of multilevel converter topologies, the discussions are limited to 3-level t-type solutions for this publication. However, it has to be noted that this does not limit the applicability of the proposed concept to higher-order multilevel systems. Figure 2a,b shows two versions of a three-phase grid-connected power electronic inverter based on Si–IGBTs (either two- or three-level), which can be equipped by a SiC MOSFET half-bridge circuit (one stage for each phase).

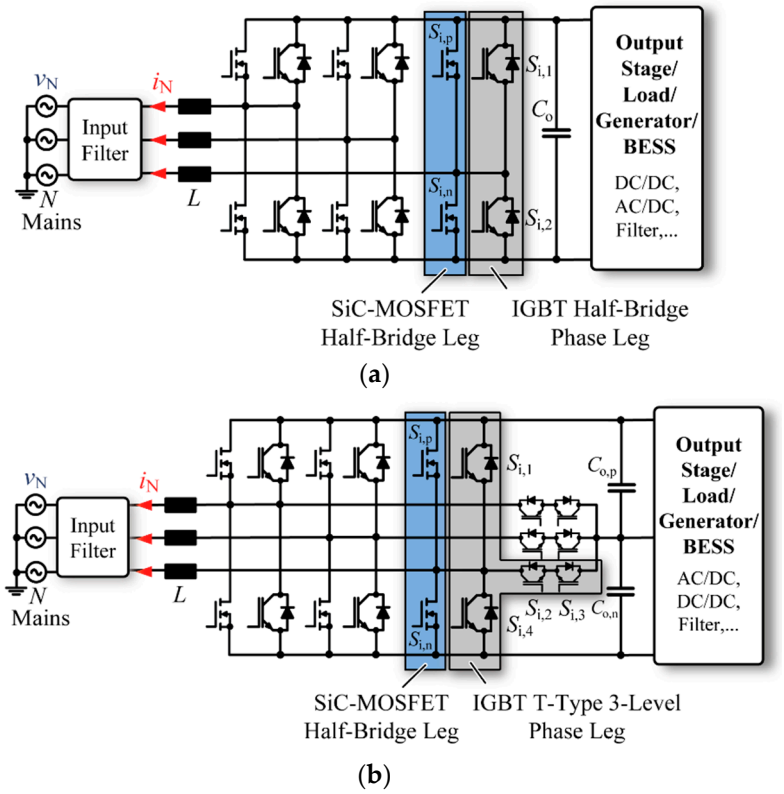


Figure 2. Three-phase grid-connected (**a**) 6-switch or (**b**) t-type IGBT-based rectifier/inverter with equipped 3 different SiC half-bridge legs for each converter input phase.

The enhanced circuit benefits from already existing passives, i.e., input filter, DC-link capacitor, etc. which can be utilized in terms of operation. For grid-connected applications, SiC is currently the most effective choice if single-stage voltage characteristics, cost, and switching losses are considered. Due to its unipolar and ohmic characteristics, SiC MOSFETs come with lower conduction losses up to a specific current level compared to the classical IGBT. During partial load conditions, IGBTs are suffering from their diode-like *V*/*I* output characteristics, which makes them inefficient for lower current values. Therefore, if the efficiency of the inverter drops below a critical value (which can be specified in terms of power or input current), the Si–IGBT devices are deactivated, and the equipped SiC inverter takes over the handling of the energy transmission from input- to output-side. Thus, the solicited energy transfer can still be maintained and guaranteed under improved system efficiency performance (as illustrated in Figure 1). If a lower DC-link voltage than 600 V is required (e.g., for the current state of the art motor drive inverters), all the implemented SiC devices could be substituted by GaN transistors (Figure 3a). This brings an additional improvement in terms of semiconductor device efficiency but currently comes with higher chip cost, which delays the aspired amortization timing. Therefore, also 600/650 V SiC MOSFETs (as shown in Figure 3b) can be applied for those solutions.

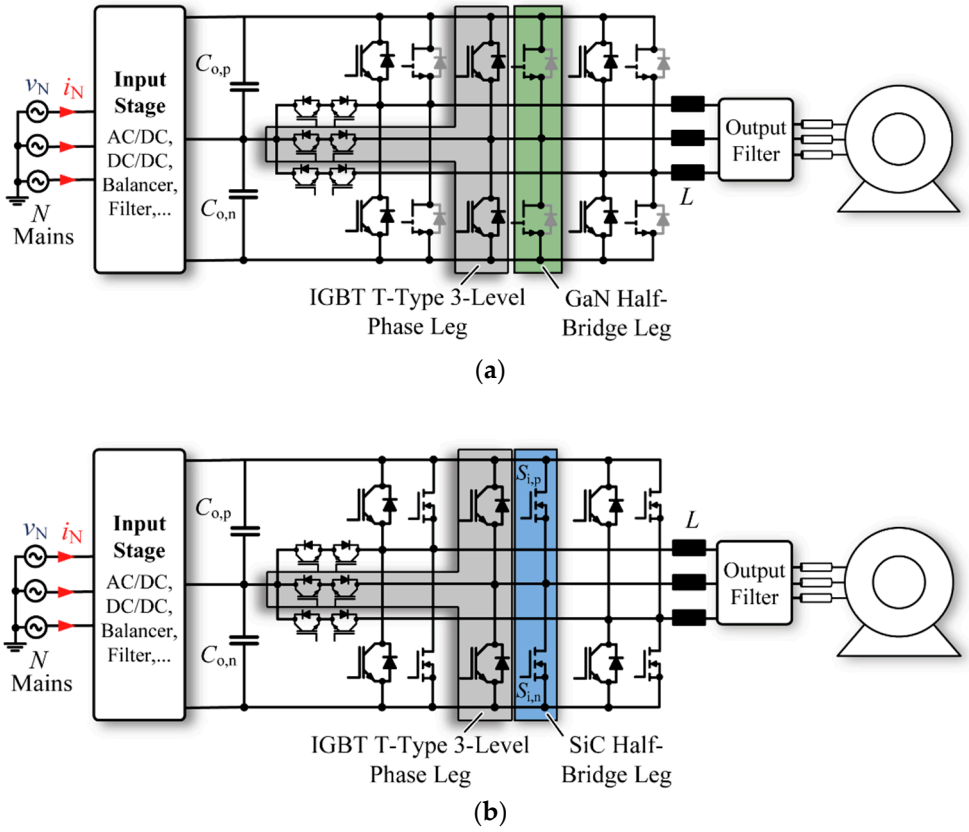


Figure 3. Three-phase IGBT-based t-type drive system with either (**a**) GaN half-bridge stages for 400 V_{DC} or (**b**) SiC half-bridge stages for 800-V_{DC} DC-link voltage levels.

2.2. General Design Strategy and Cost Optimization

In order to unveil the full potential of this secondary circuit, a detailed loss calculation of the silicon-based system is required. The critical area where the efficiency drops below, e.g., 90% of its peak value during operating under no-load/light-load or partial-load condition, has to be identified. The SiC MOSFET half-bridge branches have to be designed such, that their peak efficiency appears under the critical load condition (lowest efficiency at maximum operating hours in this specific area) of the original IGBT inverter. Dependent on parameters in particular occurring losses, operating load conditions, switching frequency of the WBG semiconductors, etc. either no additional cooling strategy is required or an existing heat sink of the IGBT inverter can be exploited. Therefore, positioning of the additional WBG switching components must be chosen such that it is fitting and complying with the existing IGBT design but optimized for fast switching to minimize switching losses of the WBG semiconductors. Besides various other factors and components, such as the adjacent gate resistance also the parasitic inductance of the current commutation path (DC-link capacitors → high-side switch → low-side switch → DC-link capacitor) is limiting the switching speed of SiC and GaN devices. Hence, an optimized positioning of both WBG devices and IGBTs must be determined under the assumption that IGBT semiconductor losses under nominal load operation must not be impaired.

Moreover, additional WBG semiconductor components also additional gate drive circuits are required and increase the cost of the adapted solution. However, dependent on the switching requirements such as turn-on and turn-off gate voltages, already existing hardware from IGBT driving circuits can be reused and exploited (e.g., DC/DC converters). In an optimized design, only one additional gate driver (cf., Figure 4) with, e.g., a bootstrap mechanism for high-side driving, is required for proper operation of the dedicated wide-bandgap half-bridge stage. Additional voltage level shifting, for example, a GaN application can be easily adapted via additional capacitors (capacitive voltage dividers), resistors, and/or Zener diodes. Those solutions in Figures 2 and 3 both consider one

half-bridge topology for each grid phase. Therefore, these implementations will result in an additional number of 6 SiC/GaN semiconductors and six gate drivers with individual output control input or three gate drivers with PWM high-side/low-side configuration. To improve the payback time of the circuit extension the operating circuit can be reduced by 2 SiC–MOSFETs (as illustrated in Figure 5a) for unbalanced two-phase operation or 4 SiC–MOSFETS for unbalanced single-phase (four-phase connectivity) operation (as depicted in Figure 5b). It has to be noted that the single-phase solution does not benefit from a reduced current ripple (evoked due to the occurring common-mode voltage) anymore as the mains neutral is directly connected to the midpoint of the split DC-link capacitors.

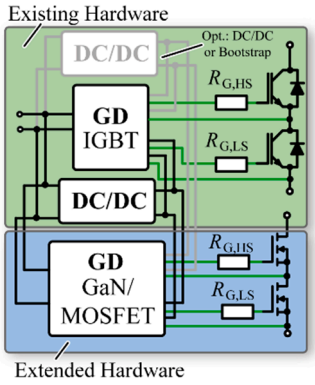


Figure 4. Auxiliary circuits for driving existing IGBTs (DC/DC converter(s), bootstrap, gate driver, ...) and reutilization for light-load operating SiC/GaN extension.

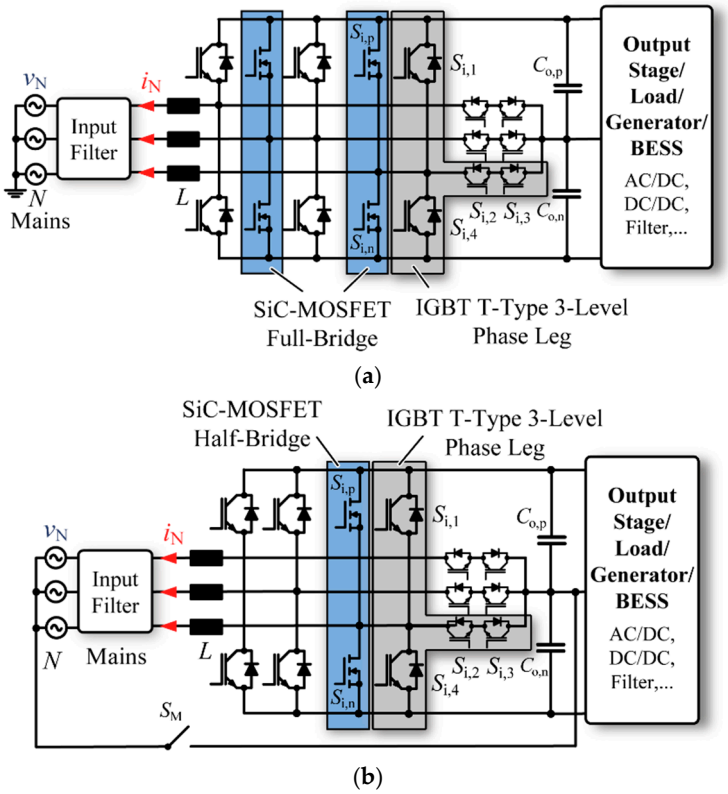


Figure 5. Grid-connected three-phase IGBT-based rectifier/inverter systems utilizing a low-cost version of the light load wide-bandgap solution by implementing merely either (**a**) 4 (two-phase operation) or (**b**) 2 (single-phase) SiC power semiconductors.

2.3. Voltage Balancing of Multilevel Converters

Especially for three- or multilevel converters also voltage balancing functionality is required to keep both positive ($C_{o,p}$) and negative capacitor ($C_{o,n}$) banks on the same voltage level. The simplest way to guarantee a symmetrical split DC-link would be resistive balancing. However, losses of this methodology become highly unfavorable, especially during light and no-load operation due to their lossy nature regarding the small input power for these operating conditions. These high losses will eliminate the expected effect of the WBG circuit and should thus be avoided. Therefore, another option could be to extend the circuit with active balancing methods relying on operational amplifiers or bipolar transistors, as discussed in [14]. If such an additional balancing circuit is required, expenses of the total extension further increase. A rather attractive and low-cost option for successful voltage balancing could be reusing existing equipment, in this particular case those IGBTs of a t-type inverter which are connected to the respective midpoint of the power stage ($S_{i,2}$, $S_{i,3}$). Voltage imbalance is usually caused according to effects such as capacitor leakage currents, the dead-time of switching circuits, etc. and thus a process that comes with rather a low dynamic. Therefore, these inner leg IGBTs shall only be operated for very short time frames during the light load condition. Furthermore, these inner switches are stressed with lower blocking voltage, which results in lower switching losses during operation compared to their outer leg counterparts.

3. Definition of Main Design Parameters for Three-Phase Six-Switch Converter Example

To demonstrate the improved efficiency and to reveal the limitations of such an additional wide-bandgap-based circuit extension during the light load operation, the following sections are covering a comparison for different components and materials (silicon—Si, silicon carbide—SiC, gallium nitride—GaN). The base for this discussion will be a three-phase six-switch converter stage, as illustrated in Figure 2a, which is commonly used in industry for all different types of power and voltage ratings (low voltage, medium voltage; low power, medium power, high power).

3.1. Pre-Design of 125 kW Grid-Connected Three-Phase Six-Switch Converter Stage

In order to create a reference model for all further discussions, basic parameters and dedicated modules are selected, and a 125 kW AC/DC converter stage is chosen. Relevant system and converter related parameters are defined in Table 1. Mains voltage and frequency parameters are defined according to European standards for low-voltage grids (400 V_{rms} and 50 Hz). The power rating of the inverter was chosen according to [15]. It should be noted that for further discussions, two additional simplifications were applied to reduce the complexity of relevant equations. First, a standard pulse width modulation (PWM) approach was selected. No space vector modulation or third harmonic injection strategies are considered. Therefore, it was opted for a total DC-link voltage (V_{DC}) of 800 V to meet a modulation index M of 0.813. The additional margin of 0.187 is required to compensate dynamic events which must be compensated by current and voltage controller routines. The modulation index for such a three-phase six-switch inverter is defined by

$$M = \frac{2 \cdot \sqrt{2} \cdot V_{N,rms}}{V_{DC}} = 0.813. \quad (1)$$

Table 1. System-level design specification of the three-phase converter (nominal rating).

Design Parameter	Value
Mains voltage:	V_{LL} = 400 V_{rms}
Mains frequency	f_N = 50 Hz
Total DC-link voltage	V_{DC} = 800 V
Nominal power	$S_N = P_N$ = 125 kW

Second, it is assumed that the midpoint of the DC-link is connected to the artificial star point of the Y-connected input filter capacitors and/or neutral created by the 3-phase grid formation. This allows for simpler analytical equations compared to a floating setup. However, in such configuration, the current ripple of each phase is considerably higher due to the fixed midpoint of the DC-link and the mission common-mode voltage, which is usually introducing additional voltage levels manipulating the current ripple characteristics for the whole sinusoidal period of $0 \leq \varphi \leq 2\pi$.

The selected converter stage is bidirectional. Thus, it can deliver power from the grid to load or vice versa. A phase angle of $\Phi = 0$ denotes power delivery from the grid to load. A phase angle of $\Phi = \pi$ indicates power flow from load/source to grid. Furthermore, typically, grid-connected power electronics also must support the grid with additional reactive power. Adaptation of the phase angle Φ results in different active and reactive modes/operation of the converter. Therefore, for all further calculations, the fundamental relations apply,

$$S_{\mathrm{N}} = \sum_{i} V_{\mathrm{N,rms,i}} \cdot I_{\mathrm{N,rms,i}} = 3 \cdot V_{\mathrm{N,rms}} \cdot I_{\mathrm{N,rms}} \tag{2}$$

$$P_{\mathrm{N}} = 3 \cdot V_{\mathrm{N,rms}} \cdot I_{\mathrm{N,rms}} \cdot \cos(\Phi) \tag{3}$$

$$Q_{\mathrm{N}} = 3 \cdot V_{\mathrm{N,rms}} \cdot I_{\mathrm{N,rms}} \cdot \sin(\Phi) \tag{4}$$

$$I_{\mathrm{o}} = 3 \cdot \frac{V_{\mathrm{N,rms}}}{V_{\mathrm{DC}}} \cdot I_{\mathrm{N,rms}} \cdot \cos(\Phi) \tag{5}$$

where S_{N}, P_{N} and Q_{N} denote apparent, active and reactive power, respectively. I_{o} defines the averaged DC-current after capacitive filtering. The switching frequency of such converters in the 100 kW region is typically between 5–10 kHz, depending on whether the solution is optimized for power density or efficiency. For this evaluation, a switching frequency of 10 kHz is chosen in order to demonstrate the potential of the proposed additional WBG-based light-load circuit enhancement. Based on the specifications defined in Table 1 the nominal current rating for each phase results in:

$$I_{\mathrm{N,rms}} = \frac{S_{\mathrm{N}}}{3 \cdot V_{\mathrm{N,rms}}} = 181 \text{ A}. \tag{6}$$

According to a rule of thumb derived from on [15], the current rating of the two-level IGBT power module at a case temperature of 100 °C should be 3–5 times higher than the nominal current rating per respective phase (depending on maximum power rating). Therefore, an Infineon FF600R12KE4 [16] 1200 V/600 A IGBT module was chosen for this investigation. The module comprises of a high-side and low-side IGBT and a reverse conducting diodes. Very general applications of such modules are motor drives, wind turbine related power electronics, UPS systems and high-power converters.

Considering previously described assumptions for control and reference setup the current ripple of the two-level topology with sinusoidal excitation results in

$$\Delta i_{\mathrm{L}}(\varphi) = \frac{V_{\mathrm{DC}}}{4 L f_{\mathrm{sw}}} \left[M^2 \sin(\varphi)^2 - 1 \right] \tag{7}$$

for $0 \leq \varphi \leq 2\pi$, a maximum current ripple value of:

$$\left| \Delta I_{\mathrm{L,max}} \right| = \frac{V_{\mathrm{DC}}}{4 L f_{\mathrm{sw}}} \tag{8}$$

and a minimum ripple of:

$$\left| \Delta I_{\mathrm{L,min}} \right| = \frac{V_{\mathrm{DC}}}{4 L f_{\mathrm{sw}}} \left[1 - M^2 \right] \tag{9}$$

The averaged and rms values of the current ripple for each phase compute to:

$$\left|\Delta I_{\mathrm{L,avg}}\right| = \Delta I_{\mathrm{L,max}}\left[1 - \frac{M^2}{2}\right] \tag{10}$$

and

$$\Delta I_{\mathrm{L,rms}} = \Delta I^2_{\mathrm{L,max}}\left[1 - M^2 + \frac{3}{8}M^4\right], \tag{11}$$

respectively. Thus, an inductor L_{inv} of 250 µH was chosen to allow a maximum current ripple of approximately 30% of the nominal input current $I_{\mathrm{N,rms}}$.

3.2. Pre-Design of 10 kW SiC Light-Load Converter Stage

As already mentioned in Section 1 and discussed in Section 2 of this manuscript, the equipped additional WBG-based semiconductor components should be designed for considerably lower rated power, in order to support the system with outstanding efficiency during the light-load operation. Furthermore, it benefits from already existing DC-link and input inductors. In a best-case scenario, the light-load converter should be rated for at least <10% P_{N}. For the current example, a light-load rating of 8% regarding the SiC converter stage was chosen, which results in a rated power of 10 kW. In order to keep the rule of thumb from [15] and allow comparable results, Infineon's IMZ120R030M1H [17] 1200 V/30 mΩ with a current rating of 45 A for a case temperature of 100 °C is utilized for the WBG-based hookup. It is worth noting that the choice of semiconductors and components such as input/output inductors always highly dependent on the application and dedicated parameters. The chosen parameters in Sections 3.1 and 3.2 should give the reader an idea of relevant effects and considerations for such light-load converter stages and can thus vary for final product design.

3.3. Summary of Design Results

In Table 2 summary of chosen operating parameters such as the switching frequency, values of inductance, IGBT modules for nominal power (three-phase, 125 kW total active power for unity power factor operation) and SiC–MOSFET discrete (three-phase, 10 kW active power for unity power factor operation), is given.

Table 2. System-level design specification of the three-phase converter (nominal rating).

Design Parameter	Value
Switching frequency Si/SiC	f_{sw} = 10 kHz
Input inductance/phase:	L_{inv} = 250 µH
Input current ripple maximum	$\lvert\Delta I_{\mathrm{Lmax}}\rvert$ = 80 A
Input current ripple minimum	$\lvert\Delta I_{\mathrm{Lmin}}\rvert$ = 27 A
Input current ripple rms	$\Delta I_{\mathrm{L,rms}}$ = 56.7 A
IGBT module (3ph./125 kW)	FF600R12KE4 1200 V/600 A
SiC MOSFET (3ph./10 kW)	IMZ120R030M1H 1200 V/30 mΩ

4. The Efficiency of Hybrid Power Stage under Light–Load Conditions

4.1. 125 kW Si IGBT Converter vs. 10 kW SiC Power Stage under Light-Load Conditions

In general, for evaluation of conduction losses of hard-switched AC/DC or DC/AC converter topologies, only losses during nominal load operation of the circuit are of interest as these are the worst-case losses under normal conditions. These losses are of interest for heatsink design and evaluation of system efficiency. As the current ripple has minor effects in terms of avg and rms values under these nominal conditions, it is often omitted to simplify relevant design equations. Besides the modulation index M and the phase shift angle (Φ) of the fundamental current, these equations are only dependent on mains rms $I_{\mathrm{N,rms}}$ or peak $I_{\mathrm{N,pk}}$ current, respectively.

Furthermore, it must be noted that an IGBT can only conduct current in a positive direction when gated. Negative currents are processed via the supplementary reverse conducting diode. A MOSFET, on the other hand, can conduct currents in both (positive and negative) directions through its channel when exceeding its threshold voltage and thus turned ON. The diode of the MOSFET is thus only relevant for switching losses and only stressed during the specified dead-time of the gate driver. As this dead-time is usually much lower than the dedicated inverse switching frequency, conduction losses of the parasitic diode can be omitted. Therefore, it has to be distinguished between topologies utilizing IGBTs and MOSFETs.

As depicted in Figure 6, it can be observed that for an IGBT-based three-phase six-switch inverter the high-side IGBT ($IGBT_p$; $IGBT_p$ turned ON) and low-side reverse conducting diode (D_n; $IGBT_p$ turned OFF) are stressed during negative input currents $i_N(\varphi)$, whereas low-side IGBT ($IGBT_n$; $IGBT_n$ turned ON) and high-side reverse conducting diode (D_n; $IGBT_n$ turned OFF) are stressed during the positive half-wave of the input current $i_N(\varphi)$.

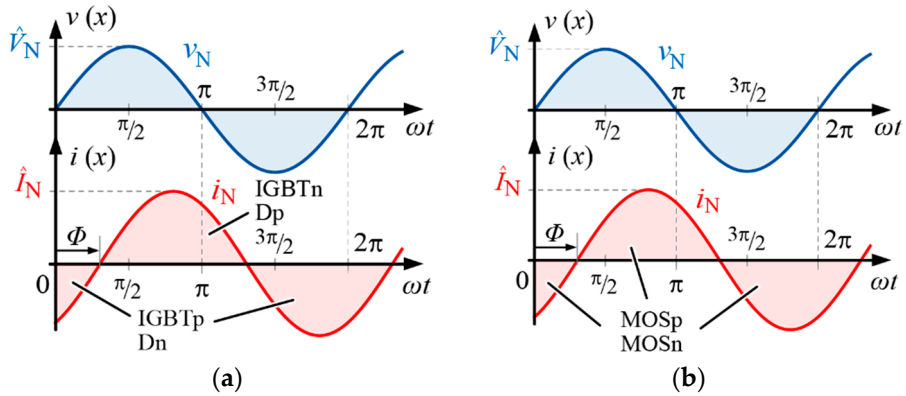


Figure 6. Current stress semiconductors of a three-phase six-switch rectifier for (**a**) an IGBT-based and (**b**) a MOSFET-based converter stage.

For a MOSFET-based three-phase six-switch converter, both high-side (MOS_p; MOS_p turned ON) and low-side MOSFET (MOS_n; MOS_p turned OFF) are conducting during one complete sinusoidal period $0 \leq \varphi \leq 2\pi$, with $\varphi = \omega t = x$ (conduction during dead-time is neglected).

4.1.1. Conduction Losses of IGBT- and SiC-Based Light–Load Setup

In order to compare the conduction losses of the three-phase IGBT inverter and the optimized SiC MOSFET power stage, it is important to specify the relevant equations to calculate the respective semiconductor conduction losses of the system.

In general, to keep the semiconductor loss evaluation process of a three-phase inverter straightforward, the nominal load condition of the inverter is considered and effects due to current ripple variations are neglected, as the current ripple only forms a minor share of the nominal sinusoidal phase current (e.g., maximum 20% of input peak current). For this study, however, light-load and no-load operations are of significant concern. During these conditions, thus, determining conduction losses of IGBT and MOSFET circuits heavily rely on impact related to the occurring current ripple. Especially during the no-load operation of the power conversion stage, the emerging current ripple is solely liable for both conduction and switching losses. For a MOSFET driven power circuit (as illustrated in Figure 7) averaged and rms relate current stress results in:

$$S_{p,MOS,avg} = S_{n,MOS,avg} = -I_{N,pk}\frac{M}{4}\cos(\Phi), \tag{12}$$

$$S_{\mathrm{p,MOS,rms}} = S_{\mathrm{n,MOS,rms}} = \frac{\Delta I_{\mathrm{L,max}}}{2}\sqrt{\left(\frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}\right)^2 + \frac{\frac{8}{3} - \frac{8}{3}M^2 + M^4}{16}}, \tag{13}$$

$$D_{\mathrm{p,MOS,avg}} = D_{\mathrm{n,MOS,avg}} \sim 0, \tag{14}$$

$$D_{\mathrm{p,MOS,rms}} = D_{\mathrm{n,MOS,rms}} \sim 0. \tag{15}$$

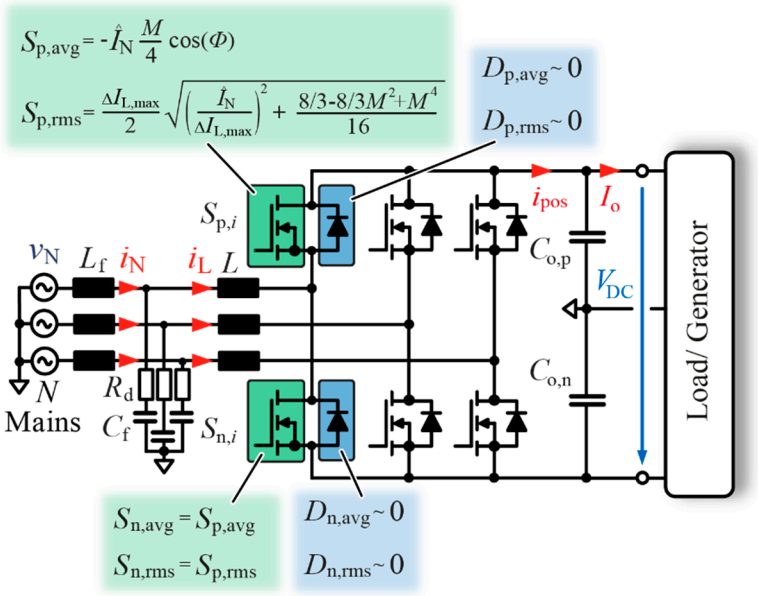


Figure 7. Current stress of a MOSFET-based three-phase six-switch inverter topology, incorporating the existing current ripple, as in particular relevant for light- and no-load operation.

As it is well-known from literature, in a MOSFET half-bridge configuration, the intrinsic diode of the MOSFET only conducts current during dead-time of each leg and, therefore, conduction losses of the forward-biased diode during these time instants can be neglected. Furthermore, it should be noted that the Equations (12)–(15) are valid during nominal-, light-load and no-load conditions, as the MOSFET channel can process current in both directions when the MOSFET is activated ($v_{\mathrm{GS}} > V_{\mathrm{th}}$) with v_{GS} being the gate-source and V_{th} the threshold voltage of the transistor, respectively. In addition, it can be observed from Equation (13) that the rms values for this topology are independent of the active and reactive loading.

In order to characterize an IGBT-based three-phase six-switch inverter in an analytical manner, it has to be distinguished between nominal and light-/no-load operation. This is caused due to the very nature of the IGBT to conduct current only unidirectional when being turned ON ($v_{\mathrm{GE}} > V_{\mathrm{th}}$). Currents in reverse direction must be processed via the dedicated antiparallel diode. Therefore, especially in light- and no-load operation when the current ripple of the circuit starts to get dominant ($I_{\mathrm{N,\,pk}} < \Delta I_{\mathrm{Lmax}}$) and a global assessment and differentiation between positive and negative sinusoidal half-wave of the input current is no longer sufficient for an accurate result. It also has to be considered that the current ripple under light- and no-load operation will split between IGBT and diode. For such an IGBT-based power stage (as illustrated in Figure 8) averaged and rms relate current stress for $I_{\mathrm{N,pk}} < \Delta I_{\mathrm{Lmax}}$ can be calculated to:

$$S_{\mathrm{p,IGBT,avg}} = S_{\mathrm{n,IGBT,avg}} = \frac{\Delta I_{\mathrm{L,max}}}{8}\left(\frac{1}{2} - \frac{M^2}{4} + \frac{I_{\mathrm{N,pk}}^2}{\Delta I_{\mathrm{L,max}}\Delta I_{\mathrm{L,rms}}} - \frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}M\cos(\Phi)\right), \tag{16}$$

$$S_{\mathrm{p,IGBT,rms}} = S_{\mathrm{n,IGBT,rms}} = \frac{\Delta I_{\mathrm{L,max}}}{2}\sqrt{\frac{1}{2}\left(\frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}\right)^2 + \frac{\frac{8}{3}-\frac{8}{3}M^2+M^4}{32} - \left(\frac{1}{4}\frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}M - \frac{3}{16}\frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}M^3 + \frac{1}{4}\frac{I^3_{\mathrm{N,pk}}}{\Delta I^2_{\mathrm{L,max}}\Delta I_{\mathrm{L,rms}}}M\right)\cos(\Phi)}, \tag{17}$$

$$D_{\mathrm{p,IGBT,avg}} = D_{\mathrm{n,IGBT,avg}} = \frac{\Delta I_{\mathrm{L,max}}}{8}\left(\frac{1}{2} - \frac{M^2}{4} + \frac{I^2_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}\Delta I_{\mathrm{L,rms}}} + \frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}M\cos(\Phi)\right), \tag{18}$$

$$D_{\mathrm{p,IGBT,rms}} = D_{\mathrm{n,IGBT,rms}} = \frac{\Delta I_{\mathrm{L,max}}}{2}\sqrt{\frac{1}{2}\left(\frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}\right)^2 + \frac{\frac{8}{3}-\frac{8}{3}M^2+M^4}{32} - \left(\frac{1}{4}\frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}M - \frac{3}{16}\frac{I_{\mathrm{N,pk}}}{\Delta I_{\mathrm{L,max}}}M^3 + \frac{1}{4}\frac{I^3_{\mathrm{N,pk}}}{\Delta I^2_{\mathrm{L,max}}\Delta I_{\mathrm{L,rms}}}M\right)\cos(\Phi)}. \tag{19}$$

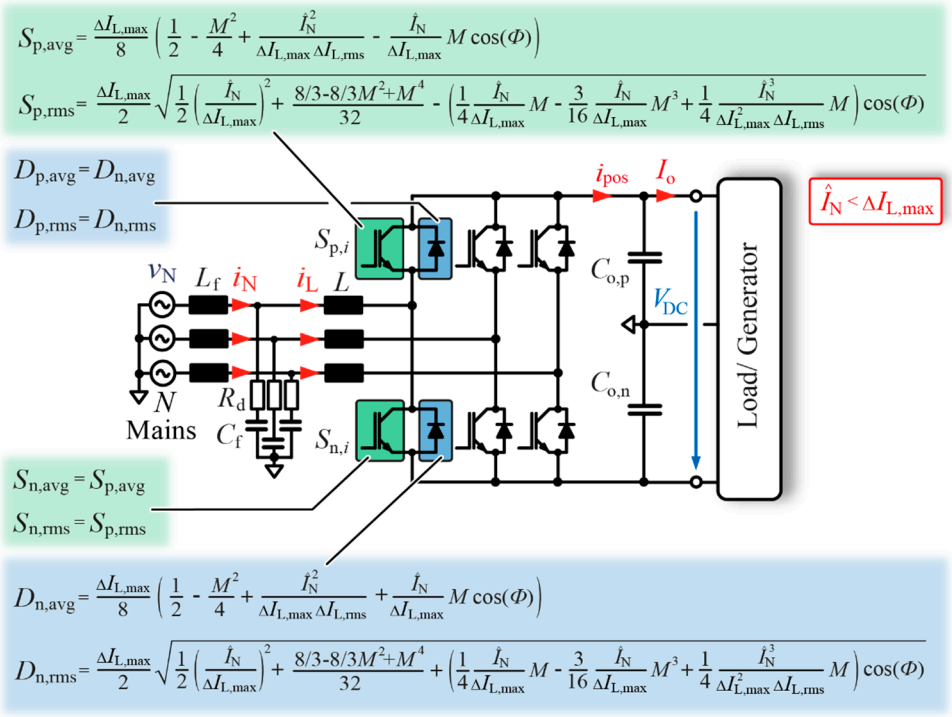


Figure 8. Current stress of an IGBT-based three-phase six-switch inverter topology, incorporating the existing current ripple, for light- and no-load operation ($I_{\mathrm{N,pk}} < \Delta I_{\mathrm{Lmax}}$).

With these equations for MOSFET and IGBT-based circuits, the conduction losses of both circuits can now be derived and investigated in detail.

The conduction losses of a MOSFET are defined by:

$$P_{\mathrm{MOS,con}} = R_{\mathrm{on,MOS}}{I_{\mathrm{MOS,rms}}}^2, \tag{20}$$

whereas $I_{\mathrm{p,MOS,rms}}$ equals $S_{\mathrm{p,IGBT,rms}}$. According to the datasheet of Infineon's IMZ120R030M1H, the on-resistance at a junction temperature of 85 °C is approximately 35 mΩ.

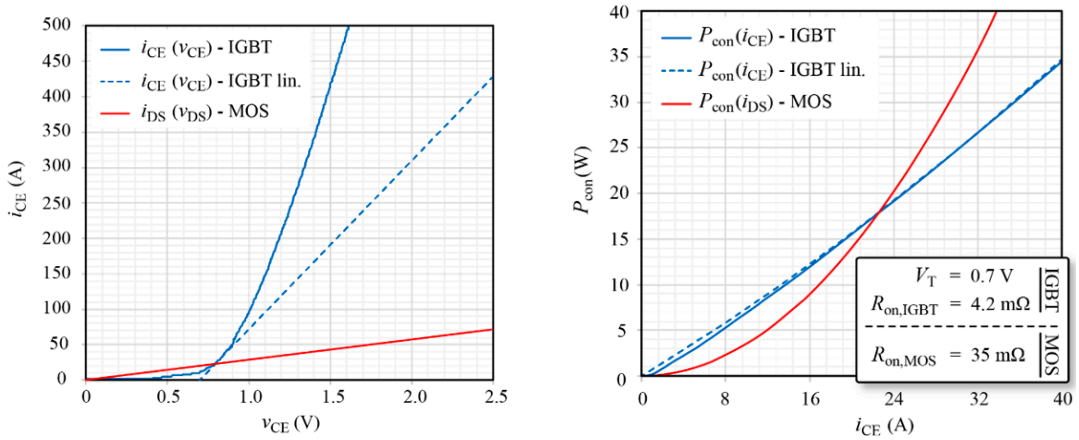
For an IGBT and dedicated antiparallel diode, the conduction losses are specified via:

$$P_{\mathrm{IGBT,con}} = V_{\mathrm{T}}I_{\mathrm{IGBT,avg}} + R_{\mathrm{on,IGBT}}{I_{\mathrm{p,IGBT,rms}}}^2, \tag{21}$$

$$P_{\mathrm{D,con}} = V_{\mathrm{D}}I_{\mathrm{D,avg}} + R_{\mathrm{D}}{I_{\mathrm{D,rms}}}^2, \tag{22}$$

where V_{T} and V_{D} representing the forward voltage of IGBT and diode, respectively. $R_{\mathrm{on,IGBT\ and}}$ R_{D} denote the equivalent resistance of IGBT and antiparallel diode.

Generally, modeling approaches to determine the required forward voltage drop and resistance refer to the nonlinear *V*/*I*-output characteristic of an IGBT. If the module with reverse conducting IGBTs is appropriately chosen, the nominal operating point of the converter lies typically within the approximatively linear region of the device (not exactly linear due to conductivity modulation of IGBT devices), which enormously simplifies the linearization process of such nonlinear curves. During light- and no-load condition, however, the IGBT module designed for 125 kW will operate in the nonlinear area (i_{CE} and i_D < 100 A) of both IGBT's and diode's *V*/*I*-output characteristics (shown in Figure 9a).



(**a**) (**b**)

Figure 9. (**a**) *V*/*I* and (**b**) *I*/*P* characteristic of a Si–IGBT to extract forward voltage and ON–resistance of an IGBT under light- and no-load condition for a 125 kW three-phase six-switch system.

For accurate results, *V*/*I* datasheet results are transferred into an *I*/*P* curve (cf., Figure 9b). The *I*/*P* curve is then used to generate a similar conduction loss characteristic according to Equation (21), which represents the original loss properties in the low power region as precisely as possible. The obtained values for V_T and $R_{on,IGBT}$ can be verified by utilizing the-in-the *V*/*I* graph (retransferred linearized model). The same approach can be applied to extract linearized diode parameters of the forward–voltage V_D and the equivalent resistance R_D. Results for IGBT and diode characteristics can be found in Table 3.

Table 3. Relevant IGBT, dedicated antiparallel diode and SiC MOSFET parameters.

Parameter	Value
MOSFET on resistance:	$R_{on,MOS}$ = 35 mΩ
IGBT forward voltage (light-load):	V_T = 0.7 V
IGBT on resistance (light-load):	$R_{on,IGBT}$ = 4.2 mΩ
IGBT anti-p. diode forward voltage (light-load):	V_D = 0.85 V
IGBT anti-p. diode on resistance (light-load):	$R_{on,IGBT}$ = 3.5 mΩ

A comparison of conduction losses of one IGBT, with dedicated antiparallel diode and the proposed SiC–MOSFET substitute are illustrated in Figure 10 and shown in Table 4. In these graphs, the losses are mapped to different phase angles $\Phi = 0°$ (see Figure 10a), $\Phi = 45°$ (shown in Figure 10b), (c) $\Phi = 90°$ (depicted in Figure 10c) and $\Phi = 180°$ (cf., Figure 10d). It should be noted that $\Phi = 0°$ implies purely active power delivered from the grid to load and $\Phi = 180°$ active power provided from the generator to the grid. It can be observed that for the chosen setup at hand, conduction loss reversal point varies between 5.5% P_o and 6.5% P_o. It can thus be concluded that below 5.5% P_o the proposed WBG upgrade always comes with lower conduction losses. In this very specific case to conduction losses of the SiC MOSFET could be further reduced if (i) a SiC MOSFET with larger chip area would be chosen or (ii) the switching frequency of the SiC–MOSFETs would be increased beyond the switching

frequency of the Si–IGBT modules. An increased switching frequency would reduce the maximum current ripple and thus rms value of semiconductor devices, which results in lower conduction losses (quadratic nature). A higher chip area, on the other hand, will diminish the on-resistance of each MOSFET and therefore reduce conduction losses (linear dependency).

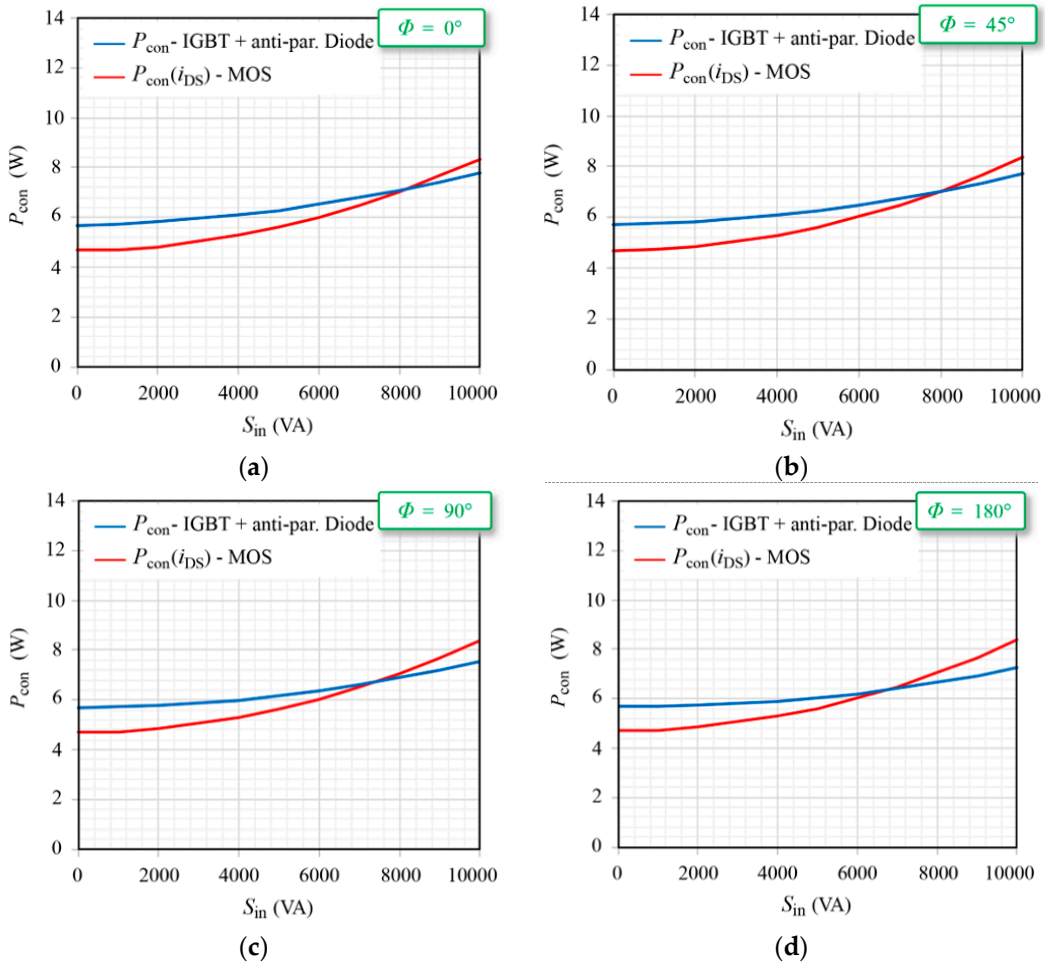


Figure 10. Conduction loss comparison of SiC MOSFET and Si–IGBT with an antiparallel diode for various load situations from 0 to 10 kVA and different phase angles of (**a**) $\Phi = 0°$ which results in $\cos(\Phi) = 1$, (**b**) $\Phi = 45°$, (**c**) $\Phi = 90°$ and (**d**) $\Phi = 180°$.

Table 4. Documented current stress and losses of IGBT with antiparallel diode and SiC–MOSFET for different phase angles and load conditions.

Φ (°)	S_{in} (kVA)	$I_{IGBT,avg}$ (A)	$I_{IGBT,rms}$ (A)	$I_{D,avg}$ (A)	$I_{D,rms}$ (A)	$I_{MOS,rms}$ (A)	$P_{IGBT,avg}$ (W)	$P_{IGBT,rms}$ (W)	$P_{D,avg}$ (W)	$P_{D,rms}$ (W)	P_{MOS} (W)
0	0	3.35	8.19	3.35	8.19	11.6	2.34	0.28	2.84	0.23	4.69
0	5000	2.54	7.63	4.62	10.11	12.7	1.78	0.24	3.93	0.36	5.61
0	10,000	2.19	8.36	6.36	13.01	15.5	1.53	0.29	5.4	0.59	8.37
180	0	3.35	8.19	3.35	8.19	11.6	2.34	0.28	2.84	0.23	4.69
180	5000	4.62	10.11	2.54	7.63	12.7	3.23	0.43	2.16	0.20	5.61
180	10,000	6.36	13.01	2.19	8.36	15.5	4.45	0.71	1.86	0.24	8.37

Ideally, the SiC–MOSFETs would be mounted on the same heatsink as the Si–IGBT modules. As this heatsink is designed to process much higher losses of Si–IGBTs and diodes during nominal operation, an extremely low thermal resistance of the external cooling setup can be expected. Therefore, the equipped circuit shows some room of flexibility and comes with an additional degree of freedom

in terms of operation of the SiC–MOSFET devices (e.g., higher switching frequency to improve the effectiveness of input/output filter (improved THDi) under light-load condition.

4.1.2. Switching Losses of IGBT- and SiC-Based Light-Load Setup

In order to derive the switching losses under the light-load condition, the commutation of both devices (IGBT and MOSFET) has to be studied in detail. For the sake of simplicity switching losses under no-load operation are determined. An occurring switching sequence that is representing the switching losses for one the IGBT device is illustrated in Figure 11. Assuming the initial condition of the negative input current ($x = 0$) and the low-side IGBT is being activated, results in the low-side diode as the current conducting device as the IGBT cannot process negative currents while gated. During the transition from negative to positive values, the input current is commutated from the low-side diode (D_n) to low-side IGBT (S_n) at nearly zero voltage of V_{CE}. Therefore, negligibly small switching losses emerge during this crossover (Figure 11—yellow circle). When S_n is turned OFF, and S_p not turned ON due to the existing dead-time, the current from S_n is commutating to D_p. Therefore, turn-off losses of the low-side IGBT S_n must be considered (Figure 11—purple circle). When the high-side IGBT S_p is activated, the input current will be still free-wheeling through the high-side diode D_p, due to its positive nature. Only when the input current reverses its sign again, the current will commutate from high-side diode D_p to high-side IGBT S_p at approximately zero voltage (Figure 11—yellow square). If the S_p is turned OFF, the input current will transition back to the negative diode D_n. This commutation process results in turn-off losses of the high-side switch S_p occurring at full DC-link voltage (Figure 11—purple square).

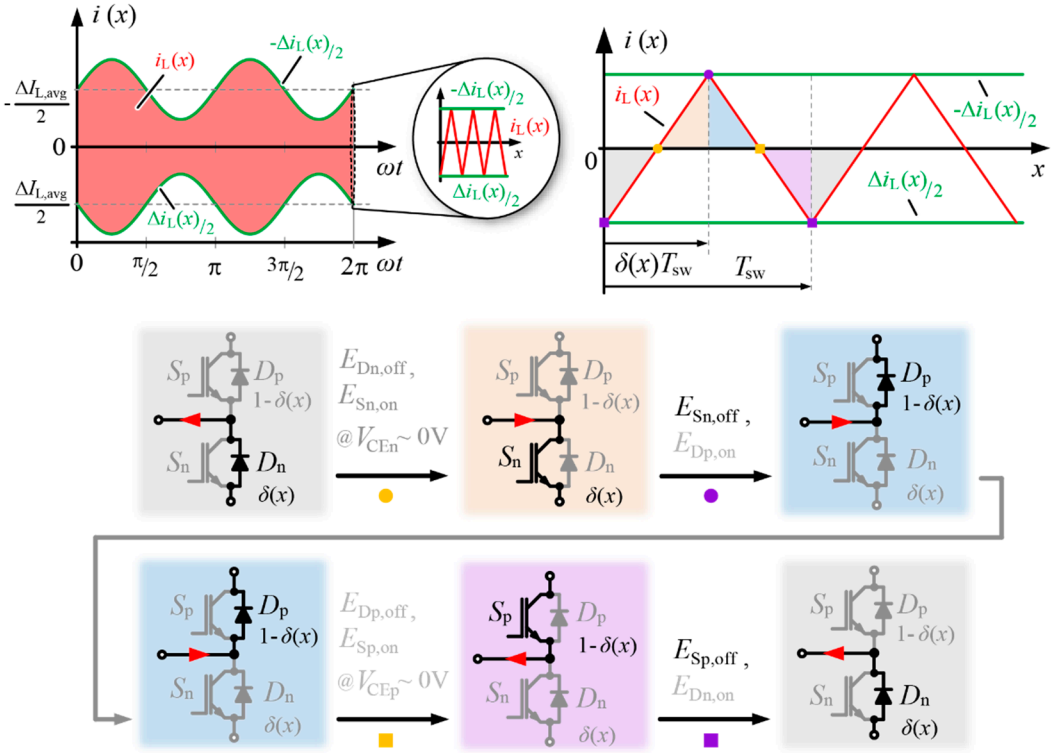


Figure 11. Derivation of switching losses of semiconductors under no-load condition.

For MOSFETs, the sequence is very similar. However, as MOSFETs can conduct current in both directions through the channel during on–state, some additional considerations must be foreseen. For the initial condition, it is considered that the input current is of negative nature, and the low-side MOSFET S_n is already turned ON and conducting current. When S_n is turned-OFF, the input current is

already positive in sign. As the high-side MOSFET S_p is still in OFF state due to the applied dead-time, the current is commutating from the low-side MOSFET to the high-side diode D_p (turn-off losses of low-side MOSFET). After the dead-time has elapsed, the input current transitions from the parasitic diode D_p to the MOSFET channel of S_p. When the high-side MOSFET is turned-OFF again, the input current already reversed in sign again. Thus, the current is handed over to the low-side diode D_n during the envisaged dead-time (turn-off losses high-side MOSFET) and transferred to the low-side MOSFET when turned ON.

Therefore, the total switching losses of each (high-side and low-side) IGBT and MOSFET can be calculated to:

$$P_{sw}\left(V_{DC}, R_g, T_j, f_{sw}\right) = f_{sw}\left(\left(1 - \frac{M^2}{2}\right) \cdot \frac{\Delta I_{L,max}}{2} \cdot k_{off}\left(V_{DC}, R_g, T_j\right) + d_{off}\left(V_{DC}, R_g, T_j\right)\right), \quad (23)$$

under the consideration that the turn-off energy approximately follows a linear characteristic in the respective current region of interest. Switching losses of IGBTs and MOSFETs and dedicated relevant parameters from linearized loss energy curves, which were extracted from the respective datasheets, are listed in Table 5.

Table 5. Turn-off loss characteristics of FF600R12KE4 IGBT and IMZ120R030M1H SiC–MOSFET under consideration of no-load operation.

Parameter	Value
$k_{off,MOS}$ (800 V, 2 Ω, 50 °C)	5 µJ/A
$d_{off,MOS}$ (800 V, 2 Ω, 50 °C)	50 µJ
$k_{off,IGBT}$ (800 V, 0.63 Ω, 50 °C)	120 µJ/A
$d_{off,IGBT}$ (800 V, 0.63 Ω, 50 °C)	4 mJ
$P_{sw,MOS}$ (800 V, 2 Ω, 50 °C, 10 kHz)—no load	1.84 W
$P_{sw,IGBT}$ (800 V, 0.63 Ω, 50 °C, 10 kHz)—no load	72.6 W

As can be observed, the switching losses of the IGBT module under no-load operation and a switching frequency of 10 kHz results in 72.6 W per IGBT, whereas the equipped SiC–MOSFET only comes with 1.84 W.

4.1.3. Total Semiconductor Loss-Overview and Optimization Prospects

Considering the equations from Sections 4.1.1 and 4.1.2, the total semiconductor losses of the three-phase setup with a switching frequency of 10 kHz results in 470 W for all 3 half-bridge IGBT modules and 39 W for 6 SiC–MOSFET semiconductors, respectively. Semiconductor standby losses during no-load operation could thus be improved by over 90% in this specific case. A summary of conduction, switching, and total losses are depicted in Figure 12.

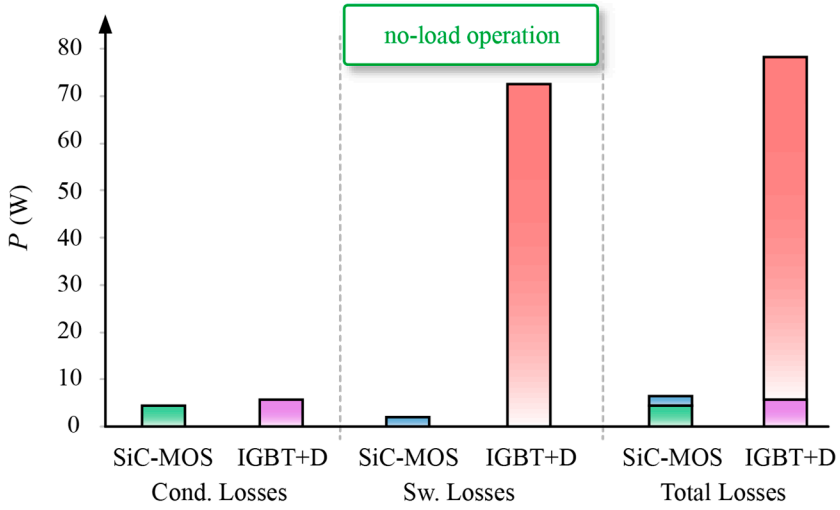


Figure 12. Comparison of conduction and switching losses of light-load SiC MOSFET and high-power IGBT modules under no-load condition.

The dominant part of IGBT related losses is associated with switching losses of the implemented modules. Therefore, a general improvement towards higher efficiency during light- or no-load operation besides a WBG upgrade circuit could be the reduction of the applied switching frequency. This, however, would increase the input inductor volume if the similar current characteristics should adhere.

Regarding the SiC–MOSFET, about 2/3 of all MOSFET related losses are related to conduction losses and 1/3 are originating due to switching losses. For a further loss reduction two different strategies are therefore proposed. First, an additional loss-reduction could be achieved by implementing a SiC device with a slightly larger chip area. Second, adapting (especially enhancing) the switching frequency during light or no-load condition leads to a lower current ripple (hyperbolic function). An investigation on total losses of the SiC–MOSFET at hand under no-load condition shows that the optimum switching frequency for minimum device losses is located around 25 kHz (illustrated in Figure 13).

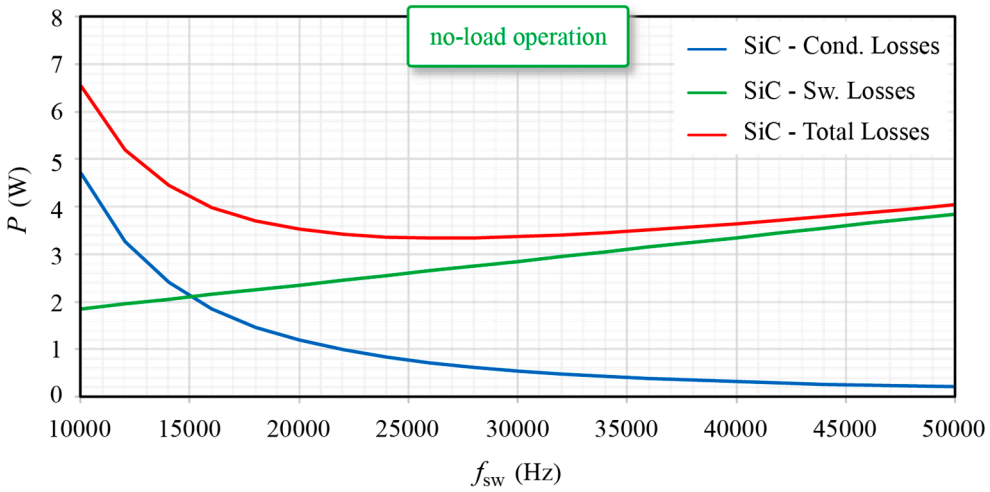


Figure 13. SiC–MOSFET loss optimization due to the adaption of switching frequency during no-load operation.

This phenomenon occurs due the fact that the same inductor of the 125 kW system is utilized for all different occurring load conditions. An enhancement of the switching frequency therefore results in a reduction of the occurring current ripple during light- and no-load operation. A lower current

ripple consequently results in lower conduction losses and increased switching losses (as the negative effect of the switching frequency is outperforming the positive impact of a lower ripple). The optimum switching frequency can be found at the local minimum of the sum of both functions.

4.2. Further Loss Improvements Due to GaN-Based WBG Technology

In Section 2.1, different topologies were presented, which also considered GaN transistor as a possible upgrade for a WBG-based extension circuit. As GaN HEMTs are currently only available up to 650 V maximum blocking voltage, integration into grid-connected power electronics inverters is only feasible in multilevel setups or for three-phase six-switch inverters with lower DC-link voltage (ideally around 400 V). Therefore, a three-phase six-switch setup with a DC-link voltage of 400 V is assumed (e.g., for electric drives). Two different types of switches are compared to each other. For the GaN transistor GaNSystems' GS66508T [18,19] 650 V/30 A was chosen. For the SiC–MOSFET, a ROHM SCT3080AL [20,21] 650 V/30 A device has opted for a reference device. The component characteristics of both SiC and GaN semiconductors are presented in Table 6. In GaN transistor datasheets of mostly all manufacturers, at present, only very little information is included regarding switching losses during hard switched operation. These losses are currently omitted as they are highly dependent on the layout requirements. To get competitive results for a SiC vs. GaN performance comparison under light-load conditions, a double pulse test bench—as illustrated in Figure 14a—was designed.

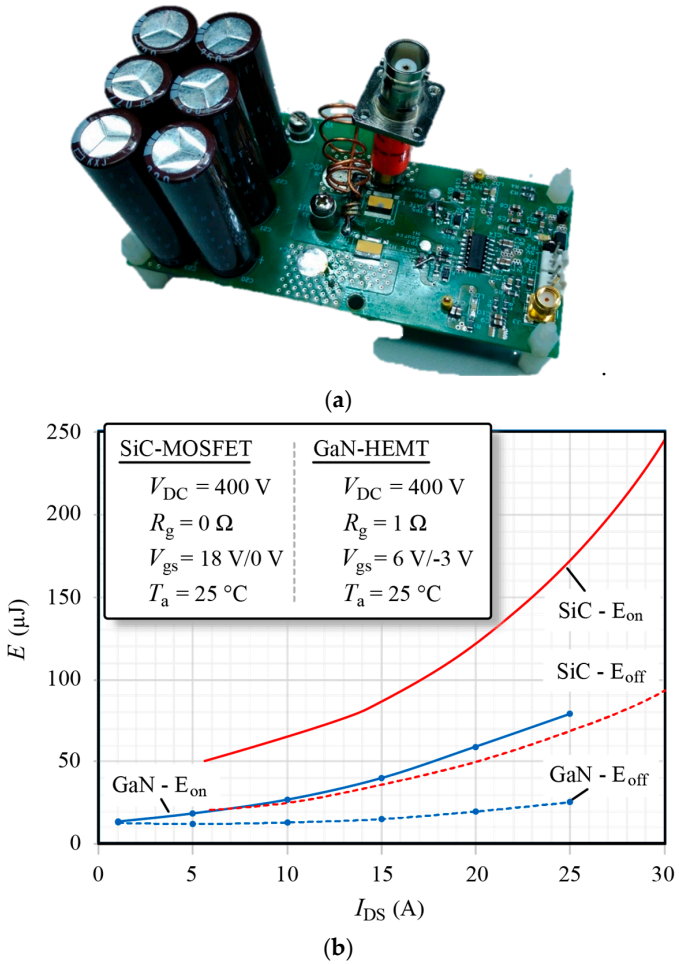


Figure 14. (**a**) Testbench for benchmarking and extraction of turn-on and turn-off switching losses of a 650 V/30 A GaN transistor; (**b**) switching loss comparison of 650 V/30 A SiC–MOSFET and GaN transistor.

Table 6. Relevant SiC MOSFET and GaN transistor parameters.

Parameter	Value
SiC–MOSFET on resistance:	$R_{on,MOS}$ = 80 mΩ
SiC–MOSFET max. blocking voltage	$V_{DS,max}$ = 650 V
SiC–MOSFET cont. drain current (T_C = 25 °C)	$I_{DS,25\,°C}$ = 30 A
GaN transistor on resistance:	$R_{on,GaN}$ = 50 mΩ
GaN transistor max. blocking voltage	$V_{DS,max}$ = 650 V
GaN transistor cont. drain current (T_C = 25 °C)	$I_{DS,25\,°C}$ = 30 A

A coaxial shunt was employed to minimize parasitic inductance of the commutation loop due to inductive coupling or wiring. Figure 14b shows the turn-on and turn-off energy loss comparison of datasheet values of the SiC–MOSFET in conjunction with a dedicated loss map of an equivalent GaN transistor. As can be observed from the data at hand, the GaN transistor will come with both, lower conduction (lower on-resistance compared to SiC MOSFET) and lower switching losses, even though a suboptimal coaxial shunt device was chosen (SDN-414 [22,23]) which includes additional wiring considerably deteriorating parasitic within the measurement setup. Therefore, even lower values than the obtained characteristics can be expected in a final operating setup without a current measurement device.

Care must be taken when junction temperatures beyond 30 °C are of interest. If both datasheets of SiC and GaN device are carefully compared to each other, it can be observed that the on-resistance of the SiC device is less sensitive to an increase in junction temperature (factor of 1.3 for T_j = 25 °C→150 °C) than the according to the parameter of the GaN-transistor, which is notably increasing (factor of >2.5 for ΔT_j = 25 °C→150 °C). Therefore, a crucial aspect could be whether it is possible to attach the equipped WBG circuitry to the existing heatsink of the IGBT setup of the nominal load inverter or not. If a direct connection between the WBG upgrade and the initial heatsink is impossible, an independent cooling strategy must be designed. Due to existing space constraints, its R_{th} will be excessing that one of the IGBT related heatsink and thus either a higher junction temperature of the additional WBG devices will occur (and result in higher conduction losses of a GaN transistor compared to the SiC device) or the critical limit of maximum power under light-load condition must be reduced to sustain low junction temperatures of WBG semiconductors.

5. Conclusions

A light-load optimized WBG extension for existing silicon-based inverters and active rectifiers for different DC-link voltage levels, which (mainly dependent on converter specifications such as switching frequency and loading, operating hours and resulting energy savings) either prefers the utilization of GaN transistors or SiC–MOSFETs was proposed and discussed. The WBG circuit can farther be simplified and optimized in terms of the minimum required WBG semiconductors and thus, cost and payback time of the additional circuitry can be reduced. Furthermore, a design example and loss comparison of a 125 kW three-phase six-switch inverter with additional light-load SiC–MOSFET power stage have revealed that a WBG upgrade can significantly reduce semiconductor losses and boost system efficiency of the proposed solution under light- and no-load condition. A further improvement could be achieved by either using GaN transistors and/or increasing the switching frequency when the light-load circuitry is commencing in operation (compared to the IGBT-based setup). As a follow-up of the current project and its promising results, it is planned to design and realized such a light-load upgrade for a conventional 125 kW inverter and analyze the benefits of the upgraded system.

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Abbreviation

Abbreviation	Meaning
AC	Alternating current
DC	Direct current
FFCS	Flywheel fast-charging system
GaN	Gallium nitride
GD	Gate driver
GHG	Greenhouse gas
IGBT	Insulated-gate bipolar transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
PV	Photovoltaic
PWM	Pulse-width modulation
ROHM	Rohm semiconductor corporation
SiC	Silicon carbide
SiC–MOSFET	Silicon carbide-metal oxide semiconductor field-effect transistor
Si–IGBT	Silicon-insulated-gate bipolar transistor
THD	Total harmonic distortion
WBG	Wide-bandgap
UPS	Uninterruptable power supply

Nomenclature

M	Modulation index
rms	Root mean square
avg	Average value
S_{N}	Nominal apparent power
P_{N}	Nominal active power
Q_{N}	Nominal reactive power
$\mathrm{P_{sw}}$	Semiconductor's switching loss
L_{inv}	Input inductance/phase
D_{p}	High-side diode
D_{n}	Low-side diode
$I_{\mathrm{N,pk}}$	Nominal peak current
$I_{\mathrm{N,rms}}$	Nominal rms current
I_{DS}	Semiconductors cont. drain current
$\lvert\Delta I_{\mathrm{Lmax}}\rvert$	Maximum of peak-to-peak input current ripple
$\lvert\Delta I_{\mathrm{Lmin}}\rvert$	Minimum of peak-to-peak input current ripple
$\Delta I_{\mathrm{L,rms}}$	Input current ripple rms
I_{o}	Output current of the converter
V_{LL}	Mains line-to-line voltage
V_{DC}	Total DC-link voltage
V_{D}	Diode forward voltage
V_{T}	IGBT forward voltage
V_{DS}	Transistor max. blocking voltage
R_{on}	On-resistance of semiconductors
R_{D}	Equivalent resistance of antiparallel diode
f_{sw}	Switching frequency
f_{N}	Mains frequency
Φ	Phase angle
k_{off}	Turn-off switching loss coefficient
ω	Angular frequency
t	Time
φ	ωt

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