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Analysis of Work-Function Variation Effects in a Tunnel Field-Effect Transistor Depending on the Device Structure

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Featured Application: This work can be applied to analyze and reduce the WFV effect of TFETs.

Abstract: Metal gate technology is one of the most important methods used to increase the low on-current of tunnel field-effect transistors (TFETs). However, metal gates have different work-functions for each grain during the deposition process, resulting in work-function variation (WFV) effects, which means that the electrical characteristics vary from device to device. The WFV of a planar TFET, double-gate (DG) TFET, and electron-hole bilayer TFET (EHBTFET) were examined by technology computer-aided design (TCAD) simulations to analyze the influences of device structure and to find strategies for suppressing the WFV effects in TFET. Comparing the WFV effects through the turn-on voltage ($V_{turn\text{-}on}$) distribution, the planar TFET showed the largest standard deviation ($\sigma V_{turn\text{-}on}$) of 20.1 mV, and it was reduced by −26.4% for the DG TFET and −80.1% for the EHBTFET. Based on the analyses regarding metal grain distribution and energy band diagrams, the WFV of TFETs was determined by the number of metal grains involved in the tunneling current. Therefore, the EHBTFET, which can determine the tunneling current by all of the metal grains where the main gate and the sub gate overlap, is considered to be a promising structure that can reduce the WFV effect of TFETs.

Keywords: tunnel field-effect transistors (TFETs); work-function variation (WFV); electron-hole bilayer TFET (EHBTFET)

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1. Introduction

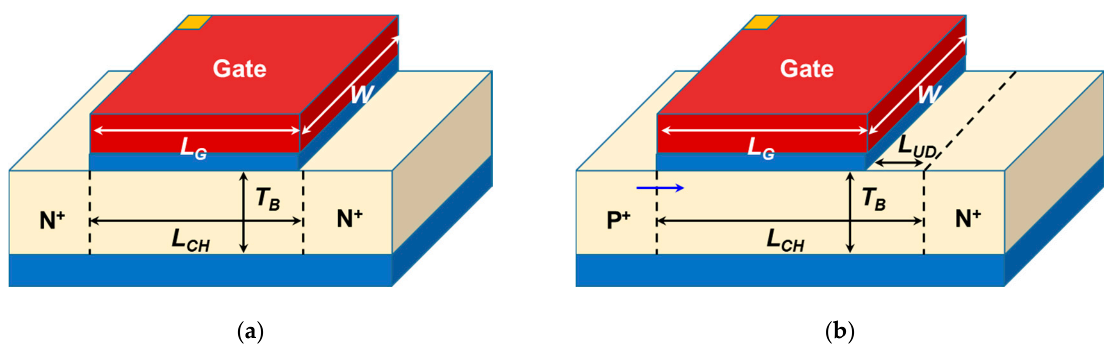
The trend towards reducing the power consumption and improving the scale-down properties of complementary metal-oxide semiconductor (CMOS) devices results in a decreased voltage supply. To achieve a high on/off current ratio at a low supply voltage, the subthreshold swing (SS) must be lowered. However, metal-oxide-semiconductor (MOS) field-effect transistors (MOSFETs) cannot lower the SS below 60 mV/dec due to the physical limitations of their operation [1–3]. To overcome this problem, new devices based on various principles have been proposed and studied, such as the negative capacitance field-effect transistor (NCFET) [4–6], resistive gate field-effect transistor (FET) (ReFET) [7], nano-electro mechanical FET (NEMFET) [8,9], positive feedback FET [10,11], impact ionization metal-oxide-semiconductor (I-MOS) [12,13], conventional transistor with an oxide-based threshold switching device [14], and tunnel FET (TFET) [15–22]. Among them, TFETs are considered

as one of the most promising ultra-low power devices due to its high CMOS process compatibility and low-level leakage current [15–22].

However, TFETs suffer from low-level on-current (I_{on}) as an alternative of MOSFETs. Therefore, there have been much research to improve the I_{on} of TFETs by modifying the materials and structures of TFETs [23–31]. Among them, metal gate technology, which is also widely used in MOSFETs, can improve the gate controllability and increase I_{on} by eliminating the polysilicon depletion effect [32]. However, metal gates have different work-functions for each grain due to different grain orientations during the deposition process. This results in a work-function variation (WFV) effect that causes variations in the threshold voltage (V_{th}) and other electrical characteristics of TFETs [33]. In this study, the WFV effects of a planar TFET, a double gate (DG) TFET, and an electron-hole bilayer TFET (EHBTFET) are compared using technology computer-aided design (TCAD) simulations to analyze the effects of the structure and to find a way to improve the WFV of TFETs. In the case of the planar TFET and DG TFET, a tunneling current occurs along the channel (lateral tunneling) at the source junction. On the contrary, the tunneling current of the EHBTFET is generated across the channel (vertical tunneling) at the body between two gates, and the electrical characteristics of this structure have been actively studied through TCAD simulations and modeling [34–38].

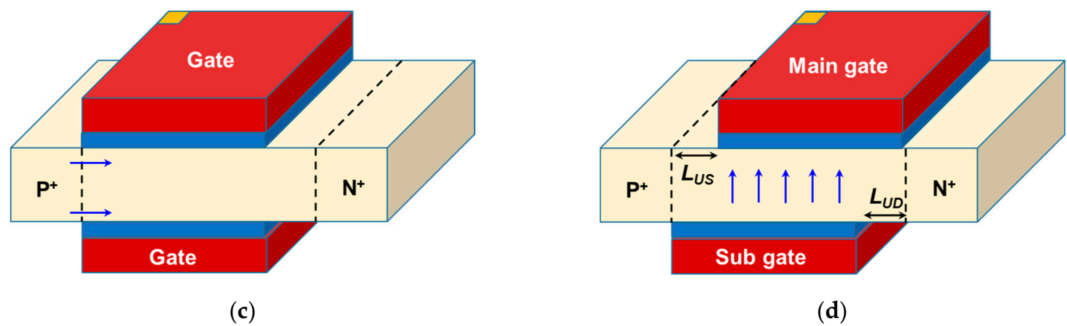
2. Device Structure and Simulation Method

Figure 1 shows the structures of MOSFET (Figure 1a), planar TFET (Figure 1b), DG TFET (Figure 1c), and EHBTFET (Figure 1d) used in this research. The design parameters used for the simulations are summarized in Table 1. In the modern integrated chip (IC) process, the grain size of the metal gate has a range of approximately 5 to 20 nm [39,40]. The grain size decreases when the DC (direct current) power of the sputtering process increases [40]. On the other hand, the grain size increases when the process temperature increases during or after the deposition process [39,41]. In this research, TiN (titanium nitride) was applied as the gate metal for the WFV effect analysis. In the case of TiN, it is also known that the grain size can be reduced by incorporating Cu or C when the TiN layer is deposited [42,43]. In this simulation and analysis, each metal grain was assumed to be a cube with a side length of 10 nm within the general range of the modern IC process. With regard to the WF value distribution of TiN, much research is still on-going, in order to develop a better understanding of the WF variation in TiN (e.g., considering the work-function (WF) of the grain boundary [44] and increment of the high-WF grain portion with the increased process temperature [41]). In this study, it was assumed that 60% of TiN grains were crystallized in <200> with 4.6 eV WF and 40% were crystallized in <111> with 4.4 eV WF, which are generally accepted values [39]. The blue arrows in Figure 1 indicate the positions where the tunneling mainly occurs in the on-state of each structure. Unlike the planar TFET and DG TFET, where tunneling occurs at the boundary between the source and channel region, EHBTFET has a tunneling current between the main gate (MG) and the sub gate (SG), as shown by the arrow in Figure 1d.



(a) (b)

Figure 1. *Cont.*



(c) (d)

Figure 1. Basic schematics and major parameter definitions of the (**a**) metal-oxide-semiconductor field-effect transistor (MOSFET), (**b**) planar tunnel field-effect transistor (TFET), (**c**) double-gate (DG) TFET, and (**d**) electron-hole bilayer TFET (EHBTFET) used in this research.

Table 1. Device parameters of devices used for the technology computer-aided design (TCAD) simulation.

Parameter	Value
Gate length (L_G)	70 nm
Channel width (W)	70 nm
Equivalent oxide thickness (EOT)	2 nm
Channel length (L_{CH})	90 nm
Channel thickness (T_B)	10 nm
Drain underlap (L_{UD})	20 nm
Source underlap (L_{US})	20 nm
MOSFET source/drain doping concentration	10^{20} cm^{-3}
TFET *p*-type source doping concentration	10^{20} cm^{-3}
TFET *n*-type drain doping concentration	10^{18} cm^{-3}
Gate work function	4.6 eV (60%) 4.4 eV (40%)

In order to compare and analyze the WFV effects of each structure, three-dimensional (3D) simulations were conducted using Synopsys Senataurus^{TM} (Ver. K-2015.06-SP1, Synopsys, Mountain View, CA, USA) [45]. Fermi–Dirac statistics, doping concentration dependent mobility, Shockley–Read–Hall (SRH) recombination, and modified local density approximation (MLDA) models were used to calculate and extract the electrical characteristics of TFETs in the simulation. For an accurate calculation of band-to-band tunneling (BTBT), a dynamic non-local BTBT model was applied with theoretically calculated parameters [46] generally used in recent TFET research [47–49].

3. Results and Discussions

Figure 2 shows the transfer characteristics of the MOSFET, planar TFET (Figure 2b), DG TFET (Figure 2c), and EHBTFET (Figure 2d) when the drain voltage (V_D) is 0.5 V and source voltage (V_S) is 0 V. The metal grain profiles of the gate area were randomly generated by the randomization algorithm provided in the Sentaurus tool, depending on the TiN grain orientation. Thirty samples with uniquely randomized metal gate grain profiles for each structure were used for the simulation and the WFV effect analysis in this research. In the case of the EHBTFET in Figure 2c, a voltage of −0.67 V was applied to the SG to transport the holes from the source region to the channel region near SG and generate BTBT between the MG and the SG. For a comparison of the WFV effects, the average and standard deviation of V_{th}, SS and I_{on} for each structure were obtained and are summarized in Table 2. The V_{th} of MOSFET is defined as the gate voltage when V_D is 0.5 V and the drain current is 10^{-12} A. Instead of V_{th}, the turn-on voltage ($V_{turn\text{-}on}$) of TFETs is defined as the gate voltage when BTBT starts to occur at the source junction and the drain current increases compared to the leakage current, and is extracted when V_D is 0.5 V and the drain current is 10^{-18} A. In this research, $V_{turn\text{-}on}$ was used for the WFV analysis instead of V_{th}, because the drain current of TFETs is much lower than that of MOSFETs,

the definition of V_{th} in TFETs is controversial [50,51], and the SS variation effect of TFETs is large [33]. SS is defined as an average swing when the drain current is increased from 10^{-12} to 10^{-10} A (MOSFET) or 10^{-18} to 10^{-16} A (TFET). I_{on} is defined as the drain current when V_G is average $V_{turn\text{-}on}$ (average V_{th} in MOSFETs) + 0.6 V and V_D is 0.5 V. As shown in Figure 2 and Table 2, the $\sigma V_{turn\text{-}on}$ of the planar TFET has the largest value (20.1 mV). In the case of the DG TFET, $\sigma V_{turn\text{-}on}$ is reduced by −26.4% in comparison to the planar TFET. Moreover, in the EHBTFET, the $\sigma V_{turn\text{-}on}$ is drastically reduced to −80.1% compared to the planar TFET, showing the smallest $\sigma V_{turn\text{-}on}$ among the three types of TFET structures. The σSS and normalized σI_{on} also show the same tendency as $\sigma V_{turn\text{-}on}$.

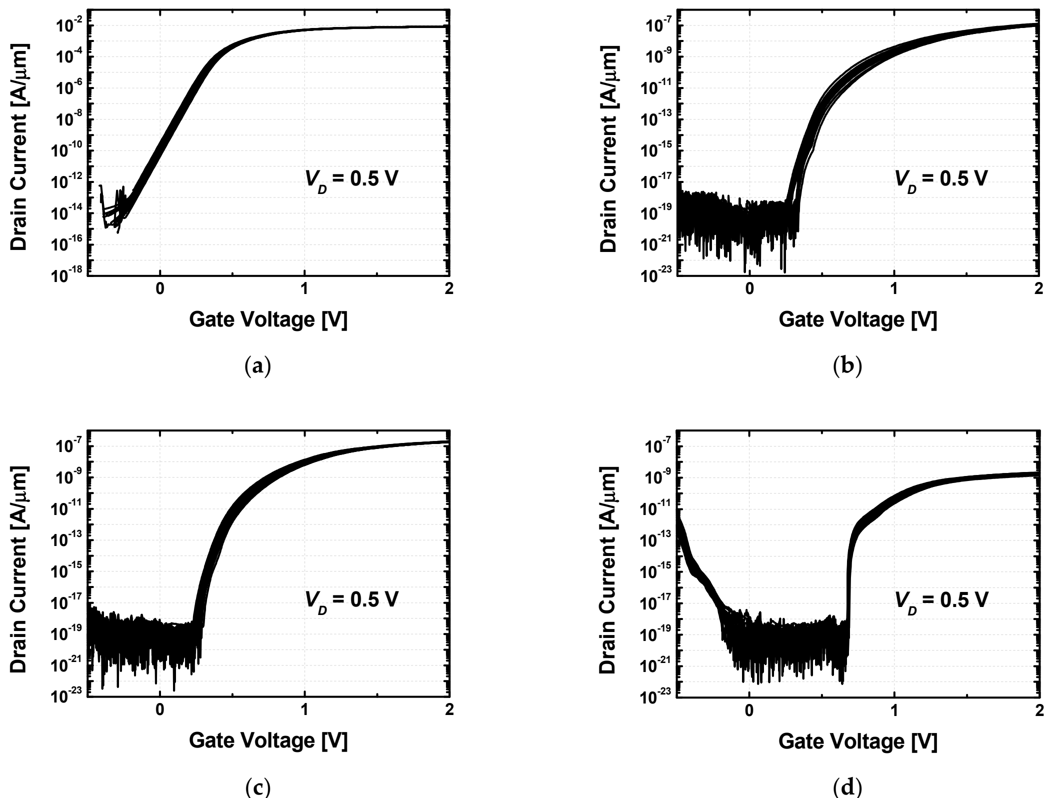


Figure 2. Transfer characteristics of the (**a**) MOSFET, (**b**) planar TFET, (**c**) DG TFET and (**d**) EHBTFET when the drain voltage (V_D) is 0.5 V.

Table 2. Average and standard deviation of the turn-on voltage ($V_{turn\text{-}on}$), subthreshold swing (SS), and on-current (I_{on}) of the devices extracted from Figure 2.

	MOSFET	Planar TFET	DG TFET	EHBTFET
Average V_{th} or Average $V_{turn\text{-}on}$	−55.0 mV	325.1 mV	283.0 mV	680.4 mV
σV_{th} or $\sigma V_{turn\text{-}on}$	14.0 mV	20.1 mV	14.8 mV	4.0 mV
Average SS	121.6 mV/decade	64.3 mV/decade	54.5 mV/decade	4.6 mV/decade
σSS	0.5 mV/decade	5.6 mV/decade	4.7 mV/decade	1.2 mV/decade
Average I_{on}	7.11×10^{-4} A/μm	1.08×10^{-9} A/μm	3.26×10^{-9} A/μm	4.33×10^{-10} A/μm
σI_{on}/Average I_{on}	0.122	0.348	0.263	0.155

V_{th}: threshold voltage.

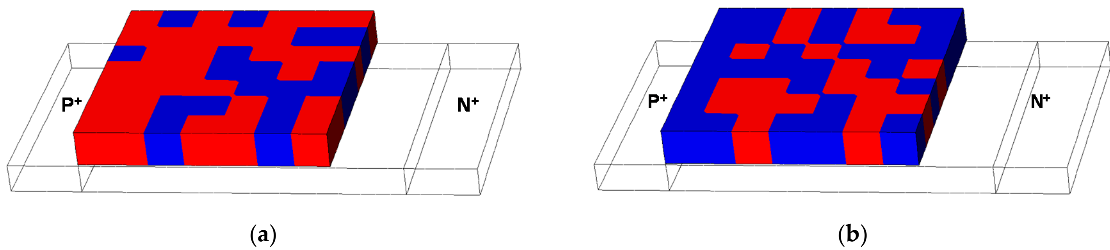
The reduction in the WFV effect on the DG TFET and EHBTFET compared to the planar TFET can be interpreted as a result of an increase in the number of metal grains that affect $V_{turn\text{-}on}$ determination. It is known that as the number of metal grains affecting $V_{turn\text{-}on}$ increases, the WFV effect is suppressed by a higher averaging effect [52–54]. When the number of grains changes, the variance of the WF

distribution (var(Φ_M)) according to the number of grains (N) can be expressed as the following equation [55]:

$$\text{var}(\Phi_M) = \frac{1}{N}\left[\sum_{i=1}^{r} P_i\Phi_i^2 - \left(\sum_{i=1}^{r} P_i\Phi_i\right)^2\right] \quad (1)$$

where Φ_i and P_i represent the WF value of each grain and the probability of achieving the WF value. As can be seen from (1), var(Φ_M) and the resulting WFV effects change when N changes. For example, as the grain size of the metal gate increases during the fabrication process (e.g., increase in the heat budget), the number of grains affecting the characteristics of the device decreases and the WFV effects increase. If the grain size is large enough that the overall gate area is filled by one metal grain, the $V_{turn\text{-}on}$ of 60% of devices is determined by a metal grain with a 4.6 eV WF and the $V_{turn\text{-}on}$ of the other 40% of devices is determined by a metal grain with a 4.4 eV WF. On the other hand, when the grain size of the metal gate is reduced during the fabrication process (e.g., by incorporating carbon into TiN), the WFV effects can be reduced [43]. If the grain size is continuously reduced and the metal gate reaches an almost amorphous state, it can be considered that there is no difference among the grain distributions of each device and the $V_{turn\text{-}on}$ values of all the devices converge to the average $V_{turn\text{-}on}$.

As the grain size controlled by the process condition can affect the number of grains and the WFV effects, the device structure of TFETs can also affect the WFV effect if the structure can change the grain number, having effects on the $V_{turn\text{-}on}$ determination. In order to analyze the reason why the $\sigma V_{turn\text{-}on}$ of the TFETs is different, depending on the structures, the metal grain distributions and the energy band diagrams were compared for the lowest and highest $V_{turn\text{-}on}$ among the simulated results of planar TFETs with the randomly generated metal grain profiles. Figure 3a,b show the metal grain distributions of planar TFETs, with the highest value of $V_{turn\text{-}on}$ at 0.367 V and the lowest value at 0.289 V, respectively. In the gate region of Figure 3a,b, a red color represents metal grains with WF of 4.6 eV, while a blue color shows other grains with WF of 4.4 eV. Comparing Figure 3a,b, there is a clear difference between the two samples in terms of the distribution of metal grains adjacent to the source region. Figure 3a, with high $V_{turn\text{-}on}$, shows that most of the metal grains close to the source region have a WF of 4.6 eV, while Figure 3b, with low $V_{turn\text{-}on}$, shows that there are more metal grains with a WF of 4.4 eV around the source region.



(**a**) (**b**)

Figure 3. Metal grain distributions of planar TFETs in extreme cases (red color: metal grains with a work-function (WF) of 4.6 eV, and blue color: metal grains with a WF of 4.4 eV) among the simulated samples. (**a**) Maximum $V_{turn\text{-}on}$ (0.367 V) case of planar TFETs. (**b**) Minimum $V_{turn\text{-}on}$ (0.289 V) case of planar TFETs.

Figure 4 shows the energy band diagrams of these two extreme cases of planar TFETs when V_D is 0.5 V and V_G is 0.4 V. Due to the difference in the distribution of the metal grains analyzed above, the energy band bending between the source and the channel region becomes larger in the case of $V_{turn\text{-}on}$ = 0.289 V (red dash line) than in the case of $V_{turn\text{-}on}$ = 0.367 V (black solid line). As a result, when the same V_G is applied, there is a difference in the tunneling width of the two cases and accordingly, the V_{th} is also different. As described above, the planar TFET is relatively vulnerable to the WFV effect, as the V_{th} of the planar TFET is only determined by the energy band of the channel adjacent to the source region, while the V_{th} of the conventional MOSFET is determined by the entire

channel under the gate [33]. In the metal grain distributions shown in Figure 3a,b, planar TFETs have a $\Delta V_{turn\text{-}on}$ of 78 mV (0.367 V–0.289 V) between the two cases. On the other hand, the DG TFET and EHBTFET show a $\Delta V_{turn\text{-}on}$ of 65 mV (0.371–0.306 V) and 5 mV (0.685–0.679 V), respectively, when one of two gates has the same metal grain distribution, as shown in Figure 3a,b.

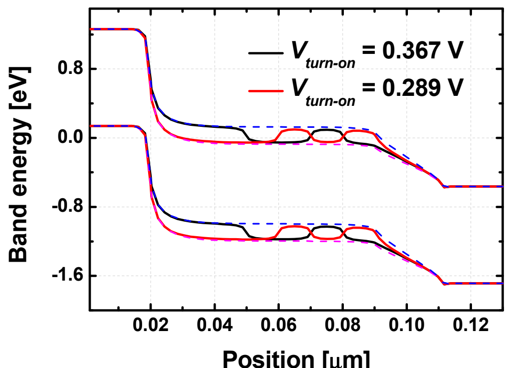


Figure 4. Energy band diagrams of planar TFETs with the highest value of $V_{turn\text{-}on}$ at 0.367 V (black solid line) and the lowest value of $V_{turn\text{-}on}$ at 0.289 V (red solid line) among the simulated samples when V_D is 0.5 V and V_G is 0.4 V. The blue dashed line and magenta dashed line show the most extreme cases in theory when the entire gate of the planar TFET is 4.6 and 4.4 eV, respectively.

As confirmed in the analysis of Figures 3 and 4, only seven metal grains near the source junction mainly affect the tunneling current and the $V_{turn\text{-}on}$ of the planar TFET. Meanwhile, in the case of DG TFETs, the addition of another gate on the opposite side doubles the number of metal grains (14 metal grains) that affect the tunneling current and reduces the effect of WFV. Unlike the planar TFET or DG TFET, in the on-state of the EHBTFET, electrons are collected under MG and holes are collected under SG. As the bias of MG increases, energy band bending and a tunneling current are generated in the channel between the two gates. The EHBTFET has a tunneling current at the channel between MG and SG, and all of the metal grains (70 metal grains) where MG and SG overlap are included in $V_{turn\text{-}on}$ determination, which greatly reduces the effect of WFV.

This analysis can be confirmed indirectly by comparing the probabilities of the most extreme theoretical cases of the planar TFET, DG TFET and EHBTFET. As discussed above, the $V_{turn\text{-}on}$ of the planar TFET and DG TFET is controlled by the metal grains near the source. Therefore, the planar TFET has the maximum value of $V_{turn\text{-}on}$ when all WFs of seven metal grains adjacent to the source are 4.6 eV and the minimum $V_{turn\text{-}on}$ when they are all 4.4 eV; the probabilities are 2.8% (0.6^7) and 0.2% (0.4^7), respectively. Similarly, for the DG TFET, the probability of the maximum $V_{turn\text{-}on}$ is 7.8×10^{-2}% (0.6^{14}) and the probability of the minimum $V_{turn\text{-}on}$ is 2.7×10^{-4}% (0.4^{14}). In the case of the EHBTFET, as tunneling occurs from the valence band of the channel near SG to the conduction band of the channel near MG, the $V_{turn\text{-}on}$ reaches the maximum when all MG grains have a WF of 4.6 eV and all SG grains have a WF of 4.4 eV where MG and SG overlap, as shown in Figure 5a; its probability is 2.0×10^{-20}% ($0.6^{35} \times 0.4^{35}$). Additionally, in the opposite case, as shown in Figure 5b, the $V_{turn\text{-}on}$ reaches the minimum and its probability is equal to the probability of the maximum $V_{turn\text{-}on}$. By comparing the probabilities of the most extreme cases in the three structures, it was confirmed that the EHBTFET has the smallest probabilities, and this difference is caused by the difference in the number of metal grains that affect the $V_{turn\text{-}on}$.

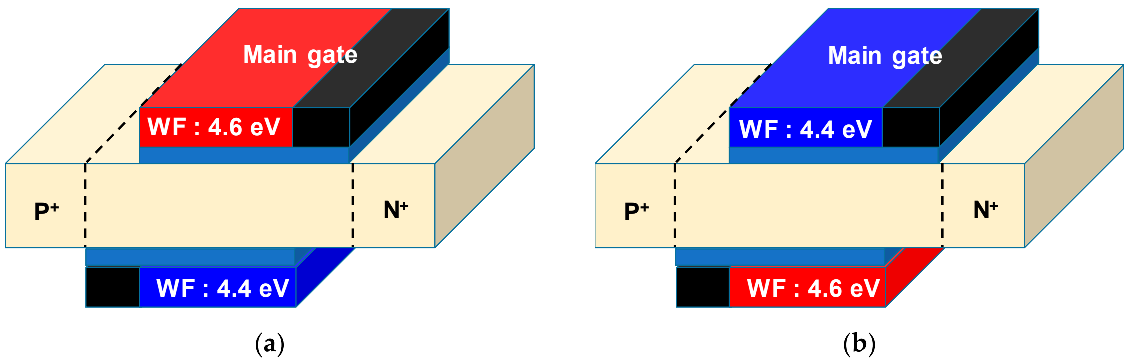


Figure 5. Expected metal grain distributions of EHBTFETs in the most extreme theoretical cases (red color: metal grains with a WF of 4.6 eV, blue color: metal grains with a WF of 4.4 eV, and black color: metal grains that have less effect on the $V_{turn\text{-}on}$ of EHBTFET). (**a**) Expected maximum $V_{turn\text{-}on}$ case of EHBTFETs in theory. (**b**) Expected minimum $V_{turn\text{-}on}$ case of EHBTFETs in theory.

In order to prove that the WFV improvement of the EHBTFET is due to the large number of metal grains, the $\sigma V_{turn\text{-}on}$ of the planar TFET, DG TFET, and EHBTFET was examined while reducing the L_G of the EHBTFET, as shown in Figure 6. The WFV effects of the planar TFET and DG TFET were determined by the metal grains located at the edge between the source and the channel. Therefore, the $\sigma V_{turn\text{-}on}$ of the planar TFET and DG TFET is not significantly affected by the change in the gate length. On the other hand, when the L_G of the EHBTFET decreases, the number of metal grains in the overlapping areas of MG and SG decreases and the $\sigma V_{turn\text{-}on}$ of the EHBTFET increases accordingly. By comparing when L_G was 70 nm and when L_G was 30 nm, it can be seen that the $\sigma V_{turn\text{-}on}$ of the EHBTFET increased from 4.0 to 9.9 mV as the number of metal grains affecting the tunneling current decreased from 70 to 14, respectively. Therefore, if L_G continues to decrease, the WFV effects of the EHBTFET are expected to be similar to those of other TFET structures. In addition, the electrical performance (e.g., I_{on}) also degrades as the tunneling area (i.e., overlap area between main and sub gates) of the EHBTFET decreases with the smaller L_G. Consequently, when the scaling down of TFETs continues, it is necessary to maintain the L_G by using a vertical channel [38] to maintain the advantages of the EHBTFET in the WFV effects.

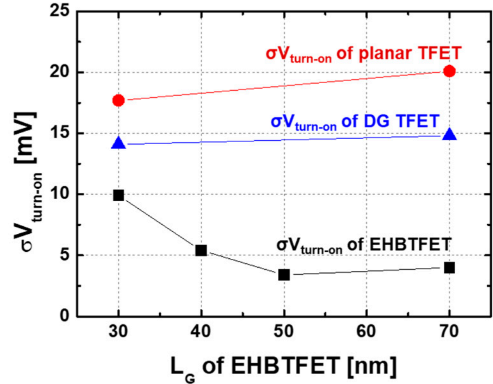


Figure 6. The $\sigma V_{turn\text{-}on}$ of the planar TFET, DG TFET, and EHBTFET when the L_G is changed. While reducing the L_G, the L_{CH} is reduced by the same length, and L_{UD} and L_{US} are kept at 20 nm.

4. Conclusions

In this research, the WFV effects of the planar TFET, DG TFET, and EHBTFET were compared and analyzed by TCAD simulation. As a result of extracting the $\sigma V_{turn\text{-}on}$ and examining the metal grain distributions, it was confirmed that the planar TFET has the greatest WFV effect because only a few metal grains around the source region affect the $V_{turn\text{-}on}$. On the other hand, the EHBTFET is the

most immune from the WFV effect, as all of the metal grains where MG and SG overlap determine the $V_{turn\text{-}on}$.

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Conflicts of Interest: The authors declare no conflict of interest.

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