Small-Signal Analysis and Control of Soft-Switching Naturally Clamped Snubberless Current-Fed Half-Bridge DC/DC Converter

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Abstract: This paper presents small-signal analysis of a soft-switching naturally clamped snubberless isolated current-fed half-bridge (CFHB) DC-DC converter using state-space averaging. A two-loop average current controller was designed and implemented on a digital signal processor. The complete design procedure is presented here. Simulation results using software PSIM 11.1 are shown to validate the stability of the control system and the controller design. Experimental results for the step changes in load current vividly demonstrated satisfactory transient performance of the converter and validated the developed small-signal model and the control design.

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1. Introduction

Electric transportation, energy storage, renewable energy systems, hybrid electric vehicles (HEV), and fuel cell vehicles require bidirectional power electronics for power processing [1–4]. A DC-DC front-end converter is the major part of a fuel cell inverter, which boosts the low-voltage fuel cell stack's voltage to the peak of utility line alternating current (AC) voltage [5]. Among various categories of high-frequency (HF) soft-switching isolated DC-DC converters, a current-fed converter is popular in fuel cell applications. Fuel cells produce low-voltage direct current (DC), which has a wide variation with load current and requires a high voltage conversion ratio [6–10]. Current-fed topologies offer high voltage gain with a stiff DC input current [11]. The historical problem with current-fed converters has been the necessity of a passive snubber [12,13] or an active-clamping circuit [14–16] to clamp voltage overshoot across the semiconductor devices at their turn-off. Passive snubbers lead to poor efficiency because the energy stored by the clamping capacitor is later dissipated into the resistor. However, better efficiency is obtained, along with zero voltage switching (ZVS) of the semiconductor devices, with an active-clamping circuit [14–16], at the cost of additional footprints of floating active device(s) and a large HF clamp capacitor for accurate and effective voltage clamping. Additionally, the boost factor of the converter is reduced as well as the high peak, and circulating currents can be observed at light load. In [17], a new modulation technique of high-voltage side devices was proposed to solve the voltage spike problem of primary devices, eliminating the requirement for an external snubber. A current-fed half-bridge DC-DC converter was proposed as shown in Figure 1 with a new modulation,

which was studied in [17] to achieve zero current switching (ZCS) commutation of semiconductor devices along with natural device voltage clamping.
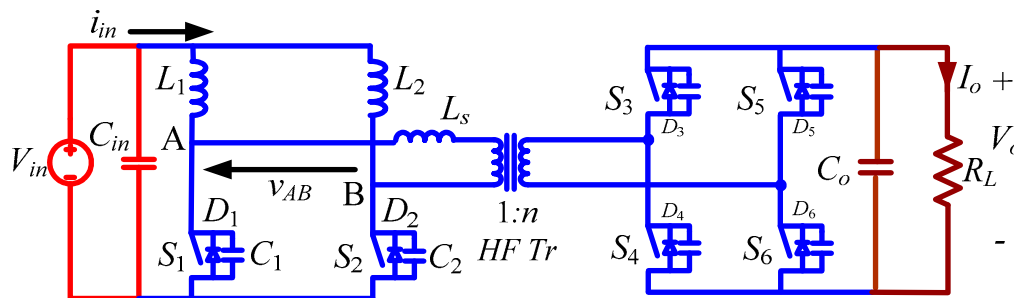

Figure 1. The zero current switching (ZCS) naturally clamped current-fed half-bridge isolated DC-DC converter. Reproduced with permission from [17], IEEE, 2020.

Steady-state analysis, power circuit design, and steady-state experimental performance results of the converter have previously been presented in [17]. However, its small-signal modeling, controller design, and dynamic performance results have not yet reported. The authors reported the small-signal modeling and derived the transfer functions in [18]. Controller design and simulation results were presented to show initial results and investigation on the transient performance of the converter. This paper presents systematic small-signal analysis and experimental results to demonstrate the closed-loop dynamic performance of the converter.

2. Small-Signal Analysis

The following procedure was followed to derive the small-signal model and converter transfer functions:

(1)　Make assumptions
(2)　Define state variables
(3)　Write state equations for each interval of operation
(4)　Average the state equations over a switching cycle
(5)　Introduce perturbation in state variables
(6)　Equate AC and DC quantities and proceed with AC equations
(7)　Take Laplace transform
(8)　Prepare matrix small-signal model
(9)　Calculate desired transfer functions

The following assumptions were made for the small-signal modeling of the converter: (1) all the power semiconductor devices are lossless and ideal; (2) inductors L_1 and L_2 are large enough to maintain constant current through them; (3) inductor L_s includes the leakage inductance of the HF transformer; steady-state operating waveforms are shown in Figure 2; (4) snubber/device capacitance charging and discharging intervals are short and neglected.

The primary side devices S_1 and S_2 are operated with identical gating signals phase-shifted with each other by 180°. The duty cycle of the primary switches is always kept above 50%. The operation during different intervals in a one-half switching cycle is explained with equivalent circuits shown in Figure 3.
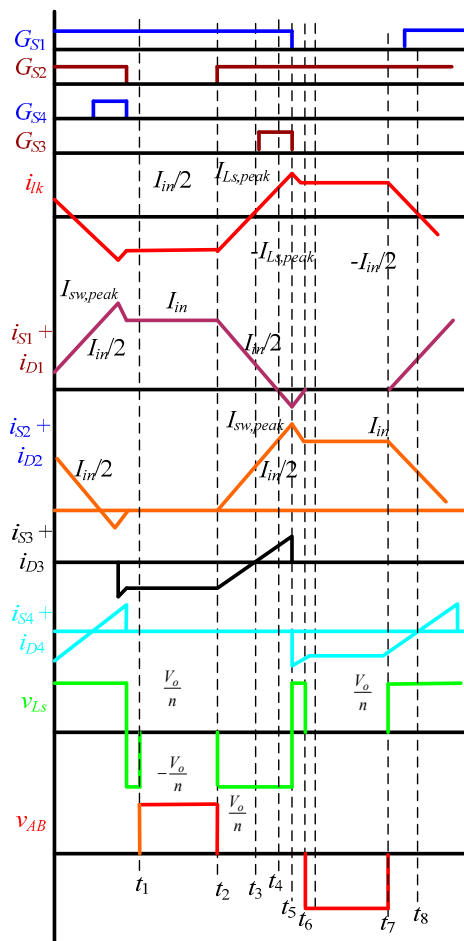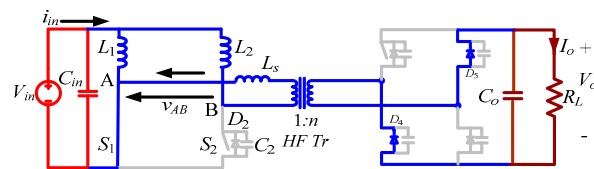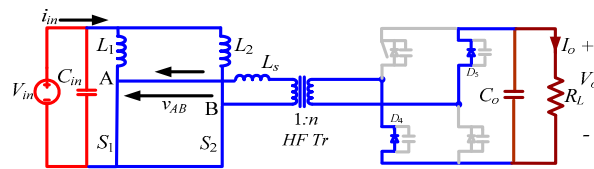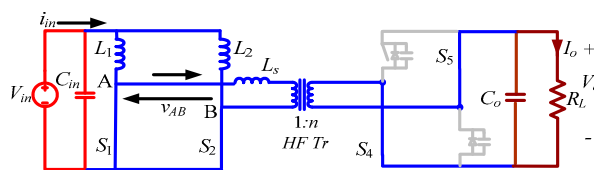
Figure 2. Operating waveforms of the ZCS current-fed converter shown in Figure 1. Reproduced with permission from [17], IEEE, 2020.

(**a**)

(**b**)

(**c**)

Figure 3. *Cont.*
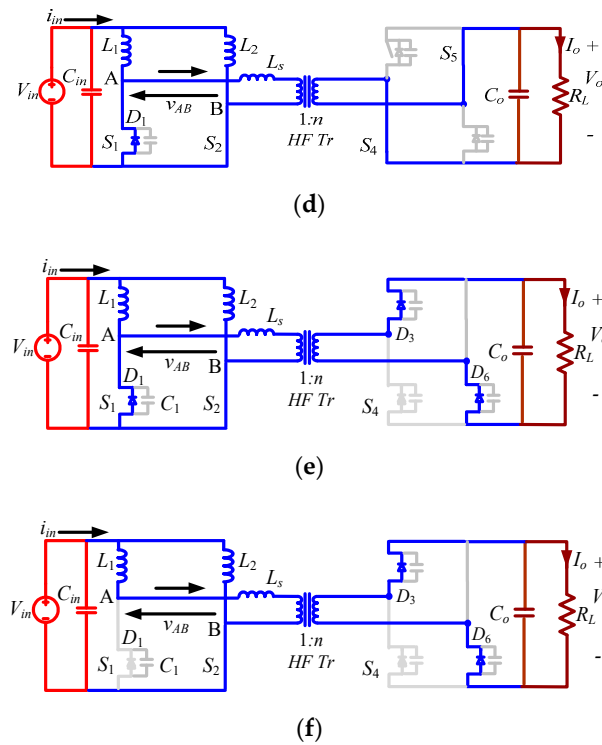
(d)

(e)

(f)

Figure 3. Equivalent circuits during different intervals of the operation for the waveform in Figure 2 Reproduced with permission from [17], IEEE, 2020. (**a**) S_2 in blocking mode; (**b**) S_2 is turned-on; (**c**) ZVS turn-on of S_4 and S_5; (**d**) ZCS turn-off of S_1 and body diode conducts; (**e**) D_3 and D_6 start conduction for rectification; (**f**) S_1 goes in blocking mode.

State variables defined for the small-signal modeling of the converter are: (1) currents through the transformer leakage inductor i_{lk1} and i_{lk2}; (2) input inductor current i_{in}; (3) output voltage v_o; (4) input voltage v_{in}; (5) duty cycle loss d.

Interval 1 (Figure 3a; $t_1 < t < t_2$)

During this interval, primary side switch S_1 and anti-parallel body diodes D_4 and D_5 of secondary switches are conducting to rectify the HF AC waveform across the transformer secondary. Power is transferred to the load through an HF transformer. Transformer primary current is negative and constant. Switch S_1 is carrying the entire input current. State equations of this interval are:

$$L_1 \frac{di_{L1}}{dt} = v_{in} \tag{1}$$

$$L_1 \frac{di_{L1}}{dt} = v_{in} \tag{2}$$

$$C_o \frac{dv_o}{dt} = \frac{i_{L_s}}{n} - \frac{v_o}{R_L} \tag{3}$$

$$L_s \frac{di_{Ls}}{dt} = 0 \tag{4}$$

Interval 2 (Figure 3b; $t_2 < t < t_3$)

Primary side switch S_2 is turned on and starts conducting. The current from S_1 is transferred to the switch S_2 through the transformer primary winding with a slope limited by transformer leakage inductance L_s. State equations of this interval are:

$$L_2 \frac{di_{L2}}{dt} = v_{in} \tag{5}$$

$$L_s \frac{di_{Ls}}{dt} = \frac{v_o}{n} \tag{6}$$

Interval 3 (Figure 3c; $t_3 < t < t_4$)

Secondary side devices S_4 and S_5 are turned on with ZVS. The current waveforms follow the same pattern and slope. State equations of interval 2 still hold good.

Interval 4 (Figure 3d; $t_4 < t < t_5$)

Primary side device S_1 turns off with ZCS, and its anti-parallel body diode starts conducting. State equations of interval 2 still hold good.

Interval 5 (Figure 3e; $t_5 < t < t_6$)

Secondary side devices S_4 and S_5 are forced commutated, and anti-parallel body diodes D_3 and D_6 of secondary switches take over the current.

$$L_s \frac{di_{Ls}}{dt} = -\frac{V_o}{n} \tag{7}$$

Equations (1), (3), and (5) hold good for inductor currents i_{L1}, i_{L2}, and output capacitor c_o.

Identically, state equations for the other half-cycle can also be derived. State equations are averaged over an HF cycle. The average value for the rate of change of i_{Ls} over one complete HF cycle is zero, and the averaged state equation is:

$$L_s \langle \frac{di_{Ls}}{dt} \rangle = 0 \tag{8}$$

So, the state variable i_{Ls} is omitted for the following analysis. Define: $d_1 T_s = t_2 - t_1, d_2 T_s = t_3 - t_2, d_3 T_s = t_4 - t_3, d_4 T_s = t_5 - t_4, d_5 T_s = t_6 - t_5, d_6 T_s = t_7 - t_6, d_7 T_s = t_8 - t_7, d_8 T_s = = t_9 - t_8, d_9 T_s = t_{10} - t_9, d_{10} T_s = t_s - t_{10}$.

The averaged state equations of defined state variables over an HF cycle are given:

$$L_1 \langle \frac{di_{L1}}{dt} \rangle = v_{in} - d_6 \frac{v_o}{n} \tag{9}$$

$$L_2 \langle \frac{di_{L2}}{dt} \rangle = v_{in} - d_1 \frac{v_o}{n} \tag{10}$$

$$C_o \langle \frac{dv_o}{dt} \rangle = i_{average} - \frac{v_o}{R_L} \tag{11}$$

where $i_{average}$ is the average current feeding the output capacitor and load from secondary side H-bridge switches and is given by:

$$i_{average} = \frac{i_{L2}}{n}(d_1) + \frac{i_{L1}}{n}(d_6) \tag{12}$$

Substituting Equation (12) into Equation (11) gives:

$$C_o \frac{dv_o}{dt} = \frac{i_{L2}}{n}(d_1) + \frac{i_{L1}}{n}(d_6) - \frac{v_o}{R_L} \tag{13}$$

The duty ratio of the main switches, including conduction of the anti-parallel diodes, is defined as:

$$d = d_{S1} = d_1 + d_2 + d_3 + d_4 + d_5 + d_7 + d_8 + d_9 + d_{10} \tag{14}$$

$$d = d_{S2} = d_2 + d_3 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9 + d_{10} \tag{15}$$

Perturbation is introduced around the steady-state values of the state variables and input voltage such that $i_{L1} = I_L + i_{L1}, i_{L2} = I_L + i_{L2}, v_{in} = V_{in} + \hat{v}_{in}, v_o = V_o + \hat{v}_o, d_{s1} = D + \hat{d}_{s1}$, and $d_{s2} = D + \hat{d}_{s2}$. The state equations are modified to the following:

$$L_1 \frac{d(I_{L1} + i_{L1})}{dt} = (V_{in} + \hat{v}_{in}) - \left(1 - D - \hat{d}_{s1}\right) \frac{(V_o + \hat{v}_o)}{n} \tag{16}$$

$$L_2 \frac{d(I_{L2} + i_{L2})}{dt} = (V_{in} + \hat{v}_{in}) - \left(1 - D - \hat{d}_{s2}\right) \frac{(V_o + \hat{v}_o)}{n} \tag{17}$$

$$C_o \frac{d(V_o + \hat{v}_o)}{dt} = \left(\frac{I_{L1} + i_{L1}}{n}\right)\left(1 - D - \hat{d}_{s1}\right) + \left(\frac{I_{L2} + i_{L2}}{n}\right)\left(1 - D - \hat{d}_{s2}\right) - \left(\frac{V_o + \hat{v}_o}{R_L}\right) \tag{18}$$

Neglecting the second order terms and steady-state or DC terms results in the following equations:

$$L_1 \frac{di_{L1}}{dt} = \hat{v}_{in} - (1 - D)\frac{\hat{v}_0}{n} + \hat{d}_{s1}\frac{V_o}{n} \tag{19}$$

$$L_2 \frac{di_{L2}}{dt} = \hat{v}_{in} - (1 - D)\frac{\hat{v}_o}{n} + \hat{d}_{s2}\frac{V_o}{n} \tag{20}$$

$$C_o \frac{d\hat{v}_o}{dt} = (1 - D)\frac{i_{L1}}{n} + (1 - D)\frac{i_{L2}}{n} - \frac{I_{L1}}{n}\hat{d}_{s1} - \frac{I_{L2}}{n}\hat{d}_{s2} - \frac{\hat{v}_o}{R_L} \tag{21}$$

Taking Laplace transform, and then solving results in:

$$sL_1 i_{L1}(s) + \frac{(1 - D)\hat{v}_o(s)}{n} = \frac{V_o}{n}\hat{d}_{s1}(s) + \hat{v}_{in}(s) \tag{22}$$

$$sL_2 i_{L2}(s) + \frac{(1 - D)\hat{v}_o(s)}{n} = \frac{V_o}{n}\hat{d}_{s2}(s) + \hat{v}_{in}(s) \tag{23}$$

$$\frac{(1 - D)}{n}i_{L1}(s) + \frac{(1 - D)}{n}i_{L2}(s) - \left(sC_o + \frac{1}{R_L}\right)\hat{v}_o(s) = \frac{I_{L1}}{n}\hat{d}_{s1}(s) + \frac{I_{L2}}{n}\hat{d}_{s2}(s) \tag{24}$$

Writing in matrix form:

$$\begin{bmatrix} i_{L1}(s) \\ i_{L2}(s) \\ \hat{v}_o(s) \end{bmatrix} = [A(s)] \cdot \begin{bmatrix} \frac{V_o}{n} \\ 0 \\ \frac{I_{L1}}{n} \end{bmatrix} \cdot \hat{d}_{s1}(s) + [A(s)] \cdot \begin{bmatrix} 0 \\ \frac{V_o}{n} \\ \frac{I_{L2}}{n} \end{bmatrix} \hat{d}_{s2}(s) + [A(s)] \cdot \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix} \hat{v}_{in}(s) \tag{25}$$

where

$$A(s) = \begin{bmatrix} sL_1 & 0 & \frac{(1-D)}{n} \\ 0 & sL_2 & \frac{(1-D)}{n} \\ \frac{(1-D)}{n} & \frac{(1-D)}{n} & -\left(sC_o + \frac{1}{R_L}\right) \end{bmatrix}^{-1} \tag{26}$$

$$sL(i_{L1}(s) + i_{L2}(s)) + \frac{2(1 - D)\hat{v}_o(s)}{n} = \frac{V_o}{n}\left(\hat{d}_{s1}(s) + \hat{d}_{s2}(s)\right) + 2\,\hat{v}_{in}(s) \tag{27}$$

Writing in matrix form:

$$\begin{bmatrix} i_{L1}(s) + i_{L2}(s) \\ \hat{v}_o(s) \end{bmatrix} = [A(s)] \cdot \begin{bmatrix} \frac{v_o}{n} \\ \frac{I_L}{n} \end{bmatrix} \cdot \left(\hat{d}_{s1}(s) + \hat{d}_{s2}(s)\right) + [A(s)] \cdot \begin{bmatrix} 2 \\ 0 \end{bmatrix} \hat{v}_{in}(s) \tag{28}$$

where

$$A(s) = \begin{bmatrix} sL & \frac{2(1-D)}{n} \\ \frac{(1-D)}{n} & -\left(sC_o + \frac{1}{R_L}\right) \end{bmatrix}^{-1} \tag{29}$$

The control-to-output transfer function is obtained from Equation (28) by keeping $\hat{v}_{in} = 0$, resulting in the following equation:

$$\frac{\hat{v}_o(s)}{\hat{d}_{s1}(s) + \hat{d}_{s2}(s)} = \frac{\frac{(1-D)V_o}{n^2} - s\frac{L.I_L}{n}}{(LC_o)s^2 + \frac{L}{R_L}s + \frac{2(1-D)^2}{n^2}} \tag{30}$$

3. Two-Loop Closed-Loop Control Design

The two-loop control system is shown in Figure 4 with two proportional integral (PI) controllers and two identical modulators phase-shifted by 180°. Active current ripple is the major issue in the design of a fuel cell converter. The key to ripple reduction is to control the average inductor current i_L to be DC, which requires separating the bandwidths of voltage and current loops far apart using a slow voltage loop and a fast current loop [19]. Bandwidth (BW) of the inner current loop is selected to be higher than the outer voltage loop, which simplifies the design [20]. Therefore, it is possible to adjust the inductor current more quickly than the load voltage. The outer voltage loop regulates the load voltage by deriving reference for the input inductor current, $i_{L1,ref}$, and $i_{L2,ref}$ reference. Inductor currents i_{L1} and i_{L2} are tuned to this reference value by adjusting the duty ratio of the switches.
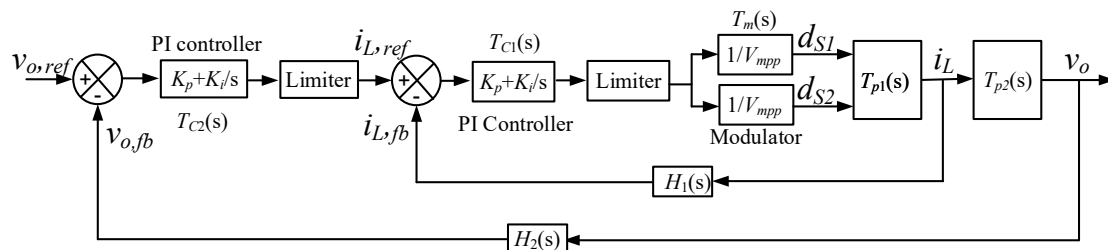

Figure 4. Complete two-loop average current control block diagram.

A bode plot of the control-to-output voltage transfer function given by Equation (30) is given in Figure 5. The phase margin (PM) is negative. This makes the system sensitive to small disturbances in operating points of input or source voltage and load current. Figure 6 shows that this transfer faction has right half plane zero, which adds a negative phase to the system. Instead of the phase increasing from 0 to 90 degrees, its phase increases from 0 to −90 degrees. This causes a delay in system response, which can lead to instability if not properly compensated.
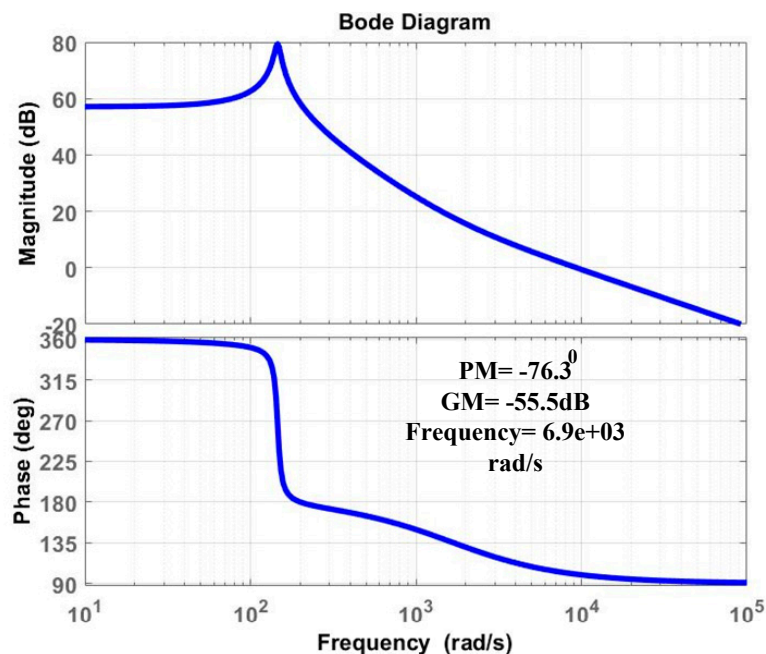

Figure 5. The control-to-output voltage transfer function of the system.
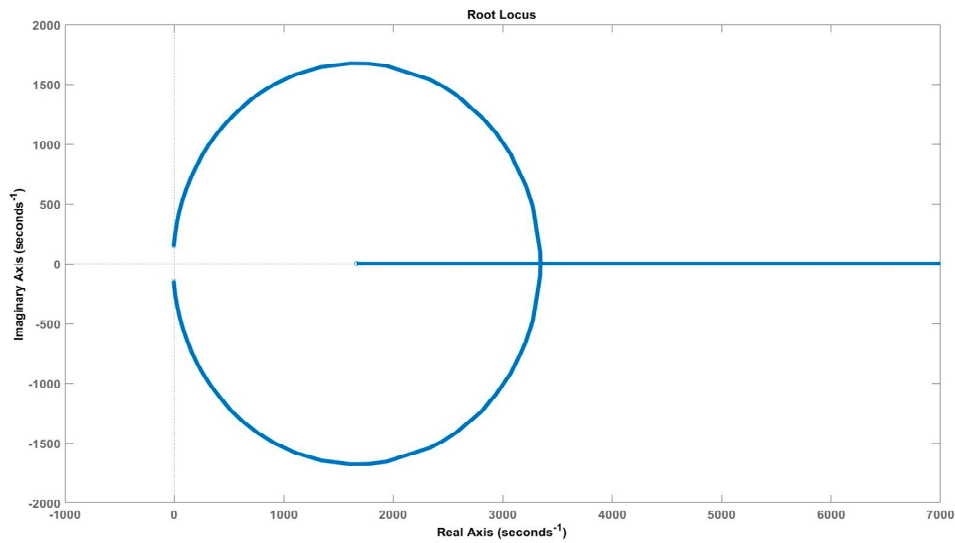
Figure 6. Pole-zero map of the control-to-output voltage transfer function of the system without controller.

3.1. Current Control Loop Design

The schematic diagram of the inner current control loop is shown in Figure 7. The input inductor current is fed back to the error amplifier with the gain of $H_1(s)$. The error is processed by a PI controller, and the output of the controller is compared with the modulator to generate the gating signals of the devices. The inductors' currents i_{L1} and i_{L2} are then regulated by adjusting the duty ratio of the switches.
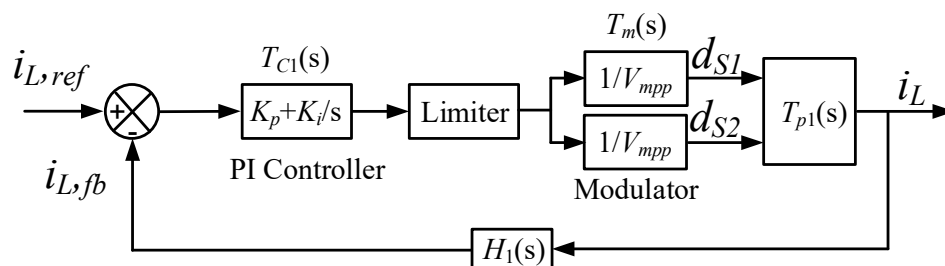

Figure 7. Inner current control loop schematic diagram.

Duty ratio to the inductor current transfer function is derived from Equation (27) and given by:

$$\frac{i_{L1}(s) + i_{L2}(s)}{\hat{d}_{s1}(s) + \hat{d}_{s2}(s)} = \frac{\left(\frac{C_o V_o}{n}\right)s + \frac{V_o}{nR_L} + \frac{2(1-D)}{n}\frac{I_L}{n}}{(LC_o)s^2 + \frac{L}{R_L}s + \frac{2(1-D)^2}{n^2}} \tag{31}$$

For the given specifications as shown in Table 1, the duty ratio to inductor current transfer function is given by:

$$T_{p1}(s) = \frac{i_{L1}(s) + i_{L2}(s)}{\hat{d}_{s1}(s) + \hat{d}_{s2}(s)} = \frac{0.004542s + 0.331514}{4.26 \times 10^{-8}s^2 + 5.847 \times 10^{-7}\,s + 3.472 \times 10^{-3}} \tag{32}$$

The gain margin and PM of the current control loop without controller is plotted in Figure 8, which shows PM = $90°$ at 177 krad/s. The PI controller is designed at PM of $60°$ in Figure 9 to increase the low-frequency gain and to reduce the steady-state error [21].

Table 1. Design specifications for the control system of the converter.

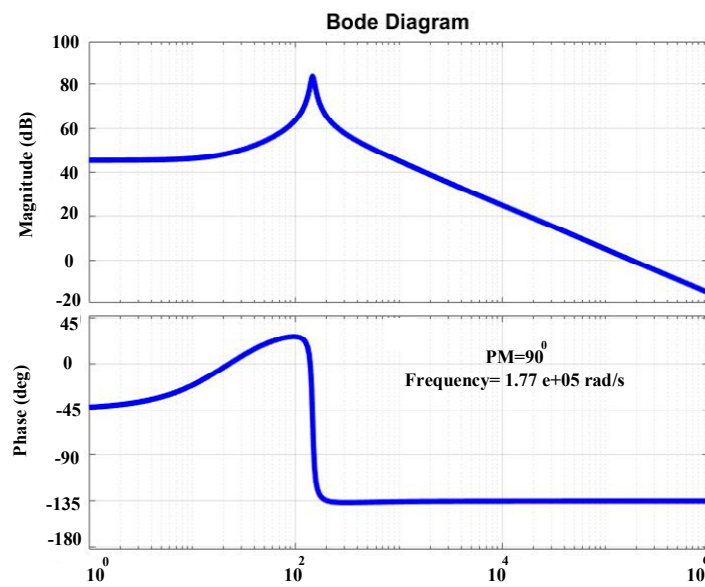|	
Input voltage V_{in}	12 V
Output Voltage V_o	288 V
Peak output power P_o	250 W
Switching frequency converter f_s	100 kHz
Leakage inductor L_{ls}	1.74 µH,
Input Boost Inductors L	200 µH,
Output Capacitor C_O	220 µF
Full-load R_L	331.77 Ω.

Figure 8. Bode plot of compensated control to input current transfer function: phase margin (PM) = 90° at 177 k rad/s.
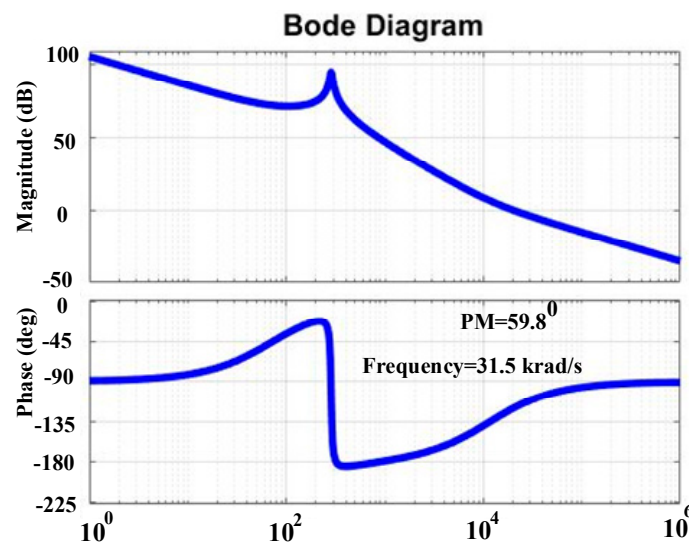

Figure 9. Bode plot of compensated control to input current transfer function: PM = 59.8° at 31.5 k rad/s (5000 Hz).

The transfer function of a PI controller is given by:

$$T_{C1}(s) = K_p + \frac{K_i}{s} = \frac{K_p(s + K_i/K_p)}{s} \tag{33}$$

The open-loop transfer function of the current loop is given by:

$$T_{OL1}(s) = T_{C1}(s) \times T_m(s) \times T_{p1}(s) \times H_1(s) \tag{34}$$

LEM sensor LA25-NP is used to sense the inductor current and to provide the isolation between power circuit and controller. Here, $H_1(s)$ is the current feedback gain and $T_m(s)$ is the overall gain of the modulator.

Here, the current feedback gain is selected as $H_1(s) = 1$.

Overall gain of the modulator is chosen to be:

$$T_m(s) = \frac{1}{10} \tag{35}$$

To realize PM = 60°, the following angle condition for the open-loop transfer function is applied:

$$T_{OL1}(jw_c) = PM - 180° \tag{36}$$

$$T_{OLI}(jw_c) = \frac{106572K_p\left(jw_c + \frac{K_i}{K_p}\right)(jw_c + 73.02\ )}{jw_c(jw_c{}^2 + \ 13.72\,jw_c + 81502.34\,jw_c)} \tag{37}$$

To realize the desired crossover frequency, the following gain condition of unity is applied for the open-loop transfer function, i.e., $\left|T_{OL1}(jw_c)\right| = 1$:

$$k_p{}^2\left(1.5625 \times 10^{10} + \frac{k_i{}^2}{k_p}\right) = 4.875 \times 10^{11} \tag{38}$$

PI controller parameters are designed to obtain PM of 60° [21,22] at the gain crossover frequency of 31.5k rad/s (5000 Hz) (Figure 9). Low-frequency gain is improved. It results in the gain K_p and K_i as 0.16 and 7269.58, respectively.

3.2. Voltage Control Loop Design

The outer voltage control loop regulates the output voltage at the reference value by setting reference for the current through the input inductors as shown in Figure 10. The inner current control loop has faster dynamics compared to the outer voltage loop. Hence, the current loop dynamics are neglected during the design of the voltage controller [23]. Its transfer function is not included, and the perturbation in the duty cycle can be neglected. Therefore, the inductor current to output voltage transfer function $T_{p2}(s)$ is obtained as:

$$T_{p2}(s) = \frac{v_o(s)}{\hat{\imath}_{L1}(s) + \hat{\imath}_{L2}(s)} = \frac{(1 - D)}{nC_o\left(s + \frac{1}{R_L C_o}\right)} \tag{39}$$

$$T_{P2}(s) = \frac{0.35}{0.001848s + 0.025} \tag{40}$$

LEM sensor LV20-P is used to sense output voltage and also to provide the necessary isolation. Here, the voltage feedback gain is chosen as:

$$H_2(s) = 24 \tag{41}$$

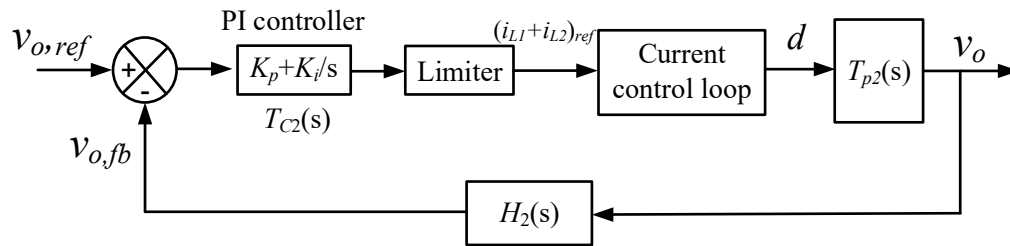The PI controller transfer function $T_{C2}(s)$ is given by Equation (33).

Figure 10. Outer voltage control loop schematic diagram.

Figure 11 shows the bode plot for the uncompensated voltage control loop. For the given specifications and selected component values, the crossover frequency is high with poor low-frequency gain.
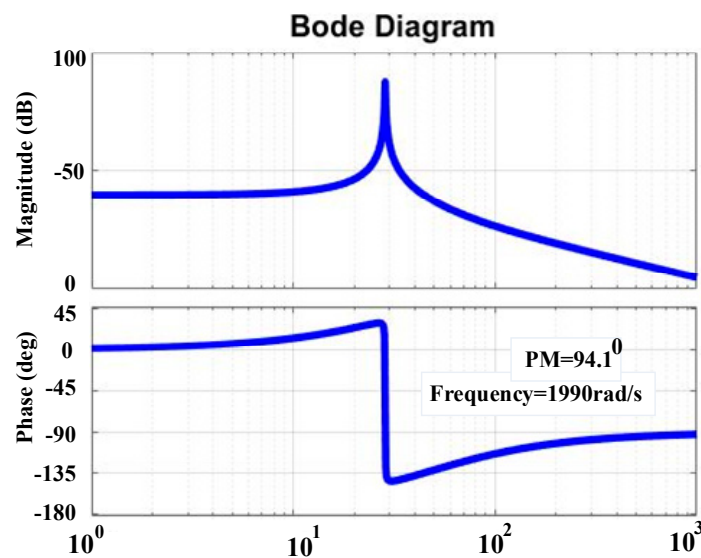

Figure 11. Bode plot of uncompensated plant in voltage control loop: PM = 94.1° at 1990 rad/s.

The overall open-loop transfer function of the voltage loop is given by:

$$T_{OL2}(s) = T_{C2}(s) \times T_{p2}(s) \times H_2(s) \times \frac{1}{H_1(s)} (47) \tag{42}$$

$$T_{OLI}(s) = \frac{0.35 K_p \left(s + \frac{K_i}{K_p} \right)}{0.001848 s^2 + 0.025 s} \tag{43}$$

The gain crossover frequency for the voltage controller is selected to be 10 times slower than that of the inner current loop. Application of angle and gain conditions similar to the current control loop for the desired PM of 60° [a] at gain crossover frequency of 3150 rad/s results in the gain K_p and K_i as 16.83 and 9767.8, respectively. Taking into account the dynamics of the current control loop, the overall transfer function of the system can be given as Equation (44).

$$T_{OL}(s) = \left[\frac{T_{C1}(s) \times T_{p1}(s) \times T_m(s) \times H_1(s)}{1 + T_{C1}(s) \times T_{p1}(s) \times T_m(s) \times H_1(s)} \right] \times T_{C2}(s) \times T_{p2}(s) \times H_2(s) \times \frac{1}{H_1(s)} \tag{44}$$

The Bode plot of the compensated voltage control loop is shown in Figure 12. Low-frequency gain is improved, indicating reduced steady-state error. The desired positive PM of 60° indicates a stable system rejecting disturbances for wide operating input voltage and load power variations.
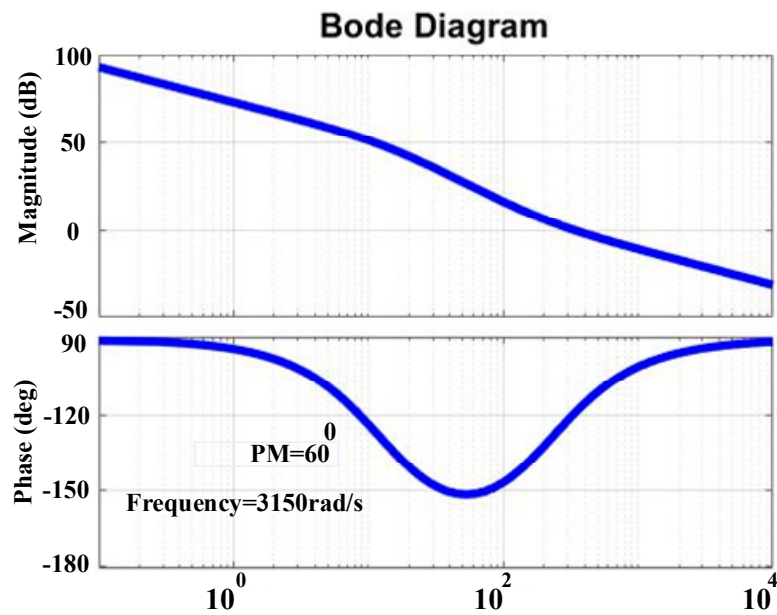
Figure 12. Bode plot of the compensated voltage control loop system: PM = 60° at 3150 rad/s (500 Hz).

4. Simulation and Experimental Results

The simulation model of the circuit topology and two-loop control was developed on software package PSIM 11 and was run to capture waveforms and observe transient performance of the converter under load-current variations. Simulation results are illustrated in Figures 13 and 14.
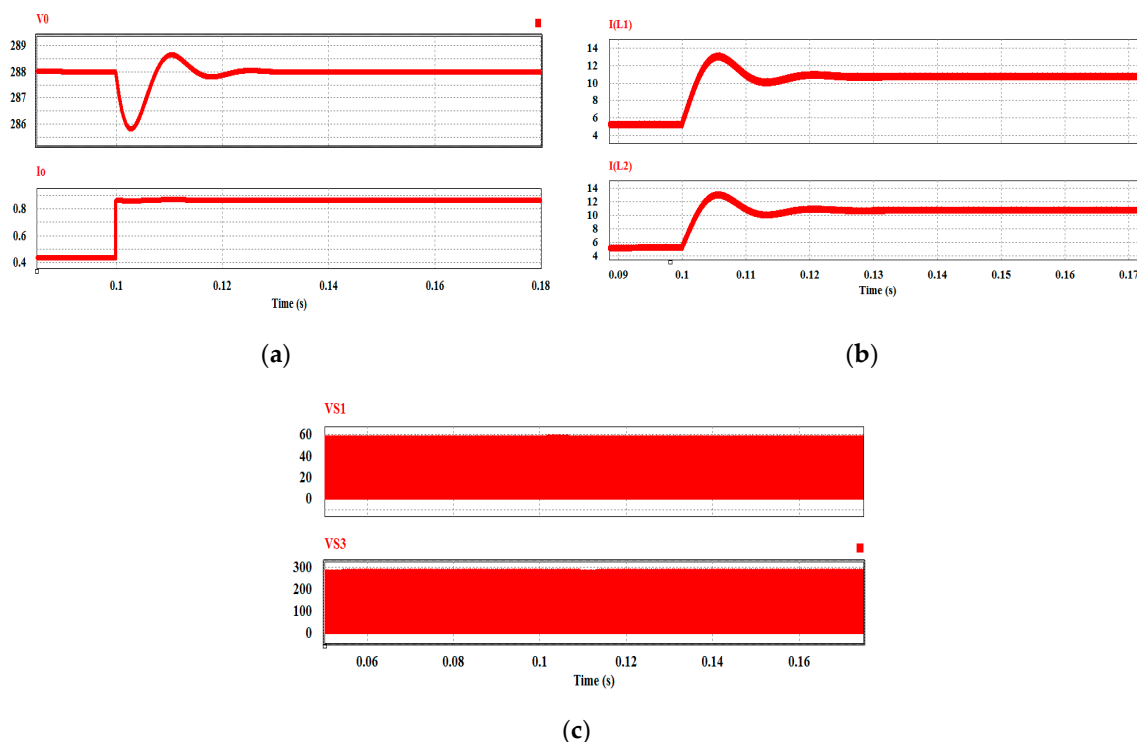

(a)

(b)

(c)

Figure 13. Simulation waveforms for V_{in} = 12 V with step change in load from 50% load to rated full load; (**a**) V_o is output voltage, I_o is output current, (**b**) I_{L1} and I_{L2} are input inductor currents, and (**c**) V_{s1} and V_{s3} are voltages across the switches S_1 and S_3, respectively.
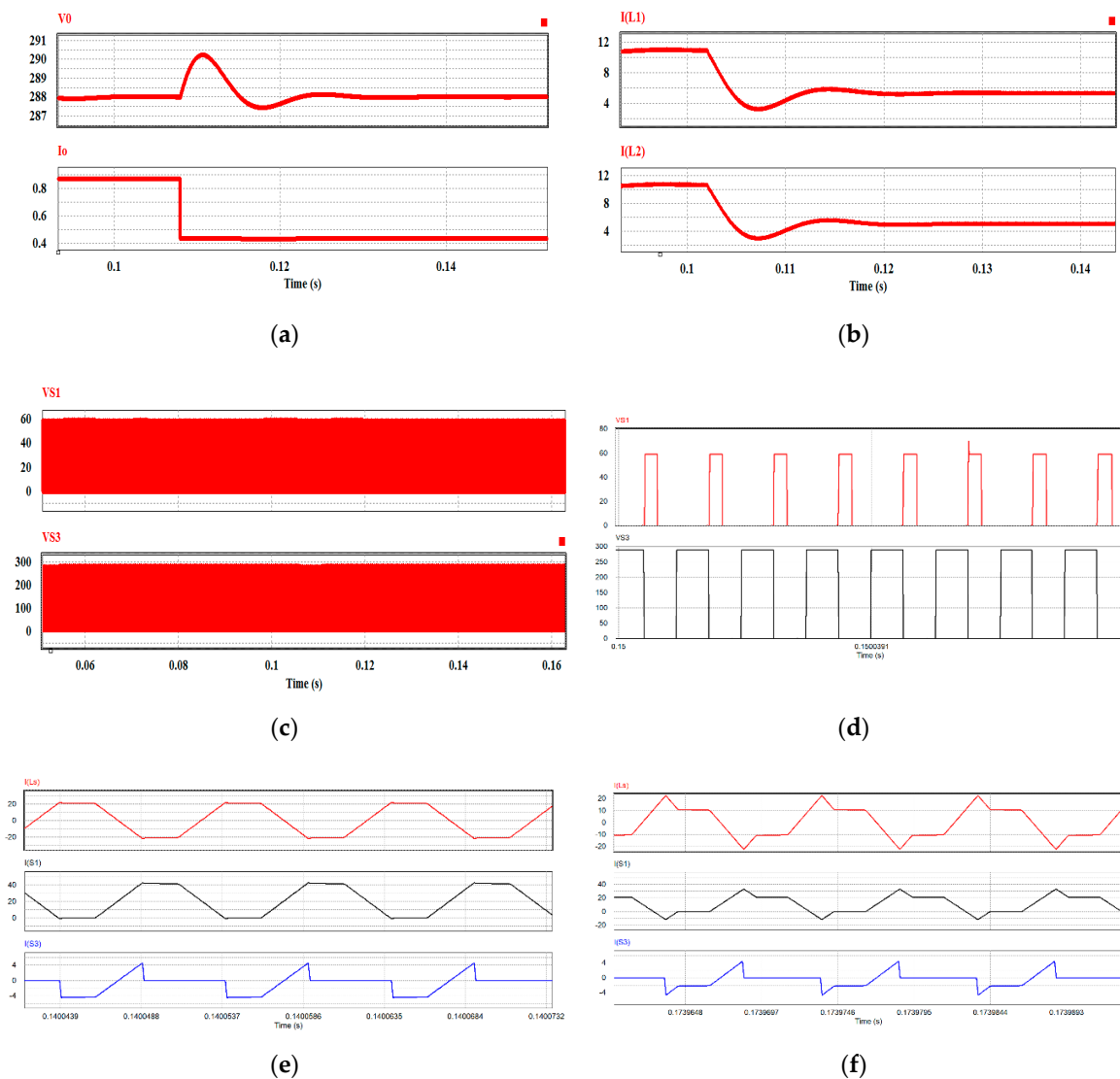
(a)

(b)

(c)

(d)

(e)

(f)

Figure 14. Simulation waveforms for V_{in} = 12 V with step change in load from rated load to half load with identical nomenclature. (**a**) V_o is output voltage, I_o is output current, (**b**) I_{L1} and I_{L2} are input inductor currents, and (**c**) V_{s1} and V_{s3} are voltages across the switches S_1 and S_3, respectively, (**d**) zoomed waveform of V_{s1} and V_{s3}, (**e**). I_{Ls} is the transformer primary current and I_{S1} and I_{S2} are the current through the switches S_1 and S_3, respectively at full-load steady-state and (**f**) I_{Ls} is the transformer primary current and I_{S1} and I_{S2} are the current through the switches S_1 and S_3, respectively at half-load steady-state.

The load is changed from 50% load to rated load (Figure 13) and from full load to 50% load (Figure 14). It should be observed that the overshoot or undershoot in output voltage for both step changes is 2V, which demonstrates the excellent stability of control. Load current and the two input inductor currents smoothly change to the next steady-state value. The settling time of the inductors' current and load voltage is nearly 25 ms. The voltage across the primary switches (VS1) is clamped at the reflected output voltage, and the voltage across the secondary devices (VS3) is clamped at the output voltage V$_o$ without any overshoot during the load transients, ensuring safe operation of the converter. Figure 14d (zoomed waveform in transient period) shows voltage across the primary side devices is clamped at the reflected output voltage, while voltage on the secondary side devices is always clamped at output voltage. Figure 14e,f shows steady-state (zoomed) waveforms at rated load and half load, respectively. It should be noted that primary side devices maintain ZCS, and secondary side devices maintain ZVS under both conditions.

Figure 15 shows the experimental prototype of the converter. It is operated by the designed controller, which has been tested in the laboratory for the step changes in load for a fixed 12 V input voltage. Table 2 shows the details of the components used in the hardware prototype.
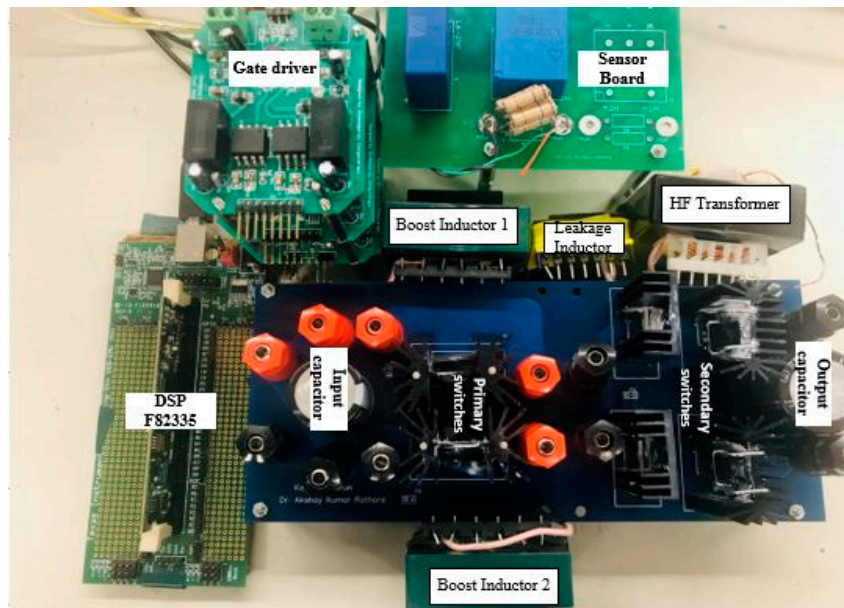

Figure 15. Laboratory prototype of the half-bridge converter.

Table 2. Component parameters of the hardware prototype.

Components	Parameters
Primary Switch (S_1, S_2)	IRFB4127PbF 200 V, 76 A, $R_{ds,on} = 17$ mΩ
Secondary Switch (S_3, S_4)	IPP60R125CP 650 V, 11 A, $R_{ds,on} = 0.125$ Ω
Series Inductor	TDK5901PC40Z core, 3.9 μH
HF transformer	3C95ETD49 ferrite core; $N_1 = 5$, $N_2 = 45$
Boost Inductors	3C95ETD49 ferrite core, $N = 42$, $L = 200$ μH
Output Capacitor C_O	220 μF, 450 V electrolytic capacitor 0.68 μF, 450 V high frequency film capacitor

Gating signals for the semiconductor devices are generated by Texas Instruments (TI) digital signal processor (DSP) TMS320F28335. Experimental waveforms for the step change in load are shown in Figures 16 and 17. Figure 16 demonstrates the experimental waveforms of inductor current i_L, voltage V_{AB}, and output voltage V_o with respect to time for the step change in load from rated load to 50% load. The similar waveforms for step change in load from 50% to rated load are manifested in Figure 17. Overshoot and undershoot in the output voltage are negligible during load transients. Further, output voltage V_o is maintained at the constant value. The variations in inductor current I_L and V_{AB} (transformer primary voltage, that is, the sum of voltage across the two primary switches S_1 and S_2) are within safe limiting values. Therefore, the switches do not experience any voltage spike during transition, which ensures safe and normal operation of the converter. Inductor current I_L is adjusted to their new steady-state values smoothly. The settling time is nearly 20 ms. This demonstrates stable performance over a wide load variation. It should be noticed that the experimental settling time is higher than the simulation value because the hardware experiences power loss, voltage drop, stray inductance/capacitance, system delay, and parasitic elements, which cause aberration from the ideal model. Better dynamic performance may be achieved by proper tuning of the controller parameters.
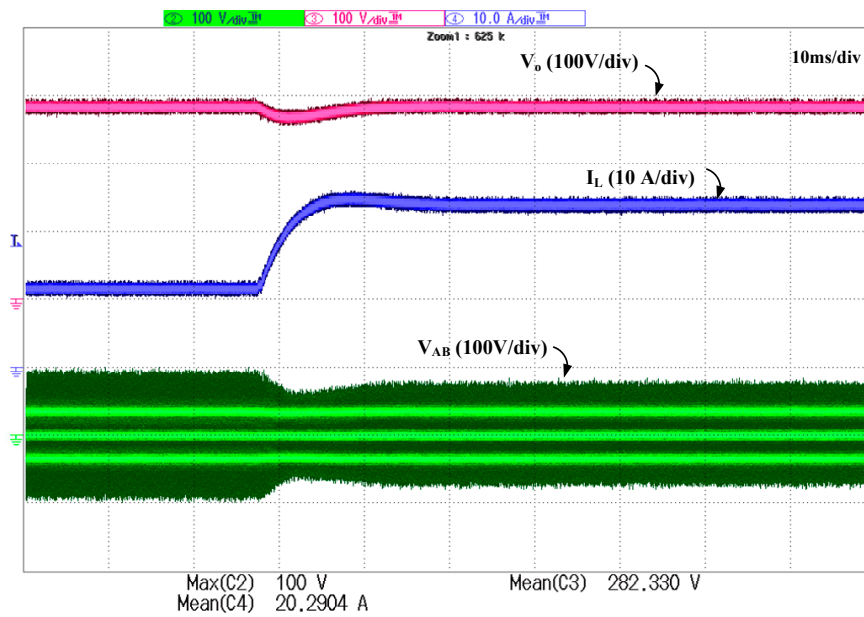
Figure 16. Hardware result for step change in load from 50% load to full load: (1) voltage V_{AB} (100 V/div), (2) inductor current i_L (10 A/div), and (3) output voltage V_o (100 V/div).
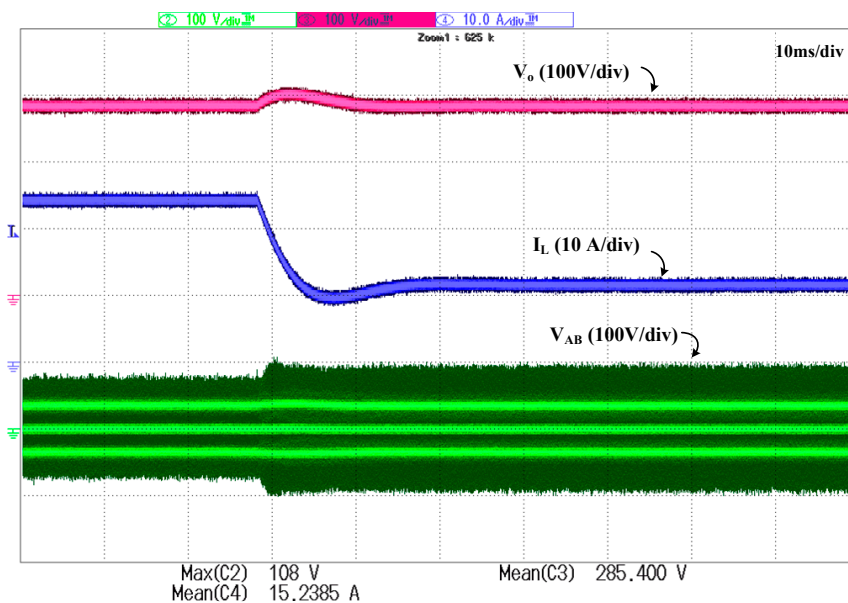

Figure 17. Hardware result for step change in load from full load to 50% load: (1) voltage V_{AB} (100 V/div), (2) inductor current i_L (10 A/div), and (3) output voltage V_o (100 V/div).

Figures 18 and 19 show the steady-state zoomed waveforms under half load and full load, respectively. Figures 18a and 19a show the gate-to-source V_{GS} and drain-to-source V_{ds} voltage waveforms across primary side MOSFET and transformer primary current i_s waveform at half load and full load, respectively. It is clearly demonstrated that the current through the switch naturally goes to zero. The negative current shows the antiparallel body diode conduction across the switch before turning off the gating signals, ensuring ZCS turn-off of the primary side semiconductor devices.
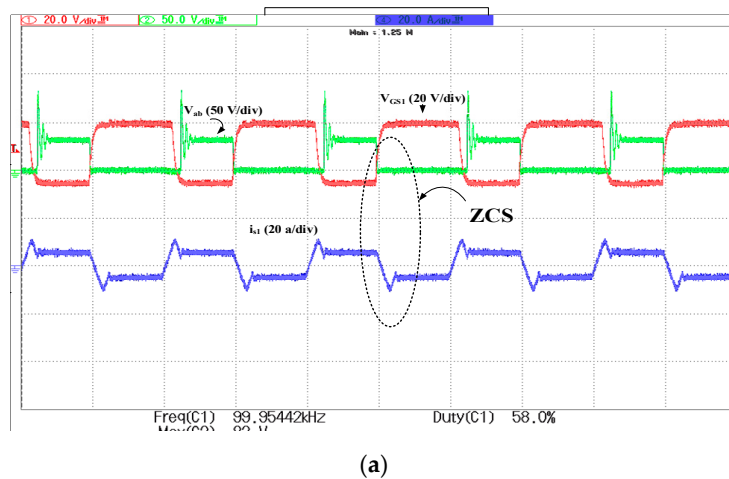
(**a**)
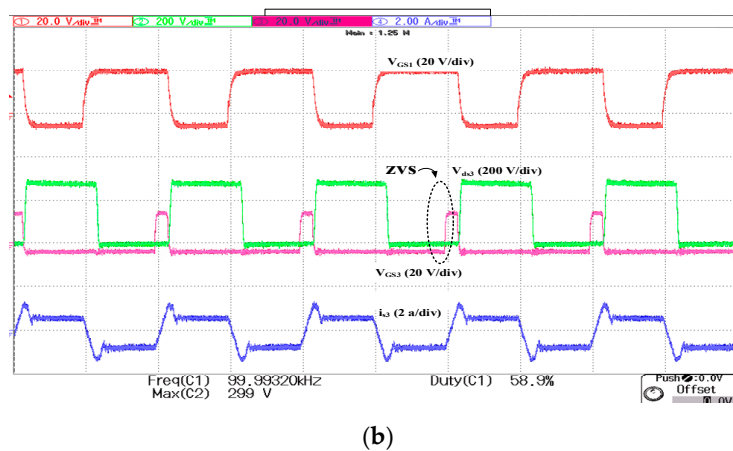
(**b**)

Figure 18. Experimental results for v_{in} = 12 V at 50% load: (**a**) gate-to-source voltage V_{Gs1} (20 V/div), current across primary-side MOSFET i_{s1} (20 A/div), and voltage V_{AB} = 50 V/div; (**b**) gate-to-source voltage V_{GS3} (20 V/div), drain-to-source voltage V_{ds3} (200 V/div), and current across secondary-side MOSFET i_{s3} (2 A/div).
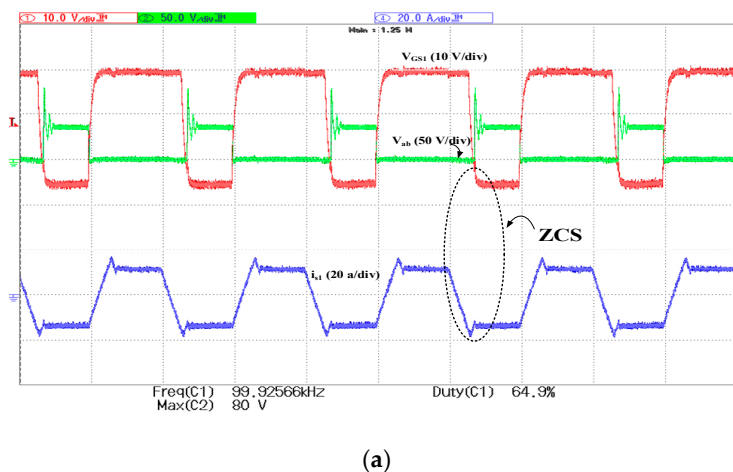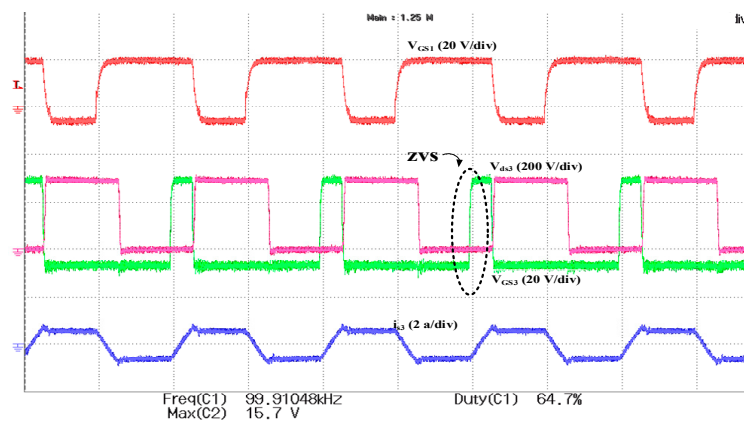

(**a**)

Figure 19. *Cont.*

(**b**)

Figure 19. Experimental results for v_{in} = 12 V at full load: (**a**) gate-to-source voltage V_{Gs1} (20 V/div), current across primary-side MOSFET i_{s1} (20 A/div), and voltage V_{AB} = 50 V/div; (**b**) gate-to-source voltage V_{GS3} (20 V/div), drain-to-source voltage V_{ds3} (200 V/div), and current across secondary-side MOSFET i_{s3} (2 A/div).

Voltage waveforms V_{GS} and V_{DS} across the devices clearly demonstrate the ZCS of the primary side devices and ZVS of the secondary side devices under both load conditions. The results are satisfactory during the transients that occurred due to sudden load disturbances while maintaining the steady-state performance. The steady-state performance is retained at the originally proposed in [17]. Corresponding gate-to-source V_{GS} and drain-to-source voltage V_{ds} waveforms of the secondary side devices are shown in Figures 18b and 19b. In these waveforms, gate-to-source voltage (V_{GS}) is applied when the voltage across secondary device V_{DS} is zero already, which ensures ZVS operation in secondary devices. It confirms the soft-switching of all the devices.

Table 3 shows the comparison between the conventional active-clamped converter and the proposed snubberless topology. It is clear from the comparison that the snubberless operation with proposed control has several merits in terms of voltage gain, efficiency, reduced current, transformer size, and soft-switching range. Simple control has resulted in these merits with a demerit of limited duty range.

Table 3. Comparison of proposed snubberless topology with active-clamped topology.

Topology	Active-Clamped	Proposed Snuberless
Soft-switching	ZVS (soft-switching at turn-on)	ZCS (soft-switching at turn-off)
Soft-switching range	Limited range (soft-switching is lost with the source voltage variation)	Full range (inherent soft-switching for the entire operating range)
Device voltage	Higher voltage and variable with duty cycle	Clamped at reflected output voltage and duty cycle independent
Boost Capability (voltage gain)	Voltage gain (boost) is compromised; 20% reduction at rated load	Natural boost gain
Device RMS current	Circulating current is present that increases average and RMS value	10% reduction in the rms current due to the absence of active clamp
Device peak current	1.5× input current	Same as input current (33% less)
Transformer current	Same as input current	Half of the input current (50% less)
Efficiency	High	2% improvement
Power flow	Unidirectional	Bidirectional
Duty cycle variation	Wide range (0 to 1)	Limited (0.5 to 1)
Transformer	Higher turns ratio, higher kVA rating and volume	Relatively lower turns ratio, reduced kVA rating and volume (40% less)

5. Conclusions

This paper studied small-signal modeling and derived transfer functions of an isolated naturally clamped snubberless current-fed half-bridge DC-DC converter. A two-loop average current controller was designed offering fixed-frequency duty cycle modulation of the semiconductor devices using two controllers. Initial verification of the small-signal model and the controller was done using PSIM 11 and investigation of the dynamic performance of the converter. Experimental results on a laboratory hardware proof-of-concept prototype demonstrated the satisfactory and smooth transient performance of the converter and the effectiveness of the designed closed-loop controller. The simplicity of implementation and practicality of the proposed control are the benefits of the overall system. The proposed analysis is effective for non-isolated as well as interleaved half-bridge and interleaved-boost topologies. It is suitable for fuel cell applications.

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