

Article

# A Non-Volatile Memory Based on NbO<sub>x</sub>/NbSe<sub>2</sub> Van der Waals Heterostructures

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Abstract: Two-dimensional (2D) van der Waals (vdW) layered transition metal dichalcogenides (TMDs) materials have been receiving a huge interest due to atomically thin thickness, excellent optoelectronic properties, and free dangling bonds. Especially the metallic TMDs, such as MoTe<sub>2</sub> (1T' phase), NbS<sub>2</sub>, or NbSe<sub>2</sub>, have shown fascinating physical properties through various applications, such as superconductor and charge density wave. However, carrier transport of metallic TMDs would be degraded due to the poor stability in ambient conditions. To date, achieving both high device performance and long-term stability is still a huge challenge. Thus, an alternative way to develop both unavoidable native oxide and metallic TMDs is under consideration for new era research. In this respect, 2D metallic TMD materials have attracted high attention due to their great potential in neuromorphic-based devices with metal-insulator-metal structures, making it possible to produce scalable, flexible, and transparent memory devices. Herein, we experimentally demonstrated a synthesized metallic NbSe<sub>2</sub> by a chemical vapor deposition method with a highly uniform, good shape distribution and layer controller ranging from 2–10 layers. Together, for the first time, we proposed the  $NbO_x/NbSe_2$  heterostructure memristor device based on the native  $NbO_x$  oxide on the interface of multi-layer  $NbSe_2$  flakes. The ultra-thin native  $NbO_x$  oxide of 3 nm was formed after a period of oxidation time under air condition, which acts as a memristive surface in the Au-NbOx-Au lateral memristor device, in which oxygen vacancies form a conductive filament. Our NbO<sub>x</sub>/NbSe<sub>2</sub> hetero-tructured memristor exhibits a stable memory window, a low-resistance-state/high-resistance-state ratio of 20, and stable endurance properties over 20 cycles at a low working voltage of 1 V. Furthermore, by the retention property test, non-volatile characteristics were confirmed after over 3000 s in our best data. Through a systematic study of the NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructured memristor device, this report will open new opportunities for next-generation memory devices application.

Keywords: 2D nanomaterials; chemical vapor depositions; memristor

# 1. Introduction

As the amount of data to be processed by the development of an information technology (IT) industry increases, demands on memory chips with high performance and miniaturization have increased rapidly. Accordingly, studies on next-generation memories based on new structures and



materials have been actively conducted [1–4]. In terms of scaling down the limitation of silicon-based memories, the two-dimensional (2D) van der Waals (vdW) layered transition metal dichalcogenide (TMD) materials have received great attention due to their excellent properties, such as atomically thin thickness [5], high mobility [6], various bandgaps [7], transparency [8], flexibility [9] and free dangling bonds [10]. This enables the potential development of various nano-scaled high-performance devices not only in memories, but also in field-effect transistors [11], photodetectors [12], biosensors [13], diodes [14], and so on. However, most of the studies until now have been mainly based on mechanical exfoliation methods with limitations of flake size and low yield, which restrict their application to commercialized-devices. Thus, synthesis on mass-produced 2D materials for large scale and low cost through the chemical vapor deposition (CVD) method has been proposed [15–17].

Among them, there has been a demand for utilizing metallic 2D materials for fabricating metal-insulator-metal (MIM) structures for next-generation memory, resistive switching random-access memory (ReRAM) [18,19], which has been spotlighted with attractive advantages, such as fast switching speed, low operation voltage, and good scalability, making it one of the most promising candidates for next nonvolatile memory devices [1–4]. Despite such favorable demands, the sensitive metallic 2D materials were easily degraded due to poor stability in ambient conditions [18]. To address such poor stability of metallic TMDs, passivation or interfacial engineering have been introduced [20–22]. Nonetheless, to achieve both high device performance and long-term stability is still hugely challenging. Thus, another alternative way to develop both unavoidable native oxide and metallic TMDs is under consideration for new era research. In this respect, the sensitive metallic TMD vdW material can be utilized as resistive memory by forming an ultra-thin native oxide on the surface of host materials under ambient conditions, which can act as a memristive surface memristor with an oxygen vacancy, forming a conductive filament [23,24].

In this study, we have experimentally demonstrated the synthesis of NbSe<sub>2</sub> flake by the CVD approach with highly uniform, good shape distribution and layer controller ranging from 2 layers to 10 layers. Furthermore, for the first time, we proposed the NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure memristor device based on the native NbO<sub>x</sub> oxide on the interface of multi-layer NbSe<sub>2</sub> flake. The ultra-thin native NbO<sub>x</sub> oxide of 3 nm was formed after a period of oxidation time under air condition, which acts as a memristive surface in the Au-NbO<sub>x</sub>-Au lateral memristor device, in which oxygen vacancies forming a conductive filament. Our NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructured memristor exhibits a stable memory window with reversible switching processes at a low working voltage of 1 V. Furthermore, the memristor shows a low-resistance-state (LRS)/high-resistance-state (HRS) ratio of about 20 and non-volatile properties via a retention test of 3000 s. Moreover, good endurance without any degradation up to 20 endurance cycles was demonstrated. Our strategy to fabricate feasible memristor for next-generation memory devices suggests new opportunities based on the CVD-grown 2D metallic materials.

### 2. Materials and Memristor Fabrication

# 2.1. Synthesis of NbSe<sub>2</sub> by Using Chemical Vapor Deposition (CVD) Method

Figure 1a shows a schematic of a CVD growth of NbSe<sub>2</sub> flakes. Firstly, the ammonium niobium oxalate (ANO)-C<sub>4</sub>H<sub>4</sub>NNbO<sub>9</sub>·xH<sub>2</sub>O (Sigma-Aldrich) was used as the niobium (Nb) precursor. The stock solution of Nb was prepared by dissolving a calculated amount of ANO powders in a deionized (DI) water. (0.3 g/10 mL) The sodium hydroxide (NaOH) was used as a promoter and medium solution of iodixanol (Opti Prep density gradient medium, Sigma Aldrich) which enhances the adhesion between the solution and the growth substrate during the liquid source coating process. These compositions were mixed in a precise ratio and then uniformly shaken with a speed of 300 rpm to obtain a homogeneous solution phase. The mixed solution was then deposited on a 300-nm thick SiO<sub>2</sub>/Si substrate by a spin-coating with a speed of 3500 rpm for 1 min. Next, the coated substrate was annealed at 500 °C for 30 min in the air to convert ANO into Nb<sub>2</sub>O<sub>5</sub> as well as burn carbon from Opti [25]. For a typical CVD growth process, the coated substrate was placed on a ceramic plate and loaded in the center of the

quartz tube of a CVD chamber. Here, the solid selenium (Se) was located at an entrance region with a distance of 17 cm from the center of the quartz tube of the chamber. Note that the distance of the Se source was controlled at various positions from 17 to 18.5 cm for controlling the heating temperature of the source, which will be discussed in detail later (Figure 1b). The temperature was controlled at 380 °C at the Se source location while the growth reaction was performed at 800 °C for 20 min under the flowing of 300 sccm N<sub>2</sub> and 20 sccm H<sub>2</sub> gas, which was used as a carrier gas during the whole growth process (Figure S1). Finally, the chamber was rapidly cooled down by opening the furnace after completing the whole synthesis process.



**Figure 1.** Synthesis settings and characteristics of chemical vapor deposition (CVD)-grown NbSe<sub>2</sub>: (**a**,**b**) The schematic image and photo image of synthesis settings for NbSe<sub>2</sub> Growth. The ammonium niobium oxalate-C<sub>4</sub>H<sub>4</sub>NNbO<sub>9</sub>·xH<sub>2</sub>O (ANO) source-coated substrate was loaded in the center of the CVD chamber and the solid Se was located at the upstream region where the distance is 17 cm from the center of the quartz; (**c**) optical microscope image of as-grown NbSe<sub>2</sub>; (**d**) Raman mapping image according to A<sub>1g</sub> mode; (**e**) the out-of-plane A<sub>1g</sub> mode at 225 cm<sup>-1</sup> and the in-plane E<sub>2g</sub> mode at 250 cm<sup>-1</sup> were observed.

# 2.2. Fabrication of NbO<sub>x</sub>/NbSe<sub>2</sub> Heterostructured Memristor Device

The as-grown NbSe<sub>2</sub> flake sample was transferred to a target substrate by a typical wet-transfer approach [26]. Firstly, the as-grown NbSe<sub>2</sub> sample was coated with a poly-methyl-methacrylate (PMMA) C4, which formed a support layer. Then, the substrate was etched with a diluted hydrogen fluoride (HF) acid solution to separate the grown sample/PMMA film from the growth substrate. With several rinsing with deionized (DI) water, it was transferred onto a target SiO<sub>2</sub>/Si substrate. Finally, after drying the transferred sample, the PMMA support layer was removed by acetone and rinsed again via isopropyl alcohol (IPA) solution. (Figure 1c)

The native oxide layer (NbO<sub>x</sub>) was formed by exposing the grown NbSe<sub>2</sub> sample to the air at room temperature for several days (in our case, 21 days), resulting in NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure, where the NbO<sub>x</sub> layer can act as a memristive surface. To fabricate the memristor device, the metal electrodes (source and drain) for a probe contact were patterned on NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructures using e-beam lithography followed by e-beam deposition of Cr/Au (5/50 nm). Electrical and memristive feature measurements for NbSe<sub>2</sub> and NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructures were performed using a probe station and a semiconductor analyzer (Keysight B1500A) at room temperature.

### 3. Results

# 3.1. Characterization

### 3.1.1. NbSe<sub>2</sub> Material Characterization

The NbSe<sub>2</sub> flake was characterized by Raman spectroscopy at room temperature under a 0.4-mW laser power and 532-nm wavelength excitation laser (XperRam200, Nano base) (Figure 1d). The spatially resolved Raman mapping images are shown according to  $A_{1g}$  and  $E_{2g}$  modes, as shown in Figure 1d and Figure S2, respectively. As a result, the intensity of both peaks ( $A_{1g}$  and  $E_{2g}$ ) was distributed uniformly. It suggests that we successfully grew high uniformity of the NbSe<sub>2</sub> flake using the CVD method. In the middle part of the NbSe<sub>2</sub> flake, there was a damage point, which was attributed to the laser focus during the measurement process. In Figure 1e, it is clearly shown that the Raman peak of our NbSe<sub>2</sub> flake is located at about 225 cm<sup>-1</sup> and about 250 cm<sup>-1</sup> of NbSe<sub>2</sub>, which are assigned to the out-of-plane mode  $A_{1g}$  peak and the in-plane mode  $E_{2g}$  peak in NbSe<sub>2</sub> flake [27].

To further optimize our CVD-grown NbSe<sub>2</sub> flake, we conducted experiments to meticulously explore possibly contributing to the NbSe<sub>2</sub> thickness as a function of Se source distance  $(d_{Se})$  from the center of the quartz. Figure 2 shows the NbSe<sub>2</sub> flake grown with different distances between the Se solid source and center of the quartz, ranging from 17 to 18.5 cm while fixing all other parameters. It is noted that the one-zone CVD chamber was used for synthesis. The temperature set for the growth (800 °C for this experiment) can be kept well at the center of the quartz tube but gradually declines as it goes toward the edge of the quartz tube. Thus, controlling the loading position of Se ( $d_{Se}$ ) in the quartz tube can be interpreted as controlling the heating temperature of the Se source. Base on that, the NbSe<sub>2</sub> flake thickness concerning the d<sub>Se</sub> for 17–18.5 cm was separately measured in Figure 2a–h. At a long  $d_{Se}$  (18.5 cm), the NbSe<sub>2</sub> flake showed a thickness of 2.4 nm as confirmed by atomic force microscopy (AFM) height profile function (Figure 2a,b). With decreasing the  $d_{Se}$  to 18 cm, the NbSe<sub>2</sub> flake thickness was increased to 4.8 nm (Figure 2c,d). Furthermore, with decreasing the  $d_{Se}$  to 17.5, 17 cm, the thickness of the NbSe<sub>2</sub> flake increased up to 7.2 and 12 nm, respectively (Figure 2e-h). These tendencies can be explained as follows. The different heating temperatures of Se induce different flow rates of the selenium vapor by affecting the vaporizing speed of Se and consequently affect the selenization amount of  $Nb_2O_5$  [27]. The selenization amount during growth can heavily determine the thickness of the NbSe<sub>2</sub>, because the NbSe<sub>2</sub> form a stacking layer over the grown flakes rather than expanding towards the SiO<sub>2</sub> surface, which can form a larger flake. Note that the SiO<sub>2</sub> surface is not flat and has many dangling bonds, which result in high energy barrier energy and low diffusion  $NbSe_{0,1,2}$  radicals [28]. Thus,  $NbSe_2$  growth at the SiO<sub>2</sub> surface is remarkably limited and, therefore, the staking of NbSe<sub>2</sub> is perpendicularly formed. Figure 2i summarizes the thickness of NbSe<sub>2</sub> flake corresponding to the d<sub>Se</sub> (for 17–18.5 cm). The error bar indicates  $\pm 10$  °C and  $\pm 2$  nm for the x and *y*-axis, respectively. From the data, with increasing the  $d_{Se}$ , the thickness of NbSe<sub>2</sub> flake decreased due to the selenization process as described above. According to the height profiles in atomic force microscopy (AFM, SPA 400, Seiko Instruments) images along with the d<sub>Se</sub> ranging from 17-18.5 cm, the different thicknesses of 2.4 to 12 nm, corresponding to the 2 layers, 4 layers, 6 layers, and 10 layers, are defined.

Together, Raman spectroscopy also identifies the thickness of the CVD-grown NbSe<sub>2</sub> (Figure 2j). For the measurements, a laser power of 0.4 mW and an excitation wavelength of 532 nm were used. At room temperature, the intensity of the peaks ( $A_{1g}$  and  $E_{2g}$ ) of thin-layer NbSe<sub>2</sub>, such as 2 or 4 layers, were shown weekly. However, as the thickness increased, such as to 6 or 10 layers, the intensity of the two peaks increased noticeably, which is in good agreement with the previous reports [27].



**Figure 2.** Different thickness of CVD-grown NbSe<sub>2</sub> via controlled growth parameter. (**a**–**h**) The microscope images, height profiles of 2 layer, 4 layer, 6 layer, and 10 layer NbSe<sub>2</sub>. The thickness of the flakes was controlled by the different distances to the Se from the center of the quartz; (**i**) the thickness tends to increase as the distance decreases, meaning that it increases the heating temperature of the Se source; (**j**) Raman spectrum according to the different thickness of the flakes under a 532-nm excitation wavelength laser.

For more optimal conditions for NbSe<sub>2</sub> growth, the roles of H<sub>2</sub> and the ratio of the carrier gas were examined (Figure S3). Without H<sub>2</sub> flow, there are only NbSe<sub>2</sub> particles grown, while the NbSe<sub>2</sub> flake size tends to be small under high H<sub>2</sub> concentration (N<sub>2</sub>/H<sub>2</sub> = 300/40~60). This is because it has been reported that H<sub>2</sub> plays a reducer agent in the growth reaction [29]. Thus, in the absence of H<sub>2</sub>, there are insufficient NbSe<sub>0,1,2</sub> radicals for growth, while H<sub>2</sub> also promotes the chemical etching effect rather than the formation of NbSe<sub>2</sub> under a high flow of H<sub>2</sub> [30]. From these perspectives and our results, 300/20 sccm for carrier gas ratio was found to be the optimal condition.

# 3.1.2. NbSe<sub>2</sub> Electrical Characterization

We now describe the electrical characteristic of our NbSe<sub>2</sub> flakes field-effect transistor (FET) device at room temperature under a high vacuum ( $1 \times 10^{-6}$  Torr), Figure 3a. Figure 3b shows the transfer characteristics of the NbSe<sub>2</sub> FET device at V<sub>gs</sub>, sweeping from -50 to 50 V at various V<sub>ds</sub> ranging from -0.5 to 0.5 V. As a result, our NbSe<sub>2</sub> flakes show an intrinsically metallic behavior with no gate dependence from -50 V to 50 V and a high on-current of 0.1 mA. Figure 3c shows the output characteristics of the NbSe<sub>2</sub> FET device at varying V<sub>gs</sub> of -50 V to 50 V. As the results indicate, an ohmic contact behavior with a linear relation between I and V were observed with no current difference according to different gate voltage biasing, in agreement with transfer curve results. These properties were also confirmed in our other NbSe<sub>2</sub> devices (Figure S4).



**Figure 3.** Electrical properties of the CVD-grown NbSe<sub>2</sub> field-effect transistor (FET) device. (a) Optical image of the NbSe<sub>2</sub> device with drain and source electrodes; (b) transfer characteristic with gate voltage sweep from -50 V to 50 V under constant drain bias ranges from -0.5 V to 0.5 V. No switching property was observed according to the gate voltage. (c) Output characteristic with drain voltage sweep from -0.5 V to 0.5 V under constant gate bias ranges from -50 V to 50 V. Under different gate biases, a similar current level of drain bias was observed, which also shows the metallic properties, no gate dependency.

### 3.2. Properties of the NbO<sub>x</sub>/NbSe<sub>2</sub> Heterostructured Memristor Device

Considering the highly electrical conductivity of our NbSe<sub>2</sub> flakes, we built the NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure for a memristor device as shown in Figure 4a. Before discussing, it is noted that the thin NbSe<sub>2</sub> flakes (below six layers) are very sensitive in ambient, which is easily damaged in a short period, suggesting unsuitability for our heterostructure memristor device (Figure S5). To perform this concept device, we are using the thick NbSe<sub>2</sub> flakes of 10 layers (Figure 4b). By exposing the thick NbSe<sub>2</sub> flakes under an ambient condition for 21 days, the native NbO<sub>x</sub> layer was formed on the NbSe<sub>2</sub> interface. Our NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure is operating in a lateral direction (Au-NbO<sub>x</sub>-Au) by resistance switching through the lateral NbO<sub>x</sub> layer on top of NbSe<sub>2</sub>. Furthermore, in the NbO<sub>x</sub>/NbSe<sub>2</sub> lateral memristor, total resistance (R<sub>tot</sub>) can be considered as NbSe<sub>2</sub> resistance (R<sub>NbSe2</sub>) + NbO<sub>x</sub> resistance (R<sub>NbOx</sub>) (Figure S6) [31]. In the case of a low resistance state (LRS), R<sub>tot</sub> is more influenced by R<sub>NbSe2</sub> compared to R<sub>NbOx</sub> because of the formation of conductive filament interior of the oxide layer. Thus, during the LRS state, low R<sub>tot</sub> can be realized by using a thicker metallic NbSe<sub>2</sub> layer, resulting in high-performance LRS.

Figure 4b shows the optical microscope images and AFM mapping images of intrinsic multi-layer NbSe<sub>2</sub> flake (top-panel) and the NbO<sub>x</sub>/NbSe<sub>2</sub> flake (bottom panel) are depicted. The intrinsic multi-layer NbSe<sub>2</sub> was observed to have a 12-nm thickness (black solid line in Figure 4c). After a period of 21 days in the air condition, the native NbO<sub>x</sub> oxide was formed. The height of the flake was increased up to 15 nm (blue solid line in Figure 4c) which can be interpreted as forming a 3-nm NbO<sub>x</sub> native oxide layer on top of the intrinsic NbSe<sub>2</sub> flake.

Figure 4d shows the current–voltage (I–V) characteristic of our NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure memristor device. The inserted image is an optical microscope image of our device. Voltage was swept as  $0 \text{ V} \rightarrow +1 \text{ V} \rightarrow -1 \text{ V} \rightarrow 0 \text{ V}$  between the drain and the source electrode with the duration time of 0.1s, which showed reproducible and nonvolatile hysteretic resistive switching behavior in synaptic memory. During the positive voltage sweep, the current increased via migration of positively charged oxygen vacancies (conductive filament (CF) formation), with which the device showed the HRS to LRS transition. The resistance state kept LRS with the reverse voltage sweep. Then, again, the reset transition process started at -1V, and the LRS to HRS transition was exhibited during the negative voltage sweep. Here, the noise had occurred during the I–V switching measurement, which is probably due to the non-uniform and ultra-thin native oxide layer (~ 3 nm NbO<sub>x</sub>). It is suggested that the conductive

filament pathway can be randomly formed and induce the current noise in the set/reset process during the extraction/recovery process of oxygen vacancies. The retention time and cyclic endurance were also examined to elucidate memory functionalities. In Figure 4e, a single writing pulse of  $V_W = +1 V$  and -1 V was applied to switch memory into LRS and HRS, respectively, with a typical switching time of 0.1 s. The reading current was read out with a small reading bias of  $V_R = 0.1 V$  and was defined as the current of HRS (black dotted line) and LRS (red dotted line). Moreover, no degradation was shown up to over 20 endurance cycles, maintaining a stable on/off ratio of 20. The retention property of the NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure memristor was also conducted under a 10-mV reading voltage, resulting in over 250 s as shown in Figure 4f. The short retention time is because of our measurement set up as following, by (i) I–V switching, (ii) retention time test, and (iii) endurance test. To get all good electrical characteristics at once, the retention time was measured until ~250 s. To further prove the retention ability of our device, we measured other devices by focusing on the retention test on the same substrate. As a result, our best data were obtained at ~3000 s in retention time under a 10-mV reading voltage (Figure S7), where both LRS and HRS were stably remained, confirming the non-volatile properties of our NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure memristor device.

For understanding the resistance switching behavior in the memristor, the formation process of conductive filaments (CFs) should be preceded. The mechanism of conductive filaments in our NbSe<sub>2</sub>/NbO<sub>x</sub> heterostructure memristor is depicted in Figure 4g. In particular, if the voltage is biased to the drain electrode, the electric field is applied to the NbO<sub>x</sub> layer and the movement of oxygen ions inside the oxide layer is generated. This movement causes positively charged oxygen vacancies in the oxide layer which acts as the CF. Accordingly, the source and drain electrodes are connected, and a switch-on state is maintained by exhibiting a low-resistance-state (LRS) at the oxide layer (high-resistance-state (HRS) to LRS transition, Set). In contrast, under reverse bias, the conductive filaments disappear via filling the oxygen vacancies by moving oxygen ions, which results in HRS on the oxide layer (LRS to HRS transition, Reset). To confirm the conduction mechanisms in our NbO<sub>x</sub>/NbSe<sub>2</sub> memory device, the I–V curve of Figure 4d was replotted with a double-logarithmic scale as shown in Figure S8. According to the graphs, our device followed the Space Charge Limited Conduction (SCLS) mechanism with the most accepted factor as oxygen vacancies in our device [32,33]. The details are discussed in the Supplementary Note 1.

Besides, an exposing time in the air is an important factor for realizing our heterostructure memristor device. We compared the I–V characteristic to the influence of the oxidation period, expected to provide the large on/off current ratio of LRS/HRS (Figure 4h and Figure S9). As result, with increasing the oxidation time, the HRS keeps decreasing while the LRS remains stable. More details about the relationship between the oxidation time and the device performance are explained in Supplementary Note 2. Our NbSe<sub>2</sub>/NbO<sub>x</sub> heterostructure memristor device was mostly stable at 21 days of oxidation time in ambient conditions. To prove that, we measured our device under ambient and vacuum conditions, as shown in Figure S10. From the data, the device shows well repeatable memory behavior in both conditions, indicating that the elimination of oxygen in the air was un-affected by our device performance. Thus, we can conclude that the non-volatile memory behavior of our NbSe<sub>2</sub>/NbO<sub>x</sub> heterostructure originates from the NbO<sub>x</sub> oxide layer on the NbSe<sub>2</sub> interface, which is similar to the NbS<sub>2</sub> material in the previously reported study [31].

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**Figure 4.** NbO<sub>x</sub>/NbSe<sub>2</sub> van der Waals memristive memory properties. (**a**) The schematic image of the NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure memristor. On top of the multi-layer NbSe<sub>2</sub>, NbO<sub>x</sub> was formed. (**b**) Optical microscope image and corresponding atomic force microscopy (AFM) mapping images of the intrinsic NbSe<sub>2</sub> flake (top panel) and NbO<sub>x</sub>-formed NbSe<sub>2</sub> flake (bottom panel). (**c**) The height profile of NbO<sub>x</sub>/NbSe<sub>2</sub> and NbSe<sub>2</sub> heterostructures. It is increased by about 2 nm compared to intrinsic flakes (12 nm), which can prove the formation of the NbO<sub>x</sub>. (**d**) Typical current–voltage curves of the memristor. The inset figure is the corresponding memristor device. (**e**) Endurance characteristics against repeated resistance switching cycles under 0.1 V read voltage. (**f**) Retention properties of the memristor under 0.01 V read voltage. Non-volatile properties were observed over 3 min without any resistance switching. (**g**) Schematics of memristive switching mechanism by conductive filament formation and rupture processes via migration of oxygen vacancies. (**h**) Hysteresis variation of the NbO<sub>x</sub>/NbSe<sub>2</sub> hetero memory device according to the oxidation period of the NbSe<sub>2</sub> flake in the air.

# 4. Conclusions

In conclusion, we have demonstrated the synthesis of NbSe<sub>2</sub> flakes by the CVD approach via specifically controlled Se source distance from the center of the quartz ( $d_{Se}$ ) and the carrier gas ratio ( $H_2$ :N<sub>2</sub>). Concerning these efforts, we had successfully grown the NbSe<sub>2</sub> flakes with highly uniform, good shape distribution, controlling layers from 2 to 10 layers. Together, we proposed the NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructure memristor device based on the native NbO<sub>x</sub> oxide on the interface of NbSe<sub>2</sub> flakes. Here, the NbO<sub>x</sub> oxide layer acts as a memristive surface in the Au-NbO<sub>x</sub>-Au lateral memristor device, in which oxygen vacancies form a conductive filament. Our memristor shows an LRS/HRS ratio of 20 and stable cyclic endurance properties at a low working voltage of 1 V. Furthermore, by retention test, non-volatile characteristics were confirmed at 3000 s. This systematic study of the NbO<sub>x</sub>/NbSe<sub>2</sub> heterostructured memristor device is expected to open the possibilities of a viable next-generation memory device.



**Supplementary Materials:** The following are available online at http://www.mdpi.com/2076-3417/10/21/7598/s1, Figure S1: The CVD growth condition for NbSe2 flakes; Figure S2: Raman mapping image according to E2g mode at 250 cm<sup>-1</sup> of the CVD-grown NbSe2; Figure S3: CVD NbSe2 growth tendency according to the optimization of carrier gas ratio (N2:H2); Figure S4: Electrical characteristics of various other CVD-grown NbSe2 flakes; Figure S5: The oxidization effect of the thin CVD-grown NbSe2 flake; Figure S6: Formation of channels in a memristor device structured with NbOx/NbSe2 heterostructure; Figure S7: Retention properties of the NbOx/NbSe2 memristor under 0.01-V read voltage; Figure S8: I–V curves of NbOx/NbSe2 memory devices, displayed on a double-logarithmic scale; Figure S9: I–V characteristic of NbOx/NbSe2 heterostructure memristor along with the influence of oxidation time (0–24 days); Figure S10: Electrical comparison of memristor under vacuum and ambient condition. Supplementary Note 1: Explanation of the conduction mechanism of our NbOx/NbSe2 memory device based on the SCLC mechanism; Supplementary Note 2: Explanation of the relationship between the exposure time and device performance.

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