Article

A Non-Volatile Memory Based on NbOx/NbSe2 Van Der Waals Heterostructures

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Figure S1. The CVD growth condition for NbSe2 flakes.

Figure S2. Raman mapping image according to E_{2g} mode at 250 cm⁻¹ of the CVD-grown NbSe₂.

Figure S3. (a-e) CVD NbSe₂ growth tendency according to the optimization of carrier gas ratio (N2:H2).

Figure S4. (a,b) Electrical characteristics of various other CVD-grown NbSe2 flakes. Both output characteristics showed linear properties; (**c**,**d**) no gate modulation was observed under gate bias sweep in the transfer characteristics, indicating the metallic behavior of NbSe2.

Figure S5. The oxidization effect of the thin CVD-grown NbSe2 flake. (**a**) Optical microscope image of the as-grown NbSe2 flake. The flake thickness was about 3~4 nm, corresponding to three to four layers of NbSe2. (**b**) Optical microscope image of the oxidized NbSe2 flake after several days (within a week). The overall surface was damaged and disappeared.

Figure S6. Formation of channels in a memristor device structured with a NbO_x/NbSe₂ heterostructure. The resistance of the metallic NbSe2 layer and the resistance of the NbO_x oxide layer, which began to be conductive by conductive filament formed by oxygen vacancy.

Figure S7. Retention properties of the NbO_x/NbSe₂ memristor under a 0.01-V read voltage. Non-volatile properties were observed for 3000 s without any resistance switching.

Figure S8. I-V curves of NbO_x/NbSe₂ memory devices displayed on a double-logarithmic scale. The linear fitting result in both On-state and Off-state: (**a**) positive SET range and (**b**) negative RESET range.

Figure S9. (a-i) Characteristics of the NbO_x/NbSe₂ heterostructure memristor along with the influence of oxidation time (0–24 days). Stable memory characteristics were confirmed when the oxidation period was over 21 days.

Figure S10. Electrical comparison of memristor under vacuum and ambient condition.

Supplementary Note 1

To prove the conduction mechanism in our NbO_x/NbSe₂ memory device, I–V curves (Figure 4d, manuscript) are replotted on a double-logarithmic scale as shown in Figure S8. According to the results, our device was followed by the Space Charge Limited Conduction (SCLC) mechanism [32,33], which is a commonly observed in resistive memory devices. Here, the SCLC mechanism was relatively observed with two regions of distinct slope, followed by the Ohmic law (I α V) in a low electric field region and Child's law (I α V²) in a high electric field region. From the results (Figure S8), both the SET range (Figure S8a) and RESET range (Figure S8b) are showing the observation of (i) I α V and (ii) I α V², which assigned to the dominant of SCLC mechanism. Based on the SCLC theory, the most commonly accepted factor which contributed to the SCLC conduction is oxygen vacancy. This result is consistent with a previous report [31].

Supplementary Note 2

In Figure S9, the relationship between the exposure time and memory behavior indicates that the oxidation time influenced the device performance, suggesting that the thickness of NbO_x is a key factor for contributing to the on/off ratio. In particular, the on/off current ratio of the device exposed in ambient for 21 days (Figure S8. h) showed 20 times higher than a pristine NbSe₂ device (Figure S8. a). To improve the on/off current ratio, we tried to speed up the oxidation by the heating effect. However, the oxide layer formed at room temperature is usually an amorphous phase, which provides a higher concentration of native defects (oxygen vacancies) than the oxide layer formed by the heating effect. Therefore, the native oxidation under ambient conditions at room temperature was more suitable for our devices. According to that, our device showed a stable on/off current ratio of around 20.