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Investigation on the Hump Behavior of Gate-Normal Nanowire Tunnel Field-Effect Transistors (NWTFETs)

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Abstract: The hump behavior of gate-normal nanowire tunnel field-effect transistors (NWTFETs) is investigated by using a three-dimensional technology computer-aided design (TCAD) simulation. The simulation results show that the hump behavior degrades the subthreshold swing (*SS*) and on-current (I_{on}) because the corners and sides of nanowires (NWs) have different surface potentials. The hump behavior can be successfully suppressed by increasing the radius of curvature (*R*) of NWs and reducing gate insulator thickness (T_{ins}).

Keywords: hump behavior; corner; surface potential; gate-normal nanowire tunnel field-effect transistor (NWTFET)

1. Introduction

The aggressive downscaling of metal oxide semiconductor field-effect transistors (MOSFETs) has raised some problems regarding the off-current (I_{off}) and supply voltage [1]. A tunnel field-effect transistor (TFET) has been considered as one of the most promising candidates for extremely low-power applications thanks to its low I_{off} and abrupt on–off switching [2,3]. However, TFETs suffer from low on-current (I_{on}) [4]. For higher I_{on}, several strategies have been proposed: the introduction of low bandgap materials [5], and hetero-gate-dielectric (HG) [6] and hetero-material-gate (HMG) structures [7]. Additionally, gate-normal TFETs were proposed to boost I_{on} by increasing the tunneling cross-sectional area [8–11]. The band-to-band tunneling (BTBT) generation of gate-normal TFETs occurs perpendicular to the channel in the gate–source overlap region. Thus, the gate-normal tunneling area can be enlarged by increasing the gate–source overlap length (L_{ov}) to increase I_{on}.

Recently, silicon nanowire (SiNW) TFETs have been developed for superior subthreshold swing (*SS*), I_{off}, and short-channel-effect immunity [12,13]. The fabrication of SiNW TFETs using a top-down process has great advantages in terms of being a reproducible process, having compatibility with CMOS and having good control over the dimensions, while a bottom-up process has been seriously limited due to a difficulty in the fabrication process [14–16]. In this manuscript, as shown in Figure 1, gate-normal NWTFETs are discussed, which combine the advantages of gate-normal TFETs and NWFETs. One of the most serious problems of gate-normal NWTFETs is the hump behavior stemming from the three-dimensional corner effect: the surface potentials are different between the corner and side of an NW. This means that different BTBT turn-on voltages exist in an NW, which induces the hump behavior of degrading *SS* and I_{on} [17]. Thus, it is necessary to suppress the corner effect of gate-normal NWTFETs. There are several studies on the hump behavior of TFETs and various methods of mitigating hump behavior [18–21]. However, this study discusses the hump behavior originated from the geometrical effect of the three-dimensional NW structure. Even if many studies have been performed regarding the corner effect of NWMOSFETs [22–25], that of gate-normal NWTFETs has rarely been discussed.

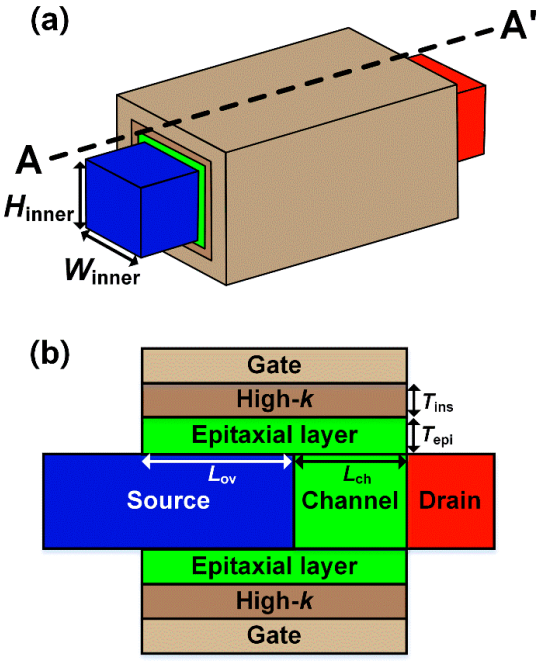

Figure 1. (**a**) Bird's eye and (**b**) cross-sectional views of simulated gate-normal nanowire tunnel field-effect transistors (NWTFETs) with the normalized radius of curvature (R_{norm}) of 0.

In this manuscript, the hump behavior of gate-normal NWTFETs is investigated and its solution is proposed by three-dimensional (3D) technology computer-aided design (TCAD) simulation.

2. Device Structure and Simulation Methodology

Figure 1 shows the bird's eye and cross-sectional views of gate-normal NWTFETs. It features a gate–source overlapped thin intrinsic epitaxial layer to fix the tunnel width. The device parameters are summarized in Table 1. The channel length (L_{ch}) is 20 nm. The gate–source overlap length (L_{ov}) is 40 nm. Both the inner width (W_{inner}) and inner height ($H_{in\ ner}$) are 20 nm, respectively. The gate insulator thickness (T_{ins}) is 2 nm. The epi-layer thickness (T_{epi}) is 2 nm. The source (N_S) and drain doping concentrations (N_D) are 10^{20} cm^{-3}, respectively.

Table 1. Device parameters for simulation.

Parameters	Values
L_{ch}	20 nm
L_{ov}	40 nm
W_{inner}, H_{inner}	20 nm
T_{ins}	2 nm
T_{epi}	2 nm
N_S	1×10^{20} cm^{-3} (p-type)
N_D	1×10^{20} cm^{-3} (n-type)
N_{ch}, N_{epi}	Intrinsic

3D TCAD device simulation has been performed by using a commercial simulator [26]. For the accurate calculation of the BTBT generation rate, a dynamic nonlocal BTBT model is used after calibration [27]. Additionally, the Shockley–Read–Hall recombination, Philips unified mobility model and Fermi distribution are used in our simulation. On the contrary, quantization effects and the gate leakage current have not been considered. The threshold voltage (V_T) is defined as the gate voltage (V_G) when the drain current (I_D) is equal to 0.1 nA/μm, while the turn-on voltage ($V_{turn\text{-}on}$) is defined as V_G when I_D is equal to 0.01 fA/μm. The I_{on} and I_{off} are defined as I_D when the overdrive

voltages ($V_G - V_{turn\text{-}on}$) are 0.5 V and −0.2 V, respectively. The average *SS* (SS_{avg}) is calculated from $V_G = V_{turn\text{-}on}$ to $V_G = V_{turn\text{-}on}$ + 0.5 V. Drain-induced barrier thinning (*DIBT*) is calculated as the V_T difference between V_D = 0.05 V and 0.5 V.

3. Simulation Results and Discussion

3.1. Analysis of Hump Behavior of Gate-Normal NWTFETs

Figure 2 shows the simulated transfer curves of the gate-normal NWTFETs, which show clear hump behavior degrading SS and I_{on}. Two noteworthy phenomena are observed. First, hump behavior occurs and the SS is abruptly changed around V_G = 0.7 V. In order to analyze the hump behavior, the electron BTBT generation rates in the gate–source overlap region are simulated at around V_G = 0.7 V at V_D = 0.5 V. As shown in Figure 3, gate-normal BTBT occurs at the corners earlier than at the sides, which is called the corner effect. To be specific, the area wherein BTBT occurs is extended from the corner to the side as V_G increases. In addition, the electron BTBT generation rate is not constant through the NW, and is stronger at the corner. This means that different BTBT turn-on voltages exist in an NW, which induce the hump behavior. Second, as shown in Figure 2, the hump becomes more severe as V_D decreases. At low V_D, it is vulnerable to the hump because the influence of the gate increases as the V_D decreases, while the hump is more affected by the structure of the gate.

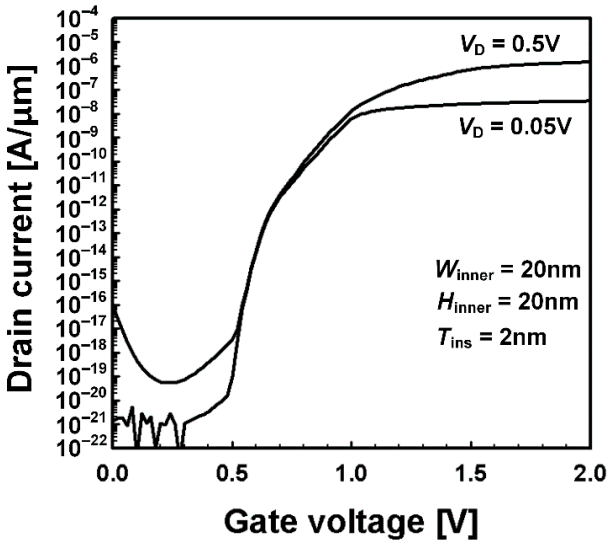

Figure 2. Transfer curves of the gate-normal NWTFETs for V_D values of 0.5 V and 0.05 V. It is shown that gate-normal NWTFETs suffer from hump behavior, which degrades *SS* and I_{on}.

The definition of the corner and side of an NW is shown in Figure 4. Because the tunneling width is determined by the epi-layer thickness (T_{epi}), gate-normal tunneling occurs mainly in the epi-layer [28]. Thus, by integrating electron BTBT generation rates over the cross-section of an NW, electron BTBT generation rates per channel length are calculated. In order to evaluate the influence of the corners on I_D, the electron BTBT generation rates at the corners and sides are compared with each other. Figure 5 shows that gate-normal tunneling occurs first in the corner region and then in the side region of an NW. The corner effect is dominant at a low V_G while it becomes less strong as V_G increases. Thus, it degrades the on–off transition abruptness of the total electron BTBT generation rates. Figure 6a shows the 2D contour of electrostatic potential. As shown in Figure 6b,c, the surface potential is higher at the corner than at the side in the entire range of V_G. This is because the charge at the corner is shared by the surrounding gate. The charge sharing effect at the corner contributes to the higher surface potential compared with the side one [29,30]. The difference in surface potentials in an NW affects the energy band diagrams of gate-normal NWTFETs. Figure 7 shows the energy band diagrams extracted,

at the corner and side, from the middle of the gate–source overlap region, respectively. Gate-normal tunneling, which is a main current mechanism of the gate-normal NWTFETs, occurs vertically in the gate–source overlap region, whereas the current is conducted laterally along the gate-controlled surface channel [10]. Then, in order to induce gate-normal tunneling, the band alignment in the direction perpendicular to the channel in the gate–source overlap region should be required [28]. When the V_G is 0.6 V, the conduction energy band edge (E_C) of the epi-layer is aligned with the valence energy band edge (E_V) of the source region at the corner, while the E_C of the epi-layer is not aligned with the E_V of the source region at the side. This is because the higher surface potential of the corner leads the energy band of the surface to shift down, which causes the gate-normal tunneling to turn on early. Thus, the corner and side of an NW have different BTBT turn-on voltages, which induce the hump behavior.

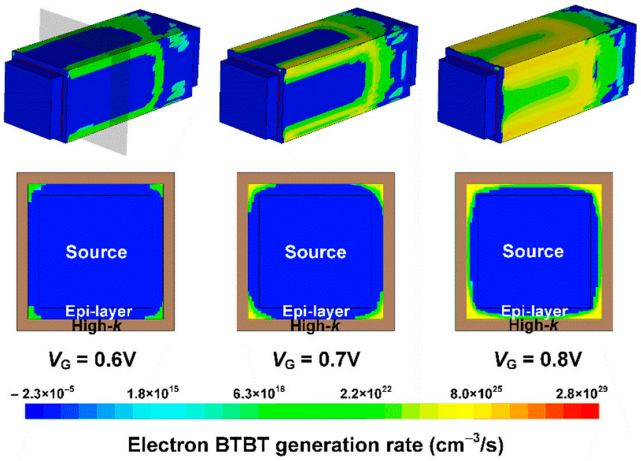

Figure 3. 3D and 2D contour plots of electron band-to-band tunneling (BTBT) generation rates of gate-normal NWTFETs at V_G = 0.6V, 0.7V, and 0.8V at V_D = 0.5V.

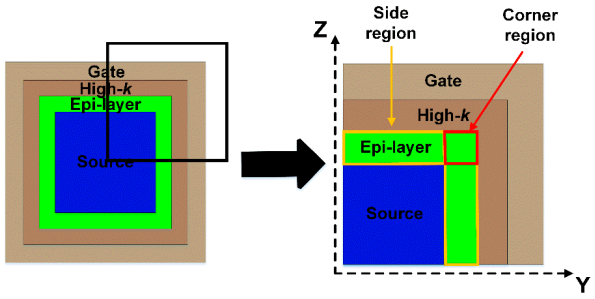

Figure 4. Definition of corner and side of a nanowire (NW).

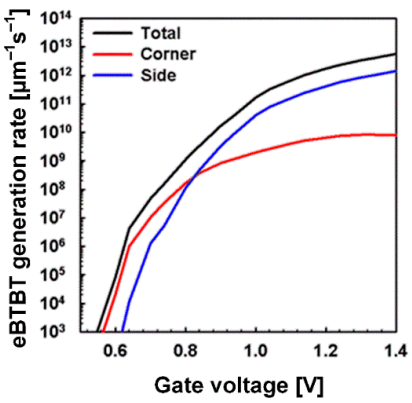

Figure 5. Electron BTBT generation rates per channel length extracted in the corner, side and total region as a function of V_G.

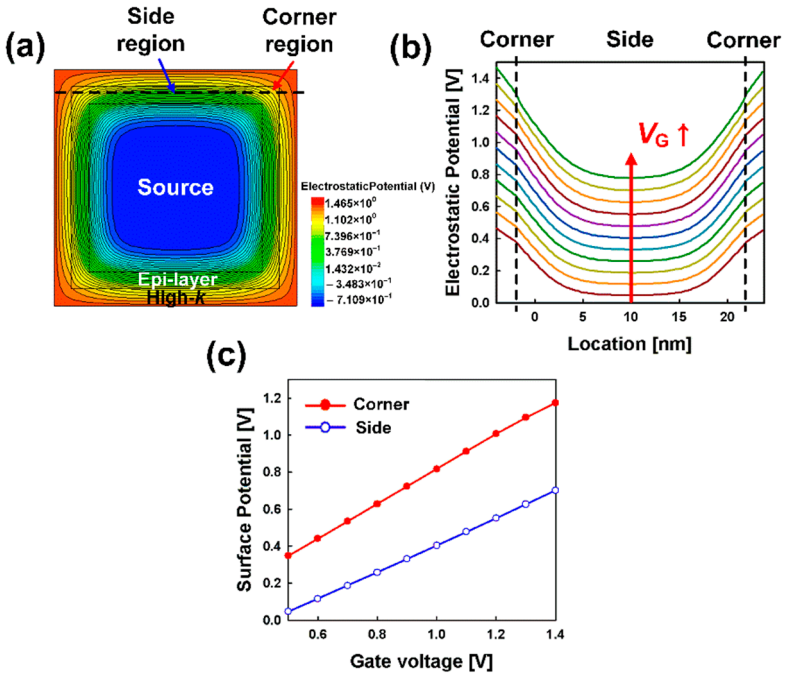

Figure 6. (**a**) 2D contour of electrostatic potential distribution at V_G = 1.5 V, (**b**) electrostatic potential of cut line as V_G increases (0.5 V–1.5 V), (**c**) surface potential at the corner and side.

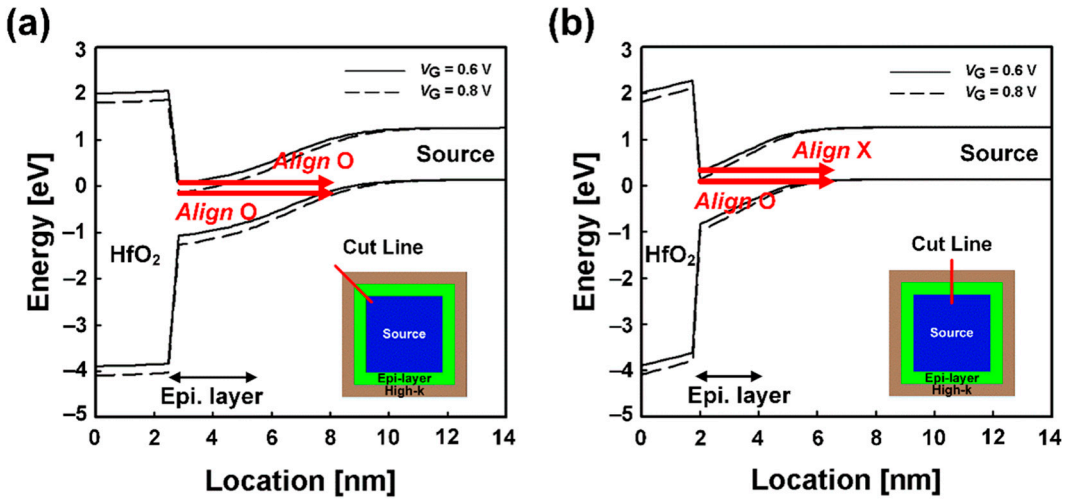

Figure 7. Energy band diagrams of the gate-normal NWTFETs extracted at the (**a**) corner and (**b**) side.

3.2. Hump Suppression by Rounding NW Corners and Reducing Gate Insulator Thickness

In order to improve the *SS* and I_{on} of the gate-normal NWTFETs, the hump behavior must be suppressed. In this paragraph the radius of curvature (R) of an NW and T_{ins} are optimized for the suppression of the hump behavior. The normalized R (R_{norm}) is defined as $2R/W_{inner}$. The three R_{norm} values are discussed as shown in Figure 8: 0, 0.4, and 1. Figure 9 shows the simulated transfer curves of the gate-normal NWTFETs with various R_{norm}s ranging from 0 to 1. As the R_{norm} increases, the hump behavior becomes weaker because the surface potential difference between the corner and side becomes smaller, as shown in Figure 10. The surface potential difference in an NW becomes 0 as R_{norm} becomes 1. In addition, as the corner behavior is alleviated, the short channel behavior is suppressed down [22,23]. Thus, it is observed that the $V_{turn\text{-}on}$ increases, the SS_{avg} improves, the I_{on}/I_{off} ratio increases, and the *DIBT* decreases, as shown in Figure 11. In the case of a cylindrical NW whose

R_{norm} is 1, the gate-normal BTBT evenly occurs on the entire surface. The gate-normal NWTFET whose R_{norm} is 1 shows a twofold higher I_{on} and a 5.4-fold higher I_{on}/I_{off} than that whose R_{norm} is 0.

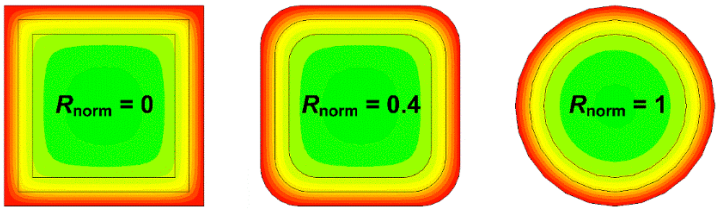

Figure 8. Cross-section of NWs with different *R*s.

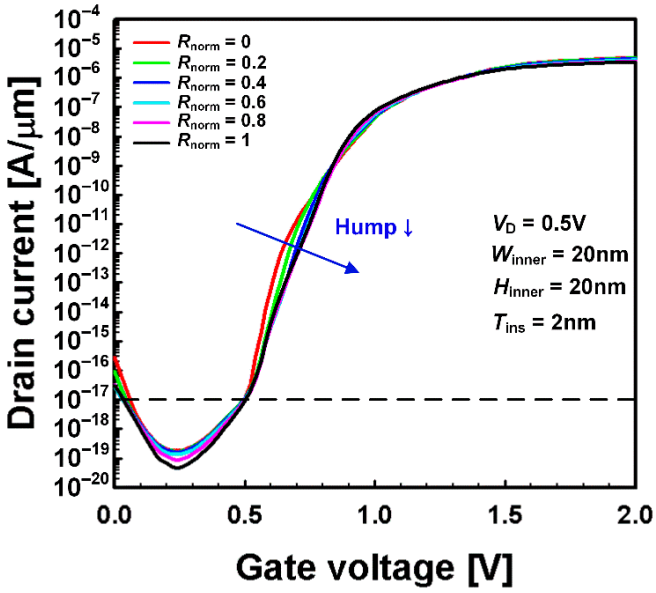

Figure 9. Transfer characteristics of gate-normal NWTFETs with the variation in the normalized radius of curvature of the corners (R_{norm}) from 0 to 1. It is shown that the hump is suppressed with the increasing of R_{norm}.

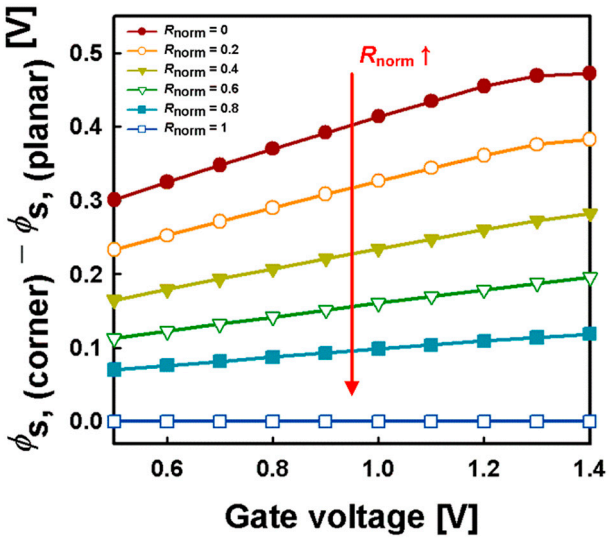

Figure 10. Surface potential difference between the corner and side with the variation in R_{norm}.

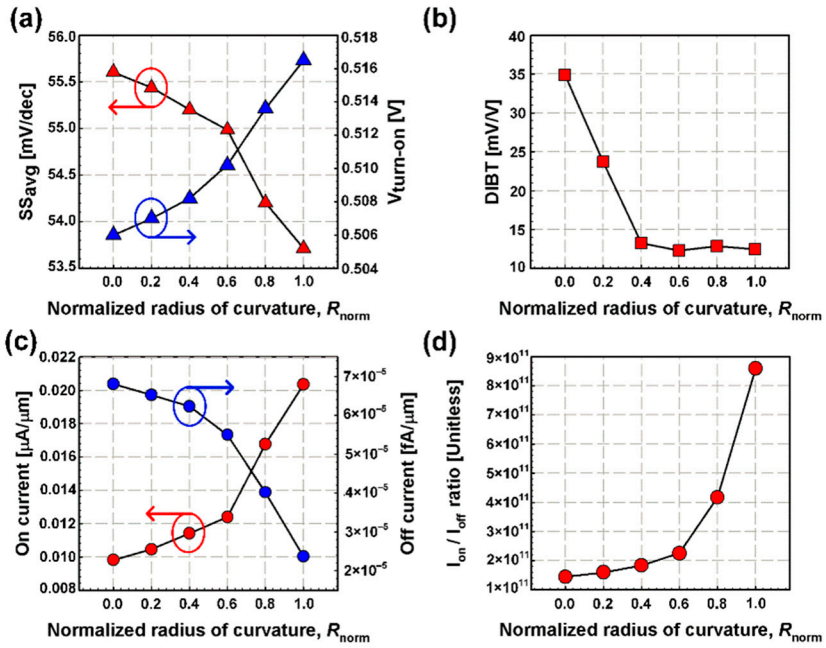

Figure 11. (**a**) SS_{avg} and $V_{turn\text{-}on}$, (**b**) *DIBT*, (**c**) I_{on} and I_{off} and (**d**) I_{on}/I_{off} ratio as a function of R_{norm}.

Another way to suppress the hump behavior is to reduce the T_{ins}. Figure 12 shows the simulated transfer curves with various T_{ins}s. As T_{ins} decreases, that hump is suppressed and the *SS* is improved because the gate's controllability over the channel becomes better. The surface potential on the gate–source overlap region increases as the T_{ins} decreases. However, as shown in Figure 13a, the potential at the side becomes higher than that at the corner as the T_{ins} decreases. It should be noted that the potential at the corner is less sensitive to T_{ins} than that at the side because the corners of an NW are surrounded by the gate [17]. Thus, as shown in Figure 13b, the surface potential difference between the corner and side decreases as the T_{ins} decreases. In other words, the difference in BTBT turn-on voltages in an NW is reduced, which means less hump behavior.

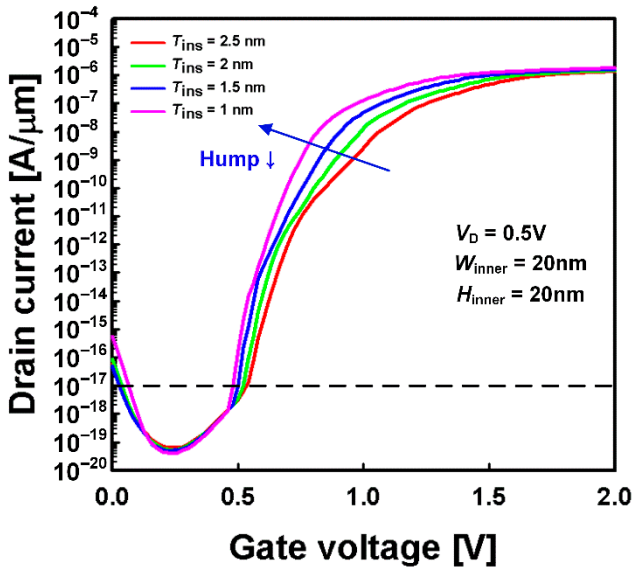

Figure 12. Transfer characteristics of NW gate-normal TFETs with the variation in thickness of gate insulator (T_{ins}).

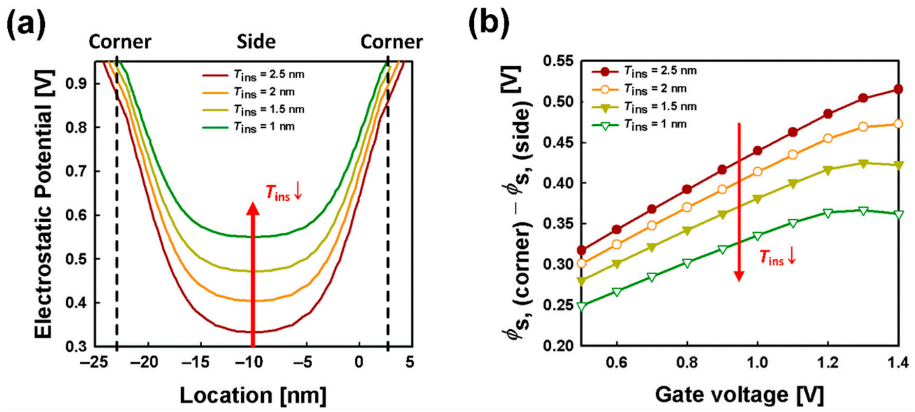

Figure 13. (**a**) Electrostatic potential with the variation in T_{ins} at V_G = 1 V; (**b**) Surface potential difference between the corner and side with the variation in T_{ins}.

4. Conclusions

The hump behavior of gate-normal NWTFETs is analyzed by using 3D TCAD simulation. It is discussed that the hump originates from the corner effect induced by the surrounding gate. BTBT occurs at the corner earlier than at the side due to the higher surface potential at the corner. By increasing R_{norm} and decreasing T_{ins}, the hump behavior can be suppressed. Cylindrical gate-normal NWTFETs with low T_{ins} are recommended for extremely low-power applications.

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