applied sciences

MDPI

Article

Evaluation of the Potential Electromagnetic Interference in Vertically Stacked 3D Integrated Circuits

Dipesh Kapoor [1], Cher Ming Tan [1,2,3,4,*] and Vivek Sangwan [5]

1 Center for Reliability Sciences & Technologies and Electronic Engineering Department, Chang Gung University, Taoyuan 33302, Taiwan; dipeshkapoor.dk@gmail.com
2 Institute of Radiation Research, College of Medicine of Chang Gung University, Taoyuan 33302, Taiwan
3 Department of Mechanical Engineering, Ming Chi University of Technology, New Taipei City 24301, Taiwan
4 Department of Urology, Chang Gung Memorial Hospital, Linkou, Taoyuan 33302, Taiwan
5 Center for Reliability Sciences & Technologies, Chang Gung University, Taoyuan 33302, Taiwan; sangwanvivek81@gmail.com
* Correspondence: cmtan@cgu.edu.tw

Received: 4 December 2019; Accepted: 16 January 2020; Published: 21 January 2020

Featured Application: Three-dimensional integrated circuit (3D-IC) is the trend for future C development because of its small form factor, high performance, low cost, and heterogeneous integration in system-in-package technologies. Several issues associated with 3D-IC besides their fabrication processes are being addressed, such as heat dissipation and so on, however, the electromagnetic interference between stacks has not been considered. In view of the high operating frequency, high power requirements of today IC, and together with the decreasing separation between the stacked dies, investigation on the subject matter is necessary, as they will soon become important. Unfortunately, the study of electromagnetic interference (EMI) within 3D-IC is difficult from the measurement, as elaborated in this paper. In this work, we develop a simulation methodology and show the importance of EMI evaluation for 3D-IC, and we also illustrate the presence of minimum separation between the stacked dies for the avoidance of EMI.

Abstract: Advancements in the functionalities and operating frequencies of integrated circuits (IC) have led to the necessity of measuring their electromagnetic Interference (EMI). Three-dimensional integrated circuit (3D-IC) represents the current advancements for multi-functionalities, high speed, high performance, and low-power IC technology. While the thermal challenges of 3D-IC have been studied extensively, the influence of EMI among the stacked dies has not been investigated. With the decreasing spacing between the stacked dies, this EMI can become more severe. This work demonstrates the potential of EMI within a 3D-IC numerically, and determines the minimum distance between stack dies to reduce the impact of EMI from one another before they are fabricated. The limitations of using near field measurement for the EMI study in stacked dies 3D-IC are also illustrated.

Keywords: 3D-IC (three-dimensional integrated circuit); electromagnetic interference; near field measurement

1. Introduction

Three-dimensional stack-dies integrated circuit (3D-IC) is a technology used for multi-functionality and high-speed circuit devices [1]. 3D-IC has received much interest recently because of its small form factor, high performance, and heterogeneous integration in system-in-package technologies [2–4].

Three-dimensional technologies can provide higher chip-to-chip bandwidths at lower power levels that cannot be accomplished with available conventional packaging techniques. Additionally, they also offer the potential for low cost through heterogeneous integration. Interposers offer the first step to 3D integration of ICs, which simplifies physical planning and thermal management [4]. To achieve higher performance and reliability in 3D-IC, new design rules have to be developed because of the specific electrical, mechanical, and thermal constraints of 3D stacks [5–7].

Although stacking of chips began from memory and later on extend to logic chip, the technology of stacking is now also extending to radio frequency applications, which consist of mixed-signal IC to benefit from the 3D integration including shorter propagation delay; full isolation between analog and digital circuits in mixed-signal 3D-IC [8,9]; and lower parasitic, which can reduce power consumption. With the 5G chip, this will be a trend.

Despite the above-mentioned advantages, there are several challenges associated with 3D-ICs. The two most significant challenges are the quality of the wafer–wafer bonding and thermal management. Three-dimensional technology poses a major challenge in thermal management owing to the increase in power density and number of vertically stacked active layers [10,11]. Therefore, researchers have made efforts to solve for the thermal stress issue in 3D-ICs through thermally aware floor planning or task scheduling [12].

Besides these challenges, there is another emerging challenge that has been rather overlooked, namely the electromagnetic coupling between stack dies [13–15]. These electromagnetic couplings are known as electromagnetic interferences (EMIs), which are a consequence of high frequency switching currents, complex power delivery paths, and an increase in parasitic couplings in comparison with 2D integration.

The increase in the parasitic couplings between stacked dies is the result of the decreasing stack up distances between them, as shown in Figure 1, as extracted from the works of [16–23]. In 2017, this distance decreased to 15 µm [16] from 150 µm in year 2000 [22], which is a 10-fold decrement. This decrease is necessary in order to maximize the advantages of 3D vertical integration including shorter interconnect lengths, greater integration density, and lower power consumption, which enhances the overall performance of the system with such technologies. The main driving forces to keep the stack distance lesser between the stacked dies are the increased demand of dies with faster data exchange rate, lower power consumption, and smaller size, and such a decreasing trend is expected to continue in the future.

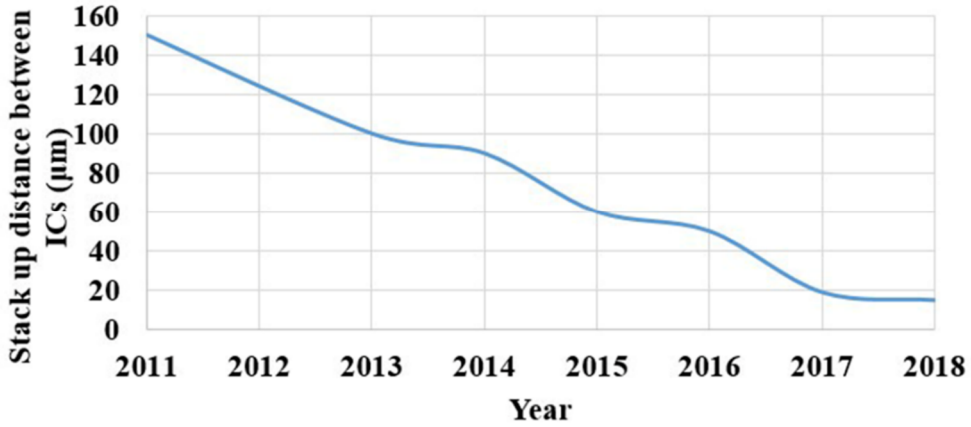

Figure 1. Three-dimensional stack-dies integrated circuits (3D-ICs) trend for vertical distance between ICs [16–23].

With this decreasing trend of the distance between the dies, one limitation will be the thermal dissipation of the 3D-IC, and another one will be the electromagnetic interference between them. If

one of the dies in the 3D-IC stack is the source of EMI, it could affect the nearby dies when the distance between them is small. This work explores the latter limitation.

This limitation depends on two factors. One is the circuit susceptible to EMI and another one is the parasitic coupling. The former one requires ingenious circuit design, which is beyond the scope of this work.

To reduce the parasitic coupling with the decreasing distance between the dies, several possibilities are available. Adding of ground plane between them or adjusting the placement of vias to conduct away the electromagnetic field are some examples. Irrespective of the methods employed, a method to evaluate the EMI in the stack before fabrication of the 3D stack dies will be necessary.

Near-field (NF) measurement is the basic for the detection of EMI at IC level. In the work of [24], the correlation between near field scanning and electrostatic discharge susceptibility measurement of the CPU IC is studied, which is an initial study for the application of NF measurement. In another paper [25], a procedure is shown to characterize radiated EMI and nearby conducting objects using near-field scanning measurements. Yu et al. [26] proposed a model from near-field measurement to calculate the magnitude and phase of the dipoles. In the work of [27], Slattery showed that near field scanning can be utilized to calculate far field from the IC. ICs are often the primary source of radiated emissions, and near field magnetic field can help engineers to track down EMI culprit and solve the problems with a robust IC design [28].

With the well-known rapid decrease of the intensity of EM wave with the distance [29], if the source for high EMI is from the die in the middle of the stack of a 3D-IC, such near field measurement will not be able to pinpoint the source of high EMI. Therefore, a computational method is required, and if the computation can be performed before the fabrication of the dies, the cost and time for re-design can be saved significantly, and it is this necessity that forms the motivation of this work.

While the equation of the intensity of electromagnetic field strength versus distance is well known, the 3D distribution of the field strength in the presence of various materials within each die, as well as the 2D distribution of electromagnetic field over a given circuit on a die, are to be determined in order to evaluate the EMI. This work proposes a simulation method from a given GDSII file for such evaluation, and we aim to provide the evaluation before the fabrication of the 3D-IC.

The example studied in this work on the stacking of power amplifier ICs is expected to be the future, and research is being done on the thermal management [30–33]. While thermal management research is being considered, the impact of electromagnetic interference (EMI) among the stack dies has not been studied. This work represents the first of its kind. Advancements in the functionalities and operating frequencies of integrated circuits (IC) have led to the necessity of measuring their EMI. The stacking of power amplifier chips in this work can be considered as an extreme case so as to bring out the important of the EMI consideration in stack dies more vividly, and it is also a good example of generalization of ICs with multi functionality of communication, high performance, and high frequency IC technology. The methodology developed here can be applied easily to other cases of stack dies.

2. Integrated Circuit under Study

This work employs the gallium nitride high electron mobility transistor (GaN-HEMT) power amplifier IC as an example, which operates on frequency range of 2–4 GHz (S-band of electromagnetic spectrum). This IC possess the current advancements in frequency and power, which makes it a potential candidate to study the effect of EMI in this work. To illustrate the methodology developed here, we use a hypothetical 3D-IC where we stack up two and three of this same IC to form the 3D-IC in this work, and the severity of EMI in the stacked dies is also computed.

An optical image of the power amplifier IC under study at 1600× magnification is shown in Figure 2. Its input power (Pin) is 28 dBm and the corresponding output power (Pout) is 30.3 dBm. Drain to source voltage (VDS) of the transistors is 26 V with the gate to source voltage (VGS) of −2.8 V. The dimensions of the IC are 1700 μm × 1400 μm × 107.92 μm.

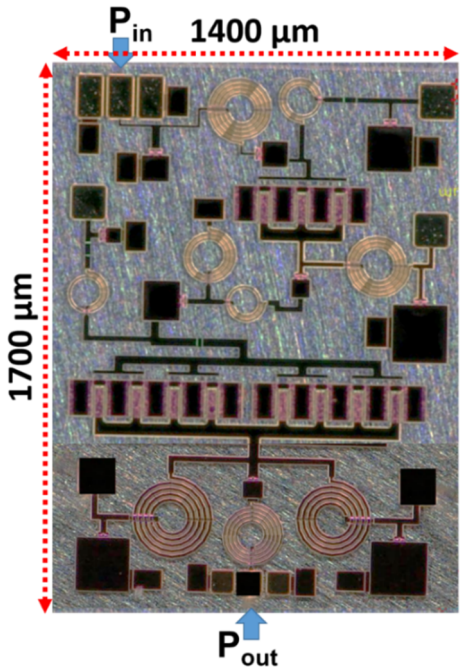

Figure 2. Image of power amplifier IC at 1600× magnification captured (using Leica S8 APO equipment).

3. Simulation Methodology

Recently, Tan et al. [34] developed a method to "fabricate" an IC from its GDSII file in a computer under ANSYS environment. Once the IC is fabricated, the ANSYS high frequency structure simulator (HFSS) is employed to compute the EM field distribution over the surface of the chip. ANSYS HFSS has a limitation that it cannot simulate transistors. To overcome the limitation of ANSYS HFSS, transistors are removed from the layout and respective voltages and currents as obtained from circuit simulator are inputted at respective circuit nodes for the proper functionality of the IC. With such replacements, our circuit can be completed, and the currents thus computed will be accurate. In this work, the values of these voltages and currents are obtained from the advanced design systems (ADSs) file of the circuit during the circuit simulation in the post layout phase. Figure 3 shows the flow chart of the method as also reported in the work of [28] for clarity, and Figure 4 shows the "fabricated" IC in the ANSYS environment. With this method, the magnetic field distribution of the IC can be obtained at different frequencies (2, 3, and 4 GHz). The method is verified with experimental results, as shown in the work of [34].

In Figure 4a, black circles represent input ports, while Pin is another input port used in simulation in HFSS.

The following equations are used in determining the electromagnetic distribution as given below [35]:

$$\nabla \times (\frac{1}{\mu_r} \nabla \times E(x,y,z)) - k_0^2 \varepsilon_r E(x,y,z) = 0\,, \tag{1}$$

$$H = \frac{\nabla \times E}{-j\omega\mu}\,, \tag{2}$$

$$\nabla \times (\frac{1}{\mu_r} \nabla \times E(x,y,z)) - (k_0^2 \varepsilon_r - jk_0 Z_0 \sigma) E(x,y,z) = 0, \tag{3}$$

$$E(x,y,z) = \int_S (j\omega\mu_0 H_{\tan} G + E_{\tan} \times \nabla G + E_{normal} \nabla G) dS, \tag{4}$$

where

$E(x,y,z)$ is a phasor representing an oscillating electric field;
k_0 is the free space wave number;
$\omega \sqrt{\mu_0 \varepsilon_0}$, where ω is the angular frequency, which is $2\pi f$;
μ_r is the complex relative permeability;
ε_r is the complex relative permittivity;
S represents the radiation boundary surfaces;
j is the imaginary unit ($\sqrt{-1}$);
ε_0 is the relative permeability of the free space;
H_{tan} is the component of the magnetic field that is tangential to the surface;
E_{normal} is the component of the electric field that is normal to the surface;
E_{tan} is the component of the electric field that is tangential to the surface;
G is the free space Green's function;
J is the current density.

Equations (1)–(3) are employed in the finite element method (FEM). FEM solves for the three-dimensional electromagnetic field, taking x, y, and z directions in consideration, and solves for the volume distribution using the curl function. As we are dealing with 3D IC, FEM in ANSYS HFSS will be most appropriate for the determination of EM distribution.

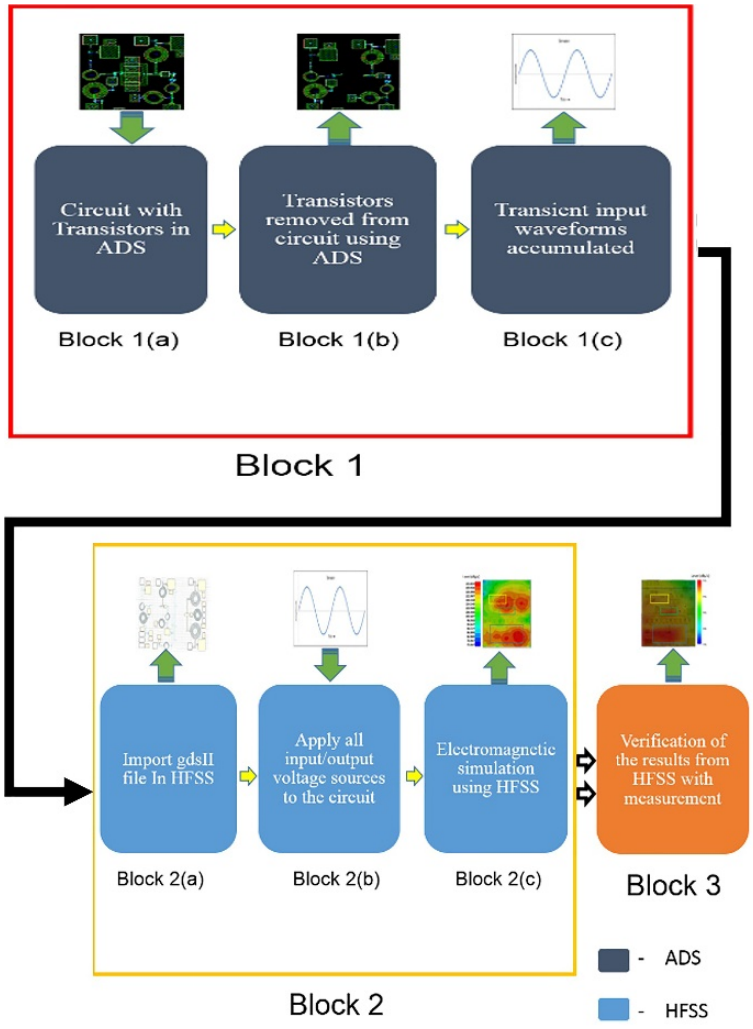

Figure 3. Flow chart of the methodology followed for simulation [28]. ADS, advanced design system; HFSS, high frequency structure simulator.

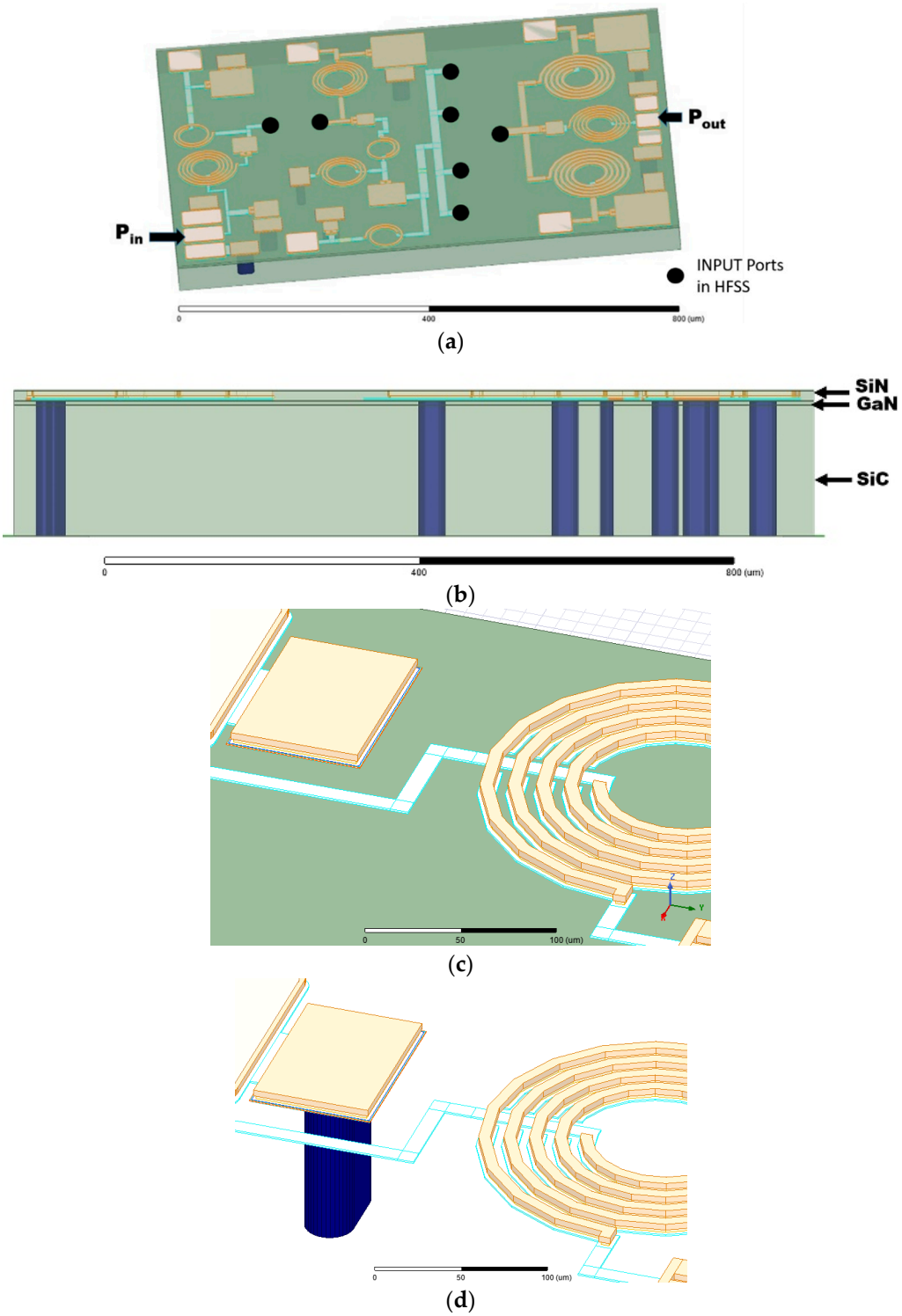

Figure 4. Power amplifier IC layout in HFSS: (**a**) 3D isometric view where black circles represent input ports, (**b**) side-view with dielectric layers information about material, (**c**) zoomed in view of layout with substrate, and (**d**) zoomed in view of layout without substrate (blue color represents via). GaN, gallium nitride; SiC, silicon carbide; SiN, silicon nitride.

To perform electromagnetic field calculation, FEM is necessary. This necessity can be seen by comparing the magnetic field simulation using HFSS (which utilizes FEM) and SIwave (which uses method of moments (MOM)). Figure 5a shows the test structure used for magnetic field simulation and Figure 5b shows the results. One can see a significant difference in the amplitude and distribution

of the magnetic field between the two methods. As solved Maxwell equations in FEM (3D method) will be more accurate, MOM (2.5D method) should be used with caution.

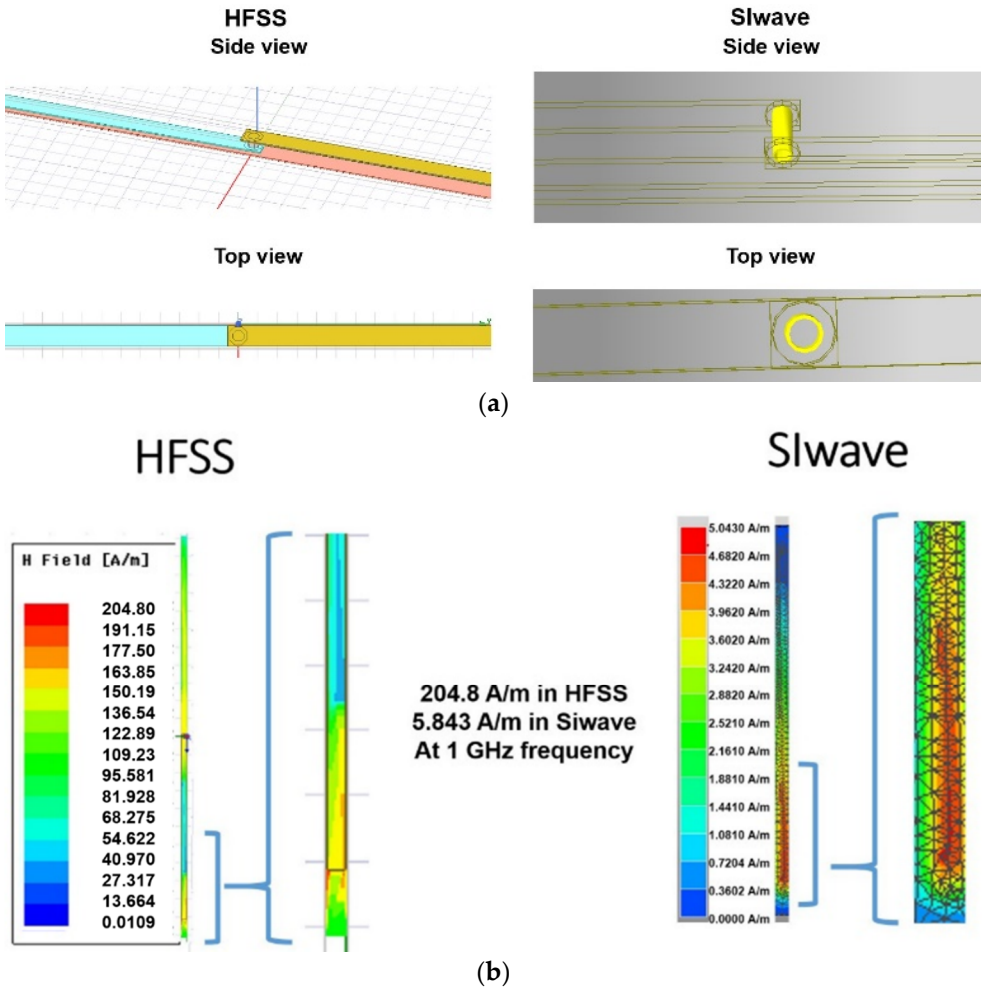

Figure 5. Comparison of method of moments (MOM) and finite element method (FEM) simulation: (**a**) side and top view of test structure used for simulation, (**b**) magnetic field distribution in HFSS (3D method) and SIwave (2.5D method) software, respectively.

The impact of the H-field is more significant than electric field emissions in vicinity of the device, as wave impedance for the H-field is small and increases with the distance from the source [36]. After some distance from the source, wave impedances of the H-field and electric field become same, which is found to be 318 mm for the present case, as calculated using the Equation in the work of [36]. However, near field measurements in the present scenario are conducted at 0.2 mm, and thus magnetic field analysis becomes important. For the effect of EMI on 3D-IC circuits, the distance is even smaller, and hence magnetic field computation is the focus of this work.

Dielectric layers used in ANSYS HFSS simulation methodology are silicon carbide (SiC), GaN, and silicon nitride (SiN) to resemble the actual IC. Perfect electric conductor (PEC) boundary condition is used for ground plane and lumped port excitation is provided [34]. The overall electromagnetic simulation takes around 20 min.

Figure 6 shows the simulation result for 3 GHz operating frequency, respectively. Such a simulation method has been verified experimentally in our other works [34].

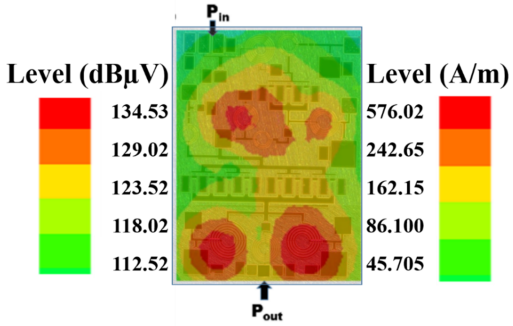

Figure 6. Magnetic field distribution obtained through HFSS simulation over the gallium nitride high electron mobility transistor (GaN-HEMT) power amplifier IC at 3 GHz operating frequency.

4. Electromagnetic Field Intensity Distribution

Figure 7 shows the magnetic field strength of the device under test plotted at various vertical distances and operating frequencies from the surface of the IC. The maximum magnetic field strength of 1.07×10^5 A/m, at 3 GHz operating frequency, is present at the top surface of the IC, and it decreases to 4.60×10^4 A/m drastically within a very small change in distance (around 1 μm) from the surface of the IC. At 40 μm vertically from the surface of the IC, the maximum magnetic field strength is reduced to approximately 10^3 A/m, and it is reduced to around 10^2 A/m at 140 μm above the surface. This is expected as the magnetic field is inversely proportional to square of the distance according to inverse square law [27]. Therefore, with the current commercial near field measurement at 200 μm from the surface, the severity of EMI from an IC can be underestimated, but this can be unimportant as the EMI strength decreases rapidly outside the package. However, such EMI can affect the nearby circuits within a chip and has yet been overlooked. Either these nearby circuits can be on the same die, or they can be on the stacked die, if they are close. If the strong EME source is within the stack dies instead of the topmost die, its identification will not be possible with the current near field measurement. In fact, even if the hot spot for EME is on the topmost die, its identification will be difficult, as illustrated below.

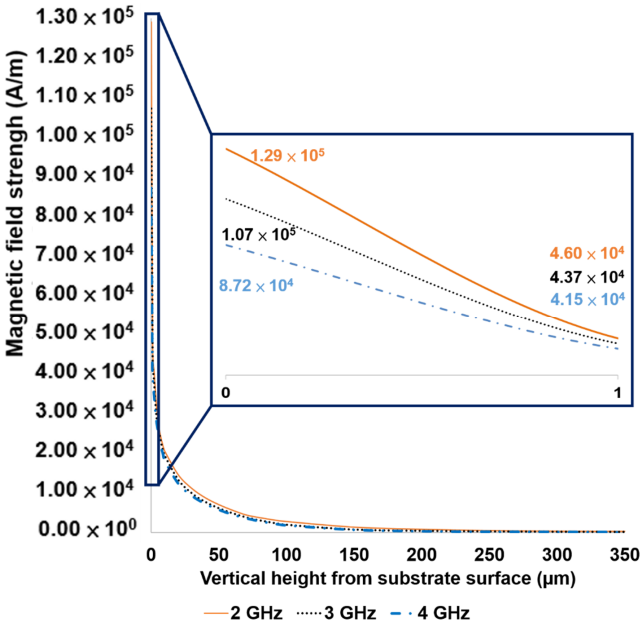

Figure 7. Maximum magnetic field strength versus vertical height of reference plane at different operating frequencies (2, 3, and 4 GHz).

Figure 8a shows the magnetic field distribution at the surface of the IC, where the spot for high EME can be identified with high precision. As the observational plane moves away from the surface, the area of the hot spot disperse, and this dispersion renders it difficult to identify the actual source of EME precisely. At 50 µm, several hot spots of EME appear as a result of the dispersion, and this can result in tackling the wrong parts of a circuit to reduce the EMI. Such a situation will be very likely for stacked dies in 3D. In other words, even if high EME exists on a die, localization of hot spot through electromagnetic field measurement will not be possible.

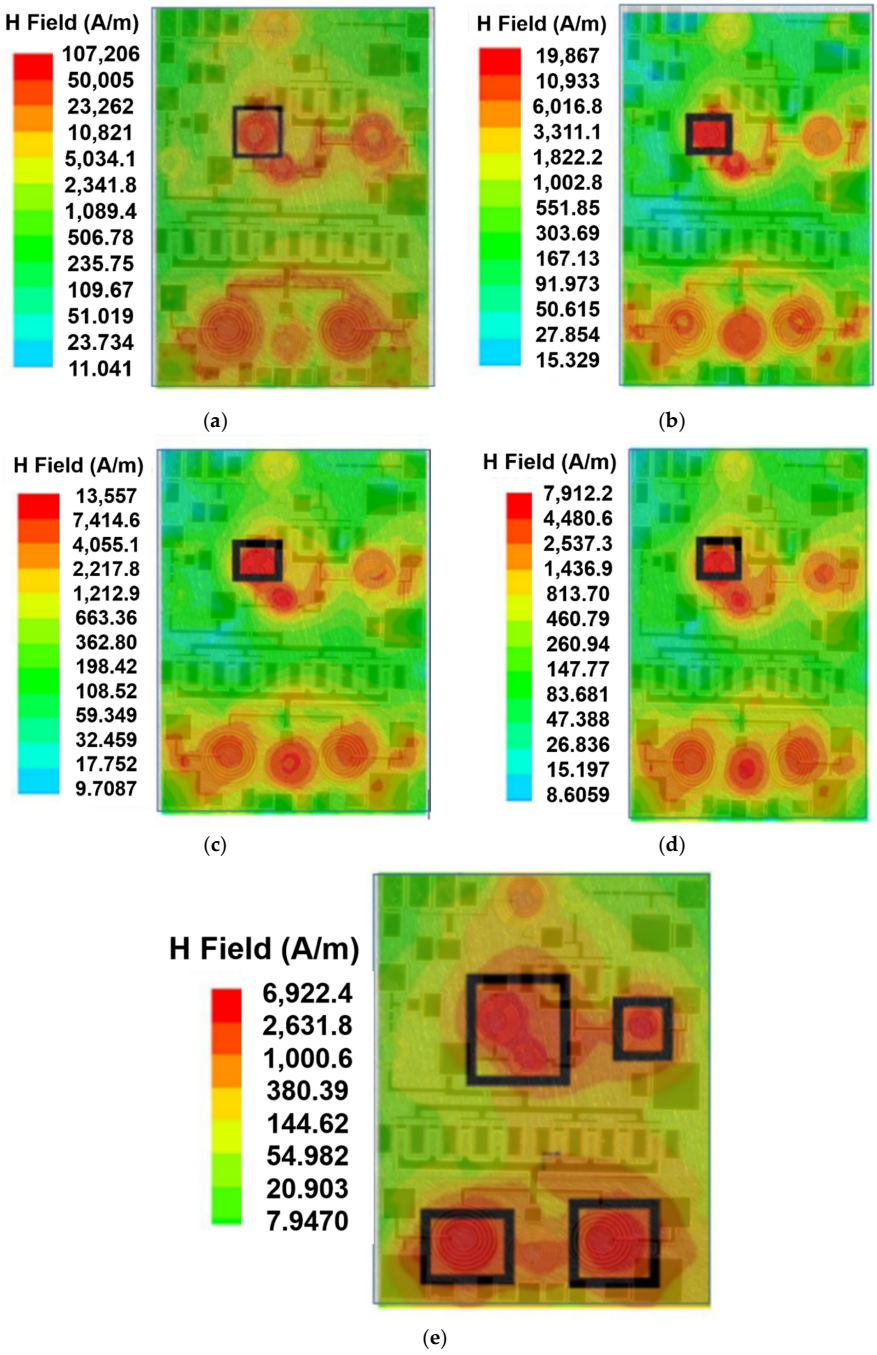

Figure 8. Maximum magnetic field strength for an operating frequency of 3 GHz at different vertical heights: (**a**) 0 µm (black box represents the maximum emission region), (**b**) 10 µm, (**c**) 20 µm, (**d**) 40 µm, and (**e**) 50 µm.

In fact, the above results indicate that the vertical distance for near field (NF) scanning should be in the region from 10 to 40 µm. However, below 10 µm, the equipment required to perform NF measurement is not available and, beyond 40 µm, the precision to find the source of EMI is low. Thus, simulation of EM field strength is necessary. In practical measurement, the probe distance is usually set at 200 µm to prevent the damage to the probe during scanning.

As the electromagnetic field strength decreases significantly over the distance, one can determine the minimum distance between dies separation for 3D-ICs, so that the effect of EMI from a die will have minimum effect on other dies in a stack. To investigate this minimum separation between the dies, simulation is performed on a hypothetical 3D-IC using GaN-HEMT power amplifier IC, as shown in Figure 9, with two dies (2D-3D-IC) and three dies (3D-3D-IC) aligned vertically to each other. The vertical separation between the dies (denoted as 'X') varies from 25 µm to 300 µm in this work.

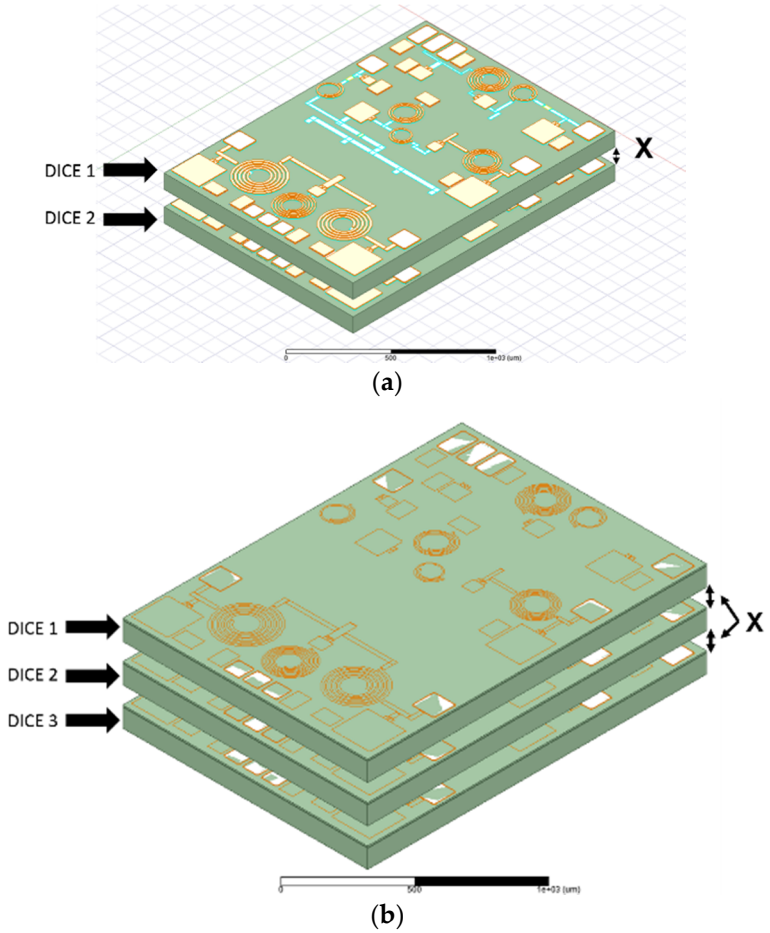

Figure 9. Hypothetical 3D-IC layout in HFSS: (**a**) two layers in stack of 3D-IC (2D-3D-IC) and (**b**) three layers in stack of 3D-IC (3D-3D-IC).

Figure 10 shows the magnetic field distributions on the surface of the topmost die as the distance between the two dies vary in 2D-3D-IC. Change in 'X' changes the magnitude of the magnetic field distribution significantly, as expected, especially when the distance between them is very small. The distribution pattern remains the same, as all the operational conditions are identical.

Figure 11 shows that the maximum magnetic field strength for 2D-3D-IC at the surface is 7.44×10^5 A/m, where the red line represents the maximum magnetic field strength for single IC at the surface, which is 1.07×10^5 A/m. We are seeing more than double in the maximum magnetic field strength with an additional die. This value decreases rapidly as we increase the dies' separation, but it is always more than 1.07×10^5 A/m, showing the significant effect of EMI from one die to another in a stack. The EMI increases up to seven times when two dies stack up.

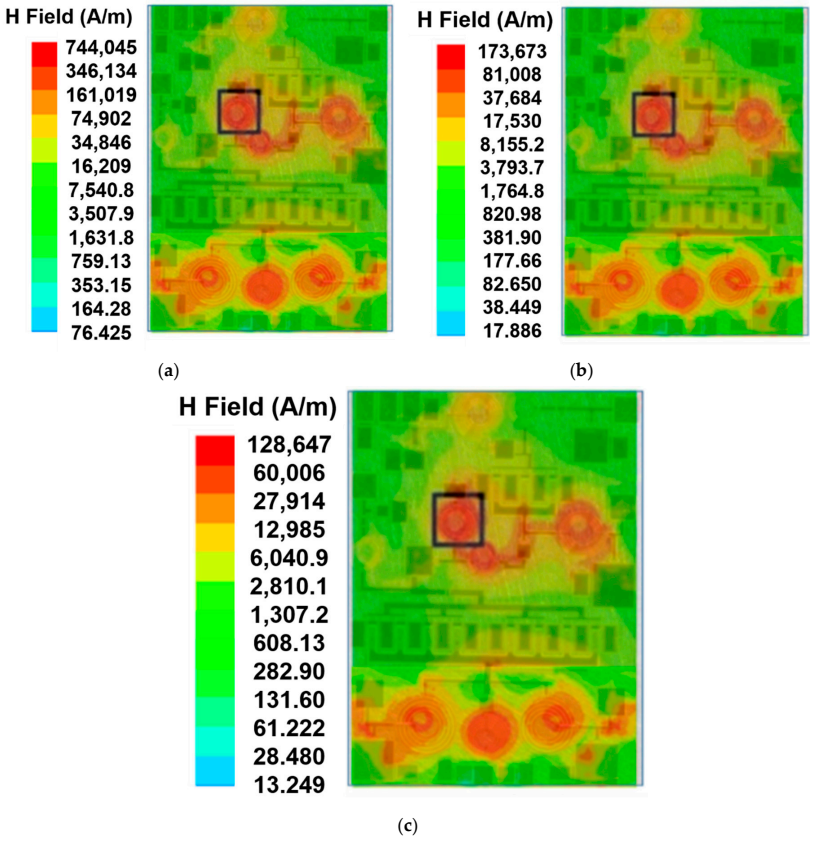

Figure 10. Maximum magnetic field strength at the surface of top IC with different vertical separation between the dies in a stack of 3D-IC with two layers. The vertical separation is as follows: (**a**) 0 µm, (**b**) 50 µm, and (**c**) 300 µm, respectively, and the operating frequency is 3 GHz.

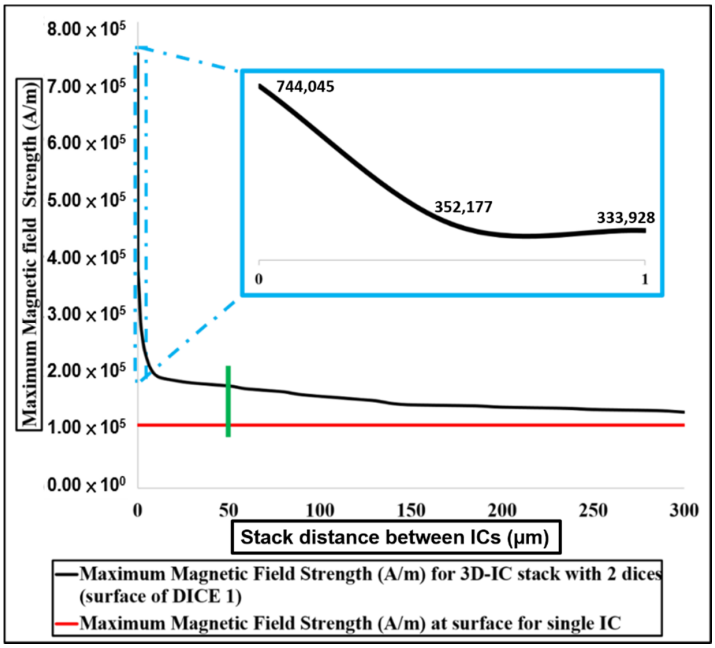

Figure 11. Maximum magnetic field strength versus the distance between the layers of 2D-3D-IC at 3 GHz operating frequency.

Figure 12 shows the difference in the maximum magnetic field for 2D-3D-IC and 3D-3D-IC, where the black line represents the maximum magnetic field strength for single IC at the surface, which is 1.07×10^5 A/m. The maximum magnetic field strength for 3D-3DIC structure obtained is 4.28×10^6 A/m. Although this maximum value decreases as we increase the dies' separation, it will always be greater than 7.44×10^5 A/m, which is maximum magnetic field strength of the 2D-3D-IC structure. In other words, the more dies are stacked up, the higher will be the maximum magnetic field strength. Hence, it could be possible that each die in a stack may not have high EME, and the stacked structure could have very high EME that renders circuit malfunction.

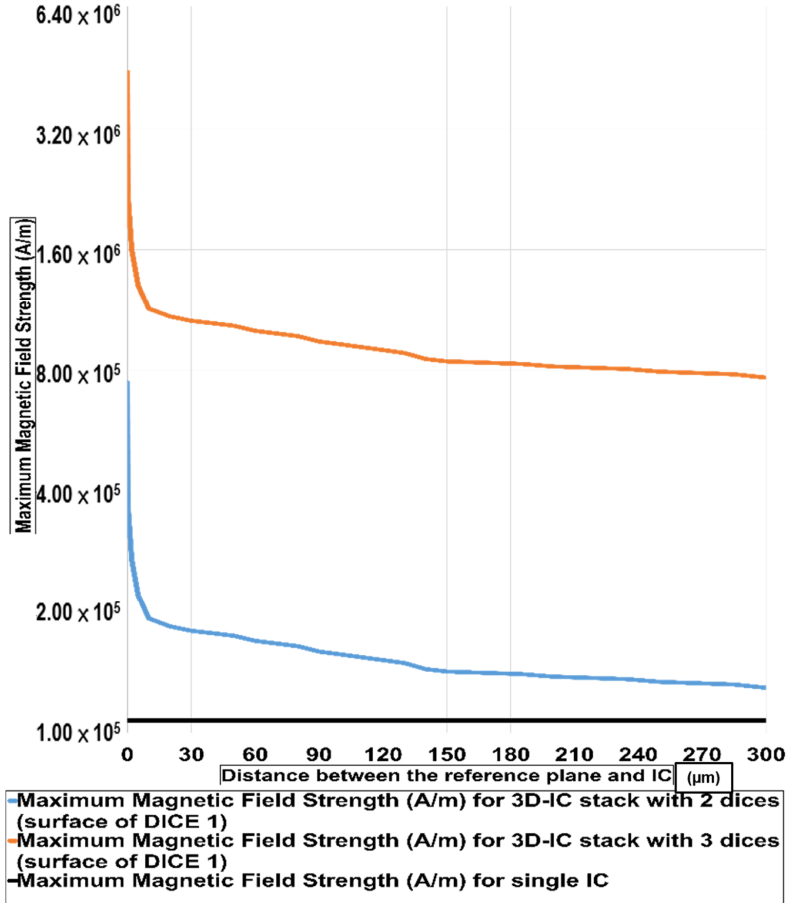

Figure 12. Maximum magnetic field strength versus the distance between the reference plane and topmost layer of 3D-IC at 3 GHz operating frequency.

Figure 13 shows the maximum magnetic field strength on the top surface of each die in the 3D-3D-IC stack, and one can see that the maximum field strength occurs at the top surface of the middle die. This is expected as it is placed in the middle of the two dies and it gets the emissions from the top and bottom dies.

With the decrease of 'X' in 3D-ICs, an increase in the EMI can be expected. Tradeoff is thus required to keep the emissions and distance in check, and it requires careful evaluation, which is demonstrated in this work.

For the example used in this work, the optimum distance between stack of dies should be around 50 µm for 2D-3D-IC, while this value increases to 105 µm for 3D-3D-IC, shown by green lines in Figures 11 and 13, respectively. These values are considered because further increase in 'X' does not result in a significant reduction in the magnetic field. If the lowest EMI is needed, then 'X' should be even more, but there is a limit on the minimum magnetic field achievable, which is higher with a higher number of stacked dies.

The lowest EMI in 3D-IC structure is always higher than the single IC, as can be seen in Figures 12 and 13, and thus reduction of EMI from a 3D-IC architecture is critical.

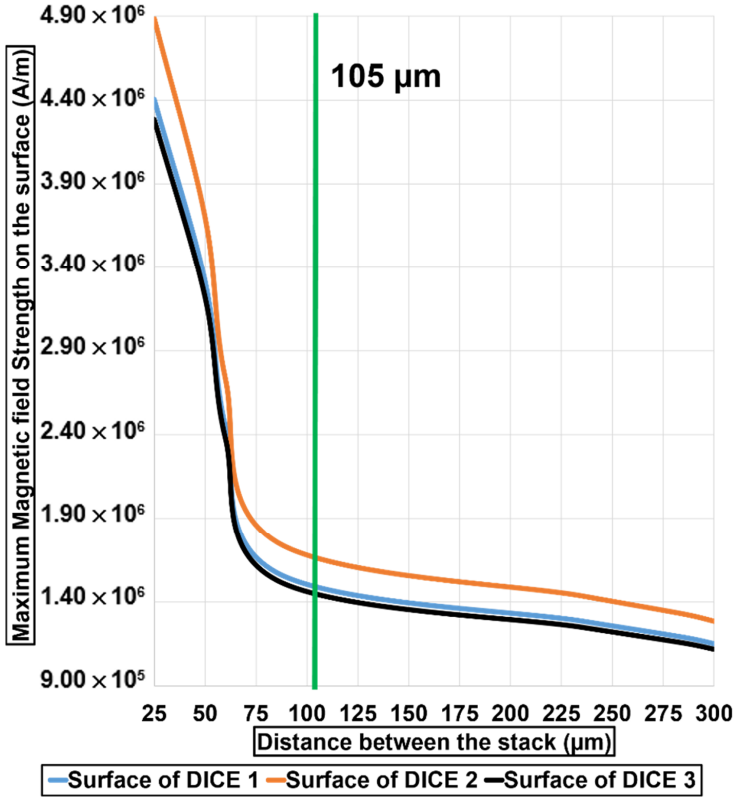

Figure 13. Maximum magnetic field strength versus the distance between the layers of 3D-IC at 3 GHz operating frequency at the top surface of all the dies.

5. Conclusions

Integrated circuits for high-speed applications are prone to electromagnetic interference (EMI) issues. For detecting these EMIs, near field electromagnetic measurement is an important tool, as it is helpful in determining the locations of high electromagnetic emission (EME hot spots) within the IC. As the 3D stack dies technology is increasingly important owing to its several advantages, the EMI issue within the stacked dies must be considered when the stack dies are high frequency and high power.

However, near field electromagnetic measurement is ineffective to identify the hot spots of electromagnetic emission within the stacked dies, as illustrated in this work, and a computational method is developed to evaluate and identify the EME hot spots in integrated circuits with experimental verification. Using this method, we found that the EMI issue within the stack dies is a lot more severe. This work shows that the minimum value of the maximum magnetic field strength for 3D-stacked IC, as the distance between the stack increases, is about six times higher than an un-stacked IC. If the stack distance is smaller, the magnetic field strength can be as high as 16 times as compared with an unstacked IC. Thus, a minimum distance between the stack must be maintained. The actual minimum distance depends on the electromagnetic susceptible of the designed circuit. The method developed in this work can be done at the IC design stage before fabrication, enabling optimization of the stack distance as well as circuit design for reducing the EMI, and eliminating the significant cost of fabrication owing to improper design.

Author Contributions: Conceptualization, C.M.T.; Methodology, D.K.; Software, D.K.; Validation, D.K.; Formal analysis, V.S.; Investigation, D.K.; Resources, C.M.T.; Data curation, V.S.; Writing—original draft preparation, D.K.;

Writing—review and editing, C.M.T.; Visualization, D.K.; Supervision, C.M.T.; Project administration, C.M.T.; Funding acquisition, C.M.T. All authors have read and agreed to the published version of the manuscript.

Funding: This work was funded by the Chang Gung University research Grant QZRPD123 and CIRPD2F0024.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Zhan, C.J.; Juang, J.Y.; Lin, Y.M.; Huang, Y.W.; Kao, K.S.; Yang, T.F.; Lu, S.T.; Lau, J.H.; Chen, T.H.; Lo, R.; et al. Development of fluxless chip-on-wafer bonding process for 3DIC chip stacking with 30 μm pitch lead-free solder micro bumps and reliability characterization. In Proceedings of the 2011 IEEE 61st Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, USA, 31 May–3 June 2011; pp. 14–21. [CrossRef]
2. Knickerbocker, J.U.; Andry, P.S.; Dang, B.; Horton, R.R.; Interrante, M.J.; Patel, C.S.; Polastre, R.J.; Sakuma, K.; Sirdeshmukh, R.; Sprogis, E.J.; et al. Three—Dimensional silicon integration. *IBM J. Res. Dev.* **2008**, *52*, 553–569. [CrossRef]
3. Dang, B.; Wright, S.L.; Andry, P.S.; Sprogis, E.J.; Tsang, C.K.; Interrante, M.J.; Webb, B.C.; Polastre, R.J.; Horton, R.R.; Patel, C.S.; et al. 3D chip stacking with C4 technology. *IBM J. Res. Dev.* **2008**, *52*, 599–609. [CrossRef]
4. Emma, P.G.; Kursun, E. Is 3D chip technology the next growth engine for performance improvement? *IBM J. Res. Dev.* **2008**, *52*, 541–552. [CrossRef]
5. Chaabouni, H.; Rousseau, M.; Leduc, P.; Farcy, A.; Thuaire, R.E.F.A.; Haury, G.; Valentian, A.; Billiot, G.; Assous, M.; de Crecy, F.; et al. Investigation on TSV impact on 65nm CMOS devices and circuits. In Proceedings of the 2010 International Electron Devices Meeting, San Francisco, CA, USA, 6–8 December 2010; pp. 796–799. [CrossRef]
6. Cherman, V.O.; de Messemaeker, J.; Croes, K.; Dimcic, B.; van der Plas, G.; de Wolf, I.; Beyer, G.; Swinnen, B.; Beyne, E. Impact of through silicon vias on front-end-of-line performance after thermal cycling and thermal storage. In Proceedings of the 2012 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, USA, 15–19 April 2012; pp. 5–9. [CrossRef]
7. Beyne, E. Electrical, thermal and mechanical impact of 3D TSV and 3D stacking technology on advanced CMOS Devices-Technology directions. In Proceedings of the 2011 IEEE International 3D Systems Integration Conference (3DIC), Osaka, Japan, 31 January–2 February 2012. [CrossRef]
8. Yahalom, G.; Ho, S.; Wang, A.; Ko, U.; Chandrakasan, A. Analog-Digital Partitioning and Coupling in 3D-IC for RF Applications. In Proceedings of the 2016 IEEE International 3D Systems Integration Conference (3DIC), San Francisco, CA, USA, 8–11 November 2016; pp. 1–4.
9. Uemura, S.; Hiraoka, Y.; Kai, T.; Dosho, S. Isolation Techniques Against Substrate Noise Coupling Utilizing Through Silicon Via (TSV) Process for RF/Mixed Signal SoCs. *IEEE J. Solid-State Circuits* **2012**, *47*, 810–816. [CrossRef]
10. Li, F.; Nicopoulos, C.; Richardson, T.; Xie, Y.; Narayanan, V.; Kandemir, M. Design and management of 3D chip multiprocessors using network-in-memory. *Proc. Int. Symp. Comput. Archit.* **2006**, *2006*, 130–141. [CrossRef]
11. Loi, G.L.; Agrawal, B.; Srivastava, N.; Lin, S.C.L.S.C.; Sherwood, T.; Banerjee, K. A thermally-aware performance analysis of vertically integrated (3-D) processor-memory hierarchy. In Proceedings of the 43rd annual Design Automation Conference, San Francisco, CA, USA, 24–28 July 2016; pp. 991–996. [CrossRef]
12. Mizunuma, H.; Yang, C.L.; Lu, Y.C. Thermal modeling for 3D-ICs with integrated microchannel cooling. In Proceedings of the 2009 International Conference on Computer-Aided Design, San Jose, CA, USA, 2–5 November 2009; pp. 256–263. [CrossRef]
13. Koo, K.; Lee, S.; Kim, J. Vertical noise coupling on wideband low noise amplifier from on-chip switching-mode DC-DC converter in 3D-IC. In Proceedings of the IEEE Electromagnetic Compatibility of Integrated Circuits (EMC Compo), Dubrovnik, Croatia, 6–9 November 2011; pp. 35–40.
14. Sicard, E.; Jianfei, W.; Shen, R.; Li, E.P.; Liu, E.X.; Kim, J.; Cho, J.; Swaminathan, M. Recent Advances in Electromagnetic Compatibility of 3D-ICs-Part II. *IEEE Electromagn. Mag.* **2016**, *5*, 65–74. [CrossRef]
15. Sicard, E.; Jianfei, W.; Shen, R.J.; Li, E.P.; Liu, E.X.; Kim, J.; Cho, J.; Swaminathan, M. Recent advances in Electromagnetic Compatibility of 3D-ICs-Part I. *IEEE Electromagn. Mag.* **2015**, *4*, 79–89. [CrossRef]

16. Agrawal, A.; Huang, S.; Gao, G.; Wang, L.; DeLaCruz, J.; Mirkarimi, L. Thermal and Electrical Performance of Direct Bond Interconnect Technology for 2.5D and 3D Integrated Circuits. In Proceedings of the 2017 IEEE 67th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 30 May–2 June 2017; pp. 989–998. [CrossRef]
17. Chen, S.; Tzeng, P.; Hsin, Y.; Wang, C.; Chang, P.; Chen, J.; Chen, T.; Hsu, T.; Chang, H.; Zhan, C.; et al. Implementation of Memory Stacking on Logic Controller by Using 3DIC 300mm Backside TSV Process Integration. In Proceedings of the 2016 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, 25–27 April 2016; Volume 2, pp. 1–2. [CrossRef]
18. Zhang, C.; Thadesar, P.; Zia, M.; Sarvey, T.; Bakir, M.S. Au-NiW mechanically flexible interconnects (MFIs) and TSV integration for 3D interconnects. In Proceedings of the 2014 International 3D Systems Integration Conference (3DIC), Kinsdale, Ireland, 1–3 December 2014; pp. 1–4. [CrossRef]
19. Chen, J.C.; Chen, E.H.; Tzeng, P.J.; Lin, C.H.; Wang, C.C.; Chen, S.C.; Hsu, T.C.; Chen, C.C.; Hsin, Y.C.; Chang, P.C.; et al. Low-cost 3DIC process technologies for Wide-I/O memory cube. In Proceedings of the 2015 International Symposium on VLSI Technology, Systems and Applications, Hsinchu, Taiwan, 2–3 June 2015. [CrossRef]
20. Yang, C.C.; Hsieh, T.Y.; Huang, W.H.; Wang, H.H.; Shen, C.H.; Shieh, J.M. Sequentially stacked 3DIC technology using green nanosecond laser crystallization and laser spike annealing technologies. In Proceedings of the 2015 IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits, Hsinchu, Taiwan, 29 June–2 July 2015; pp. 389–391. [CrossRef]
21. Madhour, Y.; Zervas, M.; Schlottig, G.; Brunschwiler, T.; Leblebici, Y.; Thome, J.R.; Michel, B. Integration of intra chip stack fluidic cooling using thin-layer solder bonding. In Proceedings of the 2013 IEEE International 3D Systems Integration Conference (3DIC), San Francisco, CA, USA, 2–4 October 2013; pp. 1–8. [CrossRef]
22. Ki, W.M.; Kang, M.S.; Yoo, S.; Lee, C.W. Fabrication and bonding process of fine pitch Cu pillar bump on thin Si chip for 3D stacking IC. In Proceedings of the 2011 IEEE International 3D Systems Integration Conference (3DIC), Osaka, Japan, 31 January–2 February 2012; pp. 3–6. [CrossRef]
23. Kang, S.; Cho, S.; Yun, K.; Ji, S.; Bae, K.; Lee, W.; Kim, E.; Kim, J.; Cho, J.; Mun, H.; et al. TSV optimization for BEOL interconnection in logic process. In Proceedings of the 2011 IEEE International 3D Systems Integration Conference (3DIC), Saka, Japan, 31 January–2 February 2012. [CrossRef]
24. Ahmad, H.; Izadi, O.H.; Shinde, S.; Pommerenke, D.; Shumiya, H.; Maeshima, J.; Araki, K. A study on correlation between near-field EMI scan and ESD susceptibility of ICs. In Proceedings of the IEEE International Symposium on Electromagnetic Compatibility Signal/Power Integrity, Washington, DC, USA, 7–11 August 2017; pp. 169–174. [CrossRef]
25. Jin, S.; Cracraft, M.A.; Zhang, J.; DuBroff, R.E.; Slattery, K. Using near-field scanning to predict radiated fields. International Symposium on Electromagnetic Compatibility. In Proceedings of the 2004 International Symposium on Electromagnetic Compatibility (IEEE Cat. No.04CH37559), Silicon Valley, CA, USA, 9–13 August 2004; Volume 1, pp. 14–18. [CrossRef]
26. Yu, Z.; Koo, J.; Mix, J.A.; Slattery, K.; Fan, J. Extracting physical IC models using near-field scanning. In Proceedings of the IEEE International Symposium on Electromagnetic Compatibility, Fort Lauderdale, FL, USA, 25–30 July 2010; pp. 317–320. [CrossRef]
27. Slattery, K.P. A comparison of the near field and far field emissions of a Pentium (R) clock IC. In Proceedings of the IEEE EMC International Symposium. Symposium Record. International Symposium on Electromagnetic Compatibility, Montreal, QC, Canada, 13–17 August 2001; Volume 1, pp. 547–551. [CrossRef]
28. Xiaopeng, D.; Deng, S.; Hubing, T.; Beetner, D. Analysis of chip-level EMI using near-field magnetic scanning. In Proceedings of the International Symposium on Electromagnetic Compatibility, Silicon Valley, CA, USA, 9–13 August 2004; Volume 1, pp. 174–177. [CrossRef]
29. Stefanini, I.; Markovic, M.; Perriard, Y. 3D Inductance and Impedance Determination Taking Skin Effect into Account. In Proceedings of the IEEE International Conference on Electric Machines and Drives, San Antonio, TX, USA, 15 May 2005; Volume 2, pp. 74–79. [CrossRef]
30. Lau, J.H.; Yue, T.G. Thermal management of 3D IC integration with TSV (through silicon via). In Proceedings of the 2009 59th Electronic Components and Technology Conference, San Diego, CA, USA, 26–29 May 2009; pp. 635–640.

31. Patrick, L.; de Crecy, F.; Fayolle, M.; Charlet, B.; Enot, T.; Zussy, M.; Jones, B.; Barbe, J.C.; Kernevez, N.; Sillon, N.; et al. Challenges for 3D IC integration: Bonding quality and thermal management. In Proceedings of the 2007 IEEE International Interconnect Technology Conferencee, Burlingame, CA, USA, 4–6 June 2007; pp. 210–212.
32. Kiran, P.; Loh, G.H. Thermal analysis of a 3D die-stacked high-performance microprocessor. In Proceedings of the 16th ACM Great Lakes Symposium on VLSI, Providence, RI, USA, 16–18 May 2010; pp. 19–24.
33. Lau John, H.; Yue, T.G. Effects of TSVs (through-silicon vias) on thermal performances of 3D IC integration system-in-package (SiP). *Microelectron. Reliab.* **2012**, *52*, 2660–2669.
34. Sangwan, V.; Kapoor, D.; Tan, C.M.; Lin, C.H.; Chiu, H.C. High Frequency Electromagnetic Simulation and Optimization for GaN-HEMT Power Amplifier IC. *IEEE Trans. Electromagn. Compat.* **2018**, *61*, 564–571. [CrossRef]
35. Ansys Inc. *Ansys HFSS Technical Notes*; ANSYS: Canonsburg, PA, USA, 2017.
36. Ott, H.W. *Electromagnetic Compatibility Engineering*; John Wiley Sons: Hoboken, NJ, USA, 2009.