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Scalable Implementation of Hippocampal Network on Digital Neuromorphic System towards Brain-Inspired Intelligence

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Abstract: In this paper, an expanded digital hippocampal spurt neural network (HSNN) is innovatively proposed to simulate the mammalian cognitive system and to perform the neuroregulatory dynamics that play a critical role in the cognitive processes of the brain, such as memory and learning. The real-time computation of a large-scale peak neural network can be realized by the scalable on-chip network and parallel topology. By exploring the latest research in the field of neurons and comparing with the results of this paper, it can be found that the implementation of the hippocampal neuron model using the coordinate rotation numerical calculation algorithm can significantly reduce the cost of hardware resources. In addition, the rational use of on-chip network technology can further improve the performance of the system, and even significantly improve the network scalability on a single field programmable gate array chip. The neuromodulation dynamics are considered in the proposed system, which can replicate more relevant biological dynamics. Based on the analysis of biological theory and the theory of hardware integration, it is shown that the innovative system proposed in this paper can reproduce the biological characteristics of the hippocampal network and may be applied to brain-inspired intelligent subjects. The study in this paper will have an unexpected effect on the future research of digital neuromorphic design of spike neural network and the dynamics of the hippocampal network.

Keywords: brain-inspired intelligence; hippocampal network; dynamical oscillation; neuromorphic engineering

1. Introduction

Over the last few decades, numerous studies have accumulated a great deal of knowledge about brain function, but our understanding of brain mechanisms and functional dynamics remains limited [1,2]. Spiking neural networks (SNNs) have been increasingly popular in recent years due to their relationship to dynamics in human brain and enhanced biological relevance [3]. The SNNs with cognitive and motor functions, such as the hippocampal network, have been investigated with abundant in vitro and model-based experiments [4,5]. One of the most essential components of the human brain is the hippocampus, which processes short-term memory and spatial navigation information [6–9]. It can be biologically demonstrated that behavioral learning and memory in mammals are closely related to its hippocampal rhythm [10,11]. In addition, there is ample evidence that abnormal hippocampal rhythms in animals induce psychological dysfunction of the nervous system. One of the most representational examples is that abnormal electrical activity in the hippocampal neural network can cause cognitive decline and behavioral inhibition in Alzheimer's patients [12–15]. Previous experiments have shown

that hippocampal oscillations play an irreplaceable role both in the encoding and transmission of information [16]. The dynamics of neuromodulation can affect sensory processing and information processing in cognitive function [17,18]. Most of the current spiking neural network models for machine learning application use the feedforward network architecture for the sake of object classification. However, the human brain does not execute the classification task most of the time. Besides, many critical brain areas for learning do not use a feedforward architecture. On the basis of these observations, we were inspired to present a novel model with recurrent network architecture for the neuromodulatory dynamics, which are critical in the cognitive and learning process in human brain.

Although the hippocampal neural network has been investigated for a long time and applied in various fields widely, its computational process has some constraint. CPU characteristics lead to low clock rates and low memory bandwidth on traditional platforms. A high-performance computing platform in neuromorphic engineering is urgently needed. Various kinds of hardware designs have endeavored to realize the real-time computation of the human brain system in recent years. The analog neuromorphic system based on the very large scale integration (VLSI) can be more realistic and power efficient [19–21], but it has not been popularized due to its excessive resource consumption and long development time. The field programmable gate array (FPGA) has the characteristics of parallel computation, reconfigurable architecture, and distributed structure in a digital neuromorphic system [22,23]. Previous studies have focused on using FPGAs to improve the performance of neuromorphic platforms, which present different realization methods with various applications [24–27]. However, although this is important for information encoding and signal processing in the brain's cognitive system, few previous studies have considered the dynamic oscillations of the hippocampal neural network. In addition, how to effectively implement large-scale hippocampal networks with coupled synapses with random connections is a difficult challenge. Due to the shortcomings of on-chip network (NoC) technology [28], the digital implementation of the seahorse network we proposed earlier is limited in scalability and system performance [29].

Since the introduction of microchip technology, great progress has been made in its development, and large-scale on-chip system technology has been applied in more and more fields. As the architectures of the system-on-chip platform become more complex, NoC techniques are investigated and used to solve the problems of data transmission, large-scale computation, and complicated network topology [30]. The NoC structure can improve the utilization of the hardware resource and transmission rate of the data flow, which can make the topology architecture flexible and improve the system scalability. In this study, we proposed a novel NoC technique to complete the realization of a scalable digital neural morphology of the hippocampal neural network and focus on the neuromodulation oscillation dynamics of the hippocampus. In particular, the proposed FPGA-based hippocampal neural network can track biodynamics in real time under normal and even neuroregulatory conditions.

The general structure of this article is as follows. Section 2 describes the construction principle of the hippocampal neural network model, and the digital implementation of the presented hippocampal network model is described in detail in Section 3. The experimental results and the biological feasibility of the network are demonstrated in Section 4.

2. The Hippocampal Neural Network Model

As shown in Figure 1, hippocampal neural coding is closely related to peridergic pyramidal neurons and inhibitory neurons, and the hippocampal neural network can contain both important types of neurons. Pyramidal neurons are asymmetrical in the narrow region between the dendrites and the cell body, whereas the structures of the genus rabbit on both sides of the cell body of the intermediate neuron are symmetrical. As a result, the two types of neurons have different effects in the electrical field outside the cell. Besides, the network is coupled with various synaptic connections due to the relatively local dense connectivity.



Figure 1. The overall structure of hippocampus and the hippocampal network in the CA3 region. The hippocampal network consists of pyramidal excitatory neurons and inhibitory neurons. These two types of neurons are coupled to each other through excitatory and inhibitory synapses with a variety of synaptic strengths.

In this paper, Ne = 48,000 excitatory neurons and Ni = 16,000 inhibitory neurons were used to form a hippocampal network model, and the synapses between these neurons were connected with a sparsity of 20%. When neuron *i* peaks, the synaptic current of neuron *j* is weighted by the presynaptic pulse s(i, t), which is weighted by the corresponding synaptic current w(j, i). This current generation process can be regarded as the integral process of all synaptic current to the *j*th neuron, which can be defined by the following mathematical equation:

$$\partial I_S(j) / \partial t = \left(-I_S(j) + \sum_i g_{syn} w(j,i) s(i,t) \right) / \tau_S(j)$$
(1)

In the above formula, s(i, t) is used to indicate presynaptic impulse, and w(j, t) is used to describe synaptic strength. For different connections between excitatory neurons and inhibitory neurons, the parameter range of synaptic strength is different: the synaptic strength w is uniformly distributed with $w_{ee} \in [0, 0.65]$ for: excitatory-to-excitatory synapses, $w_{ei} \in [0, 2]$ for excitatory-to-inhibitory synapses, $w_{ie} \in [-1.7, -0.8]$ for inhibitory-to-excitatory synapses, and $w_{ii} \in [-1.1, -0.3]$ for inhibitory-to-inhibitory synapses. τ_s is a constant describing the synapse time constant. For excitatory neurons, $\tau_s = 0.5$ ms, and for inhibitory neurons, $\tau_s = 6$ ms. The effective gain g_{syn} , which stands for the amplitude response of the synaptic current neurons, is 8.7 ± 4.8 Hz and 21.1 ± 1.4 Hz for inhibitory neurons [31]. The firing rate of the excitatory field *E* will affect the nerve polarization of cone excitatory neurons, and *E* is proportional to the applied electric field, which can be described by the following mathematical equation:

$$\partial I_E / \partial t = (-I_E + S_E E(t)) / \tau_E \tag{2}$$

The S_E in the above formula is a description of the sensitivity of the membrane to the field determined by the cell geometry and field orientation. It should be noted that the parameter τ_E in the formula is a constant value and will not change with the iteration process. At the same time, the total input current *I* of the *j*th neuron is proposed, which is expressed as follows:

$$I(j) = \begin{cases} I_S(j) + I_E + I_{car}, & \text{for } j\text{th excitatory neuron} \\ I_S(j), & \text{for } j\text{th inhibitory neuron} \end{cases}$$
(3)

In this paper, in order to describe the impact caused by carbachol, *I_{car}* uses a Gaussian white noise current with an average value of 0. The advantage of this choice is that the operation of the endogenous hippocampal neural network can be demonstrated by applying a weak electric field.

Through the past research on neural network models, it can be found that using excitatory neurons and inhibitory neurons to build a hippocampal neural network model can achieve very good simulation results. Using phenomenological Izhikevich neuron [32] modeling, the differential equation of neuronal membrane potential V(t) is as follows:

$$V(t+1) = \begin{cases} aV^{2}(t) + (b+1)V(t) + c - U(t) + I(t), & \text{for } V(t) \le \theta, \\ V_{0}, & \text{otherwise,} \end{cases}$$
(4)

During the calculation iteration, the unit time step is selected to be 0.77 ms. The driving current I(t) is an input stimulation, and θ is the threshold value. The recovery variable U(t) can be expressed by the following equation:

$$U(t+1) = \begin{cases} U(t) + [k_U V(t) - U(t)] / \tau_U, & \text{for } V(t) < \theta, \\ U(t) + \Delta U & \text{otherwise,} \end{cases}$$
(5)

where k_U is the slope of the variation in V(t), and τ_U describes the relaxation time. The recovery of the ΔU represents variables U(t) reset after the peak. The recovery of neuronal membrane potential and the discharge rate of excitatory and inhibitory neurons in hippocampus are affected by V_0 , ΔU , τ_U , and k_U when carbachol-induced gamma oscillation emerges. Heterogeneity within the neural network is considered by using a normally distributed expression. Table 1 shows the corresponding parameter values. Based on these values, the network dynamics can be consistent with electrical biological experimental results.

	Excitatory Neuron	Inhibitory Neuron
а	0.04	0.04
Ь	5	5
С	140	140
$ au_u$	43 ± 4.3	100 ± 0
k _u	0.24 ± 0.02	0.25 ± 0
V_0	-65 ± 6.5	-65 ± 0
$\Delta \tilde{U}$	10 ± 1	1 ± 0

Table 1. Parameter values of the neuron models.

3. Digital Implementation

The proposed system uses a high-end Intel Stratix III FPGA to implement a digital neuromorphic system that can simulate large-scale hippocampal neural networks. On the FPGA chip, the hippocampal neural network is realized using the torus architecture. The enhancement of the system throughput depends on pipeline technology.

3.1. Network-On-Chip (NoC) Architecture

The digital structure of the proposed hippocampal neural network is based on the NoC architecture that can enable a scalable and cost-efficient digital neuromorphic system. It is so indispensable that it determines the hardware performance of the proposed system. In the proposed study, the torus structure is used because it can avoid the node closure on the edge of toroidal topology; thus, the system can show better performance. Figure 2 shows the detailed implementation of the proposed

NoC-based SNN. The top-level NoC structure is shown in Figure 2a, which contains 64 nucleus processors (NPs). Address event routing (AER) is essential to data communication between NPs determined by routers. The specific structure is shown in Figure 2b: Each NP contains a neuron unit, a router, a silicon synapse unit, and a configuration unit. The routers can transmit the data flow via the east, south, west, or north ports. The configuration unit is used to configure the routers, which determines the data transmission within an NP. The neuron unit is used to compute the hippocampal neurons, and the synaptic current is calculated in the silicon synapse unit. In the router module, the data flow is determined by hippocampal information processing (HIP) scheduling as shown in Figure 2c.





Figure 2. Digital implementation of the proposed hippocampal neural network. (a) Digital implementation of the network-on-chip (NoC) architecture; (b) Digital implementation of the nucleus processor (NP); (c) Digital implementation of the router.

The NoC structure proposed in this paper uses a torus topology and requires a router with a dedicated routing algorithm to carry out correct data transmission, which is quite different from the conventional network structure. In the case of inter-chip data communication, the router receives external events from four adjacent NPs and sends data streams based on programmed routing rules from the configuration unit. The Algorithm 1 shows the routing algorithm of the proposed system. The AER spike information will be firstly routed along the X direction. After it reaches the location along the X direction checked by the embedded router, the information will be then routed along

the Y direction to the destination node according to the routing table. A judgement is executed during the following routing algorithm to determine the routing direction for the shorter routing path planning. The AER data in the packet transmitted through the router is synaptic information rather than peak information, which is different from the traditional AER-based implementation of SNN.

loop
if posedge <i>clk</i> then
$\Delta x1=XC-1; \Delta x2=WN-XC;$
//WN: Width of the NoC, XC: xcurrent
$\Delta y1=YC-1; \Delta y2=HN-YC;$
// HN: Height of the NoC, YC: ycurrent
$\Delta xsign <-((xdest-XC) > 0)?0:1$
$\Delta ysign <- ((ydest-YC) > 0)?0:1$
if $\Delta xsign = 0$ then $\Delta x <-$ (xdest-XC); $\Delta xreverse <-$ (WN -xdest) + XC;
if $\Delta x \leq \Delta x$ reverse then Route the packet EAST;
else Route the packet WEST; end if
else { $\Delta xsign != 0$ }; $\Delta x <- (XC-xdest)$; $\Delta xreverse <- (WN - XC) + xdest$;
if $\Delta x \leq \Delta x$ reverse then Route the packet WEST;
else Route the packet EAST; end if
end if
if $\Delta ysign = 0$ then $\Delta y <-$ (ydest-YC); $\Delta yreverse <-$ (HN -ydest) + YC;
if $\Delta y \leq \Delta y$ reverse then Route the packet SOUTH;
else Route the packet NORTH; end if
else { $\Delta ysign != 0$ }; $\Delta y <- (YC-ydest)$; / $\Delta yreverse <- (HN - YC) + ydest$;
if $\Delta y \leq \Delta y$ reverse then Route the packet NORTH;
else Route the packet SOUTH; end if
end if
if XC=1 or XC=WN or YC=1 or YC= HN
then Route the packet UP;
// The situation that the current node is the edge node
elseif $\Delta xl \ge \Delta x2$ then Route the packet West;
else Route the packet East; end if
end if
end loop

3.2. CORDIC-Based Neuron Design

In order to solve the prior function, the coordinate rotation digital computer (CORDIC) algorithm is used in this paper to complete the conversion between rectangular coordinates and polar coordinates. The CORDIC algorithm can use the addition, shift, and look-up table operations to calculate basic transcendental functions, which are complicated for the hardware computation, including sin θ , cos θ , sinh θ , cosh θ , e^{θ} , ln θ . The major method of the CORDIC algorithm is to rotate series of angles which are related to the specific values for the approximation of the target angle, which is based on multi-iteration operations. It is worth noting that the results can become more accurate as the number of iterations increases. All the computations are based on addition and shift operation of the specific computing results. The unified CORDIC algorithm employs a parameter of the plane coordinate system m to integrate the linear rotation, circle rotation, and hyperbolic rotation in a CORDIC function set, the related equation set can be written as follows:

$$\begin{cases} X_{i+1} = X_i - m\xi_i Y_i \cdot 2^{-i} \\ Y_{i+1} = Y_i + \xi_i X_i \cdot 2^{-i} \\ Z_{i+1} = Z_i - \xi_i \cdot \theta_i \end{cases}$$
(6)

In the function set, X_i and Y_i are the result values of the *i*th iteration. Z_i is the angle value of the *i*th iteration. The number of iterations can be expressed as parameter *i*, and ξ_i is the judgment operator. If $\xi_i > 0$, then rotate counterclockwise, and if $\xi_i < 0$, then rotate in the opposite direction, that is, clockwise. This parameter has a specific angle used to represent the *i*th rotation, where m refers to the parameter of the coordinate system. The parameter m can be equal to -1, 0, 1, and different values of m correspond to different nonlinear functions. If m = -1, the function set can be used to represent sinh θ and $\cosh \theta$. If m = 0, the function set can be used to calculate multiplication and division. In addition, if m = 1, the function set can compute sin θ and $\cos \theta$. Besides, different initial values can result in different computing results. If $X_0 = A + 1/4$, $Y_0 = A - 1/4$, and m = -1, the function set can be used to solve $0.5 \ln A$.

In the research model in this paper, the Izhikevich model is mainly used in the neuron model, and the electrical synapse model is used to build the synapses. The CORDIC algorithm is used to realize the functions of multiplication, division, and exponential operations. In terms of the multiplication operation using the CORDIC algorithm, the parameters are set as m = 0, $X_0 = A$, $Y_0 = B$, and $Z_0 = 0$, and the function of $Z = A \times B$ can be calculated as:

$$\begin{cases} X_{i+1} = X_i \\ Y_{i+1} = Y_i - \xi_i X_i \cdot 2^{10-i} \\ Z_{i+1} = Z_i + \xi_i \cdot \theta_i \end{cases}$$
(7)

where $\theta_i = 2^{10-i} \times X_i$, $\xi = 1$ if $Y_i > 0$, otherwise $\xi_i = 0$. In terms of division operation, the parameters m = 0, $X_0 = B$, $Y_0 = A$, $Z_0 = 0$ and the function Z = A/B can be computed as follows:

$$\begin{cases} X_{i+1} = X_i \\ Y_{i+1} = Y_i - \xi_i X_i \cdot 2^{10-i} \\ Z_{i+1} = Z_i + \xi_i \cdot \theta_i \end{cases}$$
(8)

where $\theta_i = 2^{10-i}$, and other parameters are the same as those in the case of multiplication. The e^{θ} can be calculated by the following formula set:

$$\begin{cases} X_{i+1} = X_i + \xi_i Y_i \cdot 2^{-i} \\ Y_{i+1} = Y_i + \xi_i X_i \cdot 2^{-i} \\ Z_{i+1} = Z_i - \xi_i \cdot \theta_i \end{cases}$$
(9)

where $\theta_i = \tanh^{-1}(2^{-i})$, and it can be calculated in the range from -1.11817 to 1.11817, which is smaller than the required range. Therefore, the data can be converted through the following equation:

$$\theta = Q\ln 2 + \gamma \tag{10}$$

where $Q \in Z$, $|\gamma| \le \ln 2 = 0.6931$ and $e^{\theta} = e^{Q \ln 2 + \gamma} = 2^Q e^{\gamma}$. In this method, the range of e^{θ} can be expanded as the iteration number increases to meet the required precision.

3.3. Neuron Implementation

In this study, the Izhikevich neuron model is used to realize the neural network. The digital implementation is shown in Figure 3. In Figure 3a, the blocks "Reg" and "ADD" represent the register and adder, and "SUB" stands for the subtractor. The block "MUL" represents the multiplier which is realized based on the CORDIC algorithm in this study. For the concrete implementation of an iteration of the CORDIC algorithm refer to Figure 3b, where "MUX" is the multiplexer. The input X_i , Y_i , Z_i are the input values of the iteration, and X_{i+1} , Y_{i+1} , Z_{i+1} are the updated results of the *i* + 1 iteration. The variable is the iteration parameter of the iteration, and the specific values are based on the functions that the CORDIC algorithm implements. The CORDIC algorithms with different iterations can meet different precision requirements. The CORDIC algorithm can achieve more precision by increasing the iteration number. In this study, the CORDIC algorithm uses 21 steps of iteration.



Figure 3. Digital implementation of the single neuron. (**a**) Digital implementation of the Izhikevich model; (**b**) Digital implementation of the coordinate rotation digital computer (CORDIC) algorithm.

4. Experimental Results

In order to simulate the function of a feedforward network on hardware FPGA, this paper implements an extensible neural network based on the improved butterfly fat tree (IBFT) architecture. Stratix III EP3SE260 FPGA can effectively implement the proposed neural network. In total, 64 NPs are implemented with the time division multiplexing technique for a single NP. Each NP is responsible for 1000 virtual neurons. The hardware resource cost is shown in Table 1. Traditionally, the use of lookup tables to compute multiplication solves this problem, but this method is expensive and backward in terms of memory resources and digital signal processing (DSP) resources. It can be clearly found from Table 2 that the hardware resource cost of only 18 bits of DSP block using the traditional method exceeds all available hardware resources. In contrast, the proposed implementation method

can effectively reduce hardware resource costs in terms of the DSP and memory resources which are extravagant elements on FPGA hardware. The proposed digital neuromorphic system operates at a working frequency of 146.03 MHz.

Table 2. The hardware resource consumption when conventional and CORDIC-based implementation methods are used respectively to implement the hippocampal neural network.

Resources	Conventional	CORDIC-Based
Combinational ALUTs	19,652/203,520 (10%)	10,642/203,520 (5%)
Memory ALUTs	490/101,760 (<1%)	712/101,760 (1%)
Dedicated logic registers	8924/203,520 (4%)	11,546/203,520 (6%)
Total block memory bits	7,771,246/15,040,512 (52%)	2106/15,040,512 (<1%)
DSP block 18-bit elements	2384/768 (310%)	0/768 (0%)
Total PLLs	1/8 (13%)	1/8 (13%)

The design and programming of the proposed digital neural morphological network is realized by using the VHDL modeling language. On the premise of using ALTERA Quartus II to synthesize HDL code, a Stratix III FPGA development board with 60 nm can be successfully developed. The oscilloscope photograph of the membrane potential of the neurons in the hippocampal neural network is shown in Figure 4. This indicates that the proposed neuromorphic hippocampal neural network can accurately track the biodynamics in real time.



Figure 4. Biological behaviors of the hippocampal neural network implemented on Stratix III field programmable gate array (FPGA), which are observed on the oscilloscope device. The voltage scale is 50 mV. (a) The output of the 1st excitatory neuron in the digital neuromorphic network (time scale is 20 μ s); (b) The output of the 48,000th excitatory neuron in the digital neuromorphic network (time scale is 20 μ s); (c) The output of the 1st inhibitory neuron in the digital neuromorphic network (time scale is 20 μ s); (d) The output of the 16,000th inhibitory neuron in the digital neuromorphic network (time scale is 20 μ s).

The relationship of the computational precision, the iteration number and the CORDIC module number is shown in Figure 5a. The computational precision is defined by relative error between the CORDIC-based results and the desired results. It shows that the precision increases with increasing iteration number. The calculation accuracy will decrease as the number of CORDIC modules increases. Figure 5b reveals the relationship between the number of CORDIC modules and different kinds of the hardware resource cost. The CORDIC module can significantly reduce the hardware resource cost of the DSP block 18-bit elements and total storage bits. Considering both Figure 5a,b, it means that the CORDIC module in the proposed hardware implementation can save hardware resources while maintaining high level of computational precision.



Figure 5. Performance analysis of the proposed CORDIC module. (a) The relationship of the computational precision, the iteration number, and the number of the CORDIC modules; (b) The relationship between the number of CORDIC modules and the hardware resource cost.

In our study, we use frequency domain analysis to reveal how many signals are in a given frequency band within a given frequency range. According to the previous research results, the wavelet transform can effectively complete digital image processing and signal compression. As shown in Figure 6a,b, modulation of extracellular oscillations with negative and positive DC stimuli resulted in suppression and promotion of mean emissivity, respectively. During symmetrical modulation of low-frequency AC stimulation, the average activation rate of the hippocampal neural network increased, and the frequency of low-frequency AC stimulation was less than half (about 12 Hz) of the endogenous magnetic field frequency. In practice, symmetric modulation means that the effect of suppression is roughly the same as the effect of enhancement under stimulation of a low-frequency ac field. The suppressive neurons due to the effect of the negative cycles can fire during the positive cycles of the AC stimulation, which induces a stable network firing rate. Synchrony occurs during the emergency of subharmonic as shown in Figure 6c,d.



Figure 6. The wavelet transform of the frequency-domain analysis. (**a**) The oscillation dynamics under the modulation of negative direct current; (**b**) The oscillation dynamics under the modulation of positive direct current; (**c**) The oscillation dynamics under the modulation of low-frequency AC stimulation; (**d**) The oscillation dynamics under the modulation of high-frequency AC stimulation.

Previously we have presented several works for brain-inspired neuromorphic computing. In order to clarify the unique contribution in this study, a comparison with analysis is presented as illustrated in Table 3. These works have been inspired by different areas of the brain, which includes visual pathway, hippocampus, CPG (central pattern generator), Purkinje, and retina. Although [33] shares the same brain area with the presented study, different network structures with different aims are pursued. Study [33] uses the feedforward network structure for the implementation of the memory-related behaviors. This study presents a unique contribution for the realization of the neuromodulatory dynamics. In addition, this study presents a torus-based NoC design for hardware architecture, which presents another significant contribution in comparison with the previous studies. A previous study has revealed the advantage and necessity of the NoC design [28]. The presented study is the improved version in comparison with our previous studies [34,35]. The previous studies [34,35] use a bus-based NoC architecture. This work proposes a torus-based solution, which can further improve the NoC performance of the hippocampal network on FPGA, which is the major innovation and difference in comparison with our previous work. The weakness of the presented digital neuromorphic model is that it can only reproduce parts of the critical dynamics of the biological hippocampus. It cannot reproduce all the dynamics of the hippocampus region such as navigation, which should be further explored in a future study.

Work	Motivation	Network Structure	Hardware Architecture
[27]	Visual pathway-inspired	Feedforward	No NoC design
[34]	Hippocampus-inspired	Feedforward	No NoC design
[36]	CPG-inspired	CPG	No NoC design
[37]	Purkinje-inspired	Recurrent	No NoC design
[38]	Retina-inspired	Feedforward	No NoC design
This study	Hippocampus-inspired	Recurrent	Torus-based NoC design

Table 3. Comparison of the presented study with previous works.

5. Conclusions

In this paper, a FPGA-based scalable hardware design for hippocampal neural network is presented, and the simulation is carried out under the constraints of biological characteristics. In addition, it is of great significance to study neural information processing and neurological diseases, since the biological dynamics of reappearing neuroregulatory oscillations are realized based on the proposed digital neuromorphic system. Since the NoC techniques are used in the proposed system, which makes the proposed system more scalable than the previous studies of the digital realization of the hippocampal network. In addition, it has been proved that the application of the CORDIC algorithm in large-scale neural networks can improve the system performance. The proposed work could be used in a variety of applications, such as simulation platforms for neural network dynamics, brain-inspired intelligence, neural prostheses in brain-machine interfaces, and control circuits for neural robots. Due to the neuromodulatory dynamics of the presented neuromorphic hippocampus, the most two significant future directions are the studies for the realization of the adaptive bi-directional brain-machine interface and the compact neuroprosthetics to replace the impaired counterpart in human brain. The brain-machine interface can induce a novel kind of mixed intelligence, which is an enhanced version of artificial intelligence. In addition, due to rhythmic dynamics of the proposed digital neuromorphic hippocampus, it can be applied in the interaction between human brain and the external environment to form a human-machine-environment integration system [39]. Besides, it can also be used as a neuro-controller for intelligent robots because of the rhythmic outputs of the neuromorphic network induced by the period input signals.

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