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Optimal Design Analysis with Simulation and Experimental Performance Investigation of High-Power Density Telecom PFC Converters

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Abstract: The spread of the 5G technology in the telecom power applications increased the need to supply high power density with higher efficiency and higher power factor. Thus, in this paper, the performance of the different power factor correction (PFC) topologies implemented to work with high power density telecom power applications are investigated. Two topologies, namely the conventional and the bridge interleaved continues-current-conduction mode (CCM) PFC boost converters are designed. Selection methodology of the switching elements, the manufacturing of the boost inductors, and the optimal design for the voltage and current control circuits based on the proposed small signal stability modeling are presented. The printed circuit board (PCB) for the two different PFC topologies with a power rating of 2 kW were designed. PSIM simulation and the experiments are used to show the supply current total harmonic distortions (THD), voltage ripples, power efficiency, and the power factor for the different topologies with different loading conditions.

Keywords: telecom power supply; power factor correction (PFC); small signal stability; conventional CCM PFC; interleaved CCM PFC; total harmonic distortion (THD); UCC28180 and UCC28070 IC controllers

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1. Introduction

Many of the industrial applications including telecom power applications currently used active-controlled AC/DC converters to offer efficient power supplies with high-power density. Most of the active-controlled AC/DC converters are designed based on the boost converter technique, optimal design, and controlling of the operation of the boost converter at high power density offers high input power factor (PF), reducing total harmonic distortion (THD) and the circuit power losses, and increasing the conversion efficiency [1,2]. The AC/DC power supply with two stages, as illustrated in Figure 1, is the optimal configuration to obtain high values for the input PF and power efficiency. Two-stage active AC/DC telecom power supply consists of the PFC (power factor correction) to regulate the input power factor and the DC/DC converter stage, which is used to regulate the bus voltage of the PFC stage (320–410 V) to the telecom power applications voltage level (45–63 V) [3,4].

The front stage of the telecom AC-DC power supply is the PFC stage which implements to deliver the power conversion with lower reactive power consumption, lower total harmonic distortion (THD), and, then, input supply power with a high-power factor (PF).

According to the power applications, many types of PFC converters are widely used, such as the conventional [5–7], the interleaved [8–11], and bridgeless [12–14] PFC boost converters. The conventional PFC topology as shown in Figure 2a is the basic topology as most the other PFC converters are derived from this topology. Moreover, for most of the power applications, this circuit topology is the most commonly used circuit because of its good performance, low cost, simple operations, and lower requirements for the power and

control circuit designs, but the electromagnetic interface (EMI) level of the conventional CCM (continues-current-conduction mode) PFC is high due to the high ripple current in the input side [1,15].

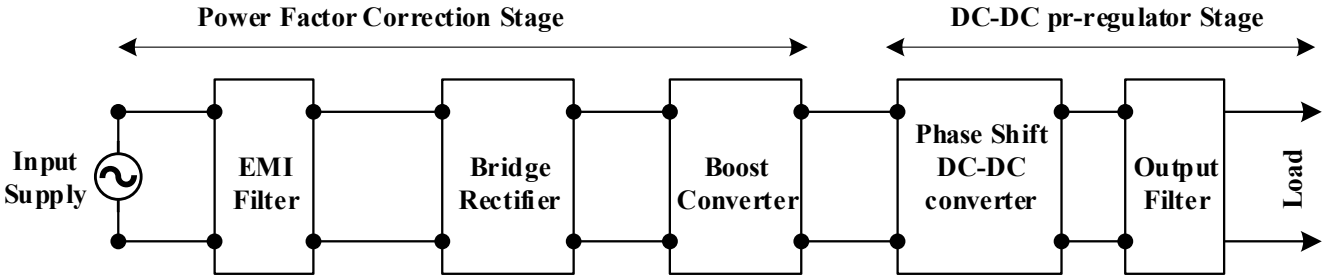


Figure 1. Construction of the industrial high-power density telecom power supply.

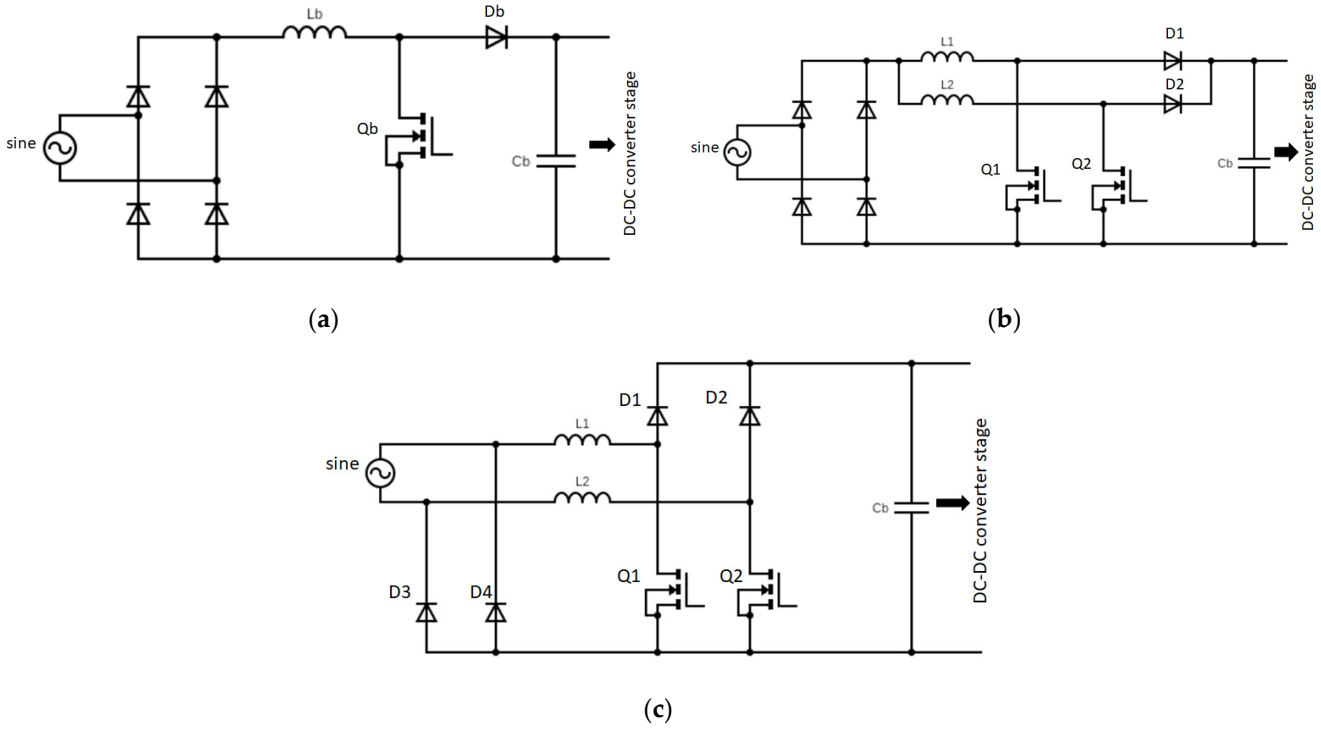


Figure 2. Schematic circuits of the different telecom PFC (power factor correction) topologies: (**a**) conventional topology; (**b**) interleaved topology; (**c**) bridgeless topology.

Another technique to implement the PFC converters can be classified as interleaved PFC boost converters as shown in the schematic circuit in Figure 2b. Interleaving means channeling the power flow from the input to the output into two or more channels and add them at the output point. By doing this, the problem of the input ripple current can be solved, also, as the number of interleaved channels increased, the power rating will be increased. Another advantage of this approach is better thermal performance as it uses two inductors which are approximately half the size of the conventional topology. The use of two inductors with a small current rating reduces the total size and total weight of the boost inductor, furthermore, it can increase the thermal performance of the converter.

Recently, different emerging techniques to improve the performance of the interleaved PFC converters are employed such as; the modification on the interleaved PFC circuit by connecting series capacitor to reduce the switching losses, reduced the voltage stress across the semiconductors as compared with the traditional interleaved boost converter [16], also, the proposed technology to minimize the input current ripple of the interleaved PFC converter by controlling the switching driving signals and without any change in the

converter model parameter, which is presented in [17]. The digitally controlled double dual boost interleaved PFC converter with high voltage gain, small input current ripple as compared with traditional interleaved PFC converter, which is presented in [18].

The bridgeless PFC typologies as shown in Figure 2c has higher efficiency as compared with the other PFC topologies since the input bridge rectifier is not used. However, most of these bridgeless topologies experience a higher level of EMI [19]. Different modifications and types of bridgeless topologies with complex design and higher costs are implemented to decrease these EMI issues [19–22]. Therefore, the use of the bridgeless PFC topology is limited in the telecom power applications, where the EMI level requires to be at the lower limits. For this reason, and to optimize the economic design for the PFC converter, the bridgeless PFC topology was excluded from the analysis, and the comparison in this work and the design analysis of the conventional and the interleaved PFC topologies are, only, performed.

The control circuits of the PFC circuits which implemented based on the boost converter technique usually contains two control loops [23–25]: the outer voltage loop, which regulate the output voltage value as the specified load value, and the inner current loop to make the AC supply current follow the AC supply voltage and regulate the circuit PF to higher values. Usually, these control loops in analogy control circuits are implemented using proportional-integral (PI) controllers [26–28]. The parameters of the PI controllers implemented to work with the boost converters are usually optimized by deriving the converter operation equations and linearized the system with using the different linearization techniques. Practically, PFC control circuits can be implemented using integrated circuits (IC) control chips such as the conventional PFC control IC's (UCC28180, UCC29950), and interleaved PFC control IC's (UCC28070, UCC28065) from Texas Instruments (Dallas, Texas, USA) (, country) [29]. The adjustment of the voltage and current control loops in these control IC's is performed by deriving the linearized small signal modeling of the converter system and choosing the closed loop control system stability criteria which are specified by the control system crossover frequency and the damping ratio [15,24,30,31].

The target of this study was to study the optimal design, manufacturing of the conventional and interleaved PFC with the high-power density and verified the performance of both topologies using the simulation and the experimental implementation. The performance of both PFC topologies was investigated by optimizing the parameters of the boost converter voltage and current control loops based on obtaining the proposed small signal stability modeling for both topologies and using the proper stability criterion for the closed loop control loops. The main parts of the power and control circuits in the two topologies were designed for the enhancement of the circuit high power factor, good conversion efficiency, a specified level of the load voltage, and current ripple contents, and the lower values of the THD follows the telecom power applications load class in the standard EN61000-3-2 [32]. The gains of the current-voltage controllers in both topologies have been optimized to adjust the controller's crossover frequency and damping ratio.

PSIM simulations have been used to test the performance of the designed PFC converters with the designed components and optimized control loops. Furthermore, the design of the printed circuit board (PCB) for both topologies using the OrCAD(, city and country) capture and ALEGRO PCB (Cadence 17.4, California, USA) (version, city and country) design software to verify the experimental performance and to make the comparative analysis between the designed PFC converters performances with different loading conditions are performed.

The following sections in this paper are organized as follows: Section 2 outlines the PFC converters magnetic parts manufacturing and switching elements selection methodology. Section 3 proposed the small signal modeling and the design techniques of the control loops for the different topologies of the PFC converters. Section 4 provides the simulation procedure and results for the different PFC topologies employed. Section 5 shows the printed circuit board (PCB) design, provides the experimental verification, and

the comparative analysis of the performance for the different PFC topologies. Section 6 is the conclusion of the paper.

2. PFC Converters Power Components Design Analysis and Selection

As shown in the different PFC topologies depicted in Figure 2, the principle operation of the different PFC topologies is based on the boost converter operation. The three main power elements in such these converters to be designed are, (1) the storage energy element represented by the boost inductor (L_b), (2) selecting the switching parts represented by the high voltage Mosfet (Q_b) and the high current fast switching diode (D_b), and (3) the design of the output filter represented by the output bulk capacitor (C_b) connecting in parallel with the high voltage output side. The following subsections outline the design analysis of the boost converter's different power components for the conventional and the interleaved PFC boost converters topologies.

2.1. The Boost Inductor Design and Manufacturing

2.1.1. Conventional PFC Boost Inductor

There are many considerations to consider when selecting the PFC boost inductors, such as the inductance value, the direct current resistance (DCR), and the saturation current value. The first step to designing the required boost inductor is to calculate the required inductance value based on the required circuit ripple current which is usually calculated as the percentage (10–40%) of the maximum input current to the boost converter [33].

For the conventional CCM PFC, the boost inductor value can be expressed as given [5]:

$$L_b = \frac{1}{\%Ripple} \times \frac{V_{in\_min}^2}{\boldsymbol{\eta}\, P_o} \times \left(1 - \frac{\sqrt{2}\, V_{in\_min}}{V_o}\right) \frac{1}{F_{sw}} \quad (1)$$

where V_{in_min} is the minimum supply input voltage, %Ripple is the inductor ripple current percentage, $\boldsymbol{\eta}$ is the desired efficiency, P_o is the power rating, and F_{sw} is the converter switching frequency.

The circuit operation of the conventional PFC boost converter working in the continuous current conduction mode (CCM) can be represented by two operation modes. Figure 3 depicts the waveforms of the inductor voltage and currents for the boost converter at different operation modes, where V_L represents the inductor voltage, I_L represents the inductor current, D is the converter duty cycle, T_{on} is the on-switching time, T_{off} is the off-switching time, T_s is the switching time, V_{in} is the boost converter input voltage, V_o is the output voltage, and ΔI_{Lrpp} is the inductor ripple current peak to peak value.

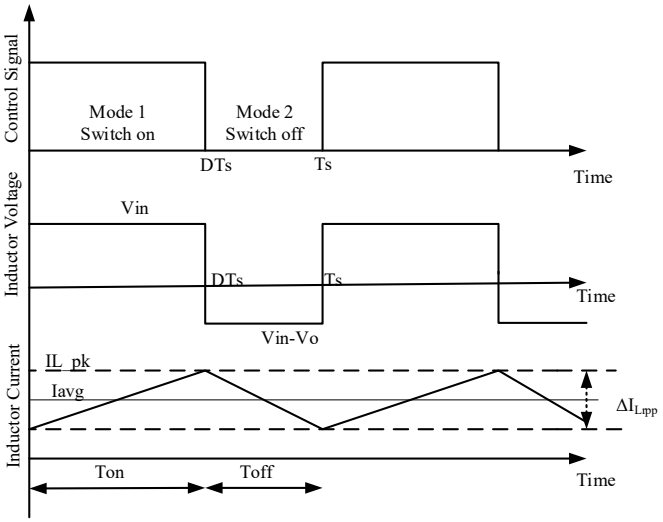


Figure 3. Boost inductor voltage and currents waveforms of the conventional PFC topology.

Mode-1, when the switch (Q_b) is closed, the energy is stored in the inductor, generating a magnetic field. Mode-2, when Q_b is opened, the current circuit impedance increases, thereby reducing the current, and the magnetic field previously created is reduced to let the current toward the load, thus, the inductor voltage polarity is reversed, which places the two sources in series, and charging the capacitor (C_b) through the fast switching diode (D_b).

The boost converter average input current is the same as the inductor average current (I_{avg}) which can be calculated at full load condition and rated output voltage as given

$$I_{avg} = \frac{P_{out}}{V_o}\left(\frac{1}{1-D}\right) \tag{2}$$

The boost converter is designed to work with supply voltage wide range (85–265) V. So, the maximum and the minimum duty cycle values are calculated as

$$D_{max} = 1 - \frac{V_{in\_min}}{V_o}\ ,\ D_{min} = 1 - \frac{V_{in\_max}}{V_o} \tag{3}$$

The average inductor currents at minimum and maximum supply voltage are calculated as

$$I_{avg\_min} = \frac{P_{out}}{V_o}\left(\frac{1}{1-D_{max}}\right)\ ,\ I_{avg\_max} = \frac{P_{out}}{V_o}\left(\frac{1}{1-D_{min}}\right) \tag{4}$$

The inductor ripple current as the percentage (%Ripple) of the converter total input current can be expressed as

$$\Delta ILrpp = \%Ripple \times I_{avg} \times 2 \tag{5}$$

From (4) and (5), and from the waveforms in Figure 3, the inductor maximum peak current is calculated as

$$I_{L\_pk} = I_{avg} + \frac{\Delta ILrpp}{2} \tag{6}$$

Using the converter parameters given in Table 1, the required inductance, and the inductor maximum peak current for the conventional CCM PFC converter can be calculated. Based on the calculated inductance and the inductor current, the inductor core, the number of turns (N), and the size of the winding wire have to be selected.

Table 1. The target PFC converters stage design specifications.

Design Parameter	Value	Unit
Supply voltage (V_{in})	220 (85–265)	V
Supply Frequency (F)	60 (47–63)	Hz
Output Voltage (V_o)	400 (320–410)	V
Output Power (P_o)	2000	W
Efficiency (η)	95%	-
Switching Frequency (F_{sw})	100	kHz
Hold Up Time (t_{hold})	10	ms
Inductor ripple (%Ripple)	20%	
voltage ripple (V_{rpp})	20	V_{pp}
Current ripple	5%	

The PFC inductor core was designed to have a high saturation level which prevents the saturation at the maximum peak current (I_{L_pk}), support the converter operation with the designed switching frequency, also, the inductor core losses have to be accepted in accordance with the temperature rise during the PFC converter operation. Kool Mu core material's with low loss, relatively high saturation level (10,500 gausses), higher switching frequency level up to 200 kHz, and the near-zero magnetostriction (ability to expand or contract in response to a magnetic field) make the Kool Mμ material good for eliminating

audible frequency noise in in-line noise filters and inductors, which also make it excellent for the implementation of the PFC circuits [34].

Choosing the inductor core in this work will be conducted by using the LI^2 method to choose the core part number from the Kool Mu chart of the Magnetic inc supplier, as shown in Figure 4, where L is the inductance value and I is the inductor average current. [34,35].

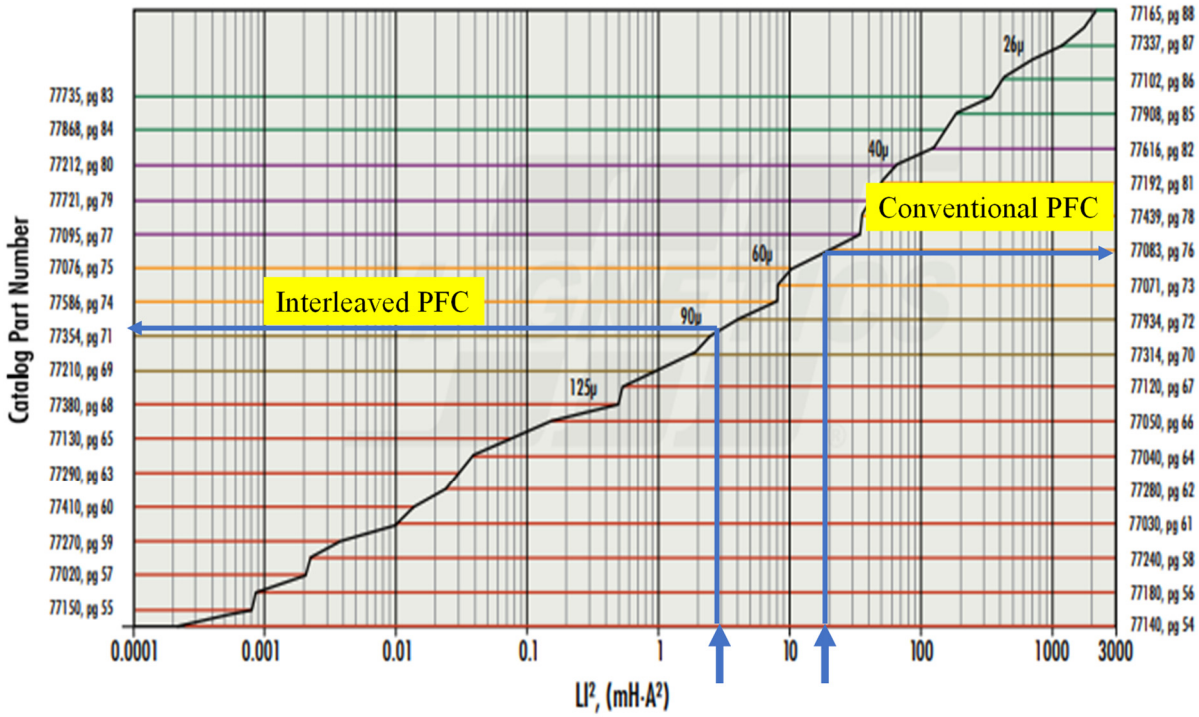


Figure 4. Boost inductor core selection for the conventional and the interleaved PFC topologies.

From the chart and with using the calculated value of the LI^2, and take in account offering the required value of the inductance with the suitable space for the wire winding around the core, the conventional PFC converter inductor is designed with using two stacked Kool Mu Toroids core with part number of 77083A7. The inductor number of turns (N) to obtain the required inductance value (L_b) can be calculated as:

$$N = \sqrt{\frac{L_b}{2\,A_{L\_min}}} \tag{7}$$

where A_{L_min} is the minimum inductance factor for each core (A_{L_min} = 74.52 nH/T^2).

The copper loss of the winding wire can be calculated on maximum value of the rms input current (I_{in_rms}) as given

$$P_{Lb\_Loss} = {I_{in\_rms}}^2 \times DCR \tag{8}$$

$$I_{in\_rms} = \frac{P_{out}}{\eta \times V_{in\_min} \times PF} \tag{9}$$

where DCR is the inductor wire DC resistance and PF is the designed converter power factor.

The inductor wire which is selected based on the inductor maximum peak current, and should meet the requirements that it should be thick so that the DCR is small and it should be possible to form the required number of turns around the core. In this work, the conventional CCM PFC inductor was manufactured with 60 turns of the copper wire with 1.15 mm diameter size around the 2-stacked Kool Mu 77083A7 toroids cores. The manufactured inductor DCR value was experimentally measured, and it was about 0.087 Ω.

2.1.2. Interleaved PFC Boost Inductor

In the interleaved PFC converter, the total power is shared among the parallel channels and the PWM signals for each channel switch are at 360/n, where n is the channels number. A 2-channel interleaved CCM PFC topology is employed in this work. Since this topology uses two inductors, L_1 and L_2, each with approximately half the size of the conventional boost PFC, so that the thermal performance of the converter will improve [36]. Furthermore, the inductor current ripple in the conventional boost PFC is the same as the input current ripple while in the interleaved boost PFC, the ratio of the boost converter input ripple current to inductor's ripple current can vary depending on the duty cycle (D) as given in Equation (7), where the current ripple cancellation in the input side of interleaved type is considered as the major advantage over the conventional type as seen at the input current ripple of the converter in Figure 5 [37].

$$\mathrm{I}_{\mathrm{in}_{\mathrm{Ripple}}} = \sum \begin{matrix} IL_{\mathrm{Ripple}} \frac{1-2D}{1-D} \text{ if } D \leq 0.5 \\ IL_{\mathrm{Ripple}} \frac{2D-1}{D} \text{ if } D > 0.5 \end{matrix} \quad (10)$$

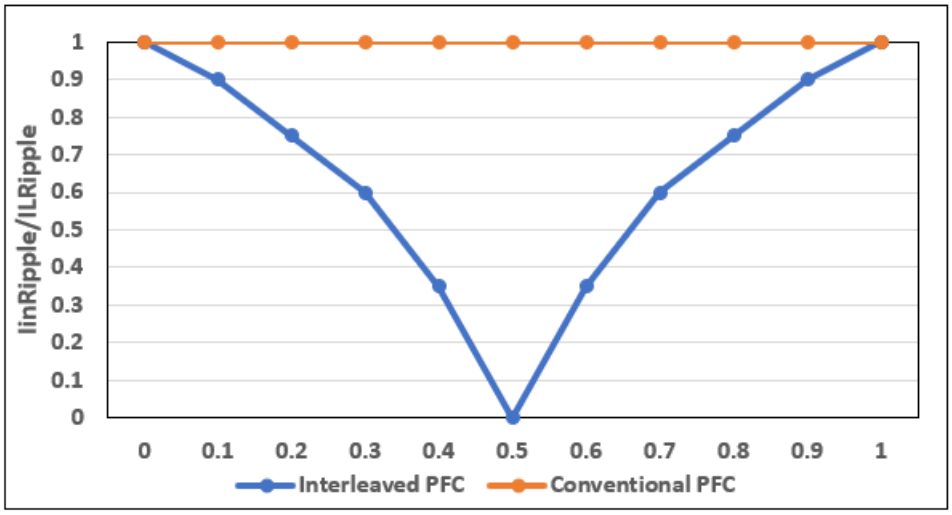


Figure 5. Normalized input ripple current vs. duty cycle in conventional and interleaved PFC.

As the result of the input current ripple cancellation, the size of the EMI filter can be reduced, and the required boost inductors (L_1 and L_2) values will be reduced which leads to reducing the volume and weight of the designed boost inductors.

The circuit operation of the designed interleaved PFC boost converter working in the continuous current conduction mode (CCM) can represent four operating modes and if the average duty cycle is less than 0.5, both switches will not be turned on at the same time which results in three operating modes describes the on-off states of the 2-channels switches as depicted in the converter waveforms in Figure 6, where V_{L1}, V_{L2} represents the inductors voltages, and I_{L1}, I_{L2} represents the inductors currents.

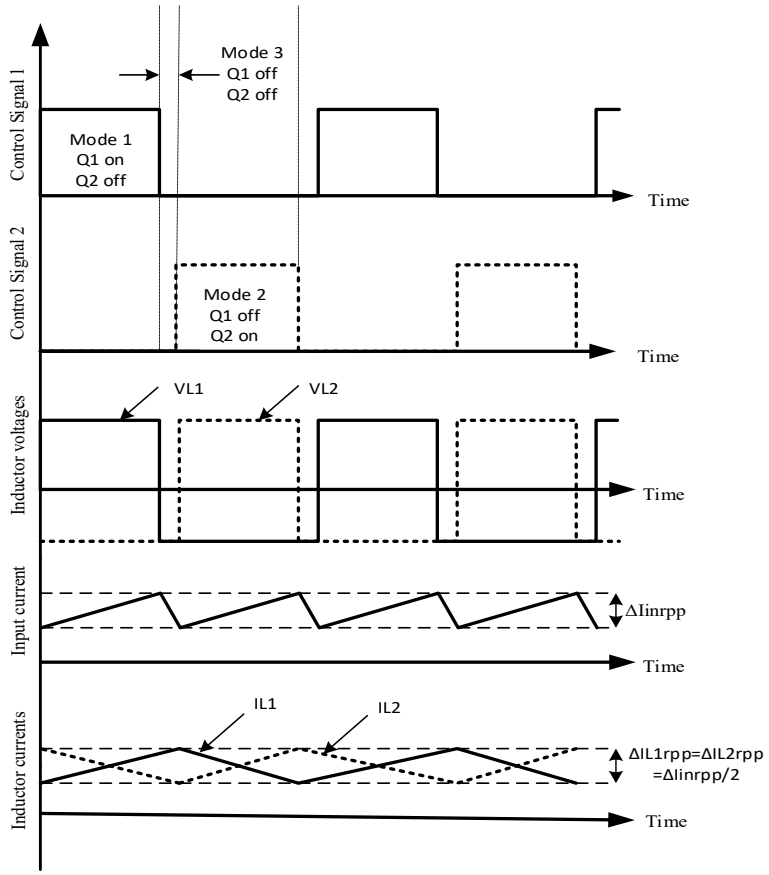


Figure 6. Voltage and currents waveforms of the interleaved CCM (continues-current-conduction mode) PFC topology.

For the interleaved PFC converter, the boost inductor at each channel can be expressed as [38,39].

$$L_1 = L_2 = \frac{D_{on}(1 - D_{on}) \times V_{out}}{ILr_{pk\_pk} \times F_{sw}} \tag{11}$$

The inductor ripple current at each channel as the percentage (%Ripple) of the converter total input current can be given as

$$I_{L1\ rpk\_pk} = I_{L2\ rpk\_pk} = \frac{\%Ripple}{2} \times \frac{I_{avg}}{2} \tag{12}$$

The peak current passing through the inductor at each channel can be given as

$$I_{L1\_pk} = \frac{I_{avg}}{2} + \frac{I_{L1\ rpk\_pk}}{2} \tag{13}$$

using the converter parameters given in Table 1, the required inductance and the inductor maximum peak current for the interleaved CCM PFC converter can be calculated.

For each channel, in order to offer the required value of the inductance with the suitable space of the wire winding around the core, the core of Kool Mu material with part number of 77354A7 was used as depicted in the chart in Figure 4, the inductor number of turns (N) to obtain the required inductance value (L_1) and (L_2) can be calculated as:

$$N_1 = N_2 = \sqrt{\frac{L_1}{A_{L\_min}}} = \sqrt{\frac{L_2}{A_{L\_min}}} \tag{14}$$

where A_{L_min} is the minimum inductance factor for the chosen core (A_{L_min}=69.92 nH/T^2).

The copper loss of the winding wire resistance (DCR) can be calculated on I_{in_rms} as given

$$P_{L1\_Loss} = P_{L2\_Loss} = \left(\frac{I_{in\_rms}}{2}\right)^2 \times DCR \quad (15)$$

where DCR is the direct current resistance of the inductors L_1 and L_2.

In this work the interleaved CCM PFC inductors in each channel are manufactured with 65 turns of the copper wire with 0.75 mm diameter size around the single Kool Mu 77354A7 toroids core. The manufactured inductor DCR value was experimentally measured, and it was about 0.055 Ω.

Table 2 shows the comparison between the boost inductor specifications designed for the conventional and the interleaved CCM PFC converters. The view of the manufactured boost inductors for both topologies is shown in Figure 7. From the manufactured boost inductors specifications and the view for both topologies, the reduction in the boost inductor weight, size, and cost can be observed in case of the interleaved topology as compared with the conventional topology.

Table 2. Boost inductor specifications for the PFC (power factor correction) topologies. CCM (continues-current-conduction mode).

	Conventional CCM PFC	**Interleaved CCM PFC**
Inductor No. of units	1	2
Core type	Kool Mu (77083A7)	Kool Mu (77354A7)
Inductive factor (A_L)	81 ± 8% (nH/T^2)	76 ± 8% (nH/T^2)
No. of Turns (N)	60	65
Winding wire	Cupper 1.15 mm	Cupper 0.75 mm
DC resistance (DCR)	0.078 Ω	0.055 Ω
Total Weight	175 g	95 g
Total cost	17.00 USD	11.00 USD

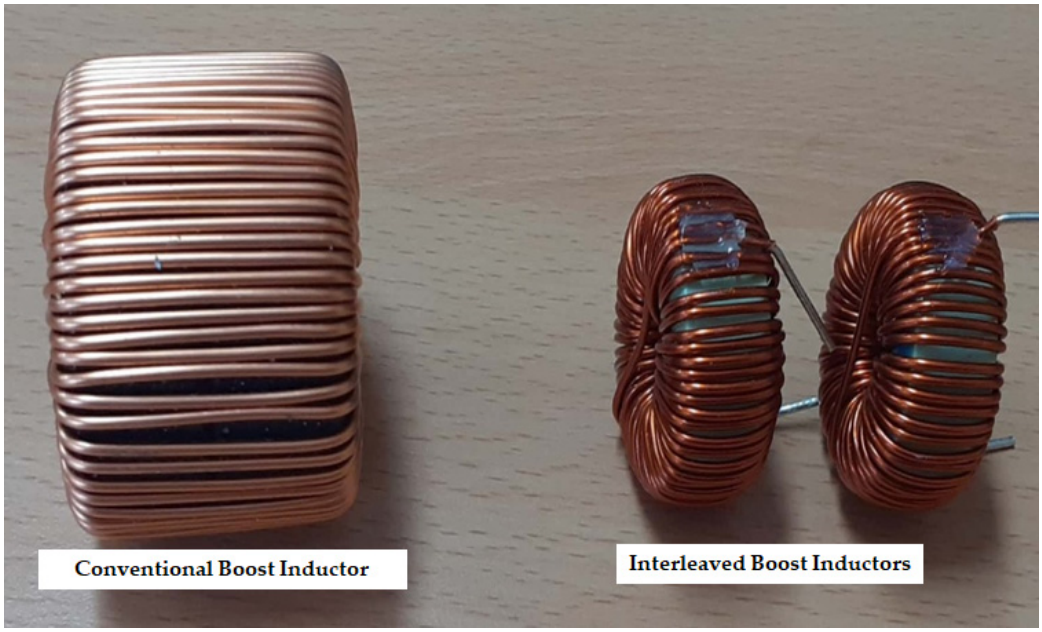


Figure 7. The manufactured PFC boost inductors.

2.2. Output Capacitor Selection

For both topologies, the design techniques of the output capacitor are the same. The output capacitor value usually calculated to meet the specified output voltage ripple using (14), also, this value should be enough to deliver the output minimum voltage hold up with the specific time (t_{hold}), as given in (15)

$$C_b \geq \frac{P_o}{2 \times \pi \times F \times V_{rpp} \times V_o} \tag{16}$$

$$C_b \geq \frac{2 \times P_o \times t_{hold}}{V_o^2 - V_{o\,min}^2} \tag{17}$$

where V_{rpp} is the peak to peak output voltage ripple. The larger value among the two equations was selected to design the output capacitor.

The capacitor rms current across the 60 Hz line cycle is given as [40]

$$I_{Cb\_rms} = \sqrt{\left(\frac{8\sqrt{2} \times P_o^2}{3\pi \times V_{in\_min} \times V_o} - \frac{P_o^2}{V_o^2}\right)} \tag{18}$$

The capacitor equivalent series resistance (ESR) is calculated as

$$ESR = \frac{DF}{2 \times \pi \times F \times C_b} \tag{19}$$

where DF is the chosen capacitor dissipation factor and can be obtained from the capacitor datasheet.

The ESR losses of the capacitor can be calculated as

$$P_{ESR\_Loss} = ESR \times I_{Cb\_rms}^2 \tag{20}$$

An important issue when choosing the output bulk capacitor for the conventional CCM PFC topology is that the ESR should be as small as possible, as it affects power efficiency and voltage regulations. A larger ESR presents more ripple, affecting the boost converter control loops stability [41]. Usually, aluminum electrolytic capacitors are used where high-power density is required, because of their small volume, these types of capacitors are also preferred in PFC applications since they provide high capacitance value with low equivalent series resistance (ESR), but these capacitor types are expensive when compared with the higher ESR types. On the other hand, the interleaving technique in PFC circuits causes the inductor current ripple reduction and then produces a reduced rms output capacitor current, so capacitors with higher ESR (lower cost) can be used.

2.3. Switching Elements Selection

2.3.1. Power Mosfet Switches Selection

The power Mosfet switches in the PFC boost converters are selected based on the maximum peak current with considering the value of the on-state drain-source resistance (Rds_{on}) to reduce the conduction losses.

In the conventional CCM PFC topology, the rms current (I_{Qb}) and the maximum peak current stress (I_{Qb_peak}) in the switch Q_b can be calculated as given in [7,40].

$$I_{Qb} = \frac{P_o}{V_{in\_min}} \sqrt{1 - \frac{8\sqrt{2}V_{in\_min}}{3\pi V_o}} \tag{21}$$

$$I_{Qb\_peak} = \sqrt{2} \times I_{Qb} \tag{22}$$

In case of the interleaved CCM PFC topology, the maximum peak current of the switches Q_1, Q_2 is the half in case of the conventional CCM PFC converter as given

$$I_{Q1\_peak} = I_{Q2\_peak} = \frac{I_{Qb\_peak}}{2} \tag{23}$$

The conduction losses ($P_{Q\ Loss\_cond}$) of the switches can be calculated at the switch rms current and using the value of the drain-source resistance of a MOSFET switch Rds_{on} at 100 C as given

$$P_{Q\ Loss\_cond} = I_{Qb}^2 \times Rds_{on} \tag{24}$$

The switching losses ($P_{Q\ Loss\_swit}$) are calculated using the rise time (t_r) and fall time (t_f) of the Mosfet gate and the capacitance losses (C_{oss}) for the chosen switch.

$$P_{Q\ Loss\_swit} = F_{sw}\left[0.5 \times V_o \times I_{in\_pk} \times (t_r + t_f) + 0.5 \times C_{oss} \times V_o^2\right] \tag{25}$$

In case of the interleaved PFC, 2 switches were used to implement the two channels boost converter, but the cost of the switching elements is still lower than the conventional topology because low current rating switches can be used. Based on the current and voltage ratings for both topologies and considering the value of the Rdson, the IPZ60R040C7 switch is used for the conventional, and 2 switches of IPW60R099P6 were used for the interleaved PFC boost converters in this work.

2.3.2. Fast Switching Boost Diode Selection

The boost diode maximum current is calculated as the maximum load current at the minimum output voltage.

In the conventional PFC converter, the boost diode D_b maximum current is calculated at the full load condition and minimum output voltage as follow

$$I_{Db\_max} = \frac{P_{out}}{V_{o\_min}} \tag{26}$$

For the interleaved PFC converter

$$I_{D1\_max} = I_{D2\_max} = \frac{I_{Db\_max}}{2} \tag{27}$$

The diode losses are estimated based upon the forward voltage (V_f) at 125 °C and the reverse recovery charge (Q_{rr}) of the diode.

$$P_{DbLoss} = V_f \times I_{Db\_max} + 0.5 \times F_{sw} \times V_{out} \times Q_{rr} \tag{28}$$

As given in (26) the boost diode has big influence on the system's performance due to the reverse recovery behavior. So, the Ultra-fast diode with very low reverse recovery time (t_{rr}) and reverse recovery charge (Q_{rr}) is necessary to reduce the switching loss.

In this work Schottky diode is used as the boost diode, the new diode technology of silicon carbide (SiC) Schottky diode with part number of (IDH16G65C5) shows its outstanding performance with almost no reverse recovery behavior. So that, the switching loss due to this diode can be ignored, and only the conduction loss due to V_f is considered.

3. The Proposed Average Small Signal Modelling and Control Circuits Design

To simulate the different PFC topologies for investigating the converter performance with the designed power components, the converter control circuit parameters have to be optimized. The analog PI controllers are used to implement the voltage and current control circuits in the different PFC topologies. The controller's parameters are obtained with using the proposed average small signal stability modeling for both of the conventional and interleaved CCM PFC topologies.

3.1. Conventional CCM PFC Topology

The control loops of the conventional CCM PFC converter are implemented with two control loops as depicted in Figure 8, the outer loop which regulate the output voltage level to the desired value, and the inner loop which used to let the input current follows the reference current to reduce the inductor current distortion and provide input power with high power factor. The mathematical equations which describe the change in the inductor current (I_{Lb}) and output voltage (V_o) for the conventional CCM PFC converter shown in Figure 2a can be given as

$$\frac{dI_{Lb}}{dt} = \frac{V_{in}}{L_b} - \frac{V_o(1-D)}{L_b} \tag{29}$$

$$\frac{dV_o}{dt} = -\frac{V_o}{R\,C_b} + \frac{I_{Lb}(1-D)}{C_b} \tag{30}$$

where R is the load resistance in ohms.

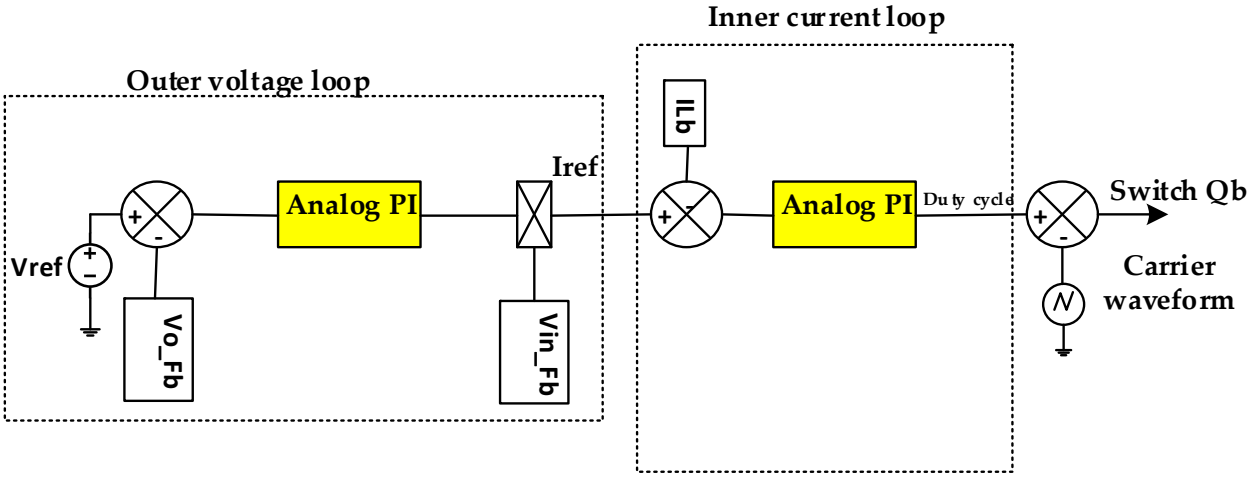


Figure 8. Implementation technique of the conventional CCM PFC analog control circuit.

Assume all variables (I_{Lb}, V_{in}, V_o, and D) are at the steady state at the selected operational point (i_{Lb}, v_{in}, v_o, and d) and the small-signal AC variation (i^*_{Lb}, v^*_{in}, v^*_o and d^*), where

$$I_{Lb} = i_{Lb} + i^*_{Lb}\,;\; V_{in} = v_{in} + v^*_{in}\,;\; V_o = v_o + v^*_o\,;\; D = d + d^* \tag{31}$$

The designed PFC control system should track and modify the duty cycle (D) based on the small-signal AC variation to regulate V_o and I_{Lb}.

Substituting Equation (29) into (27) and (28), we obtain

$$\frac{d(i_{Lb} + i^*_{Lb})}{dt} = \frac{(v_{in} + v^*_{in})}{L_b} - \frac{(v_o + v^*_o)\,(1 - d - d^*)}{L_b} \tag{32}$$

$$\frac{d(v_o + v^*_o)}{dt} = -\frac{(v_o + v^*_o)}{R\,C_b} + \frac{(i_{Lb} + i^*_{Lb})(1 - d - d^*)}{C_b} \tag{33}$$

Equations (30) and (31) can be re-written again as Equations (32) and (33) using the averaging model which consider that over the switching period in the steady state, the inductor current change, and the capacitor voltage is zero.

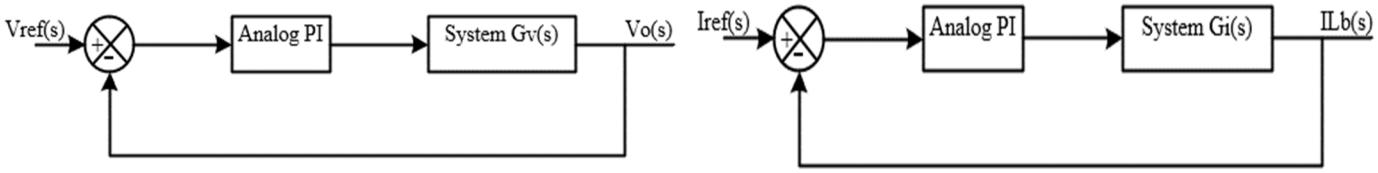
$$\frac{d(i^*_{Lb})}{dt} = \frac{1}{L_b}(v^*_{in}) + \frac{v_o}{L_b}(d^*) - \frac{(1-d)}{L_b}\,(v^*_o) \tag{34}$$

$$\frac{d(v^*_o)}{dt} = \frac{(1-d)}{C_b}(i^*_{Lb}) + \frac{i_{Lb}}{C_b}(d^*) - \frac{1}{R\,C_b}(v^*_o) \tag{35}$$

Arrange state Equations (34) and (35) in state space matrix form to obtain the state space representation of the small signal stability model for the conventional CCM PFC converter as given

$$\begin{bmatrix} i_{Lb}^{*} \\ v_{o}^{*} \end{bmatrix} = \begin{bmatrix} 0 - \left(\frac{1-d}{L_b}\right) \\ \left(\frac{1-d}{C_b}\right) \frac{-1}{R\,C_b} \end{bmatrix} \begin{bmatrix} i_{Lb}^{*} \\ v_{o}^{*} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} \frac{V_o}{L_b} \\ 0 \frac{i_{Lb}}{C_b} \end{bmatrix} . \begin{bmatrix} v_{in}^{*} \\ d^{*} \end{bmatrix} \tag{36}$$

Figure 9 presents the control blocks for the outer and inner control loops of the conventional PFC using the PI controller. The optimal parameters for the PI controllers can be obtained by deriving the voltage and current systems transfer functions using the average signal modelling.



(**a**) (**b**)

Figure 9. Block diagrams of the closed loop control systems: (**a**) outer voltage loop; (**b**) inner current loop.

For the voltage control loop; the TF of the outer voltage system $G_v(s)$ in s-domain can be obtained as the output voltage to the inductor current transfer function as (37), and the analog PI controller system can be expressed using the TF $G_{PIv}(s)$ as (38)

$$G_v(s) = \frac{v_o^{*}(s)}{i_{Lb}^{*}(s)} = \frac{|v_{in}|}{2\,V_o\,C_b s} \tag{37}$$

$$G_{PIv}(s) = K_{Pv} + \frac{K_{Iv}}{s}\,. \tag{38}$$

where K_{Pv} is the proportional gain and K_{Iv} is the integral gain of the voltage PI controller.

The closed-loop TF of the outer voltage control loop system ($G_{CLV}(s)$) can be obtained as

$$G_{CLv}(s) = \frac{V_o(s)}{V_{ref}(s)} = \frac{\frac{|v_{in}|}{2\,V_o\,C_b}.(K_{Pv}\,s + K_{Iv})}{s^2 + \frac{|v_{in}|\,K_{Pv}}{2\,V_o\,C_b}s + \frac{|v_{in}|\,.K_{Iv}}{2\,V_o\,C_b}} \tag{39}$$

For the current control loop; the TF of the inner current system $G_i(s)$ in s-domain can be obtained as the output voltage to the inductor current transfer function as (40), and the analog PI controller system can be expressed using the TF $G_{PIi}(s)$ as (41)

$$G_i(s) = \frac{i_{Lb}^{*}(s)}{d^{*}(s)} = \frac{\left(\frac{V_o}{L_b C_b R}\right).\,(sRC_b + 2)}{s^2 + \frac{1}{C_b R}s + \frac{1}{L_b C_b}(1-d)^2} \tag{40}$$

$$G_{Pii}(s) = K_{Pi} + \frac{K_{Ii}}{s} \tag{41}$$

Since the converter switching frequency (F_{sw}) was selected as about 100 kHz in this work, for high frequency analysis, the capacitor can be shorted, and the open-loop TF of the inductor current system in Equation (40) can be simplified as

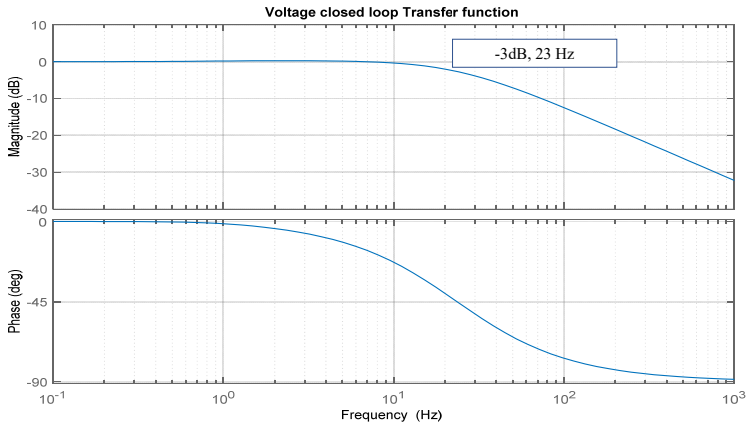
$$G_i(s) = \frac{2\,V_o}{sL_b} \tag{42}$$

The closed loop TF of the current control loop $G_{CLI}(s)$ can be obtained as

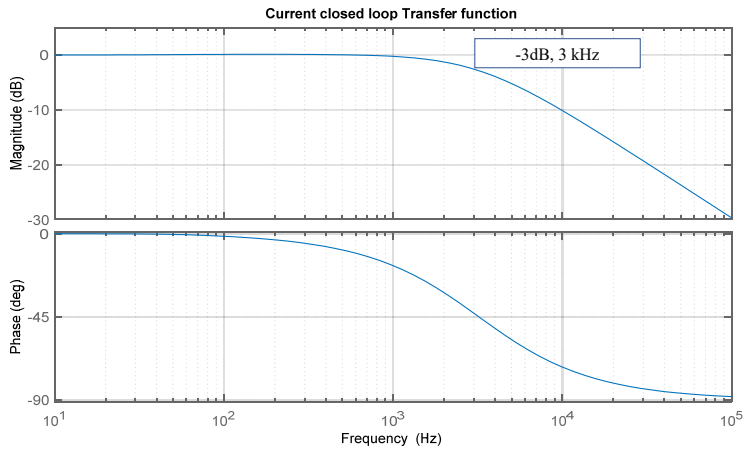
$$G_{CLI}(s) = \frac{I_{Lb}(s)}{I_{ref}(s)} = \frac{2\,V_o\,K_{Pi}\,s + 2\,V_o K_{Ii}}{s^2 L_b + 2\,V_o\,K_{Pi}\,s + 2\,V_o K_{Ii}} \quad (43)$$

Once the transfer functions of the control loops are determined, the PI controllers' gains can be designed with the standard form of the second order system TF by selecting the proper control system bandwidth and the undamped natural frequency which enhanced the optimal stability criteria. Usually, the bandwidth of the outer voltage loop must be very small to eliminate the harmonics of the output DC voltage reflected by the AC input voltage at 60 Hz [42]. What is more the bandwidth of the inner current loop must be high as compared with the outer voltage control loop to let the inductor current follows the reference current, also the current control loop bandwidth must be less than switching frequency (Fsw) to reject the noise at the switching frequency. In this work, the undamped natural frequency (ξ) was considered to be about 0.707, the closed loop bandwidth of (Wn) was assumed to be about 150 rad/s and 10,000 rad/s for the outer voltage and inner current loops, respectively. For the reliable operation of a controller to offer good performance with different loading condition, the controllers Kp and KI parameters were set to work with the minimum value of the load voltage (Vo) of 320 V with the rated input voltage.

Figure 10 depicts the bode plot of the closed-loop TF of the two control loops, which shows that the current controller offers unity gain for frequencies less than 3 kHz. This current control system, working as a low pass filter, helps to remove the switching frequency noise. Moreover, the voltage controller offers unity gain for frequencies less than 23 Hz. This voltage controller works as a low pass filter to remove the 60 Hz voltage ripple.



(**a**)



(**b**)

Figure 10. Bode plots for the control loops for the conventional CCM PFC converter: (**a**) voltage control loop; (**b**) current control loop.

3.2. Interleaved CCM PFC Topology

The average small signal modelling of the interleaved PFC can be derived in the same way as explained for the conventional boost PFC using state space averaging technique. The interleaved PFC contains two separates boost PFC converters operating 180 degrees out of phase. These two separate legs are assumed to operate identically to derive the transfer function of the model as depicted in Figure 11.

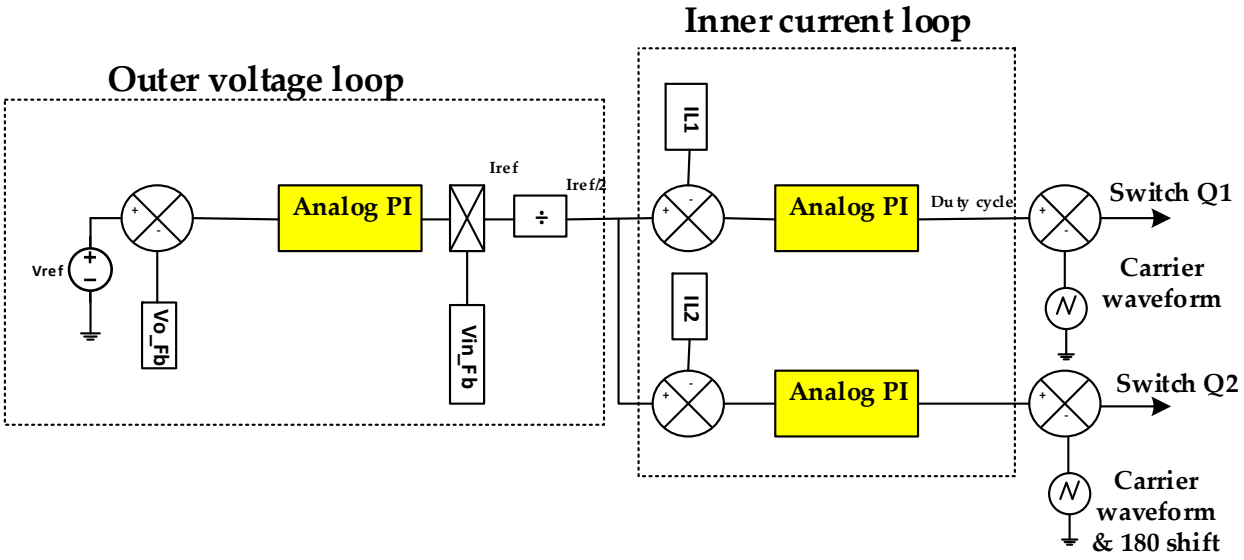


Figure 11. Implementation technique of the interleaved CCM PFC analog control circuit.

The mathematical equations which describe the change in inductors currents (I_{L1}, I_{L2}) and the output voltage (V_o) can be given as

$$\frac{dI_{L1}(t)}{dt} = \frac{V_{in}}{L_1} - \frac{V_o(1-D)}{L_1} \tag{44}$$

$$\frac{dI_{L2}(t)}{dt} = \frac{V_{in}}{L_2} - \frac{V_o(1-D)}{L_2} \tag{45}$$

$$\frac{dV_o(t)}{dt} = \frac{I_{L1}(1-D)}{C_b} + \frac{I_{L2}(1-D)}{C_b} - \frac{V_o}{R\,C_b} \tag{46}$$

Assume all variables (I_{L1}, I_{L2}, V_{in}, V_o, and D) are at the steady state at the selected operational point (i_{L1}, i_{L2} , v_o , and d) and the small-signal AC variation ($i^*_{L1}, i^*_{L2}, v^*_{in}$, v^*_o, and d^*), where

$$I_{L1} = i_{L1} + i^*_{L1};\ I_{L2} = i_{L2} + i^*_{L2};\ V_{in} = v_{in} + v^*_{in}\ ;\ V_o = v_o + v^*_o\ ;\ D = d + d^* \tag{47}$$

Substituting from (47) in Equations (44)–(46), we obtain

$$\frac{d(i_{L1} + i^*_{L1})}{dt} = \frac{(v_{in} + v^*_{in})}{L_1} - \frac{(v_o + v^*_o)\,(1 - d - d^*)}{L_1} \tag{48}$$

$$\frac{d(i_{L2} + i^*_{L2})}{dt} = \frac{(v_{in} + v^*_{in})}{L_2} - \frac{(v_o + v^*_o)\,(1 - d - d^*)}{L_2} \tag{49}$$

$$\frac{d(v_o + v^*_o)}{dt} = -\frac{(v_o + v^*_o)}{R\,C_b} + \frac{(i_{L1} + i^*_{L1})(1 - d - d^*)}{C_b} + \frac{(i_{L2} + i^*_{L2})(1 - d - d^*)}{C_b} \tag{50}$$

Equations (48)–(50) can be re-written again as Equations (51)–(53) using the averaging model as follow

$$\frac{d(i_{L1}^*)}{dt} = \frac{1}{L_1}(v_{in}^*) + \frac{v_o}{L_1}(d^*) - \frac{(1-d)}{L_1}(v_o^*) \tag{51}$$

$$\frac{d(i_{L2}^*)}{dt} = \frac{1}{L_2}(v_{in}^*) + \frac{v_o}{L_2}(d^*) - \frac{(1-d)}{L_2}(v_o^*) \tag{52}$$

$$\frac{d(v_o^*)}{dt} = \frac{(1-d)}{C_b}(i_{L1}^*) + \frac{(1-d)}{C_b}(i_{L2}^*) + \frac{i_{L1}+i_{L1}}{C_b}(d^*) - \frac{1}{R\,C_b}(v_o^*) \tag{53}$$

Arrange state Equations (51)–(53) in state space matrix form to obtain the state space representation of the small signal stability model for the interleaved CCM PFC converter as given

$$\begin{bmatrix} i_{L1}^* \\ i_{L2}^* \\ v_o^* \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{(1-d)}{L_1} \\ 0 & 0 & -\frac{(1-d)}{L_2} \\ \frac{(1-d)}{C_b} & \frac{(1-d)}{C_b} & -\frac{1}{R\,C_b} \end{bmatrix} \begin{bmatrix} i_{L1}^* \\ i_{L2}^* \\ v_o^* \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & \frac{v_o}{L_1} \\ \frac{1}{L_2} & \frac{v_o}{L_2} \\ 0 & \frac{i_{L1}+i_{L1}}{C_b} \end{bmatrix} \begin{bmatrix} v_{in}^* \\ d^* \end{bmatrix} \tag{54}$$

The transfer function (TF) of the output voltage control system for the interleaved CCM PFC converter can be obtained as given

$$G_v(s) = \frac{v_o^*(s)}{i_{L1,2}^*(s)} = \frac{|v_{in}|}{2V_o\,C_b s} \tag{55}$$

The transfer function (TF) of the inner current control loops for the inductor's currents I_{L1} and I_{L2} for the interleaved CCM PFC converter can be obtained as given

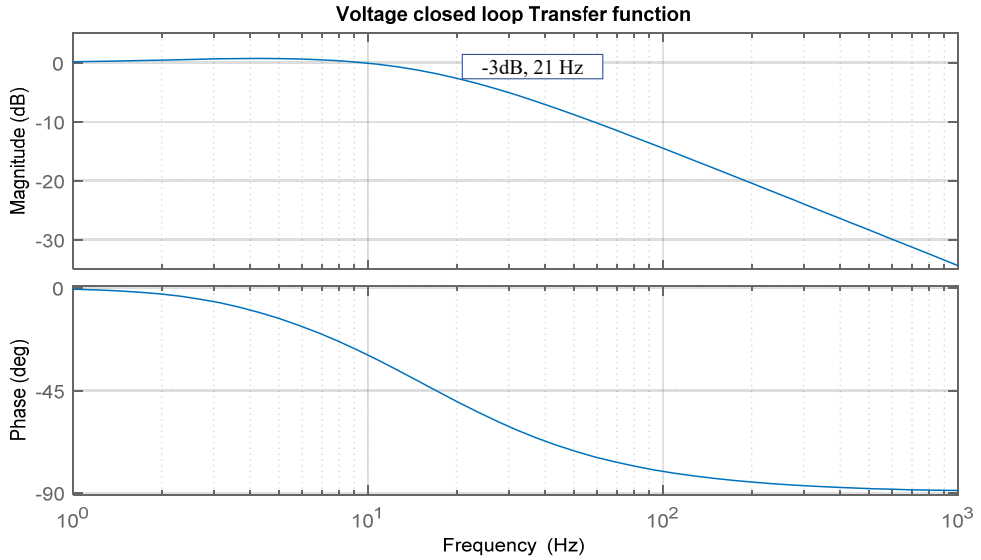
$$G_i(s) = \frac{i_{L1,2}^*(s)}{d^*(s)} = \frac{2V_o}{2R(1-d)^2} \times \frac{1 + \frac{sRC_b}{2}}{1 + \frac{sL_{1,2}}{R(1-d)^2} + \frac{s^2L_{1,2}C_b}{(1-d)^2}} \tag{56}$$

After rearranging Equation (56), the open loop TF of the inductors currents systems can be written as

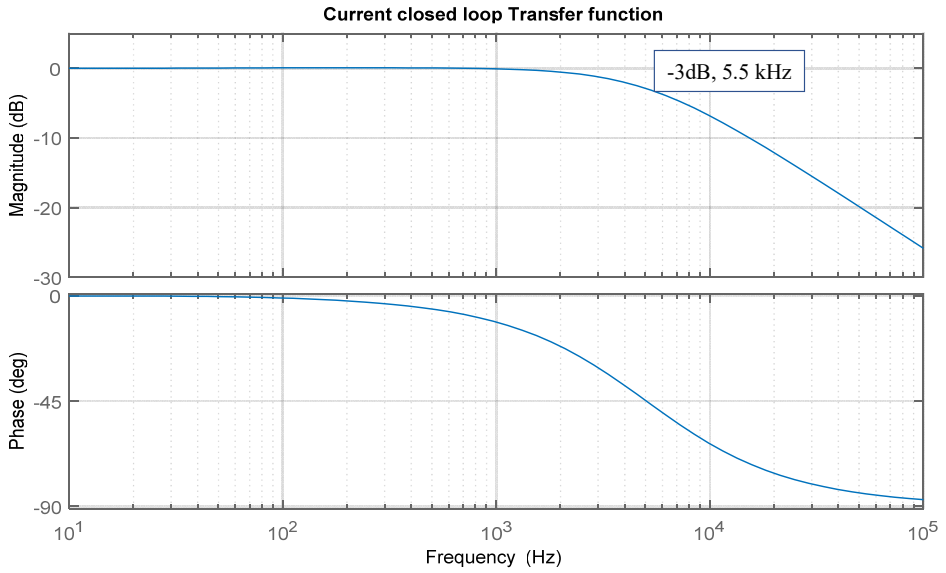
$$G_1(s) = G_2(s) = \frac{\left(\frac{V_o}{L_{1,2}C_bR}\right).(sRC_b + 2)}{s^2 + \frac{1}{C_bR}s + \frac{2}{L_{1,2}C_b}(1-d)^2} \tag{57}$$

For the interleaved CCM PFC converter, the closed loop bandwidth values were assumed to be about 150 rad/s and 18,000 rad/s for the outer voltage and inner current loops, respectively.

Figure 12 depicts the bode plot of the closed-loop TF of the control loops, which shows that the current controller offers unity gain for frequencies less than 5.5 kHz. This current control system, working as a low pass filter, helps to remove the switching frequency noise. Furthermore, the voltage controller offers unity gain for frequencies less than 21 Hz. This voltage controller works as a low pass filter to remove the 60 Hz voltage ripple.



(**a**)

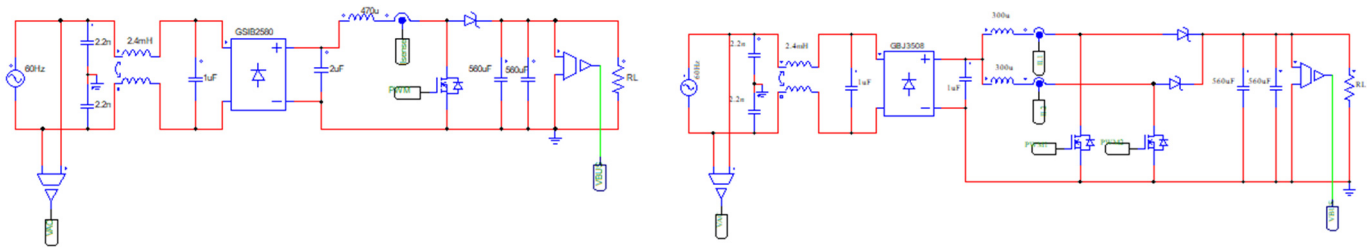


(**b**)

Figure 12. Bode plots for the control loops for the interleaved CCM PFC converter: (**a**) voltage control loop; (**b**) current control loop.

4. Simulation Results

Figure 13 shows the PSIM software (Powersim, Rockville, USA) simulation circuits for the conventional and interleaved PFC circuits with the designed power components values. The EMI filter in both topologies was designed as an LC filter with common mode coupling inductor of about 2.4 mH and suppression capacitors of about 2.2 nF [43]. For the practical simulation results, which were closest to the experimental results, the boost diode is considered as SiC Schottky diode to ignore the switching losses, the forward voltage of the boost diode is about 1.5 V, and the parameters of bridge diode, the boost converter switches for both topologies are obtained from the datasheets of the selected components.



(**a**) (**b**)

Figure 13. PSIM simulation circuit for the PFC topologies: (**a**) conventional boost PFC; (**b**) interleaved boost PFC.

At the rated input of (220 Vrms, 60 Hz) and rated load of Po = 2000 W and Vo = 400 V, the power performance for both topologies is simulated. Figures 14 and 15 show the waveforms of the input and output currents and input and output voltages as well as the circuit power factor (PF) for the conventional and the interleaved CCM PFC converters respectively. We observed that the designed conventional PFC converter offers input power factor at full load condition of 2 kW with minimum value about 0.9955 and maximum value about 0.9970. On the other hand, the interleaved converter offers a power factor with a minimum value of about 0.9975 and a maximum value of about 0.9991 during the full load operating condition. The peak to peak ripple value in the output voltage is measured of about 12.00 V in the conventional and 12.10 V in the interleaved converter which is less than the design specified value (Vrpp = 20 V) for the output voltage ripple contents in both topologies. Additionally, the output ripple current peak to peak value is measured of about 0.153 A in the conventional and 0.151 A in the interleaved converter which is less than 4% in both topologies.

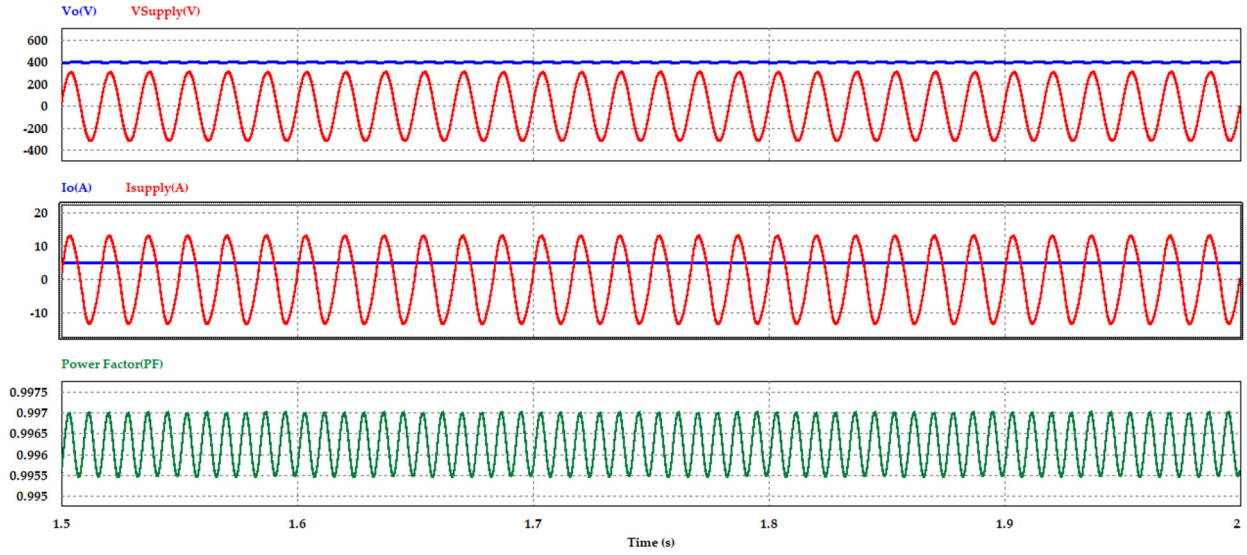


Figure 14. Voltages, currents, and input power factor for the conventional CCM PFC at full load condition.

To show the operation performance of the designed current control loops for both PFC topologies, the operation waveforms of inductor currents and the reference current are simulated. Figures 16 and 17 show the inductor's current and the reference current generated from the outer voltage control loop for the conventional and the interleaved PFC converters, respectively. It can be observed that the inductors currents successfully follow the reference current in both topologies which ensure input current follows input voltage, and offer higher input power factor values.

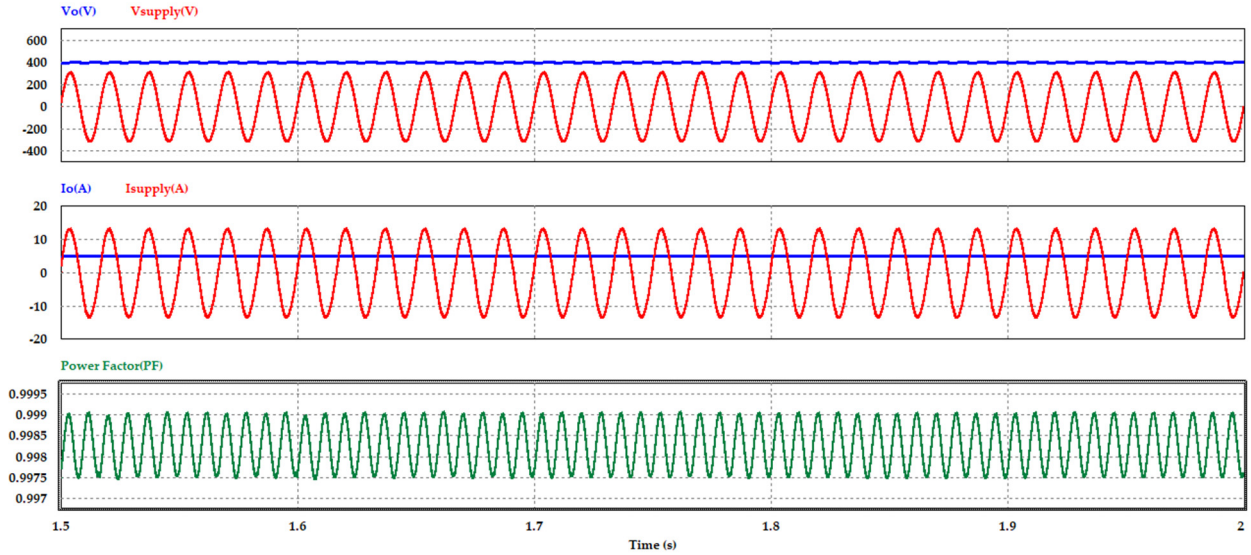


Figure 15. Voltages, currents, and input power factor for the interleaved CCM PFC at full load condition.

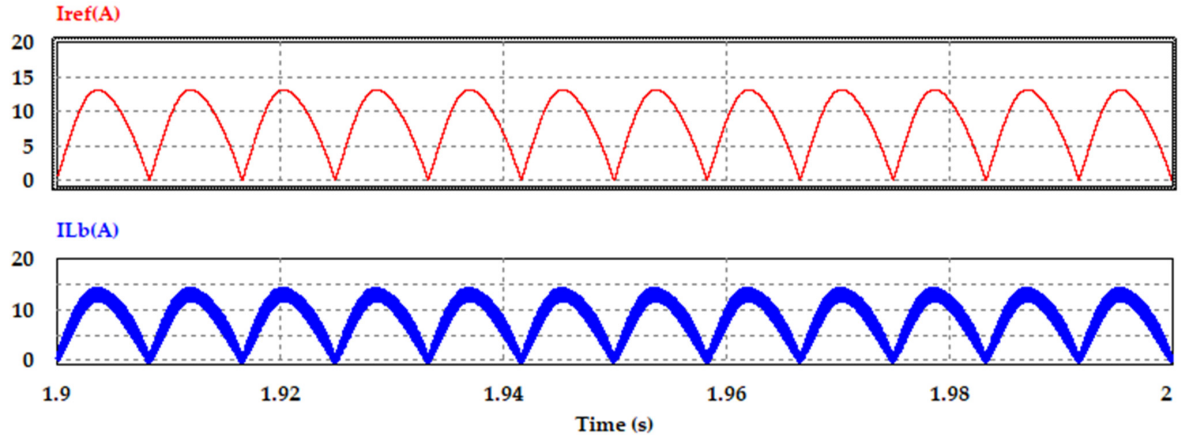


Figure 16. Inductor current and reference current for the conventional CCM PFC at full load condition.

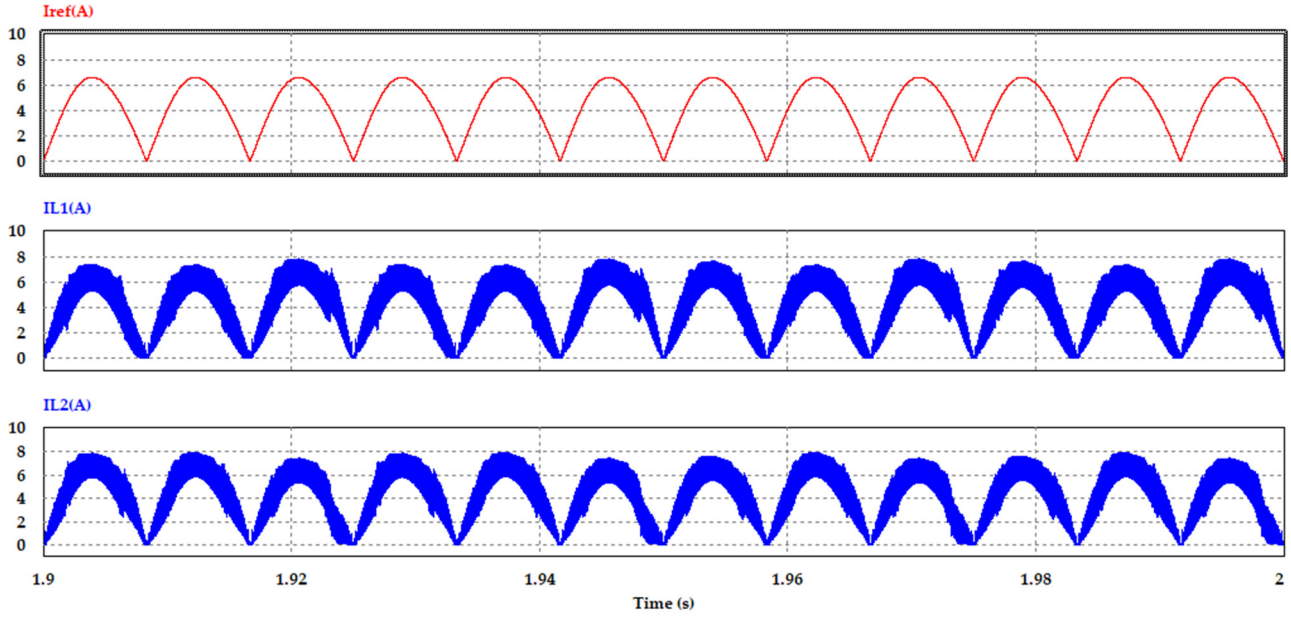


Figure 17. Inductors current and reference current for the interleaved CCM PFC at full load condition.

The dynamic performance of the outer voltage control loop to regulate the output voltage to the specified value (400V) with different input voltage conditions is simulated as shown in Figures 18 and 19 for the conventional and the interleaved PFC converters, respectively. Three operation conditions of the lower voltage, steady state voltage, and higher voltage conditions of the input supply voltage are used to test the operation of the outer voltage control loop. It can be observed that the designed outer voltage control loops based on the proposed small signal stability modeling succeed to regulate the output voltage to the specified value with very small transition time with different wide range of the input voltage conditions.

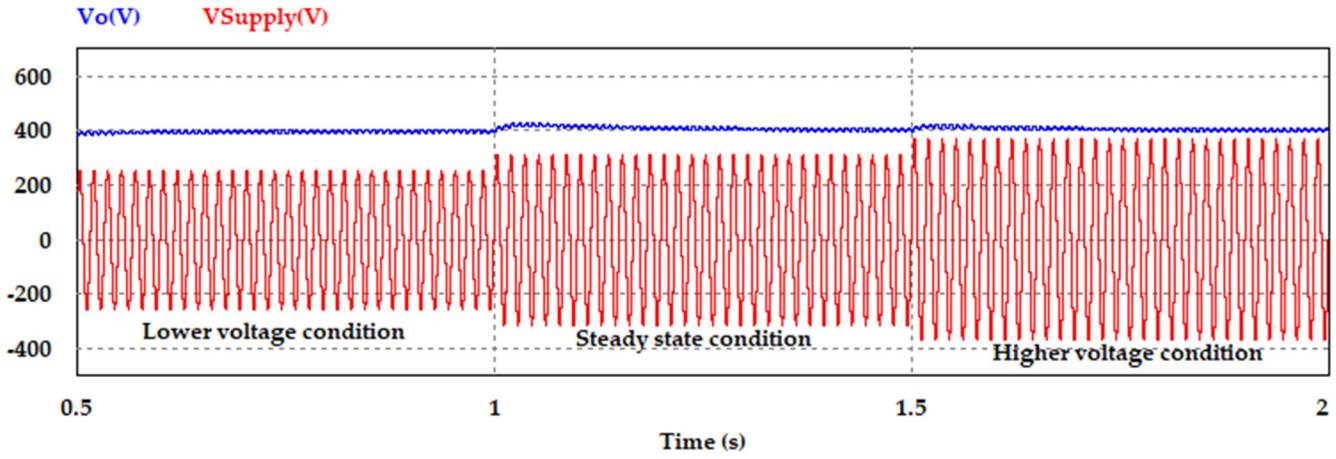


Figure 18. Output voltage dynamic performance with different input voltage for the conventional CCM PFC.

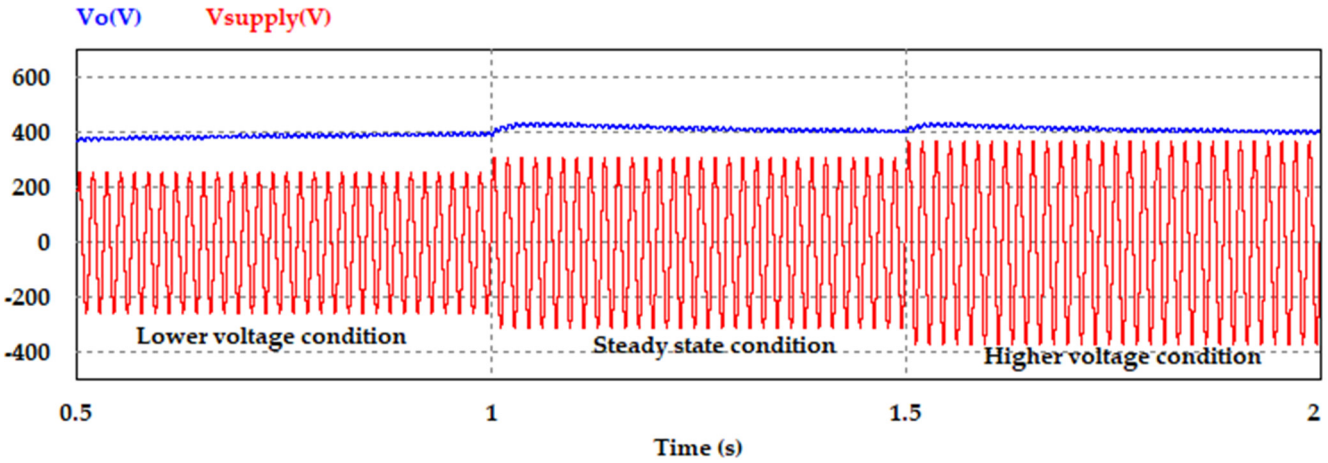
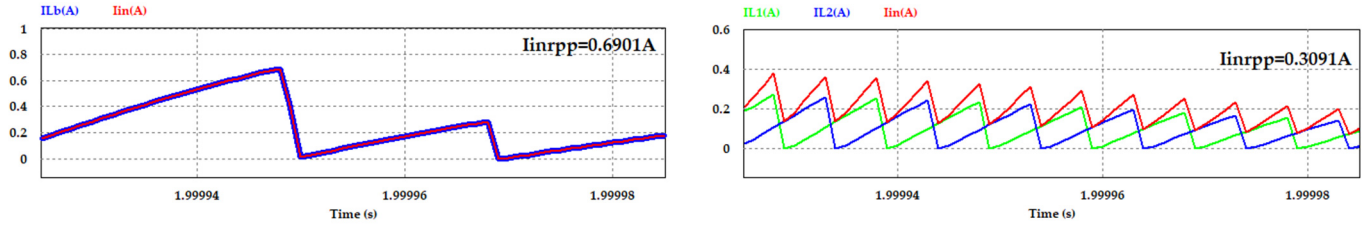


Figure 19. Output voltage dynamic performance with different input voltage for the interleaved CCM PFC.

To investigate the advantage of the current ripple cancellation in the interleaved PFC converters over the conventional PFC converters, the input current ripple for both converters is measured at the same switching period from 1.999925 to 1.999985. Figure 20 shows the waveforms of the boost converter input current and inductors currents for the conventional and the interleaved PFC converters. The total input ripples current peak to peak over this switching period is measured for both topologies, which is about 0.6901 A for the conventional PFC converter and is reduced to about 0.3091 A for the interleaved PFC converter due to the ripple current cancellation of the interleaved converters, reducing of the input current ripples leads to reducing the current total harmonic distortions and increasing the input supply power factor.



(**a**) (**b**)

Figure 20. Input ripple current measurements: (**a**) conventional boost PFC; (**b**) interleaved boost PFC.

Figures 21 and 22 shows the Fourier analysis for the input current at the full load condition of the conventional and the interleaved CCM PFC converters, respectively. It is observed that the third harmonic is the dominant harmonic in the current spectrum and it is about 0.578 A for the conventional PFC, which reduced to about 0.220 A with the interleaved PFC converter. Furthermore, the total harmonic distortion (THD) of about 4.67% in the conventional PFC converter and reduced to about 2.65% with the interleaved PFC converter. It can observe that the designed PFC converters offer harmonic level follows the harmonic standard specification IEEE 519-20142 [35] and IEC 61000-3-2 [36] for the design of the telecom power supply.

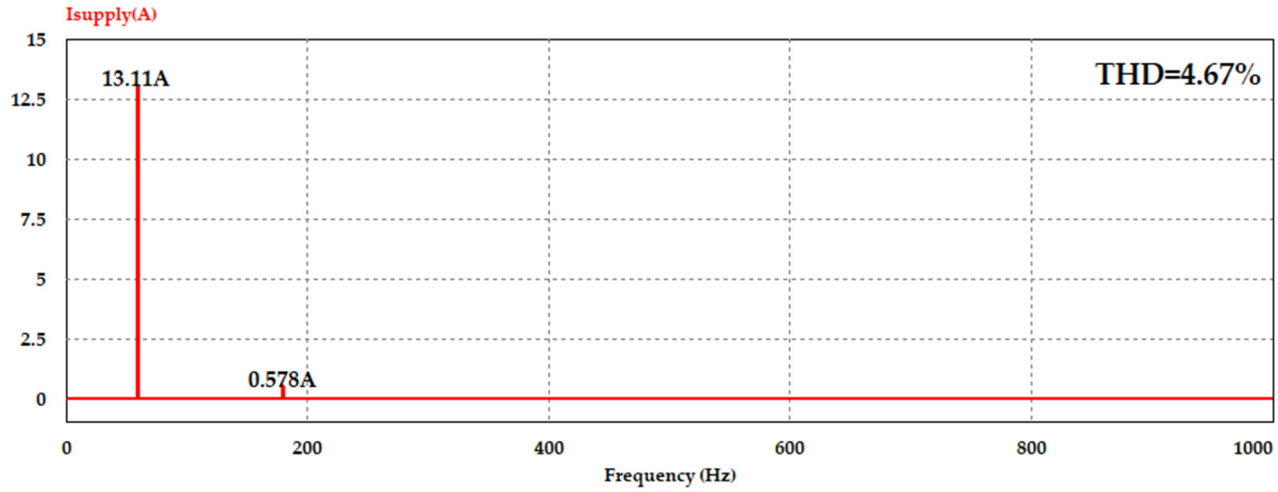


Figure 21. Supply current frequency spectrum for the conventional CCM PFC.

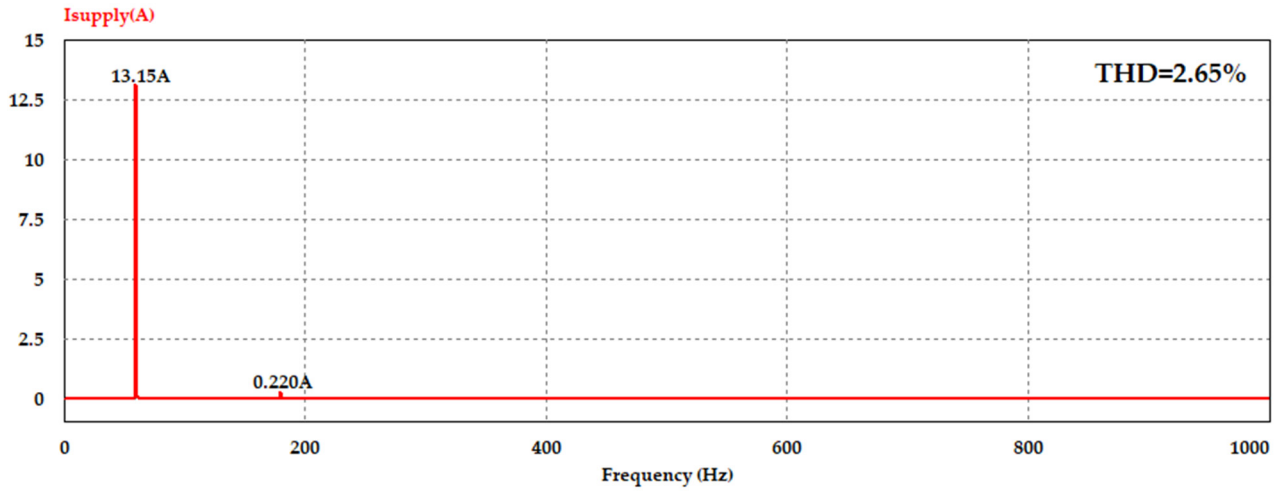


Figure 22. Supply current frequency spectrum for the interleaved CCM PFC.

5. Experimental Verification

The printed circuits board (PCB) for the 2 kW PFC converters is designed using OrCAD capture and PCB design software 17.4 (Cadence, CA, USA) using the components given in Table 3. The control circuit for the conventional PFC circuit is implemented using the UCC28180 CCM PFC controller and the control circuit for the interleaved PFC circuit is implemented using the UCC28070 interleaved CCM PFC controller from Texas instruments. With using the design calculation tools of both IC controllers, the cross over frequency for the voltage and current control loops are adjusted with the same values given in design Section 3.

Table 3. Selection elements of the different topologies.

	Conventional CCM PFC	Interleaved CCM PFC
Bridge	GSIB2580	GBJ3508
Boost Inductor	470 uH	2× 300 uH
MOSFET	IPZ60R040C7	2× IPW60R099P6
Boost Diode	IDH16G65C5	2× IDH16G65C5
Bulk capacitor	1120 uF (2× EKMR421VSN561MR50S)	1120 uF (2× ALA7DA561DE450)
PFC Control IC	UCC 28180	UCC 28070
Gate driver	1ED160N12AF	UCC27324D

Figure 23 shows the experimental setup used for testing the experimental performance for the designed PFC converters. The Kikusi DC electronic load with a power rating of about 3 kW is used for loading the converters from 25% to 100% of the full load condition.

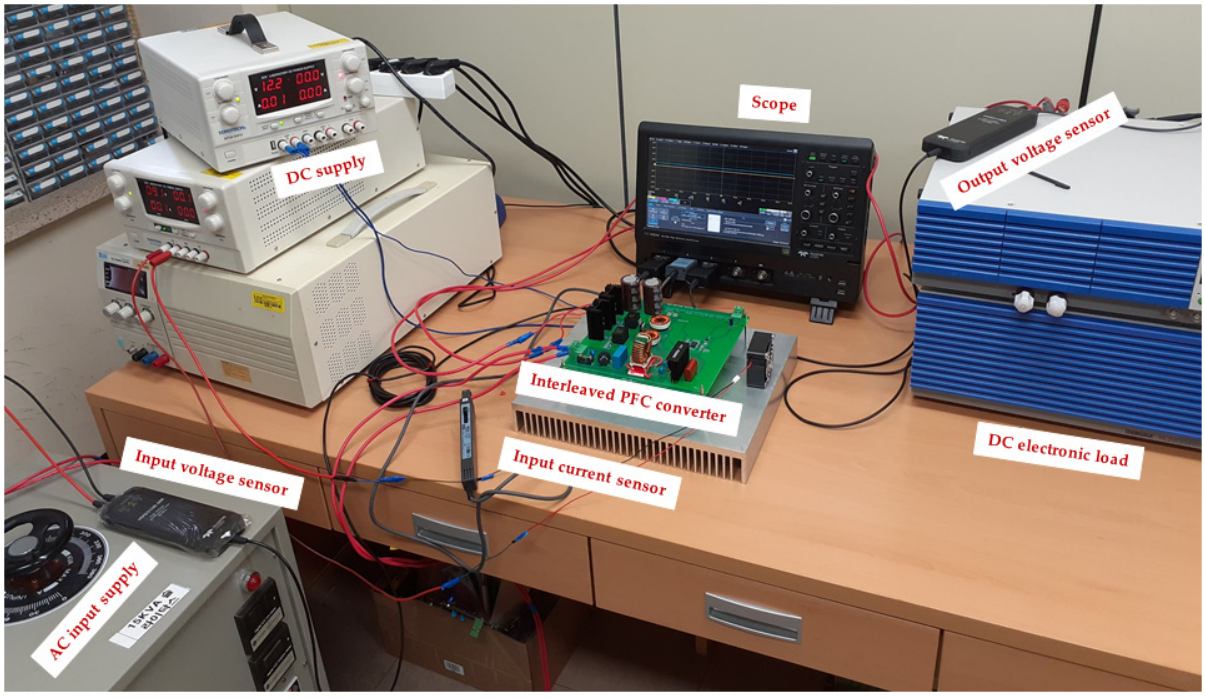


Figure 23. Experimental setup for testing of the designed PFC converters.

At the rated input of (220 Vrms, 60 Hz), different loading conditions (25%, 50%, 75%, and 100%) of the full load condition are loaded to the designed converter. Figures 24 and 25 and show the input, output voltages, input current waveforms, and the power factor measurement for the conventional and the interleaved PFC converters, respectively.

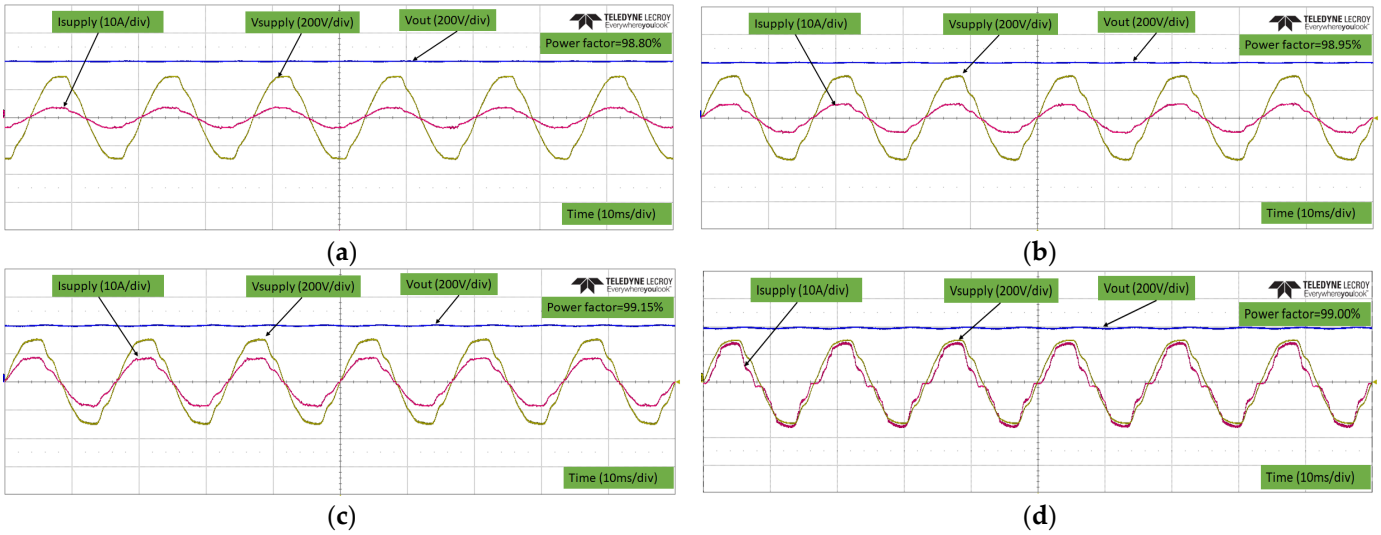


Figure 24. Input and output voltages, input current, and power factor of the designed conventional PFC converter with different loading condition. (**a**) 25%; (**b**) 50%; (**c**) 75%; (**d**) 100%.

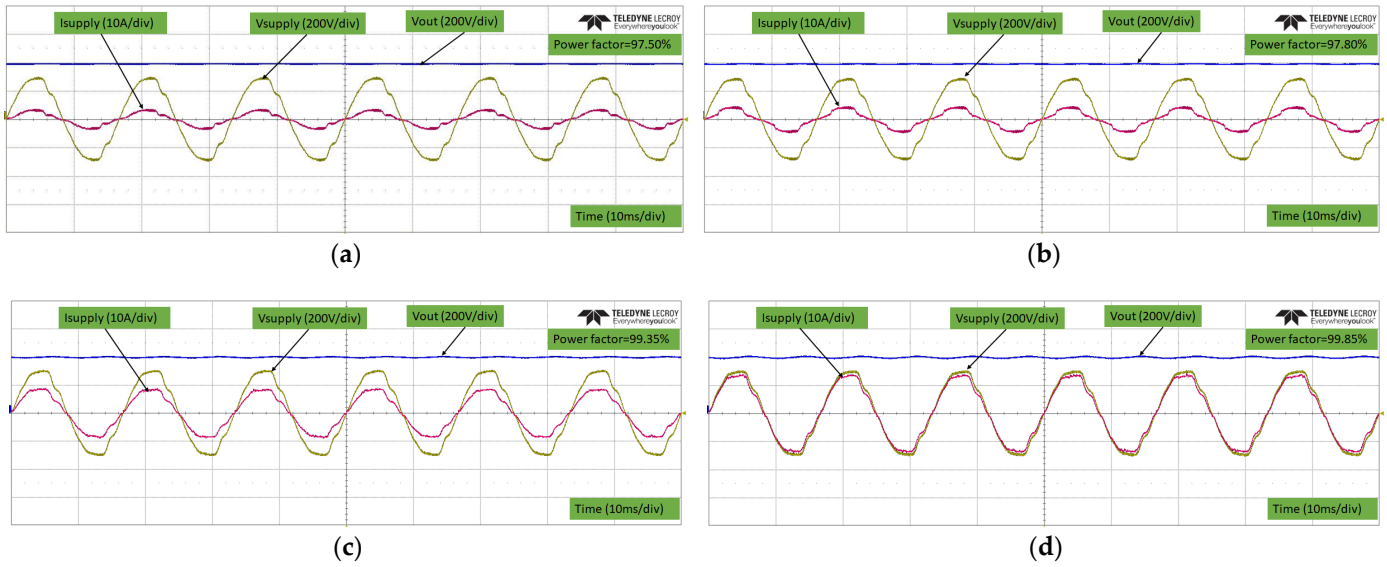


Figure 25. Input and output voltages, input current, and power factor of the designed interleaved PFC converter with different loading condition. (**a**) 25%; (**b**) 50%; (**c**) 75%; (**d**) 100%.

It is observed that the designed voltage control loops in the conventional and interleaved PFC converters ables to adjust the output voltage at a constant value of 400 V with very small ripple contents at different loading conditions. Additionally, the current control loops offer input current with a high power factor and small THD. Figure 24a shows that the conventional PFC converter offers an input power factor of about 98.8% at a lower loading condition of 25%, which is higher than an interleaved PFC converter of 97.50% with the same loading condition as shown in Figure 25a.

With the increasing of the loading condition in the conventional PFC converter, the input current distortion factor is increased due to the high voltage and current stresses in the PFC converter switch and increasing of the thermal heating of the PFC inductor which reduced the input power factor at higher loading condition. On the other hand, the channeling of the current through two channels in the interleaved PFC converter reduced the components' current and voltage stresses and also improve the thermal performance of the PFC inductors, makes the converter power factor stable at higher values at the higher

loading condition. At full loading condition of 2 kW, Figures 24d and 25d show that the conventional PFC converter offers an experimentely power factor value about 99% and the interleaved PFC converter offers a power factor value of about 99.85%.

With different loading conditions, as depicted in Figure 26, the designed PFC converters performances are tested through measurements of the THD, power factor and conversion efficiency by using the simulation and experimental tests. At 25% loading condition the efficiency of the conventional PFC converter is experimentally about 95.9% and for the interleaved PFC converter is about 93.8%, when the load is increased to about 100% loading condition, the conventional PFC converter efficiency is about 97%, and for the interleaved PFC converter is about 97.6%. It is observed that, at a low loading condition the conventional PFC converter offers higher efficiency than the interleaved converter, but when the loading power is increased the current stress and thermal losses in the conventional PFC boost inductor and Mosfet is increased which increased the thermal power losses and reduced the conversion efficiency, also increasing the current distortion factor, increasing the THD, and reducing the input power factor.

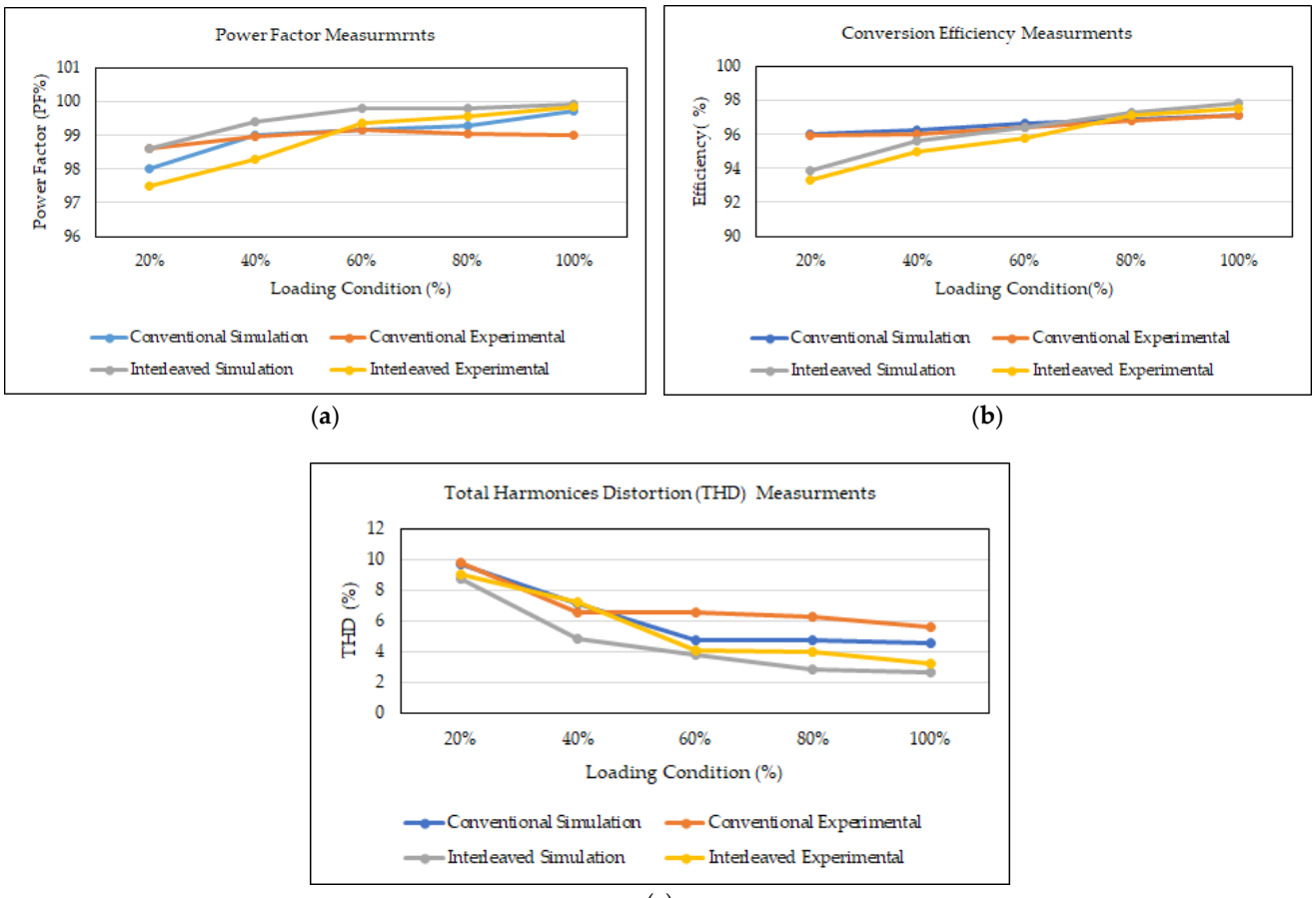


Figure 26. Performance measurements with different loading condition: (**a**) power factor (PF); (**b**) conversion efficiency; (**c**) THD (total harmonic distortions).

On the other hand, interleaving technique in the PFC converters improve the converter thermal performance, reducing the voltage, and current stresses in the boost converter components at higher loading condition which increase the conversion efficiency, and reducing the total harmonic distortion of the input current at high power loading condition as shown in Figure 26c, where the THD is reduced from 5.6% in the conventional PFC converter to about 3.2% with using of the interleaved PFC converter. Usually, in the PFC converter circuits, the input power factor is depending on the displacement factor and the

distortion factor [5], thus, reducing the current distortion factor leads to an increase in the input power factor from 99% to about 99.85% as shown in Figure 26a.

6. Conclusions

In this paper, the detailed design analysis and manufacturing of the printed circuit board (PCB) of two topologies of the telecom PFC converters with high-power density, high conversion efficiency, high input power factor, and lower THD are performed. The proposed small signal modeling is used to design the parameters of the PI controllers for the current and voltage control loops for both topologies. Simulation and experimental tests are used to test the performance of the designed converters with different loading conditions. The simulation and experimental results show that the conventional PFC topology with the proposed design offers higher efficiency and higher power factor at lower loading condition until 800 W as compared with the interleaved PFC converter, but when the loading condition is increased more than 800 W, the thermal heating in the conventional boost inductor, the boost diode, and Mosfet is increased leading to higher conduction losses and higher current distortion factor which reduced the conversion efficiency and, also, reduced the input power factor.

The experimental results show that, at the higher loading condition, the efficiency of the designed interleaved boost PFC converter is higher as compared with the conventional boost PFC converter since the power is channeled through two paths which reduced the boost inductor size and weight. Furthermore, the interleaving technique reduces the voltage and current stresses across the Mosfet switches and improves the component's thermal performance, improvement of the converter thermal performance decreases the conduction losses of the inductor, the boost diode, and the Mosfet, increased the conversion efficiency and input power factor with higher loading condition.

Author Contributions: A.H.O. created, designed and applied the proposed controlling technique. The literature review and manuscript preparation, as well as the simulations, were carried out by A.H.O. Experimental verification was carried out by A.H.O. and J.B. Final review of manuscript corrections was conducted by J.B. All authors have read and agreed to the published version of the manuscript.

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