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Highly Efficient Transformerless Inverter with Flying-Capacitor Buck–Boost for Single-Phase Grid-Connected PV Systems

Ali Salem [1,*] and Khaled Sedraoui [1,2]

[1] Department of Electrical and Computer Engineering, Faculty of Engineering, King Abdulaziz University, Jeddah 21481, Saudi Arabia; sedraoui@yahoo.com
[2] Center of Research Excellence in Renewable Energy and Power Systems, King Abdulaziz University, Jeddah 21481, Saudi Arabia
* Correspondence: eeng.alisalem@gmail.com; Tel.: +966-50-123-1487

Abstract: Grid-connected inverters (GCI) are commonly used in PV system applications to generate a regulated AC current to feed into the grid. Transformerless inverters are the most advanced inverters that are used in industry, which provide efficiency with smaller size and lower cost. This paper proposes a grid-connected single-phase transformerless inverter with the technology of common ground and the virtual DC bus concept. In this topology, the grid neutral is connected directly to the PV ground, which generates a constant common mode voltage (CMV), thus leading to the elimination of the leakage current caused by the PV array's parasitic capacitance. The proposed inverter has a buck–boost circuit with a flying capacitor to generate the DC bus for a negative power cycle, four switches, and two diodes. A unipolar sinusoidal pulse width modulation (SPWM) technique is used which reduces the output filter requirements. In addition, only one switch carries the load current during the active states of both the negative and positive power cycle, thus minimizing the conduction losses. One more advantage presented in the proposed inverter is its ability to charge the flying capacitor during all operation states due to the existence of the buck–boost circuit. Design and theoretical calculations were conducted in this paper to optimize the losses. Moreover, the PSIM simulation was used to validate the proposed topology inverter, verify the performance by showing leakage current elimination, and achieve unipolar voltage in the output bus. The simulation results show a peak efficiency of 98.57% for a 2 kW inverter, which agrees with the theoretical calculations.

Keywords: solar photovoltaic (PV); transformerless inverter; flying capacitor; common ground; buck–boost converter; leakage current; single-phase; grid-connected; common mode voltage (CMV)

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1. Introduction

In recent decades, the growth in renewable energy systems has increased exponentially. Therefore, governments and national planning makers tend towards generating electricity based on renewable resources instead of conventional electricity resources. In 2020, 80% of the new installed capacity of electricity was from renewable resources, and 91% of that was wind and solar energy [1]. Moreover, in 2017 the nominal peak power installed worldwide of solar PV was almost 405 GW, and wind energy installation was approximately 540 GW [2]. Obviously, the world tends to depend on renewable energy resources because of its reliability and environmentally friendly features, especially with the increased awareness towards global warming issues. Due to the rapid increase in the demand for clean energy, the utilization of the distributed generation (DG) by renewable energy resources has increased quickly, which has led to enhanced inverters technology to reduce the effects of the grid stability [3]. The residential PV systems are classified as stand-alone PV systems (off-grid) or grid-connected PV systems [4].

PV systems require an inverter in order to interface between the PV panels and the grid. The inverters are classified into galvanic isolated inverters and non-isolated inverters. In isolated inverters, the isolation can be achieved by a high-frequency DC side transformer or a low-frequency AC side transformer. The galvanic isolation serves to improve the overall system safety to achieve the corresponding safety standards required for grid-tied PV systems; at the same time, these transformers lead to bulky inverters with higher cost and lower efficiency [5,6]. Recently, for the residential market, transformerless inverters have been utilized due to their lower cost, higher efficiency, and smaller size [7]. The basic structure for the transformerless inverter was first presented in 1956 by McMurray, where he developed the Full Bridge FB or H-Bridge inverter family for the first time. The structure of an FB inverter can be seen in Figure 1 [8].

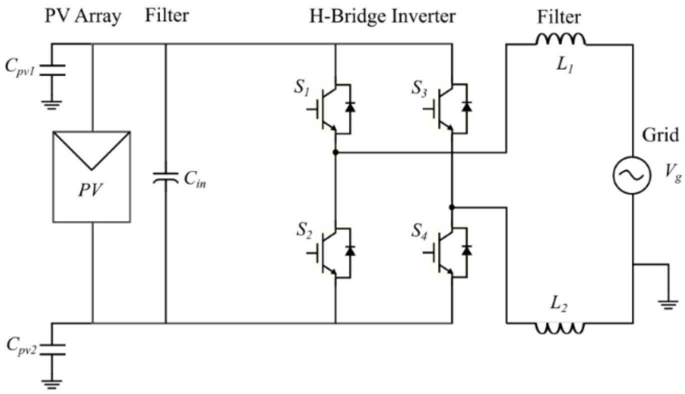


Figure 1. Full Bridge (FB or H-Bridge) structure of a transformerless inverter.

The H-Bridge structure has many drawbacks regarding safety; one limitation is the leakage current produced by the parasitic capacitance formed between PV panels and the ground. The leakage current is generated by the variation in common mode voltage (CMV), which leads to high leakage current and high electromagnetic interference (EMI) [9–11].

According to the VDE 0.126-1-1 standard, a leakage current over 30 mA must trigger a break within 0.3 s, while the leakage current range should not be more than 100 mA and the fault breaking time should not be more than 40 ms, as shown in Table 1 [12,13]. Additionally, the leakage current can be decreased by the type of modulation [14]. The leakage current path is shown in Figure 2, where $I_{Leakage}$ is the leakage current, C_{pv} the parasitic capacitance and C_{in} the DC bust coupling capacitor.

Table 1. Leakage current with discontinuity time according to VDE 0126-1-1.

Leakage Current (mA)	Fault Discontinuity Time (ms)
30	300
60	150
100	40

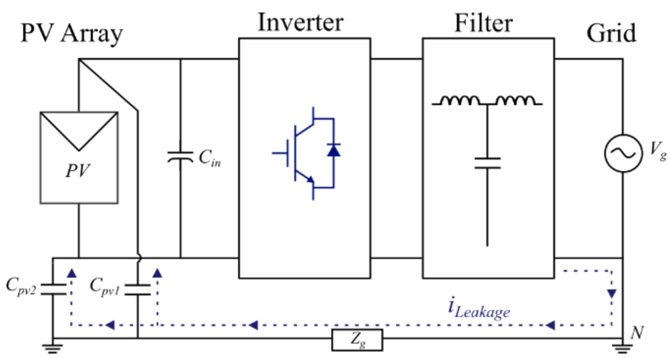


Figure 2. Common mode circuit.

Many transformerless inverter topologies have been proposed in the literature to increase the efficiency by reducing conduction losses, decreasing the CMV to satisfy grid requirements, and decreasing the number of components to reduce the costs and size [15]. One proposed inverter, called the neutral point clamped (NPC), which reduces the filter requirement, leakage current, and EMI, and a modified type of NPC called the Active NPC (ANPC), mitigate the limitations of NPC topology [16,17]. In 2005, SMA proposed a new inverter topology called H5, which reduces CMV through eliminating the high-frequency component of CMV by detaching the power grid from the PV module during the zero-voltage state [18]. Another popular transformerless inverter is the HERIC (Highly Efficient and Reliable Inverter Concept) inverter, developed by Sunways in 2006. It consists of six switches and is based on the AC decoupling method in order to isolate the output inductor filter from the PV panel parasitic capacitance and achieve unipolar SPWM [15]. Therefore, this topology leads to reduced leakage current and EMI, increasing the efficiency and reducing the size [19]. A new type of inverter with the theoretical elimination of the leakage current derived from the conventional H6 inverter was proposed in [20].

Another transformerless topology based on the common ground technology is introduced, which connects the grid ground to the PV panels ground permanently, resulting in constant CMV. Therefore, according to the capacitor current equation, the leakage current will be eliminated completely.

$$i_{CM} = C_{PV} \times \frac{dv}{dt} \tag{1}$$

where i_{CM} is the common mode leakage current, C_{PV} is the parasitic capacitance of the PV panel, and $\frac{dv}{dt}$ is the voltage variation across the parasitic capacitance. Based on the common ground method, a new concept was proposed in [6] in 2013, called the virtual DC bus, which is created by a flying capacitor. The virtual DC voltage supplies the negative current to the grid, while the positive current flows to the grid directly from the PV panel. However, in this topology, there are two or more switches in series during the active state which increases conduction losses and requires a relatively large capacitor, because it is charged only during the positive power cycle. A flying inductor inverter named after "Karschny" was proposed as a patent in [21], but it has no ability to deliver reactive power and is constructed with a large number of components. A new topology was proposed in [22] that charges the flying capacitor during the zero voltage state in both the positive and negative power cycle but has two extra diodes and one extra capacitor. Recently, a new topology proposed in [23] solved many of the drawbacks of previous types of transformerless inverters based on the flying capacitor, consisted of only four switches, one switch in series during active state, and proposed a modifying control method to lower the current stresses during the flying capacitor charging state. Additionally, it allows the capacitor to charge during the zero voltage state in both positive and negative power cycles, but it requires a bipolar blocking switch and still requires a relatively large capacitor.

This paper proposes a new transformerless inverter topology based on the common ground concept and virtual DC bus. The proposed transformerless inverter is constructed of a buck–boost converter, a two-switch inverter, and an extra two switches with two diodes to achieve freewheeling and the zero voltage state for unipolar SPWM. The buck–boost converter is utilized to supply the flying capacitor continuously, in all inverter operation states, with the required energy that will be utilized in the negative power cycle. The two switches deliver the power into the grid during the negative and positive power cycle and the freewheeling paths provide the output inductor freewheeling path and help in achieving a unipolar SPWM control scheme. The proposed inverter reduces conduction losses, only one switch in the current path during each active state, reducing the flying capacitor size and stresses and allowing the capacitor to charge during all operation states. Additionally, this eliminates the leakage current (theoretically) because of the common ground structure.

This paper is arranged as follows: Section 2 discusses the proposed topology and the principals of operation. Section 3 presents the operation modes and modulation technique.

All design equations and main component current stresses are discussed in Section 4. Discussion and simulation results are presented in Section 5. Last, Section 6 provides the conclusion.

2. Proposed Topology and Principle of Operation

The proposed topology can be subdivided into three subcircuits as shown in Figure 3: a buck–boost converter, a common ground flying capacitor, and the transformerless inverter, which contains two main switches in addition to two freewheeling switches with series diodes to generate the required unipolar SPWM.

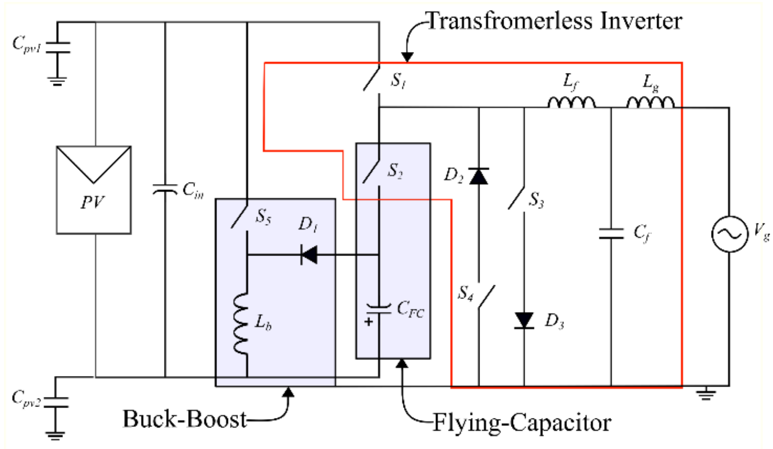


Figure 3. Proposed transformerless single-phase grid-tied inverter.

2.1. Buck–Boost Converter

The buck–boost converter is one of the basic converters that was used during the initial stages of the power electronics field. It works either to step-up or step-down the input voltage based on the duty cycle; if $D < 0.5$ the converter works in buck mode, while if $D > 0.5$ it presents the boost mode. It is an inverting converter in nature, where the converter output is negative with reference to the ground input. Figure 4 shows the buck–boost converter building blocks and its operation.

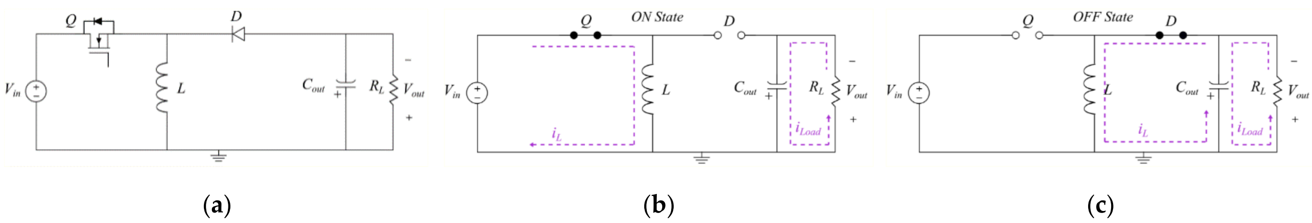


Figure 4. Buck–boost circuit and its operation: (**a**) buck–boost basic structure; (**b**) ON state circuit; (**c**) OFF state circuit.

During the ON state, Q is closed and D is open, as illustrated in Figure 4b. The current flows from the input supply into ground through the inductor L, while the output capacitor supplies the load current during this state. Figure 4c shows that during the OFF state Q becomes open and D closes, and again the inductor nature works since the current cannot be interrupted, such that the inductor becomes a current source and the charged energy in the inductor flows to charge the output capacitor and supply the load current. This charging and discharging takes place in every switching cycle. According to the inductor volt–second law, in steady state the average voltage applied on the inductor must be zero [24,25]. Applying the volt–second balance equation, the inductor average voltage equals

$$\langle V_L \rangle = \frac{1}{Ts} \int_0^{Ts} V_L(t) = 0 \tag{2}$$

$$\frac{Vout}{Vin} = \frac{D}{1-D} \tag{3}$$

Therefore, according to Equation (3), by controlling the duty cycle D we can generate the required inverted output voltage, which will be used in the proposed topology to charge C_{FC}.

2.2. Common-Ground Flying Capacitor

The flying capacitor concept was first introduced in DC–DC converters in a type of inductor-less converter called the charge pump (switched capacitor) DC–DC converter [26]. The basic idea behind using a flying capacitor in single-phase transformerless inverters was illustrated in [27] and is shown in Figure 5, where the capacitor is charged from the input voltage supply during a specific time by connecting the C_{FC} positive terminal to point 1 and the negative terminal to point 3. Afterwards, the flying capacitor positive terminal is connected to point 2 and negative terminal to point 4 to release the flying capacitor from the input supply positive terminal and generate a negative output voltage source to supply the load.

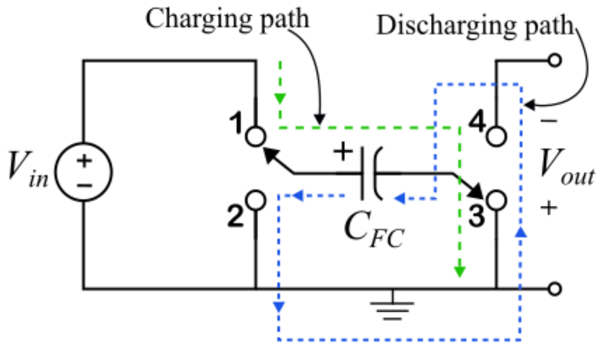


Figure 5. Illustration of flying capacitor operation.

Compared with the previously mentioned flying capacitor transformerless inverter topologies, the proposed topology presents a flying capacitor that can be charged at all times from the PV panel input, despite the inverter operation state, due to introduction of a buck–boost converter, as illustrated in Figure 6. Therefore, it requires only one switch to connect or disconnect the flying capacitor negative terminal, whereas the positive terminal is connected directly. This scheme allows the flying capacitor to charge continuously at a high frequency rate. Consequently, this leads to a smaller capacitor compared with other topologies that charge C_{FC} during the positive power cycle or freewheeling state (zero voltage state), but not during the negative power cycle (active). Moreover, this limits the charging inrush current flow into the flying capacitor due to the existence of the buck–boost inductor.

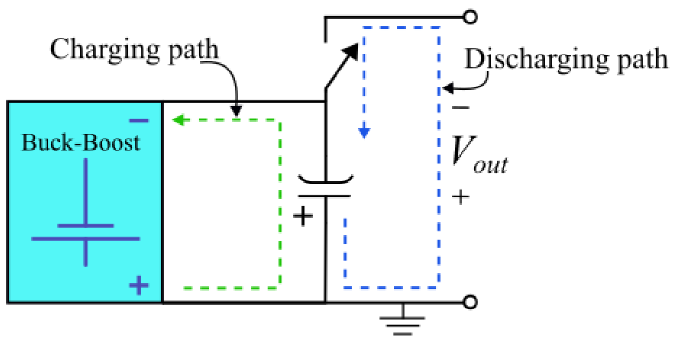
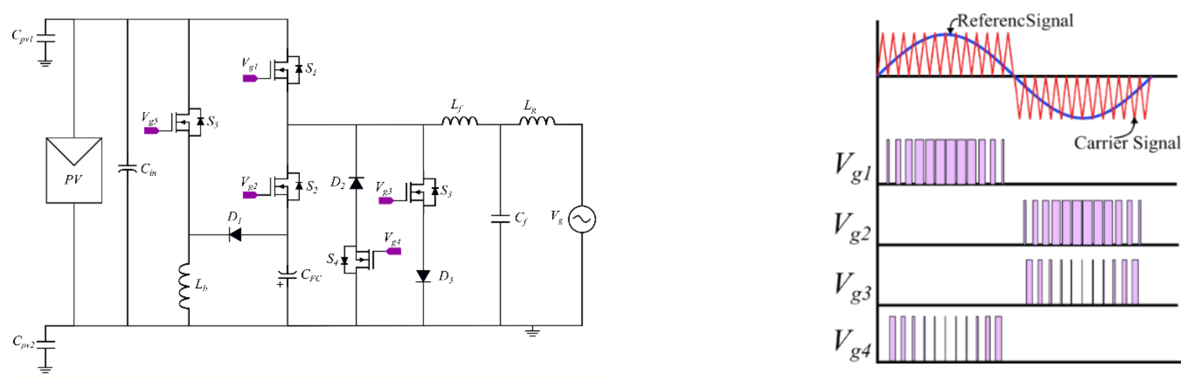


Figure 6. The proposed flying capacitor circuit.

2.3. Proposed Inverter Topology

Figure 7a presents the proposed topology, which includes five power switches (S_1, S_2 … S_5), three diodes (D_1, D_2 and D_3), one inductor (L_b) in the buck–boost configuration, and one flying capacitor (C_{FC}), in addition to the input DC link capacitor (C_{in}) and output LCL filter (L_f, L_g, C_f).



(**a**) (**b**)

Figure 7. The proposed transformerless inverter topology and its modulation technique: (**a**) the proposed transformerless inverter; (**b**) unipolar SPWM modulation signal.

The modulation technique shown in Figure 7b illustrates that in this topology, only one switch carries the load current during each power cycle; S_1 creates the positive power cycle (active state) whilst S_2 creates the negative power cycle (active state). The switches S_4 with D_2 and S_3 with D_3 work in a complementary manner with S_1 and S_2, respectively, to achieve the zero voltage level (non-active states) in the output and allow the output inductor L_f to achieve current freewheeling. Power switch S_5 works continuously to supply the power from the input side to the flying capacitor, utilizing the inductor L_b assisted by the diode D_1 in buck–boost mode. In order to reduce the passive component sizes, MOSFET switches are adopted to achieve higher frequency. Furthermore, SiC MOSFETs can be used because of their low switching losses and fast recovery of the body diode compared with conventional Si MOSFETs. Figure 7b illustrates the unipolar SPWM modulation technique used in the proposed inverter. Two sinusoidal signals are generated by 180° phase shift between each other as a reference waves (generated from the grid voltage in grid-tied inverters) and compared with triangle signal to generate required pulses. In the unipolar SPWM scheme $+V_{dc}$, 0 and $-V_{dc}$ voltage levels generated in the inverter output consequently it reduces the overall losses, required output filtration and EMI [28].

3. Operating Modes of the Proposed Inverter

As described in Section 2 the proposed topology is modulated using unipolar SPWM technique. Hence, based on that the operation of the proposed inverter is divided into positive half power cycle and negative half power cycle and each half of the power cycle has two modes of operation either active state or zero state. These four operation modes are described in this section.

3.1. Positive Cycle (Active)

The switch S_1 is switched at the gate-switching frequency generated by the modulated positive sinusoidal reference signal during the whole positive cycle. Figure 8 shows that during this state only S_1 is conducted and carries the load current, while switches S_2, S_3, and S_4 are maintained in the OFF state. Consequently, this reduces the conduction losses significantly, since only one switch in series is in the current path, represented by the blue dotted line in Figure 8. The switch S_2 experience $+2V_{dc}$ voltage, while the voltage across S_3 is $+V_{dc}$. Furthermore, during this mode, buck–boost switch S_5 conducts at high switching frequency, working as a conventional buck–boost converter with the assistance of the diode

D_1 and the inductor L_b to precharge the flying capacitor C_{FC} for the negative power cycle (the red dotted line presents the current path when S_5 is ON (i_{L_ON}) and the green dotted line shows the current path when S_5 is OFF (i_{L_OFF})).

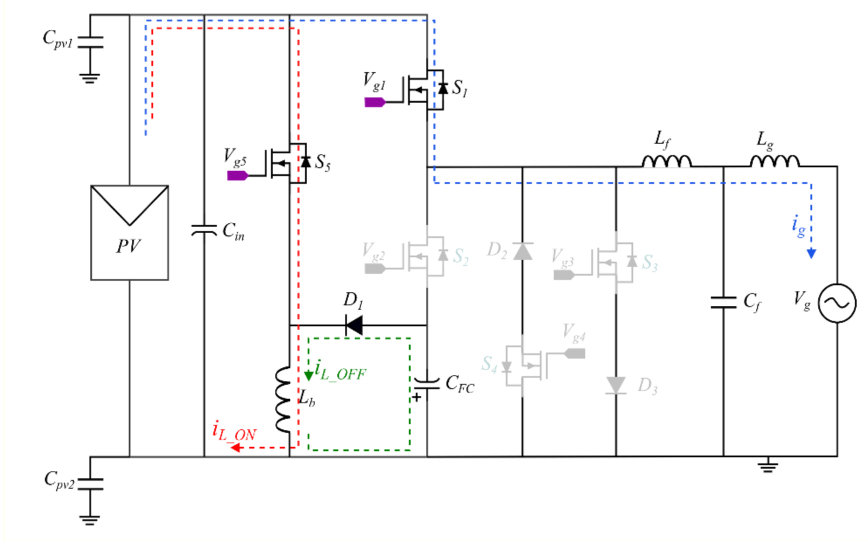


Figure 8. Positive power cycle (active) operating mode of the proposed transformerless inverter.

3.2. Positive Cycle (Zero State)

During this mode of operation, S_4 and D_2 conduct and S_4 is ON, while S_1, S_2, and S_3 are OFF during this operation mode. Thus, zero voltage is created across the output filter to achieve unipolar voltage across the output filter as required. This mode is illustrated in Figure 9, which shows the active devices during this mode of operation. Switches S_1 and S_2 experience equal voltage stresses $+V_{dc}$. The buck–boost circuit keeps running and continues charging the flying capacitor for the negative power cycle if needed.

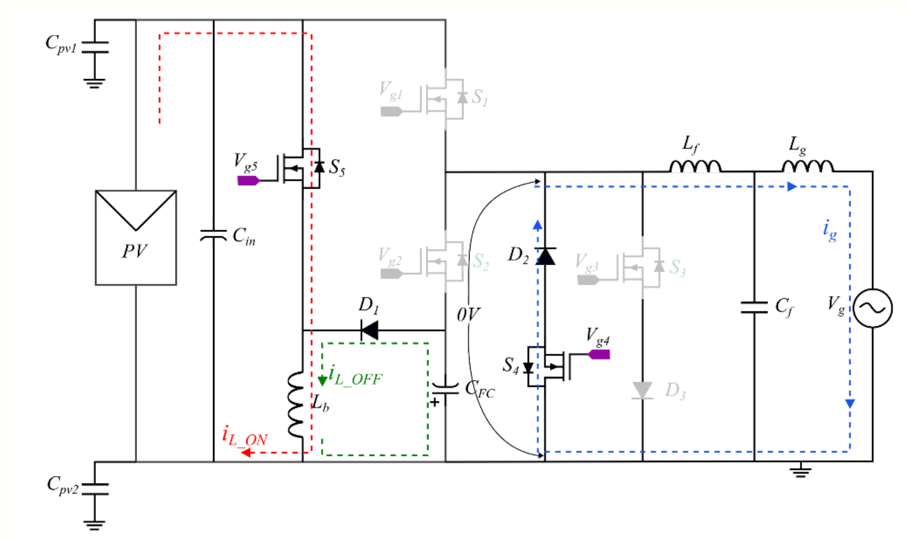


Figure 9. Positive power cycle (zero state) operating mode of the proposed transformerless inverter.

3.3. Negative Cycle (Active)

Figure 10 shows the proposed inverter configuration during this mode of operation. The flying capacitor starts discharging and works as a voltage source to supply the required negative current to the grid by activating the switch S_2 to the ON state. All other three switches of the inverter, S_1, S_3, and S_4, are OFF. Hence, only one switch in the current path conducts. In this mode, $+2V_{dc}$ voltage stress is experienced across S_1, while S_4 experiences the flying capacitor voltage $+V_{dc}$ across it. A unique feature is presented in this mode which does not exist in similar topologies in the literature. During the active negative cycle, once the flying capacitor starts to discharge the buck–boost circuit compensates for that discharged energy simultaneously by charging the flying capacitor C_{FC} to keep the required voltage level. As a result, this helps to minimize the flying capacitor size significantly. At the same time, it prevents current spikes and reduces the current stress experienced by the capacitor when it is discharged deeply then recharged.

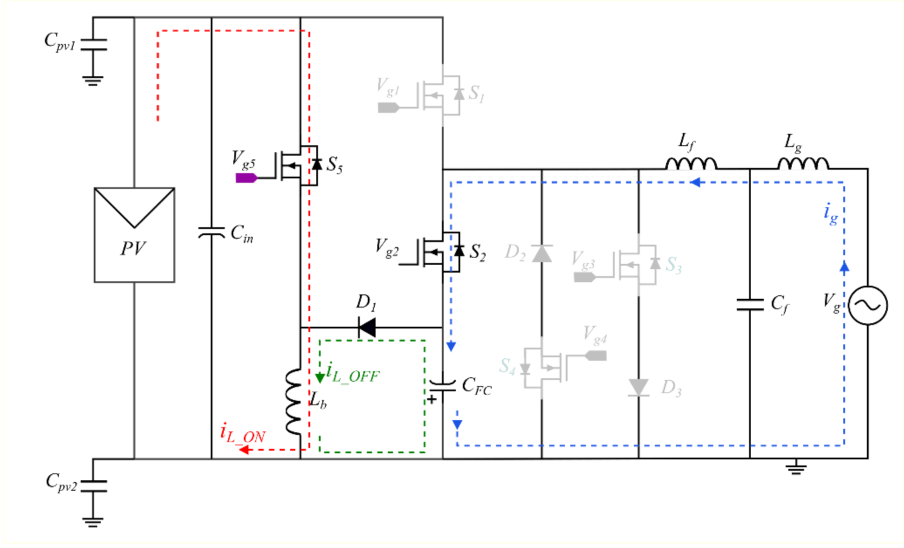


Figure 10. Negative power cycle (active) operating mode of the proposed transformerless inverter.

3.4. Negative Cycle (Zero State)

The operation of this mode is shown in Figure 11. The circuit operates in a similar manner to the positive cycle (zero state). Thus, switch S_3 is ON whilst S_4 is OFF. Hence, S_3 and D_3 conduct the freewheeling current in this mode. Throughout this operating mode, both S_1 and S_2 experience $+V_{dc}$ voltage stress. The buck–boost circuit continues to precharge the flying capacitor for the negative active mode whenever required.

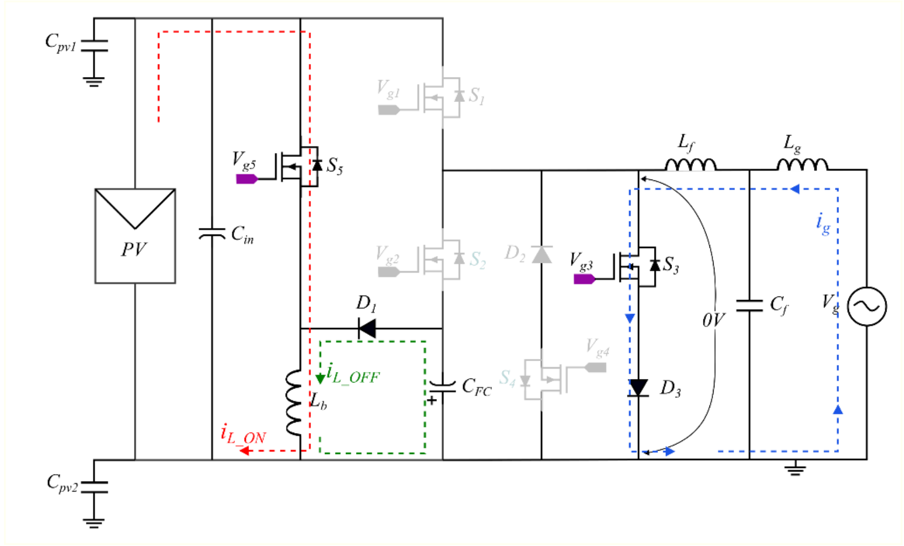


Figure 11. Negative power cycle (zero state) operating mode of the proposed transformerless inverter.

The aforementioned four modes of operation show the active switches in each mode and they continue repeating after each other. They verify the ability of the proposed inverter to generate a unipolar output voltage, V_{an}, which is thereafter filtered out by the

LCL filter to obtain the pure sinusoidal voltage and current in the grid. In addition, it shows that during the active states only one switch carries the load current, which reduces the conduction losses. The buck–boost circuit operates throughout all modes, even in the negative cycle (active) mode, as illustrated previously. This exhibits one advantage of the proposed transformerless inverter topology by reducing the flying capacitor size, in addition to limiting the charging current due to the existence of the inductor L_b in the charging path. Table 2 shows a comparative summary of the proposed topology alongside the similar inverters in [23] and [27].

Table 2. Comparative table between the proposed inverter and similar inverters.

Inverter Topology in [27]	Inverter Topology in [23]	The Proposed Inverter
Two switches in series carry the load current during the active states of the positive and negative power cycles.	Only one switch carries the load current during the active states of the positive and negative power cycles.	Only one switch carries the load current during the active states of the positive and negative power cycles.
It does not charge the flying capacitor during the active state of the negative power cycle.	It does not charge the flying capacitor during active states.	It charges the flying capacitor during all operating states.
No RB-IGBT required.	It required two switches with bipolar voltage-blocking capability, such as RB-IGBT.	No RB-IGBT required.
No proposed way to control or reduce the inrush current during the charging of the flying capacitor	The inrush current during the charging of the flying capacitor cannot be fully controlled; it ranges from 2 Iac, max to 5 Iac, max	In the proposed inverter, the flying capacitor charging current can be controlled using the buck–boost inverter because the capacitor charges through the inductor. Based on the nature of the inductor, in that it tries to oppose the current change, the slope of the current can be controlled. $I_{max} = \frac{I_o}{1-D}\left(1+\frac{r}{2}\right)$ where I_o is the output current of the buck–boost inverter, in this case I_{ac_max}, D the duty cycle, and r the ripple ratio. Hence, the maximum current can be controlled by inductor value because $r = \frac{V_{on}\ D}{L\ I_L f}$

4. Design Guidelines and Loss Analysis

Brief design guidelines and loss analysis are presented in this section to assist in the selection of the proposed transformerless inverter components and its thermal management by estimating heat losses.

4.1. Buck–Boost Components Selection

Brief guidelines to select the buck–boost circuit components are illustrated. Based on the average method analysis of the inductor in steady state, the value of the inductor can be obtained as

$$L = V_L\frac{\Delta T}{\Delta I} = \frac{V_{on}DT}{\Delta I} = \frac{V_{on}\ D}{\Delta I\ f} \tag{4}$$

where V_{on} is the voltage across the inductor in the ON state, D the duty cycle which can be calculated by Equation (3), ΔI the current ripple, and f the switching frequency. Defining a ripple ratio factor r with an optimum value of 0.4 achieves a trade-off between inductor size and output capacitor current stress [29].

$$\Delta I = rI_L \tag{5}$$

where I_L is the average current of the buck–boost inductor and I_o is the output current. Substituting (5) into (4), the value of the inductor will be

$$L = \frac{V_{on}\, D}{r\, I_L\, f} \tag{6}$$

The buck–boost diode average current and switch RMS current are addressed in Equations (7) and (8), respectively, while the voltage blocking capability must be at least rated as $2Vdc$ for both devices

$$I_D = I_o \tag{7}$$

$$I_{sw\_rms} = I_L \sqrt{D\left(1 + \frac{r^2}{12}\right)} \tag{8}$$

The flying capacitor (output capacitor of the buck–boost) is sized here based on the rated RMS current, because the voltage ripple requirement is not critical in this application; therefore

$$I_{cout\_rms} = I_o \sqrt{\frac{D + \left(\frac{r^2}{12}\right)}{1 - D}} \tag{9}$$

where I_{cout_rms} is the conventional buck–boost output capacitor RMS current. Since the flying capacitor is discharged only in the negative half cycle in the proposed inverter, the RMS current of the flying capacitor $I_{C_{FC}\_rms}$ can be averaged to

$$I_{C_{FC}\_rms} \approx \frac{I_{cout\_rms}}{2} \tag{10}$$

4.2. Inverter Compoenents Selection

Based on the power switch voltage stresses mentioned in Section 3, the discrete devices of the inverter, S_1 and S_2, must be rated to withstand at least $+2V_{dc}$, while S_3 and S_4 must be rated for $+V_{dc}$ voltage. Neglecting the phase shift caused by the output filter inductor, the duty cycle $d(t)$ and grid current $i_g(t)$ can be described as follows [6]

$$d(t) = D_m \sin(\omega t) \tag{11}$$

$$\langle i_g(t) \rangle = I_m \sin(\omega t) \tag{12}$$

where D_m is the maximum duty cycle, I_m is the amplitude of the output current, $\langle\rangle$ denotes the average value over the grid switching period T_g, and ω is the grid angular frequency. Accordingly, the current stresses of the power switches can be averaged over the grid switching cycle as

$$\langle i_{S1}(t) \rangle = d(t)\langle i_g(t) \rangle, \text{ from } 0 \; to \; \frac{T_g}{2} \tag{13}$$

$$\langle i_{S2}(t) \rangle = d(t)\langle i_g(t) \rangle, \text{ from } \frac{T_g}{2} \; to \; T_g \tag{14}$$

$$\langle i_{S3}(t) \rangle = d(t)_{zero}\langle i_g(t) \rangle, \text{ from } \frac{T_g}{2} \; to \; T_g \tag{15}$$

$$\langle i_{S4}(t) \rangle = d(t)_{zero}\langle i_g(t) \rangle, \text{ from } 0 \; to \; \frac{T_g}{2} \tag{16}$$

The duty cycle during the zero state denoted by $d(t)_{zero}$ is complementary to $d(t)$

$$d(t)_{zero} = 1 - d(t) = 1 - D_m \sin(\omega t) \tag{17}$$

The input capacitor of the DC bus can be sized based on the method suggested in [30] as

$$C_{in} = \frac{P}{2\omega\ V_{dc}\ \Delta V} \tag{18}$$

Note that V_{dc} is the DC bus voltage, P the power of the inverter, and ΔV is the maximum permissible voltage ripple. The final part of the proposed topology is the LCL stage filter, which can be designed based on the analytical method suggested in [31]

$$L_f = \frac{V_{dc}}{8\ f_{sw}\ ripple\%\ I_m} \tag{19}$$

$$C_f = \frac{x\ P}{\omega\ V_{o\_rms}{}^2} \tag{20}$$

where L_f is the filter inductor in the inverter side, f_{sw} is the switching frequency, $ripple\%$ the inductor current ripple ratio required, x is the reactive power percentage absorbed by the filter capacitor, the typical value of which is 0.05, and V_{o_rms} is the RMS output voltage of the inverter. Then, the grid side inductor L_g can be designed based on the methodologies recommended in [31–33], to limit the inverter output current harmonics according to IEEE 519-1992 and ensure system stability.

$$r_{att} = \left| \frac{\frac{1}{I_{att}} - 1}{1 - L_f (2\pi f_{sw})^2 C_f x} \right| \tag{21}$$

$$L_g = r_{att} L_f \tag{22}$$

where I_{att} is the attenuation factor to achieve the required LCL resonance and r_{att} is the ripple attenuation.

4.3. Power Loss Analysis

The efficiency of the transformer is generally assessed using weighted efficiency, using measures such as CEC efficiency or EU efficiency. Therefore, the power loss in the power semiconductors of the proposed inverter is addressed in this part. Losses can be classified into conduction and switching losses. The average conduction power P_{con} can be expressed as the voltage drop across the device multiplied by the passing current over the switching period. A comprehensive power loss analysis was carried out in [34,35]. It is recommended to use MOSFETs in the proposed inverter, and so

$$V_{on\_mos} = i(t)\ R_{ds} = \langle i_g(t) \rangle\ R_{ds} \tag{23}$$

where V_{on_mos} is the voltage drop in the MOSFET during conduction, $i(t)$ is the current passing through the MOSFET, and R_{ds} is the MOSFET resistance. Hence, the power conduction losses are

$$P_{con\_S1} = \frac{1}{T_g} \int_0^{\frac{T_g}{2}} |V_{on\_mos1}\ i_{S1}(t)| dt \tag{24}$$

where $i_{S1}(t)$ is the current in S_1 during conduction and P_{con_S1} is the average power conduction loss in S_1; since $i_{S1}(t)$ is almost unchanged in a switching cycle, the switching cycle averaging method can be utilized, and thus by substituting $\langle i_{S1}(t) \rangle$, this yields

$$P_{con\_S1} = \frac{1}{T_g} \int_0^{\frac{T_g}{2}} |V_{on\_mos1}\ \langle i_{S1}(t) \rangle| dt \tag{25}$$

Substituting (12) into (13), then (13) and (23) into Equation (25), we obtain

$$P_{con\_S1} = \frac{1}{T_g} \int_0^{\frac{T_g}{2}} \left| D_m I_m{}^2 R_{ds} \sin^3(\omega t) \right| d\omega t \tag{26}$$

Solving (26) and substituting $T_g = 2\pi$ yields

$$P_{con\_S1} = \frac{2D_m {I_m}^2 R_{ds}}{3\pi} \tag{27}$$

A similar analysis was carried out for the power switches S_2, S_3, and S_4, which yields (28), (29), and (30), respectively, as follows

$$P_{con\_S2} = \frac{1}{T_g}\int_{\frac{T_g}{2}}^{T_g} |V_{on\_mos2}\ i_{S2}(t)\ d(t)|dt = \frac{2D_m {I_m}^2 R_{ds}}{3\pi} \tag{28}$$

$$P_{con\_S3} = \frac{1}{T_g}\int_{\frac{T_g}{2}}^{T_g} |V_{on\_mos3}\ i_{S3}(t)\ d(t)_{zero}|dt = {I_m}^2 R_{ds}\left\{\frac{1}{4} - \frac{2D_m}{3\pi}\right\} \tag{29}$$

$$P_{con\_S4} = \frac{1}{T_g}\int_{0}^{\frac{T_g}{2}} |V_{on\_mos4}\ i_{S4}(t)\ d(t)_{zero}|dt = {I_m}^2 R_{ds}\left\{\frac{1}{4} - \frac{2D_m}{3\pi}\right\} \tag{30}$$

Furthermore, in the freewheeling period, the current passed through the diodes D_2 in the positive cycle and D_3 in the negative cycle, and the conduction loss of the diode can be obtained as

$$V_{on\_diode} = V_f + i(t)\ R_d \tag{31}$$

$$P_{con\_d} = \frac{1}{T_g}\int_{0}^{\frac{T_g}{2}} |V_{on\_diode}\ i(t)\ d(t)_{zero}|dt \tag{32}$$

where V_{on_diode} is the diode voltage drop during conduction, V_f is the diode forward voltage, R_d is the diode resistance, $i(t)$ the current through the device, and P_{con_d} the average diode conduction power loss. Substituting (31) into (32) yields Equation (33), and solving for $T_g = 2\pi$ and $i(t) = \langle i_g(t)\rangle$ results in (34) as follows

$$P_{con\_d} = \frac{1}{T_g}\int_{0}^{\frac{T_g}{2}} \left|\left(V_f + i(t)\ R_d\right)\ i(t)\ d(t)_{zero}\right|dt \tag{33}$$

$$P_{con\_d} = \frac{V_f\ I_m}{2\pi}\left\{2 - \frac{\pi D_m}{2}\right\} + \frac{{I_m}^2 R_d}{2\pi}\left\{\frac{\pi}{2} - \frac{4D_m}{3}\right\} \tag{34}$$

The other losses experienced by the devices are the switching losses caused by the MOSFET's transition states and the reverse recovery of the antiparallel body diodes. However, here, the MOSFET's switching losses are considered while the reverse recovery diode loss is ignored by assuming SiC MOSFETs are used, which have a very fast recovery time. Therefore, the average switching losses can be estimated as follows

$$P_{on} = \left(\frac{E_{on}}{V_{test}\ I_{test}}\right)\left(\frac{I_m\ V_{dc}}{2\pi}\right) f_{sw} \tag{35}$$

$$P_{off} = \left(\frac{E_{off}}{V_{test}\ I_{test}}\right)\left(\frac{I_m\ V_{dc}}{2\pi}\right) f_{sw} \tag{36}$$

where P_{on} and P_{off} are the ON average switching losses and OFF average switching losses, respectively, and E_{on} and E_{off} are the ON and OFF energy losses, respectively, which were measured under specific conditions with V_{test} and I_{test}. These values can be obtained from the device datasheet. f_{sw} is the switching frequency, I_m the current amplitude, and V_{dc} the bus voltage. Accordingly, the losses in the buck–boost circuit can be estimated as

$$P_{b\_con\_d} = I_o\ V_f \tag{37}$$

$$P_{con\_S5} = {I_{sw\_rms}}^2\ R_{ds} \tag{38}$$

$$P_{sw\_S5} = \left(E_{on} + E_{off}\right)\left(\frac{I_{m\_S5}\ 2V_{dc}}{V_{test}\ I_{test}}\right) f_{sw} \tag{39}$$

where $P_{b\_con\_d}$ is the buck–boost diode conduction loss, I_{m_S5} is the current amplitude through switch S_5, and P_{con_S5} and P_{sw_S5} are the S_5 conduction and switching losses, respectively. For simplicity, the worst-case losses are calculated in Equations (37)–(39), assuming a conventional buck–boost converter which needs to supply the load at all times, although in the proposed inverter it needs to supply the load during the negative half cycle only; thus, the definite losses are less than the calculated.

5. Simulation Results and Discussion

PSIM software was used to simulate the proposed inverter and evaluate its performance. The parameters used in the simulation are shown in Table 3.

Table 3. System design parameters used for the simulation.

Parameters	Value
DC Bus Input Voltage V_{dc}	400 Vdc
Grid Voltage V_g	220 Vac
Grid Frequency f_g	60 Hz
Switching Frequency f_{sw}	60 kHz
PV Array Parasitic Capacitance (C_{PV1}, C_{PV2})	80 nF
Rated Power	2 kW
Output Current (peak) I_g	12.86 A
Flying Capacitor C_{FC}	330 µF
Buck–Boost Inductor L_b	870 µH
Inverter Side Filter L_f	860 µH
Grid Side Filter L_g	280 µH
Filter Capacitor C_f	4.7 µF
Switches	C3M0021120K
Diodes	C4D20120A

As can be seen in Figure 12, the stresses on the switches are in accordance with the theoretical stresses mentioned in Section 3, where the maximum drain to source voltage across switches S_1 and S_2 equals $+2V_{dc}$, and across S_3 and S_4 equals $+V_{dc}$, whilst the buck–boost switch and diode voltage stresses equal $+2Vds$. Thus, switches S_1, S_2, S_5, and D_1 must be rated with the ability to withstand at least double the input voltage, and switches S_3 and S_4, as well as diodes D_2 and D_3, must be rated to withstand at least the input voltage.

The flying capacitor voltage V_{FC} waveform shown in Figure 13 represents a stable voltage during all periods of inverter power cycles. It presents the advantage of the buck–boost circuit in the proposed inverter topology, where it can charge the capacitor at all times irrespective of the inverter mode of operation. This leads to the minimization of the size of the flying capacitor (330 µF) as compared with similar inverters that utilize the flying capacitor concept, and it reduces the current spikes experienced by the other topologies that charge the flying capacitor directly without limiting the current, as achieved in the proposed topology by the buck–boost inductor. Another feature of this proposed inverter is shown in Figure 14: CMV is clamped to a constant value (400 V) across C_{PV1}; therefore, the leakage current is almost eliminated, and only a negligible current value of 57 nA rms is flowing in the circuit, as seen in Figure 14a,b. On the other hand, Figure 14c,d show the CMV and leakage current through the parasitic capacitance C_{PV2}. It is noted that CMV is 0 V and the leakage current is eliminated completely.

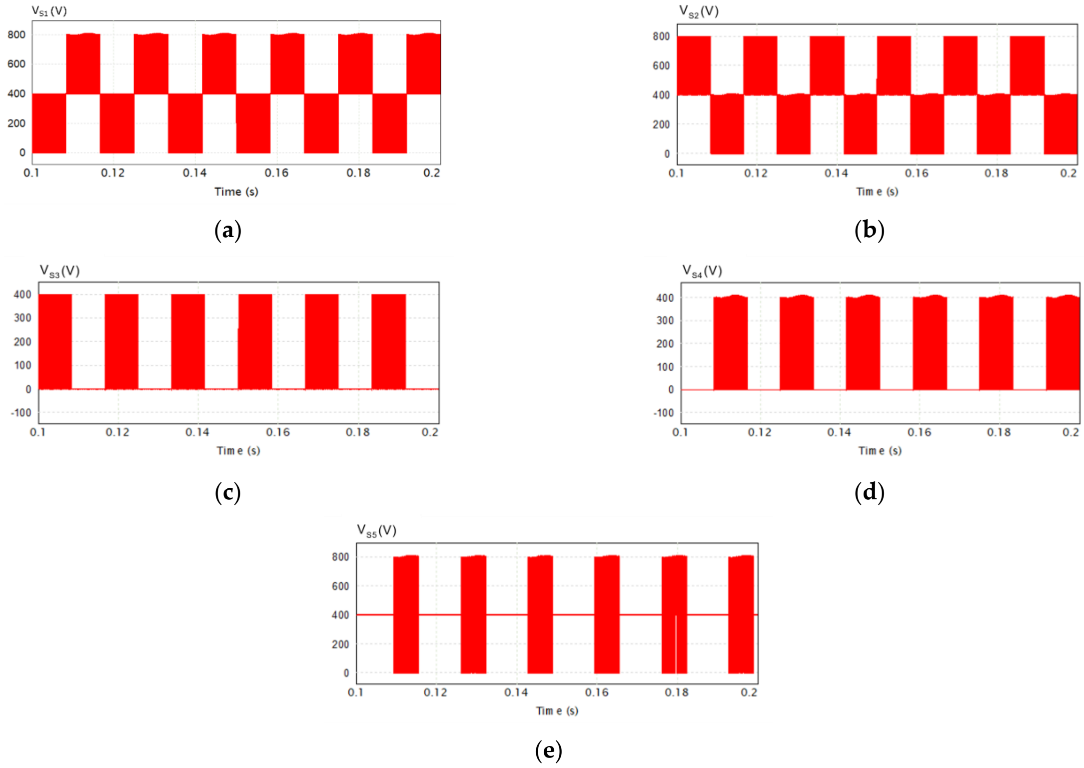


Figure 12. The simulation results of the voltage stresses on the switches: (**a**) S_1; (**b**) S_2; (**c**) S_3; (**d**) S_4; (**e**) S_5.

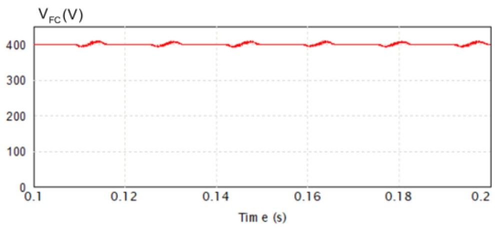


Figure 13. Waveform of the flying capacitor voltage C_{FC}.

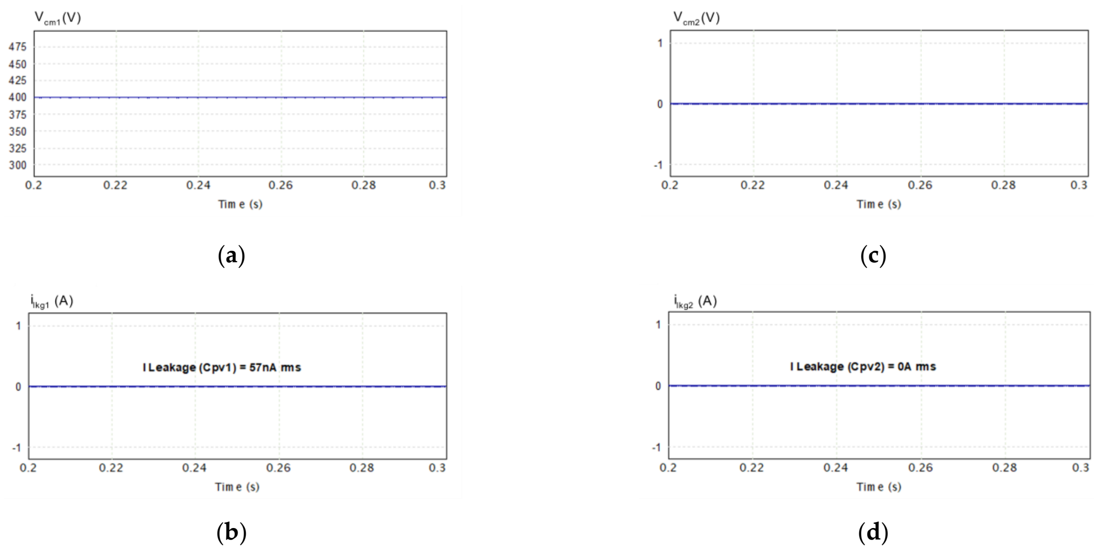


Figure 14. Common mode voltages and leakage currents across the parasitic capacitances of the PV array: (**a**) CMV across C_{PV1}; (**b**) leakage current in C_{PV1}; (**c**) CMV across C_{PV2}; (**d**) leakage current in C_{PV2}.

The isolation is guaranteed by the high impedance of the parasitic capacitance between the PV panel's body and the ground. Therefore, for the DC bus voltage supplied by the PV panels, there are only high-frequency voltage harmonics; thus, the parasitic capacitance impedance is very high, as shown in Equation (40).

$$X_{cpv} = \frac{1}{j\omega C_{PV}} \tag{40}$$

Regarding the voltage harmonics caused by switching the MOSFETs at high frequency, they are eliminated in the proposed topology by clamping the common mode voltage to a constant value, inputting DC bus voltage for C_{PV1} and the ground for C_{PV2}. For this reason, there is almost no leakage current, as shown in Equation (1). Furthermore, the input voltage has no limitations as long as the selected switches and other components in the inverter can tolerate that voltage. Consequently, the proposed topology can be used at higher voltages, given that the semiconductors can tolerate that voltage and can comply with the standard norms in terms of leakage current requirements.

The current stresses represented in the simulated waveform of Figure 15 illustrate the current experienced by each semiconductor switch of the proposed transformerless inverter during the positive and negative power cycles, in addition to the freewheeling period (zero voltage state). Figure 15a shows that S_1 carries the current injected to the grid Ig during the positive cycle (active), while S_2 carries I_g in the negative cycle (active), as can be seen in Figure 15b. Additionally, Figure 15c,d exhibit the simulation waveforms of the currents carried by S_3 and S_4 during the positive and negative freewheeling cycles to permit output inductor current freewheeling and achieve the zero voltage state for unipolar SPWM.

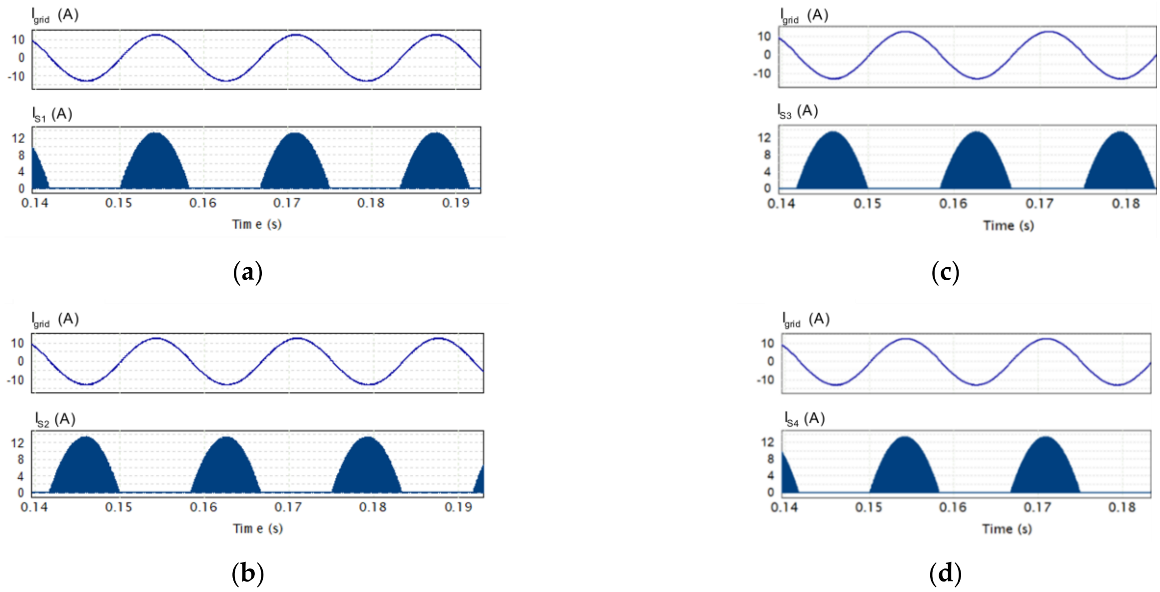


Figure 15. Current stresses in the semiconductor switches compared with grid current I_g: (**a**) S_1; (**b**) S_2; (**c**) S_3; (**d**) S_4.

As illustrated in Figure 16, the unipolar SPWM modulation technique is achieved. The simulated waveform V_{an} presents $+V_{dc}$ and *0 V* in the positive power cycle and $-V_{dc}$ and *0 V* during the negative power cycle. Hence, the three states required to implement the unipolar SPWM are conducted at $+V_{dc}$, $-V_{dc}$, and *zero* voltage. Therefore, the proposed inverter generates a unipolar output voltage, which reduces the current ripple and filter inductor losses. Hence, smaller filter inductors are required as compared to other topologies with the bipolar SPWM modulation technique. The grid voltage and currents of the simulated proposed inverter topology are illustrated in Figure 17. A sinusoidal voltage waveform with very low distortion is presented in the grid side V_g. The simulated waveforms show a unity power factor, whereby the currents are in phase with the grid voltage. Figure 17a shows the grid voltage V_g with the inverter side current I_{inv} before the LCL output filter. As shown in Figure 17a, it contains some distortion, while Figure 17b shows V_g with the injected grid current I_g after the LCL, where the effect of the LCL filter is shown clearly in smoothening the grid current I_g. The performance of the proposed transformerless inverter is evaluated in terms of the efficiency using the power loss calculations mentioned in Section 4 and compared with the simulated results obtained using the PSIM thermal module. There is a slight difference between the simulation and theoretical results, as shown in Figure 18. This is mainly due to the approximation made in simplifying the power loss equations of the buck–boost circuit, as explained previously.

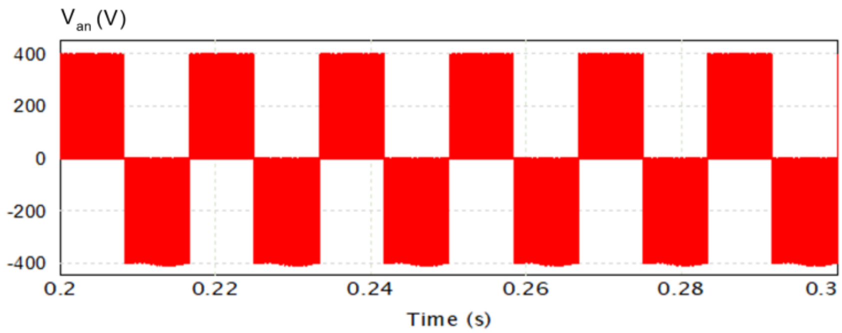


Figure 16. Output voltage of the proposed inverter V_{an}.

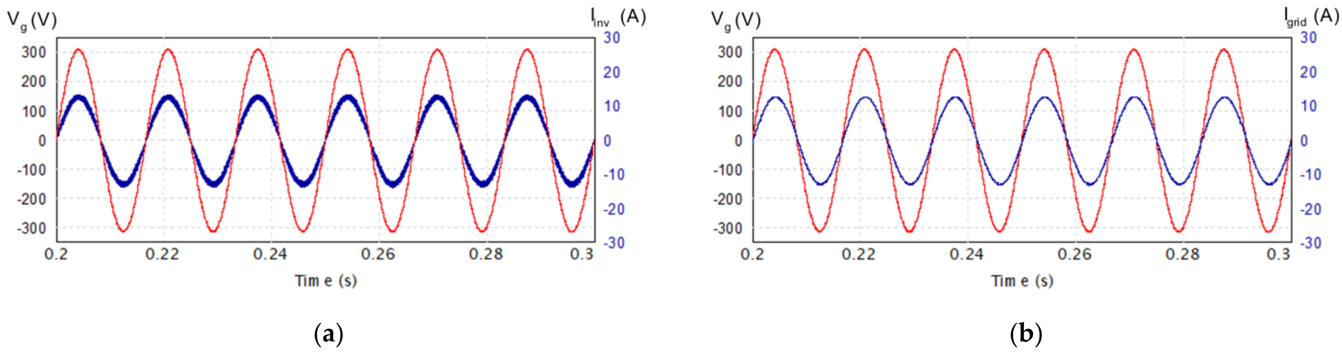


Figure 17. Grid voltage and injected current before and after LCL filter: (**a**) simulated grid voltage V_g with inverter side current I_{inv}; (**b**) simulated grid voltage V_g alongside grid current I_g.

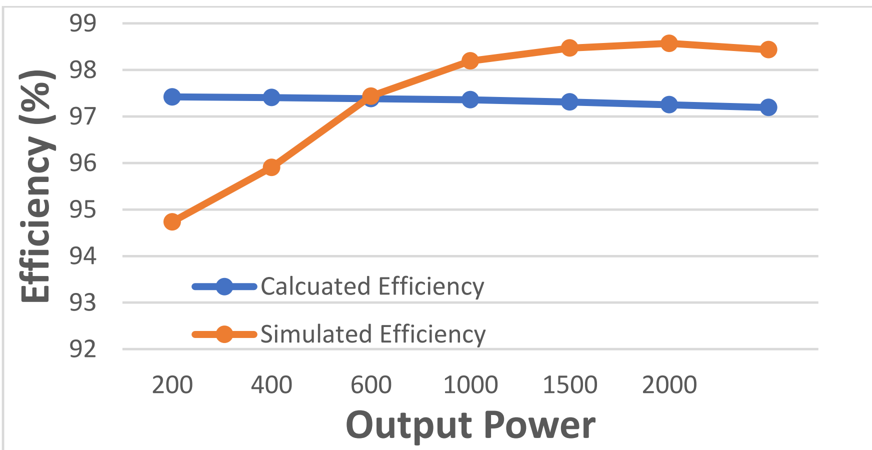


Figure 18. The efficiency of the proposed transformerless inverter.

The weighted efficiency was calculated according to California Energy Commission (CEC). The value was found to be 97.29% and 98.33% for the calculated and simulated efficiency, respectively. The CEC equation is given by

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (41)$$

There are two circuit configurations that can be implemented in the freewheeling path of the inverter, either using two branches consisting of two MOSFETs with external diodes, as suggested in the proposed topology, or using one branch consisting of two MOSFETs and utilizing the internal antiparallel diodes. Each circuit has its own pros and cons. Both configurations are shown in Figure 19.

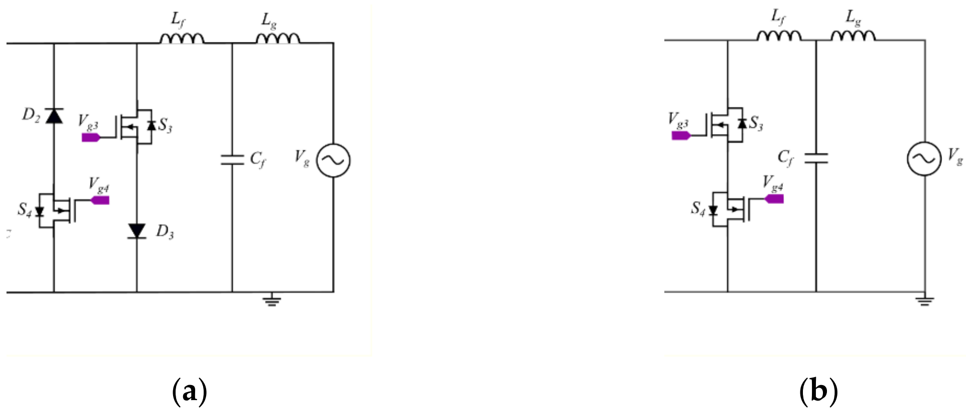


Figure 19. Freewheeling path circuit configurations; (**a**) two branches including two MOSFETs with external diodes, as suggested in the proposed inverter; (**b**) one branch with two MOSFETs.

The circuit shown in Figure 19a was chosen in the proposed topology over the circuit in Figure 19b, because it would increase the efficiency of the inverter. The antiparallel diodes in the MOSFETs, in particular, SiC, have much higher forward voltage compared with external SiC diodes, which have low forward voltage. Consequently, the efficiency of the system is increased when using external diodes at the expense of adding more devices and increasing the cost. Figure 20 shows the efficiency of the proposed inverter if using a one-branch circuit, as shown in Figure 19b.

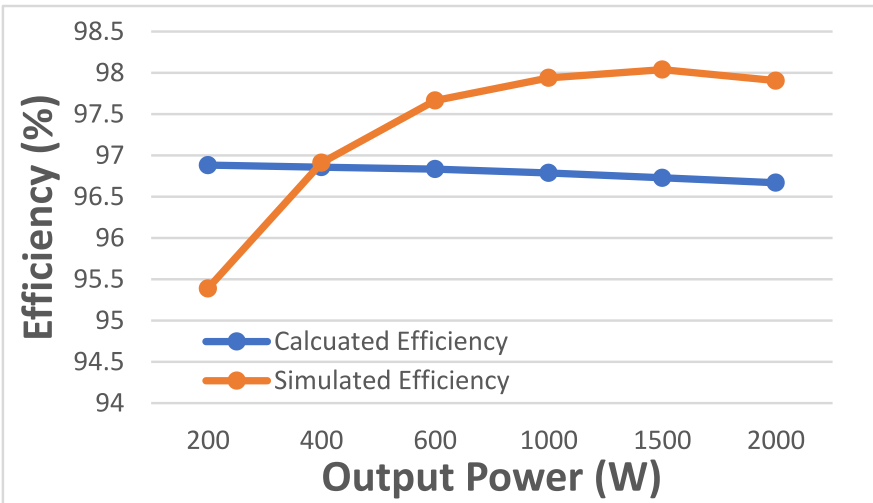


Figure 20. The efficiency of the transformerless inverter using the freewheeling circuit in Figure 19b.

The weighted efficiency was determined according to CEC. It was found to be 96.76% and 97.8% for the calculated and simulated efficiency, respectively. This is less efficient compared with the efficiency of the proposed circuit, as can be seen in Figure 18.

6. Conclusions

In this paper, a flying capacitor buck–boost transformerless inverter was proposed for single-phase grid-connected PV systems. The proposed topology differs from the similar types in the literature by its ability to charge the flying capacitor continuously, even in the negative power cycle (active). Thus, it can minimize the size of the flying capacitor and prevents an inrush current when charging the flying capacitor due to the existence of the inductor in the buck–boost circuit. The performance of the proposed inverter was verified using a PSIM simulation, which showed that the results are consistent with the theoretical analysis that was carried out. In general, the proposed transformerless inverter eliminates the leakage current, reduces the losses, and reduces the flying capacitor size and filtration requirement due to unipolar SPWM modulation. The efficiency of the proposed inverter was evaluated at 2 kW rated power using theoretical calculations and simulation results, and showed a CEC efficiency of 97.29% and 98.33%, respectively. However, it may suffer buck–boost circuit losses at powers greater than 2 kW; in particular, the switching losses. SiC devices were used in the evaluation of the proposed inverter and they are recommended to be used in their design, because of their lower switching losses at higher frequency which contribute to reduce the size of passive components. Moreover, for further efficiency enhancement, external SiC diodes were used instead of the MOSFETs antiparallel body diodes in the freewheeling path.

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