applied sciences

MDPI

Article

A High Gain Modified Quadratic Boost DC-DC Converter with Voltage Stress Half of Output Voltage

Anindya Sundar Jana [1], Chang-Hua Lin [1,*], Tzu-Hsien Kao [1] and Chun-Hsin Chang [2]

[1] Department of Electrical Engineering, National Taiwan University of Science & Technology, Taipei 106, Taiwan; d10907808@mail.ntust.edu.tw (A.S.J.); shyan2812@hotmail.com (T.-H.K.)
[2] Undergraduate Program of Vehicle and Energy Engineering, National Taiwan Normal University, Taipei 106, Taiwan; cchsin@ntnu.edu.tw
* Correspondence: link@mail.ntust.edu.tw; Tel.: +886-2-2370-3289

Abstract: The application of the high gain boost DC-DC converter is gaining more attention due to an increasingly wide range of applications for sustainable green energy solutions, as well as other high voltage applications. In this study, a modified high gain quadratic boost converter is proposed using a single switch. The proposed topology is a member of the family of the non-isolated category with a common ground feature and can operate in a wide range of duty ratios, and is able to provide the required voltage gain. In this proposed circuit configuration, a dual voltage boost cell was formed by incorporating two capacitors in series with two inductors of a conventional quadratic boost converter. Additionally, a capacitor was integrated with a second voltage boost cell. This special configuration increases the voltage gain as well as reduces the voltage stress across the switch. To show its feasibility, a 200-W prototype setup with 48 V input and 400 V output was designed, and the required PWM signal was fed from the microcontroller unit. A detailed analysis of the design parameters and losses are formulated and are shown in this paper. The simulation was performed in SIMPLIS software, and the experimental results agreed with the obtained output voltage gain. The proposed topology showed a peak efficiency of 94.5% at 150-W output power after considering the power losses in all the components of the PCB.

Keywords: DC-DC converter; quadratic boost converter; high voltage gain; non-isolated topology; ultra-fast recovery diode

Citation: Jana, A.S.; Lin, C.-H.; Kao, T.-H.; Chang, C.-H. A High Gain Modified Quadratic Boost DC-DC Converter with Voltage Stress Half of Output Voltage. *Appl. Sci.* **2022**, *12*, 4914. https://doi.org/10.3390/app12104914

Academic Editors: Bor-Ren Lin and Ke-Han Su

Received: 22 March 2022
Accepted: 8 May 2022
Published: 12 May 2022

1. Introduction

The global warming problem is becoming more severe nowadays, due to which, research across all disciplines to reduce greenhouse gases is ongoing. Generally, the burning of fossil fuels is the largest source of greenhouse gas production [1]. To make our environment cleaner, renewable energy is the most effective solution currently available. Although nuclear energy has the potential to provide sustainable green energy, its post-process (i.e., containing the nuclear waste) is very dangerous to our environment, and its harmful effect will continue for many years because of the exponential decay process [2]. Renewable energy, mainly solar power-based energy, is the only viable source for enormous amounts of energy, which very soon could fully substitute fossil fuel-based energy systems [3]. However, due to certain limitations, each solar photovoltaic cell generates a very low output voltage in terms of DC bias, whereas many appliances which utilize electricity have until now required a much higher voltage level, both in terms of AC and DC. In order to boost the output voltage and power level, a series and parallel connection of solar cells were performed, but that is still not sufficient enough [4]. On the other hand, the output voltage of the solar module can provide a maximum of 48 V, so to provide the required voltage level for the electronics, a converter is required that offers the necessary solution by working in the form of energy conversion, i.e., a boost converter. Additionally, appliances that require

a voltage level in the range of the available bias that a solar module can provide are still in need of a buck-boost converter [5–7] to maintain the voltage regulation. Moreover, as transportation systems are shifting from fossil fuel-based power to electric vehicles [8], in order to drive the vehicles the power converter needs to be capable enough to provide a sufficient voltage level for the inverter to drive the main drive system, i.e., high rated induction motor including the other application parts of the electric vehicle [9]. In addition, the application of high voltage gain DC-DC converters for industrial application has been seen for a long time [10], and in the future, they need to become more compact and sophisticated to maintain the sustainability for an application in industry 4.0 [11–14]. As a result, the research on boost DC-DC converters is drawing more and more attention as their potential application is increasing substantially. In Figure 1 the general application of DC-DC converter is presented.

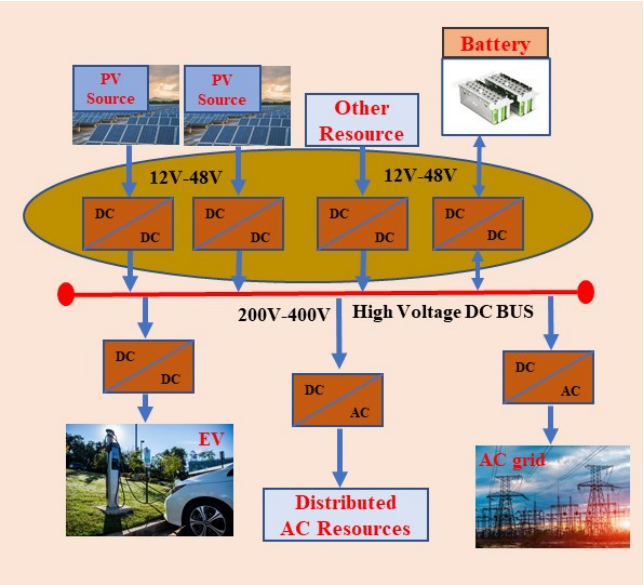

Figure 1. Application of integrated DC-DC converter for the next-generation energy system.

In general, theoretically, the well-known traditional simple boost converter can achieve a high gain (i.e., 10 times) at a duty ratio near 90–95%, but practically, it is impossible to achieve due to the presence of parasitic resistance in passive components, as it limits the charging current in the inductor loop [15]. Additionally, operating at a very high duty cycle may create a reverse recovery problem for the power diode, so it reduces the system performance by increasing the conduction loss of the converter, which further limits the system efficiency [10]. To overcome all these challenges, the operation of the boost converter is preferable at a lower duty ratio [16]. The reported quadratic boost topology has the potential to boost the voltage level by following the quadratic equation, which, interestingly, can provide much higher voltage gain at a lower duty ratio [17]. In addition, several other techniques have been extensively employed to boost the voltage gain, and the Voltage Multiplier Cell (VMC)-based configuration is one of them [18]. A switched capacitor-based DC-DC converter has already been reported by various research groups [19,20]. Though it has a very simple structure and is an effective technique that provides a high voltage gain by reserving a very low space for the converter, a high inrush current is one of the major problems for this switched capacitor VMC-based boost converter. To overcome this issue, numerous different topologies have also been reported so far [21–27]. Additionally, the high gain boost converter can also be classified as isolated and non-isolated types. Normally, the isolated topology uses magnetic coupling (i.e., coupled inductor) between the source and load to provide the isolation [21–25]. Moreover, coupled inductor-based proposed converters are quietly very popular due to their capability for providing very high

voltage gain by changing the turn ratio, but an extra clamp circuit is needed to improve the system efficiency [28,29]. Moreover, though it increases the voltage gain a more precise magnetic design is also needed. In addition, in most of the reported coupled inductor-based boost converters, the authors have designed the magnetics by a 1:1 or sometimes 1:2 turn ratio [28]. Owing to having complexity, the overall cost is always increased for a coupled inductor-based configuration. Moreover, for high power applications, the resonant converter, mostly the LLC topology, has been showing its potential over recent decades. However, from the cost and control point of view, it is much more complex, and the complexity level increases when more switches are used for the possible application [26,27]. Another major drawback of the conventional boost and conventional quadratic boost converter is the voltage stress across the switching device, which is very high as the value of the stress voltage is exactly equal to the output voltage [29–31]. Many research groups have already proposed new techniques that can reduce the voltage stress up to a certain limit [32,33]. Although some reported results have reduced the voltage stress across the switch but in order to do that, in most cases, the converter lost its simple common ground feature [34,35]. So, the integration of more passive components with series and parallel inductors of quadratic boost topology is one of the potential solutions for non-isolated based QBC, which not only helps to increase the voltage gain with lower duty but also fulfills the general requirement by reducing the voltage stress across the switch including the easy control technique. Additionally, inductors dominated by VMC utilize more inductors (i.e., more than two inductors) which further increases the converter size [36].

In this study, a new, modified high gain quadratic boost converter is presented, which was constructed with consecutive mixed voltage boost cells. The proposed converter could be used in various applications where a non-isolated high gain DC-DC converter could be considered. It has various advantages over recently reported non-high gain DC-DC boost converters, which are listed as follows.

1. Using only a single switch, the high voltage gain is achieved, which is the first potential advantage over other reported studies where more switches have been used to boost the voltage level.
2. Another advantage is the control strategy which is generally very easy for a single switch-based topology.
3. The voltage stress across the power MOSFET switch of the proposed study is very low, which is half of the output voltage.

The detailed circuit description of the proposed topology with the proper evolution process is discussed in the following section, and then the ideal and non-ideal voltage gain is calculated. After that, the design of the passive components and the efficiency calculation was conducted. In the later section, the comparison study was conducted, followed by the simulation and experiment results analysis. In the later section, the gain and phase plots are shown for stability analysis.

2. Evolution of the Proposed Modified Quadratic Boost Converter

2.1. Conventional Quadratic Boost Converter

The conventional quadratic boost converter is comprised of two inductors, L_1 and L_2, three diodes, D_1, D_2, and D_3, a single switch, and two capacitors, C_1 and C_0. The circuit diagram of the CQBC is shown in Figure 2.

In a conventional quadratic boost converter, during the first mode of operation, when the switch is on, the inductor L_1 is charged by the source voltage, whereas the inductor L_2 is charged by the capacitor C_1. At this instance, the diode D_3 will be on reverse bias, and the output capacitor, C_0, will transfer the energy to the load. During the second mode, the diode, D_1, will be on reverse bias, and both of the inductors transfer the energy to the load through diodes D_2 and D_3 with a boosted voltage, following the voltage gain formula $\frac{1}{(1-d)^2}$ where the two capacitors store the energy.

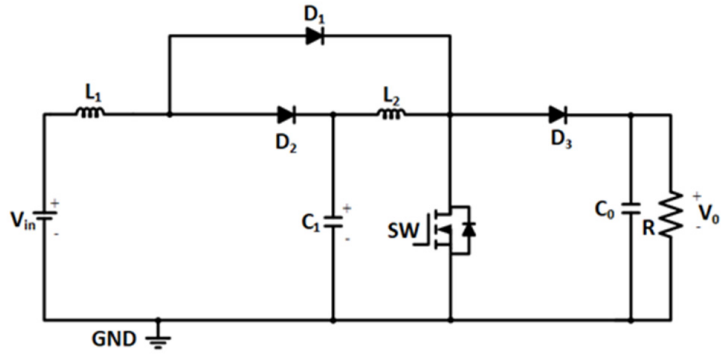

Figure 2. Circuit configuration of Conventional QBC.

2.2. Quadratic Boost Converter with Single Voltage Lift Cell

In this modified QBC shown in Figure 3, the additional capacitor C_2 is connected in series with inductor L_2, which plays a significant role in boosting the output voltage as well as reducing the voltage stress across the switch. In this topology, when the switch is on, the capacitor C_1, which transfers the energy to the inductor L_2, also charges the capacitor C_2 through the diode D_2 at the same time the inductor L_1 is energized by the input voltage. During the second mode of operation, both the inductor L_1, L_2, and capacitor C_2 are involved in boosting the output voltage. The output voltage of this modified topology is higher than the conventional quadratic boost converter, followed by the voltage gain formula $\frac{(2-d)}{(1-d)^2}$. The voltage stress of this proposed topology is reduced significantly to a certain limit which is another advantage over the CQBC.

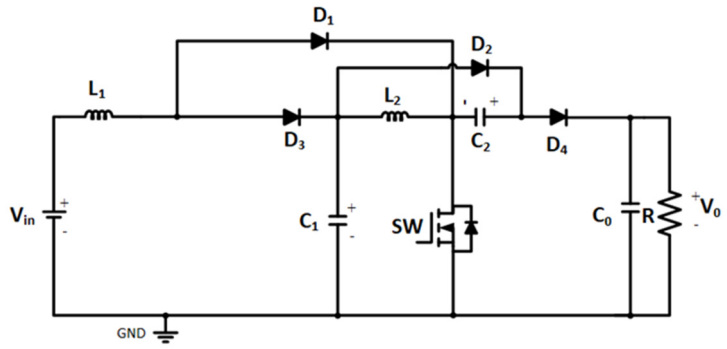

Figure 3. Circuit configuration of modified QBC with voltage lift capacitor integrated with series with Inductor L_2.

2.3. Quadratic Boost Converter with Dual Voltage Lift Cell

Further, the output voltage can be boosted by implementing the same technique with the first inductor, L_1. The proposed circuit topology by Shahrukh khan et al. [37] is shown in Figure 4 where two capacitors, C_1 and C_2, are connected in series with the inductors L_1 and L_2 respectively.

During the first mode of operation, the first voltage lift cell (i.e., L_1 and C_1) is charged by the source voltage through diode D_2. In this mode, the necessary charging current for the capacitors C_1 and C_2 is provided by the source through the diode D_1 and D_3, respectively. Whereas, the second voltage lift cell (i.e., L_2 and C_2) is charged by the capacitor C_3. During mode 2, the four passive components (i.e., L_1, L_2, C_1, C_2) transfer the energy to the load with a voltage gain following $\frac{(2-d)^2}{(1-d)^2}$. In [37], the characteristics of the converter were proposed and studied.

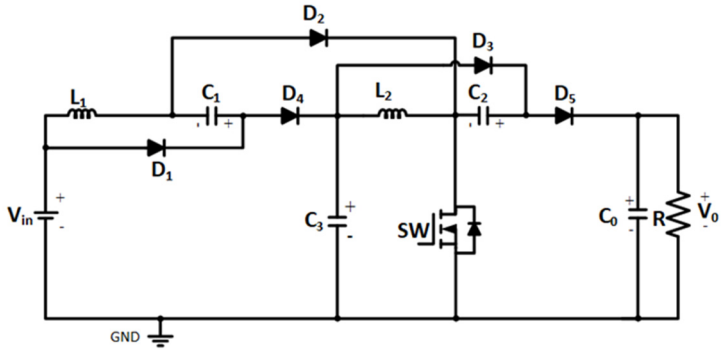

Figure 4. Circuit configuration of dual voltage lift proposed at [37].

2.4. Proposed Modified Quadratic Boost Converter with Integrated Dual Voltage Lift Cell

The generalized circuit diagram of the proposed converter is depicted in Figure 5. The studied high gain boost converter consists of two inductors, L_1 and L_2, five capacitors C_1, C_2, C_3, C_4, C_0, and six diodes D_1, D_2, D_3, D_4, D_5, D_6, and most importantly, a single power MOSFET switch S_1. The first voltage boost cell consists of four components, i.e., L_1, C_1, D_1, D_2, whereas the second integrated voltage boost cell consists of five components, i.e., L_2, C_2, C_4, D_3, and D_4. Both the configuration during two-mode of operation is discussed in a later section. In order to calculate the ideal voltage gain of the proposed converter, it was assumed that all the passive components were lossless and ideal. Additionally, the diode forward voltage drops and the parasitic resistance were ignored for calculating the ideal voltage gain, whereas, in the later section, the non-ideal voltage gain was calculated considering the diode forward voltage drop. Details of the characteristics of the two-mode operation are discussed as follows.

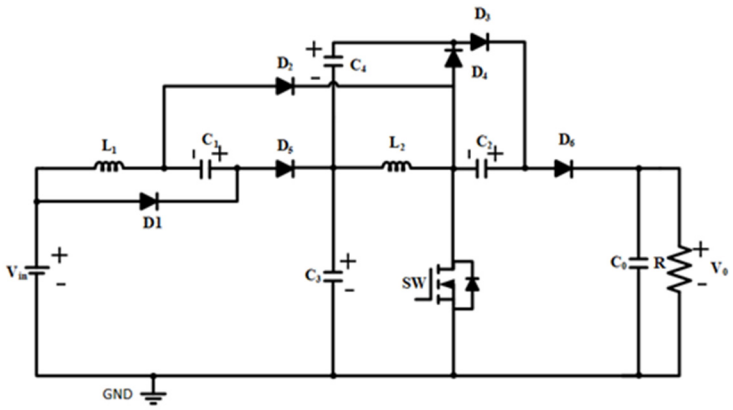

Figure 5. Circuit diagram of the Proposed converter.

2.4.1. Operation Principle and Ideal Voltage Gain Calculation, Continuous Current Mode (CCM)

Mode 1 [0, DT]: Switch ON, D_1, D_2, D_3 ON

When the switch was turned on by the PWM signal, the drain terminal was connected to the ground internally; as a result, the energy transfer process occurred from the source to the passive component and from the passive component to other passive components (i.e., capacitor to inductor). The corresponding circuit configuration is shown in Figure 6.

During this mode of operation, the diodes D_1, D_2, and D_3 will be forward biased and will carry the necessary current to transfer the energy. The diodes D_4, D_5, and D_6 will be reverse biased during the first mode of operation. The inductor L_1 and capacitor C_1 are charged by the source voltage (i.e., V_{in}) through diode D_2, where the charging current of the capacitor C_1 is supplied by the diode D_1. In the second integrated voltage lift cell, the capacitor C_3 transfers the energy directly into the inductor L_2, and the capacitor C_2 is

charged by the summation of the voltage source supplied by the capacitors C_3 and C_4. On the other hand, the output capacitor C_0 transfer the necessary load current to the load.

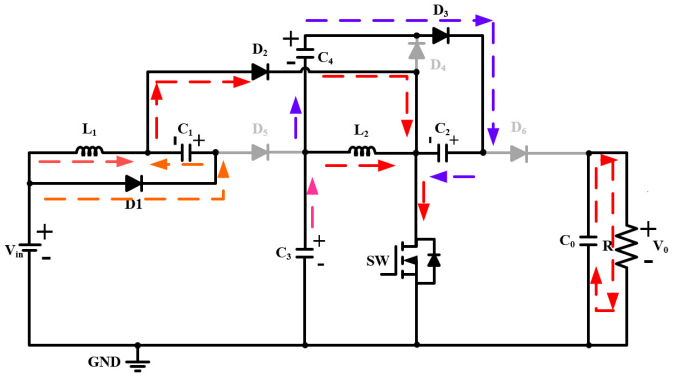

Figure 6. Circuit configuration during the first mode of operation.

The characteristics equations during the first mode of operation are as follows.

$$V_{L1} = V_{in} = L_1 \frac{di_{L1}}{dt} \tag{1}$$

$$V_{C1} = V_{in} \tag{2}$$

$$V_{L2} = V_{C3} = L_2 \frac{di_{L2}}{dt} \tag{3}$$

$$V_{C2} = V_{C3} + V_{C4} \tag{4}$$

$$V_{C0} = -V_0 \tag{5}$$

Mode 2 [DT, T]: Switch OFF, D_4, D_5, D_6 ON

During this interval period, the switch was turned off, ideally with the withdrawal of the PWM signal. The corresponding circuit configuration during mode 2 is shown in Figure 7. In this mode of operation, the energy is directly transferred from the source to the load through the passive component, and it transfers the energy to the other passive component (i.e., C_3, C_4). The diodes D_1, D_2, and D_3 will be in reverse bias; on the other hand, the D_5 and D_6 will carry the necessary current for the load. The charging current for capacitor C_4 is provided by the inductor L_2 through diode D_4.

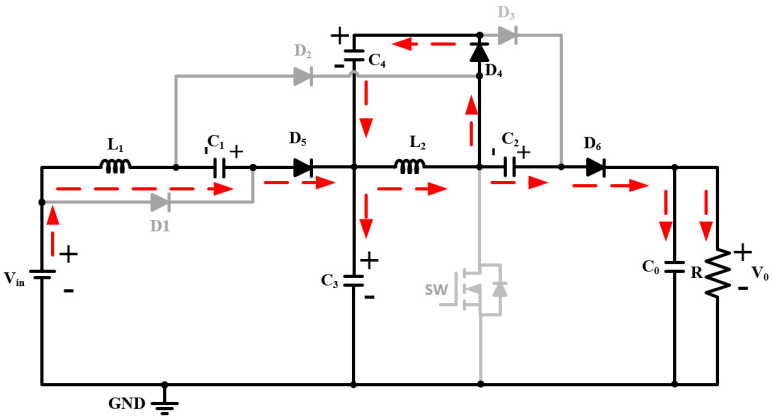

Figure 7. Circuit configurations for the second mode of operation.

The characteristics equation during this mode is derived in the following section.

$$V_{L1} = V_{in} + V_{C1} - V_{C3} \tag{6}$$

$$V_{L1} = 2V_{in} - V_{C3} \tag{7}$$

$$V_{C4} = -V_{L2} \tag{8}$$

$$V_{L2} = V_{C3} + V_{C2} - V_0 \tag{9}$$

Putting the Equation from (8) and (9) into the Equation (4)

$$V_{C2} = V_{C3} + (-V_{C3} - V_{C2} + V_0) \tag{10}$$

$$2V_{C2} = V_0 \tag{11}$$

$$V_{C2} = \frac{V_0}{2} \tag{12}$$

To obtain the voltage gain, the volt-second method is applied on both Inductor L_1 and L_2. The equations are as follows.

$$\int_0^T V_{L1}(t) \cdot dt = 0 \tag{13}$$

$$V_{in} \times dT + (2V_{in} - V_{C3}) \times (1-d)T = 0 \tag{14}$$

$$V_{C3} = \frac{(2-d)}{(1-d)} \tag{15}$$

$$\int_0^T V_{L2}(t) \cdot dt = 0 \tag{16}$$

$$V_{C3} \times dT + (V_{C3} + V_{C2} - V_0) \times (1-d)T = 0 \tag{17}$$

Putting the value of V_{C2} from Equations (12)–(17) the below equation is obtained.

$$V_{C3} \times dT + \left(V_{C3} - \frac{V_0}{2}\right) \times (1-d)T = 0 \tag{18}$$

$$V_0 = \frac{2}{(1-d)} \times V_{C3} \tag{19}$$

Putting the value of V_{C3} from Equations (15)–(20) the ideal voltage gain of the proposed converter is calculated as follows.

$$V_0 = \frac{2(2-d)}{(1-d)^2} \times V_{in} \tag{20}$$

$$Voltae\ gain\ (M) = \frac{V_0}{V_{in}} = \frac{2(2-d)}{(1-d)^2} \tag{21}$$

2.4.2. Non-Ideal Voltage Gain Calculation Considering the Diode Voltage Drop

The diode's voltage drop is one of the main factors for concern for the deviation of the output voltage from the actual voltage gain. For the non-isolated-based high gain quadratic boost converters, mainly in voltage boost cells-based QBC, there are more diodes to store the energy in the passive components (i.e., the extra passive components for boosting the voltage). The voltage reduction at each step is added together and reflected in the output voltage gain. The equivalent series resistance (ESR) value of each passive component was considered negligible. In the below section, the voltage gain is formulated considering the diode's forward voltage drop (i.e., V_D) following the same previous method as discussed in the earlier section.

Mode 1 [0, DT]:

Referring to Figure 6, during mode 1 the characteristics equations are as follows

$$V_{L1} = V_{in} - V_D \tag{22}$$

$$V_{C1} = V_{in} - 2V_D \tag{23}$$

$$V_{L2} = V_{C3} \tag{24}$$

$$V_{C2} = V_{C3} + V_{C4} - V_D \tag{25}$$

Mode 2 [DT, T]:

Referring to Figure 7, during mode 2 the corresponding equations are as follows

$$V_{L1} = V_{in} + V_{C1} - V_{C3} - V_D \tag{26}$$

$$V_{L1} = 2V_{in} - V_{C3} - V_D \tag{27}$$

$$V_{C4} = -V_{L2} + V_D \tag{28}$$

$$V_{L2} = V_{C3} + V_{C2} - V_0 - V_D \tag{29}$$

Now applying the volt-sec balance method to the inductor L_1 the corresponding voltage gain was calculated and is shown below.

$$V_{C3} = \frac{(2-d)}{(1-d)} V_{in} - \frac{(3-2d)}{(1-d)} V_D \tag{30}$$

Applying the volt-sec method on Inductor L_2 and the derived non-ideal voltage gain is shown as follows

$$V_0 = \frac{2\,(2-d)}{(1-d)^2} V_{in} - \frac{\left(7-6d+d^2\right)}{(1-d)^2} V_D \tag{31}$$

The related waveform of the ripple current of the inductor, ripple voltage of the capacitor, and the current waveform of the diode and switch are depicted in Figure 8.

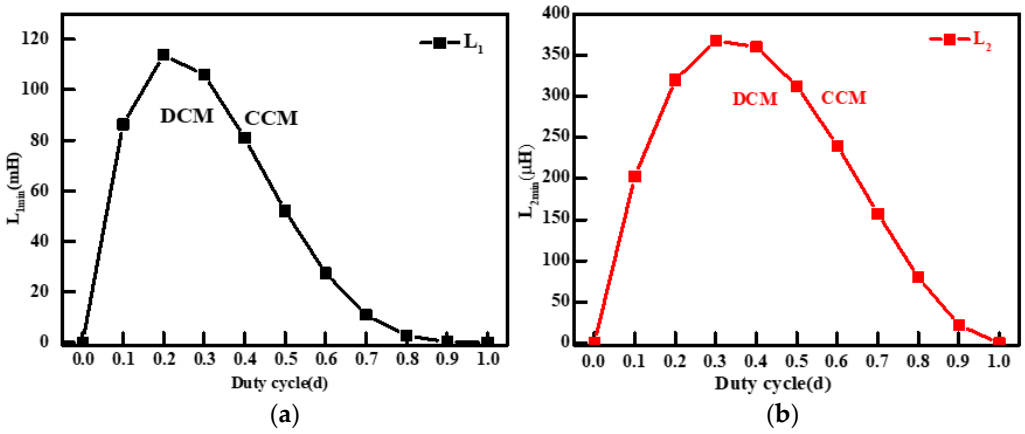

Figure 8. Minimum inductors value requirement for the operation of CCM and DCM and Boundary condition mode (**a**) value of inductor L_1 vs. duty cycle, (**b**) value of inductor L_2 value vs. duty cycle for 150 W load, V_{in} 48 V, V_{out} 400 V.

3. Design Considerations

3.1. Design of the Inductor

The inductors for this proposed topology were designed based on the current ripple and the applied voltage across it. The differential equation for each of the inductor during the first mode of operation is stated as follows. The minimum requirement value of the

inductors was also calculated, which sets the boundary of the CCM and DCM mode of the converter characteristics.

$$V_{L1} = L_1 \frac{di_{L1}}{dt} = V_{in} \tag{32}$$

$$L_1 = \frac{V_{in} dT}{\Delta i_{L1}} \tag{33}$$

$$V_{L2} = L_2 \frac{di_{L2}}{dt} = V_{C3} \tag{34}$$

$$L_2 = \frac{V_{C3} dT}{\Delta i_{L1}} = \frac{(2-d) V_{in} dT}{(1-d) \Delta i_{L1}} \tag{35}$$

$$\Delta i_{L1} = \frac{V_{in} dT}{L_1} \tag{36}$$

$$\Delta i_{L2} = \frac{V_{C3} dT}{L_2} = \frac{(2-d) V_{in} dT}{(1-d) L_2} \tag{37}$$

The average current through L_1 and L_2 are as follows

$$I_{L1} = \frac{2I_0}{(1-d)^2} = \frac{2V_0}{(1-d)^2 R} \tag{38}$$

$$I_{L2} = \frac{2I_0}{(1-d)} = \frac{2V_0}{(1-d) R} \tag{39}$$

$$(I_{L1})_{min} = \frac{2V_0}{(1-d)^2 R} - \frac{V_{in} dT}{2L_1} \tag{40}$$

$$L_1 \geq \frac{d(1-d)^4 R}{8(2-d) f_{sw}} \tag{41}$$

$$(I_{L2})_{min} = \frac{2V_0}{(1-d) R} - \frac{d(2-d) V_{in} T}{2(1-d) L_2} \tag{42}$$

$$L_2 \geq \frac{d(1-d)^2 R}{8 f_{sw}} \tag{43}$$

In Figure 8 the value of the minimum inductor vs. duty cycle was plotted from Equations (41) and (43) for the condition of the CCM, DCM, and Boundary condition mode operating mode.

3.2. Selection of the Capacitor

The capacitor was designed based on the ripple voltage ΔV_{CX}, the charging current following through it, the duty cycle, and the switching frequency f_{sw}, respectively. The corresponding differential equation of each capacitor was formulated and is given below.

$$\begin{cases} C_1 = \frac{\Delta Q_1}{\Delta V_{C1}} = \frac{\Delta I_{C1} dT}{\Delta V_{C1}} = \frac{(2-d) dV_0}{(1-d)^2 \Delta V_{C1} f_{sw} R} \\ C_2 = \frac{\Delta Q_2}{\Delta V_{C2}} = \frac{\Delta I_{C2} dT}{\Delta V_{C2}} = \frac{dV_0}{(1-d) \Delta V_{C2} f_{sw} R} \\ C_3 = \frac{\Delta Q_3}{\Delta V_{C3}} = \frac{\Delta I_{C3} dT}{\Delta V_{C3}} = \frac{dV_0}{(1-d)^2 \Delta V_{C3} f_{sw} R} \\ C_4 = \frac{\Delta Q_4}{\Delta V_{C4}} = \frac{\Delta I_{C4} dT}{\Delta V_{C4}} = \frac{dV_0}{(1-d) \Delta V_{C4} f_{sw} R} \\ C_0 = \frac{\Delta Q_1}{\Delta V_{C1}} = \frac{I_{C0} dT}{\Delta V_{C0}} = \frac{dV_0}{R \Delta V_{C0} f_{sw}} \end{cases} \tag{44}$$

3.3. Voltage Stress across Switching Device and Power Diode

The ideal voltage stress across power switch and power diodes are formulated and are shown as follows. In Figure 9 the steady state voltage and current waveform of each components is shown.

$$\begin{cases} V_{sw} = \frac{V_0}{2} \\ V_{D1} = \frac{V_{in}}{(1-d)} \\ V_{D2} = \frac{V_{in}}{(1-d)^2} \\ V_{D3} = V_{D4} = \frac{V_0}{2} \\ V_{D5} = V_{C3} - V_{in} = \frac{V_{in}}{(1-d)} \\ V_{D6} = \frac{V_0}{2} \end{cases} \tag{45}$$

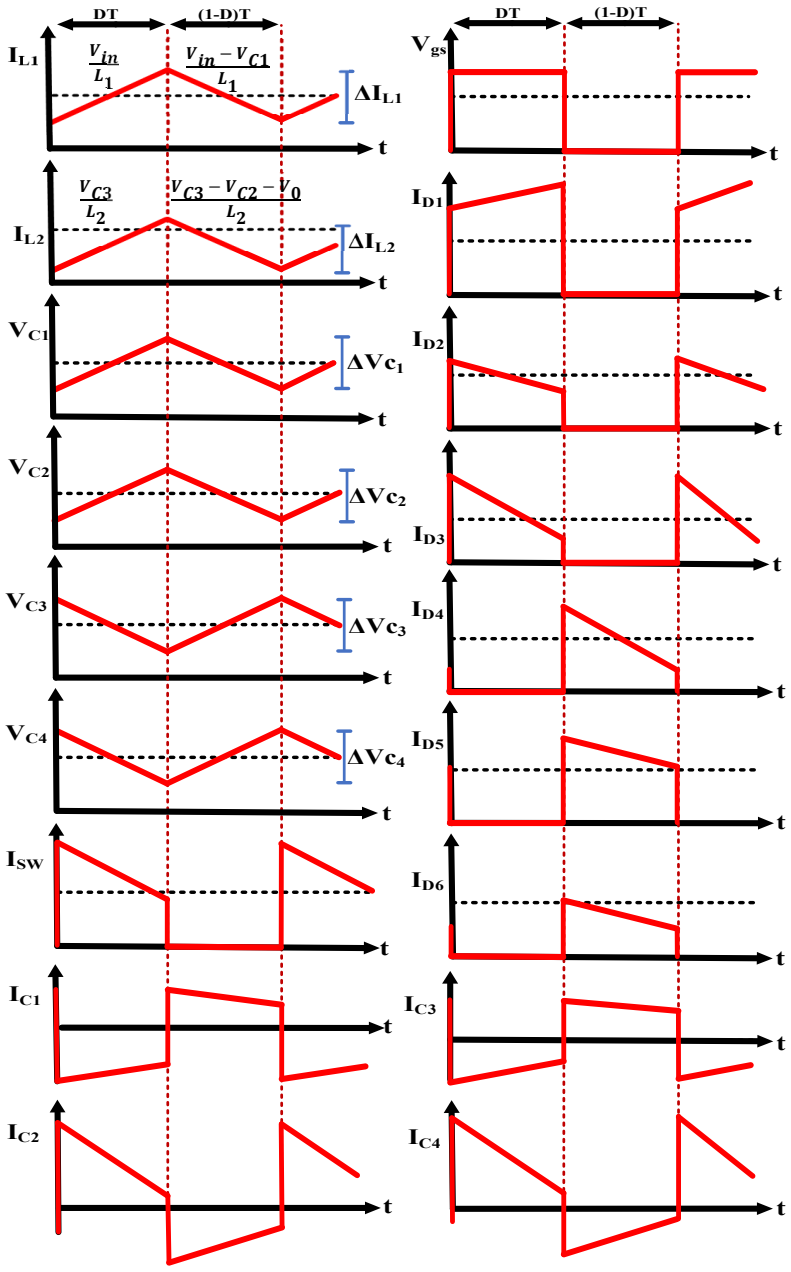

Figure 9. The corresponding steady-state waveform of CCM mode.

4. Formulation of Power Loss of the Proposed Studied Topology

To calculate the efficiency, the loss model was developed by considering the loss due to the parasitic resistance in each component of the system. In Figure 10, the corresponding circuit configuration is depicted.

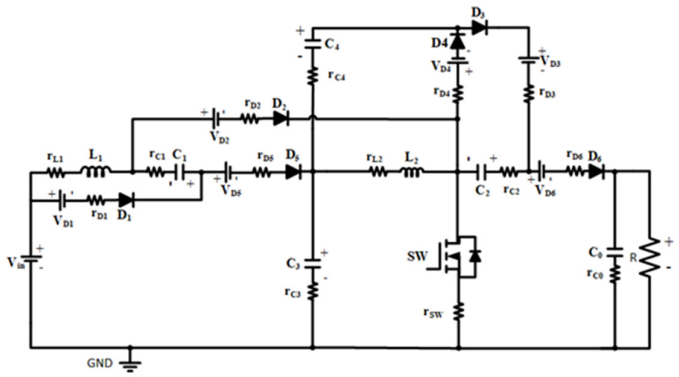

Figure 10. Equivalent circuit diagram of the studied converter with parasitic elements in each component.

4.1. Power Losses Calculation in Power Switch

The RMS current-carrying by the switch is denoted as $i_{SW_{rms}}$ and P_{SW} and P_{on+off} are the conduction loss and switching loss of the switch. The corresponding formulated loss is calculated and is shown below.

$$\begin{cases} i_{sw_{rms}} = \frac{\left(3+2d-d^2\right)<i_0>}{(1-d)^2\sqrt{(d)}} \\ P_{sw_{Con}} = {i_{SW_{rms}}}^2 r_{SW} = \frac{\left(3+2d-d^2\right)^2<i_0>^2}{d(1-d)^4} r_{SW} = \frac{\left(3+2d-d^2\right)^2<i_0>^2}{d(1-d)^4} \frac{r_{SW}}{R} P_0 \\ P_{SW} = \frac{1}{2T_S}(< i_s > V_S)\left(t_{on} + t_{off}\right) \end{cases} \tag{46}$$

4.2. Power Losses Calculation in Power Diodes

The RMS current following through the diode is represented as $i_{Dx_{rms}}$. The power loss due to ESR of the diodes is denoted as P_{rDx} and another loss due to the forward voltage drop is denoted as P_{FwDx}. So, the power loss in each diode is represented as

$$P_{Dx} = V_{FwD1} < i_{Dx} > + {i_{Dx_{rms}}}^2 r_{Dx} \tag{47}$$

$$\begin{cases} i_{D1_{rms}} = \frac{2<i_0>}{(1-d)\sqrt{(d)}} \\ P_{D1} = V_{FwD2} \frac{2<i_0>}{(1-d)} + \frac{4<i_0>}{d(1-d)^2}^2 r_{D2} \end{cases} \tag{48}$$

$$\begin{cases} i_{D2_{rms}} = \frac{2(1+d)<i_0>}{(1-d)^2\sqrt{(d)}} \\ P_{D2} = V_{FwD2} \frac{2(1+d)<i_0>}{(1-d)^2} + \frac{4(1+d)^2<i_0>}{d(1-d)^4}^2 r_{D2} \end{cases} \tag{49}$$

$$\begin{cases} i_{D3_{rms}} = \frac{<i_0>}{\sqrt{(d)}} \\ P_{D3} = V_{FwD3} < i_0 > + \frac{<i_0>}{(d)}^2 r_{D3} \end{cases} \tag{50}$$

$$\begin{cases} i_{D3_{rms}} = \frac{<i_0>}{\sqrt{(1-d)}} \\ P_{D4} = V_{FwD4} < i_0 > + \frac{<i_0>}{(1-d)}^2 r_{D4} \end{cases} \tag{51}$$

$$\begin{cases} i_{D5_{rms}} = \frac{2<i_0>}{(1-d)\sqrt{(1-d)}} \\ P_{D5} = V_{FwD5}\frac{2<i_0>}{(1-d)} + \frac{4<i_0>}{(1-d)^3}^2 r_{D5} \end{cases} \tag{52}$$

$$\begin{cases} i_{D6_{rms}} = \frac{<i_0>}{\sqrt{(1-d)}} \\ P_{D6} = V_{FwD6}< i_0 > + \frac{<i_0>}{(1-d)}^2 r_{D6} \end{cases} \tag{53}$$

The total loss by the diode can be added together and represented as

$$P_{Dtotal} = \sum_{i=1}^{6} P_{Di}$$

4.3. Power Losses in the Inductor Due to ESRs

The Root mean square current through the inductor is notified as $i_{LX_{rms}}$. The ESRs and the associated power loss are denoted as r_{LX} and P_{LX}.

$$\begin{cases} i_{L1_{rms}} = \frac{2<i_0>}{(1-d)^2} \\ P_{L1} = {i_{L1_{rms}}}^2 r_{L1} = \frac{4<i_0>^2}{(1-d)^4} r_{L1} = \frac{4<i_0>^2}{d(1-d)^3}\frac{r_{L1}}{R}P_0 \\ i_{L2_{rms}} = \frac{2<i_0>}{(1-d)} \\ P_{L2} = {i_{L2_{rms}}}^2 r_{L2} = \frac{4<i_0>^2}{(1-d)^2} r_{L1} = \frac{4<i_0>^2}{(1-d)^2}\frac{r_{L1}}{R}P_0 \end{cases} \tag{54}$$

The total loss because of the ESRs of the Inductor can be obtained as

$$P_{Ltotal} = \sum_{i=1}^{2} P_{Li}$$

4.4. Power Losses in the Capacitor

The power loss in a capacitor due to the parasitic resistance present in a capacitor is calculated by considering the RMS current flowing through each capacitor and is denoted as P_{Cx}. The equivalent series resistance (i.e., ESR) of each capacitor is represented by r_{Cx}.

$$\begin{cases} i_{C1_{rms}} = \frac{2<i_0>}{(1-d)\sqrt{d)1-d)}} \\ P_{C1} = {i_{C1_{rms}}}^2 r_{C1} = \frac{4<i_0>^2}{d(1-d)^3} r_{C1} = \frac{4<i_0>^2}{d(1-d)^3}\frac{r_{C1}}{R}P_0 \end{cases} \tag{55}$$

$$\begin{cases} i_{C2_{rms}} = \frac{<i_0>}{\sqrt{d(1-d)}} \\ P_{C2} = {i_{C2_{rms}}}^2 r_{C2} = \frac{<i_0>^2}{d(1-d)} r_{C2} = \frac{<i_0>^2}{d(1-d)}\frac{r_{C2}}{R}P_0 \end{cases} \tag{56}$$

$$\begin{cases} i_{C3_{rms}} = \frac{(1+d)<i_0>}{(1-d)\sqrt{d)1-d)}} \\ P_{C3} = {i_{C3_{rms}}}^2 r_{C3} = \frac{(1+d)^2<i_0>^2}{d(1-d)^3} r_{C3} = \frac{(1+d)^2<i_0>^2}{d(1-d)^3}\frac{r_{C3}}{R}P_0 \end{cases} \tag{57}$$

$$\begin{cases} i_{C4_{rms}} = \frac{<i_0>}{\sqrt{d(1-d)}} \\ P_{C4} = {i_{C4_{rms}}}^2 r_{C4} = \frac{<i_0>^2}{d(1-d)} r_{C4} = \frac{<i_0>^2}{d(1-d)}\frac{r_{C4}}{R}P_0 \end{cases} \tag{58}$$

$$\begin{cases} i_{C0_{rms}} = \frac{\sqrt{d}<i_0>}{\sqrt{(1-d)}} \\ P_{C0} = {i_{C0_{rms}}}^2 r_{C0} = \frac{d<i_0>^2}{(1-d)} r_{C0} = \frac{d<i_0>^2}{(1-d)}\frac{r_{C0}}{R}P_0 \end{cases} \tag{59}$$

Considering all working capacitors, the total accumulated loss can be calculated as

$$P_{Ctotal} = \sum_{i=1}^{5} P_{Ci}$$

The total efficiency of the proposed converter was calculated by the below equation

$$\eta = \frac{P_0}{P_0 + P_{Ltotal} + P_{Ctotal} + P_{Dtotal+P_{SW}}} \quad (60)$$

5. Comparison Analysis

A summary of recently proposed high gain, mostly quadratic boost-based topology, is discussed in this section. Table 1 represents the summary of the recently reported high gain boost topology, tabulating from where it specifies a few important characteristic parts of each proposed topology (i.e., components count normalized switch's voltage stress, etc.). From the specification table, it can be observed that the performance of the high gain boost converter depends on so many factors of the converter specification. It can also be noted that though the desirable performance of the high gain boost is suitable based on low voltage stress and a high voltage gain capability, sometimes it may require many passive components. So, a trade-off must be given in order to select for perfect application.

Table 1. Comparison with a similar non-Isolated boost converter.

Topology	Switches	Diode	Inductor	Capacitor	Ideal Voltage Gain	Voltage Stress (V_s/V_{in})	Common Ground	Ref
CQBC	1	3	2	2	$\frac{1}{(1-d)^2}$	$\frac{1}{(1-d)^2}$	Yes	[29]
Topology 1	1	5	2	4	$\frac{(3+d)}{(1-d)}$	$\frac{4}{(1-d)}$	No	[38]
Topology 2	1	5	2	4	$\frac{2}{(1-d)^2}$	$\frac{1}{(1-d)^2}$	No	[39]
Topology 3	1	3	3	3	$\frac{d}{(1-d)^2}$	$\frac{d}{(1-d)^2}$	Yes	[40]
Topology 4	1	3	2	2	$\frac{d(2-d)}{(1-d)^2}$	$\frac{1}{(1-d)^2}$	Yes	[41]
Topology 5	1	5	3	3	$\frac{d^2}{(1-d)^2}$	$\frac{1}{(1-d)^2}$	Yes	[42]
Topology 6	2	3	2	2	$\frac{1}{d(1-d)}$	$\frac{1}{(1-d)}$	Yes	[30]
Topology 7	1	4	2	3	$\frac{2}{(1-d)^2}$	$\frac{1}{(1-d)^2}$	No	[35]
Topology 8	1	5	3	3	$\frac{2}{(1-d)^2}$	$\frac{2}{(1-d)^2}$	Yes	[43]
Topology 9	1	5	2	4	$\frac{(2-d)^2}{(1-d)^2}$	$\frac{(2-d)}{(1-d)^2}$	Yes	[37]
Proposed	1	6	2	5	$\frac{2(2-d)}{(1-d)^2}$	$\frac{(2-d)}{(1-d)^2}$	Yes	

In the comparison table, topology 9 proposed by Shahrukh khan et al. [37] has been reported recently, and the voltage gain of the proposed topology is denoted in Table 1. In this article, our proposed topology has already overcome the voltage gain, and the normalized voltage stress was reduced compared to their study. Figure 11 presents the ideal voltage gain vs. duty ratio of the reported literature survey from Table 1. The figure justifies the voltage gain profile of the studied circuit configuration. In the later section, the voltage gain is verified by the simulated results as well as by the experimental results.

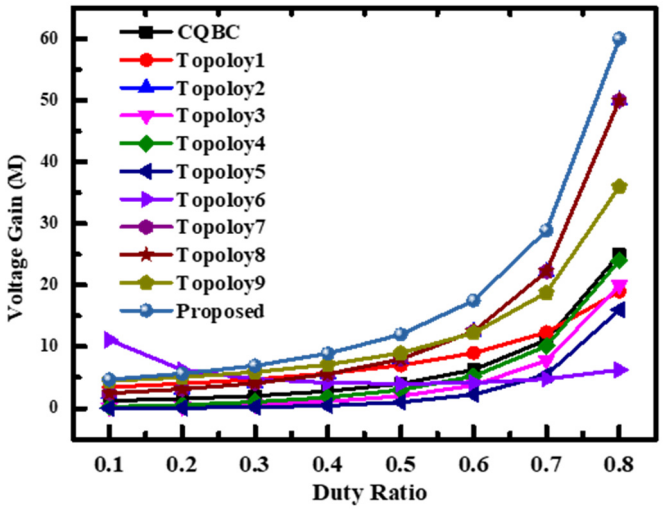

Figure 11. The voltage gain comparison plot of the recently reported proposed study.

6. Results and Discussion

This section describes the qualitative performance of the proposed high gain quadratic boost converter. The complete specification of the proposed converter is specified in the following section. A comprehensive list of the parameter's specifications is given in Table 2. The inductor of the proposed converter was designed in our laboratory following Equations (33) and (35). For the design of the inductor, an 'E' type ferrite core was used, and the turn ratios were calculated theoretically. The required air gap was added by electrical tape, and the inductance was measured at the same time. All other components, capacitor, power MOSFET, Driver IC, and STM32-MCU unit were purchased. The corresponding duty ratio for 400 V output voltage was calculated from the non-ideal voltage gain Equation (31).

Table 2. Component specifications of the proposed converter.

Component	Specification
Input Voltage	24~48 V
Output Voltage	(400~408) V
Duty ratio	0.2~0.6
f_{sw}	50 kHz
Capacitors	C_1 = 220 µF/100 V/0.1 Ω, C_2 = 100 µF/ 250 V/0.1 Ω, C_3 = C_4 =100 µF/250 V/0.1 Ω, C0 = 100 µF/450 V/0.1 Ω
Inductor	L_1 = 300 µH, L_2 = 600 µH, ESR = 0.2 Ω
Power MOSFET	SPW52N50C3, 560 V, 52 A 0.07 Ω
Diodes	CMPFCD86, (600 V, V_F-1.5 V, I_F-8 A) RF150TF3S(SIMPLIS) (600 V, V_F-1.5 V, I_F-8 A)
Microcontroller	STM32, Nucleo H743ZI2
Gate Driver IC	TLP250H
Fuse	6.3 A
Power supply	Chroma programmable DC power supply, 621OOH-600S
Input Power	158.6 W
Output Power	150 W
Load Resistance	Chroma programmable electronic load simulator model 63. 1075 Ω, I_0-0.374 A

6.1. Simulation Results and Potential Verification

To validate the performance of the converter, the proposed circuit was stimulated in SIMPLIS software. The circuit parameter value was selected exactly as described in Table 2. The only difference in the simulation configuration is the power diode. A different diode model (RF1501TF3S) has been chosen due to not having the same diode model number of the diode in SIMPLIS simulation software, which has the same specification as compared to the used diode model (i.e., CMPFC86) for experimental verification, The simulation was carried out with an input voltage of 48 V at a switching frequency of 50 kHz. All of the components were selected as ideal components. The load resistance was selected according to the 150-W output power. Figure 12 shows the circuit configuration from SIMPLIS software.

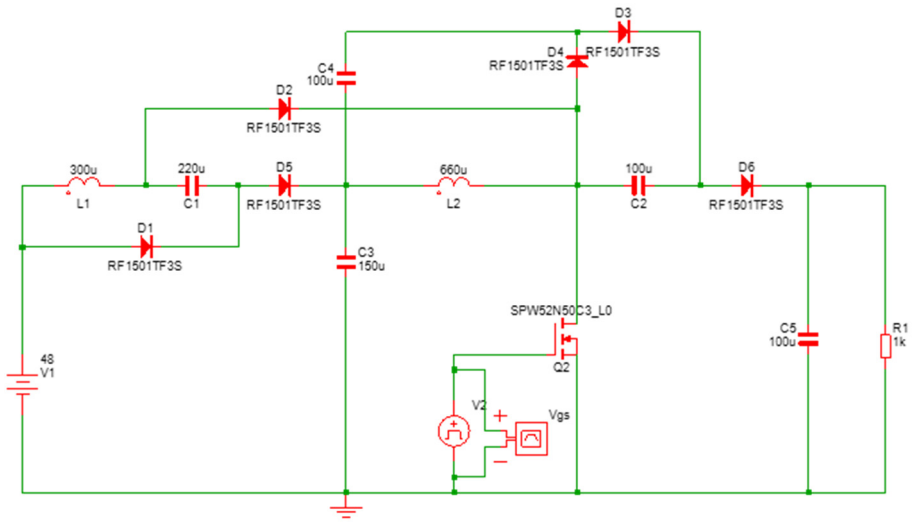

Figure 12. Pictorial representation of proposed circuit simulated in SIMPLIS software.

Simulation Results of the Proposed Boost Converter at Duty d = 0.4, Output Power 150-W

Though the actual duty cycle was considered 0.4, in the experimental section, the MOSFET was not turned off at exactly at the duty cycle of 0.4; instead, it was turned off at duty 0.402 due to the Miller effect. So, the simulation was carried out by selecting the duty cycle of 0.402 and the corresponding theoretical output voltage, referring to Equation (22) was calculated as 428 V. However, due to the presence of a diode forward voltage drop the actual voltage deviates, and as a result the real voltage gain is always lower than the ideal gain. From the datasheet of the diode's model, the forward voltage drops (i.e., 1.5 V) of the diode were taken into consideration, and referring to Equation (31), the actual output voltage was calculated (i.e., 408 V). However, due to the presence of parasitic resistance in the passive component, the actual voltage is further reduced, which is reflected in the experimental results in the later section.

In Figure 13, the simulated waveform of the (a) input voltage (V_{in}), (b) duty cycle (V_{gs}), (c) switch voltage stress of the switch (V_{DS}), and (d) output voltage (V_0) are shown, respectively. The results show that the output voltage obtained by the simulation was about 408 V which is matching, according to the previously discussed value. The voltage stress of the diodes is shown in Figures 14 and 15. The voltage across each of the working capacitors is shown in Figure 16, whereas the plot of the inductor currents is shown in Figure 17, respectively.

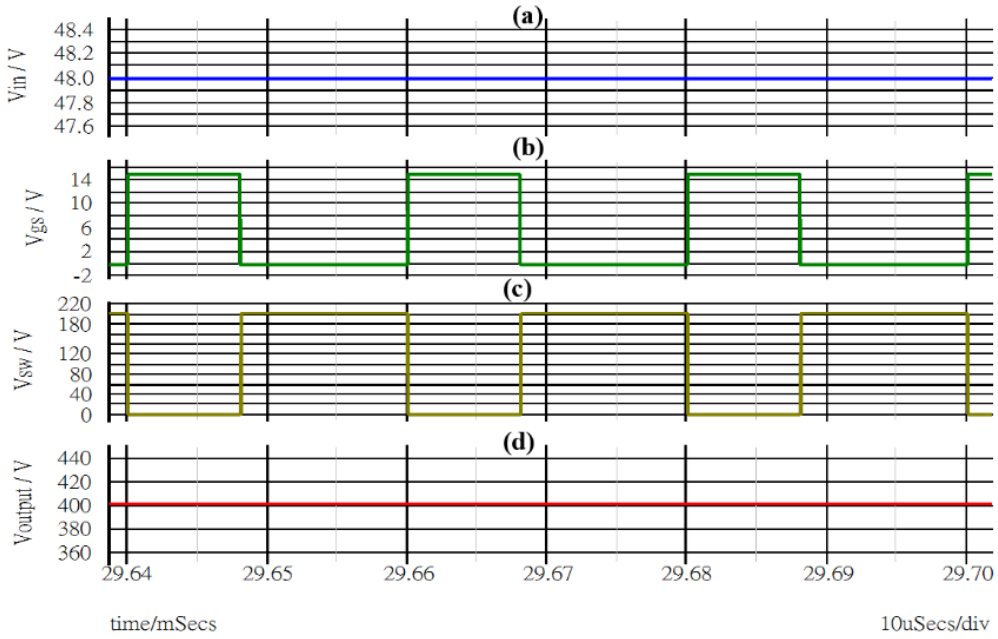

Figure 13. Simulated waveform of (**a**) input voltage (V_{in}), (**b**) duty cycle (V_{gs}) at duty d = 0.402, (**c**) switch's voltage stress (V_{DS}), and (**d**) output Voltage (V_0).

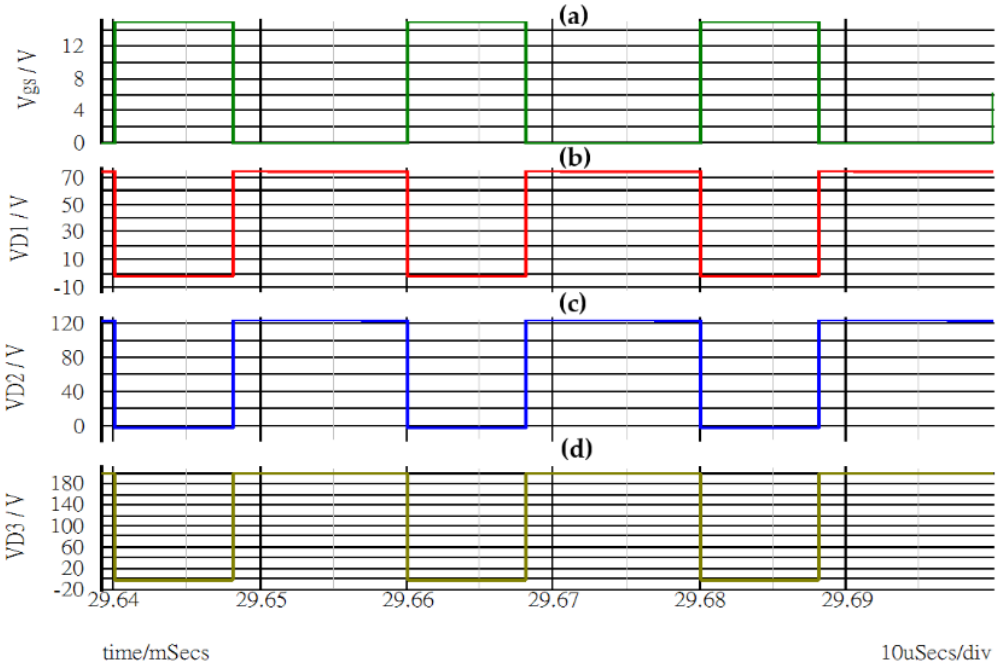

Figure 14. Simulated waveform of (**a**) duty cycle (V_{gs}) at duty d = 0.402, (**b**) Voltage stress of diode D_1 (V_{D1}), (**c**) Voltage stress of diode D_2 (V_{D2}), and (**d**) Voltage stress of diode D_3 (V_{D3}).

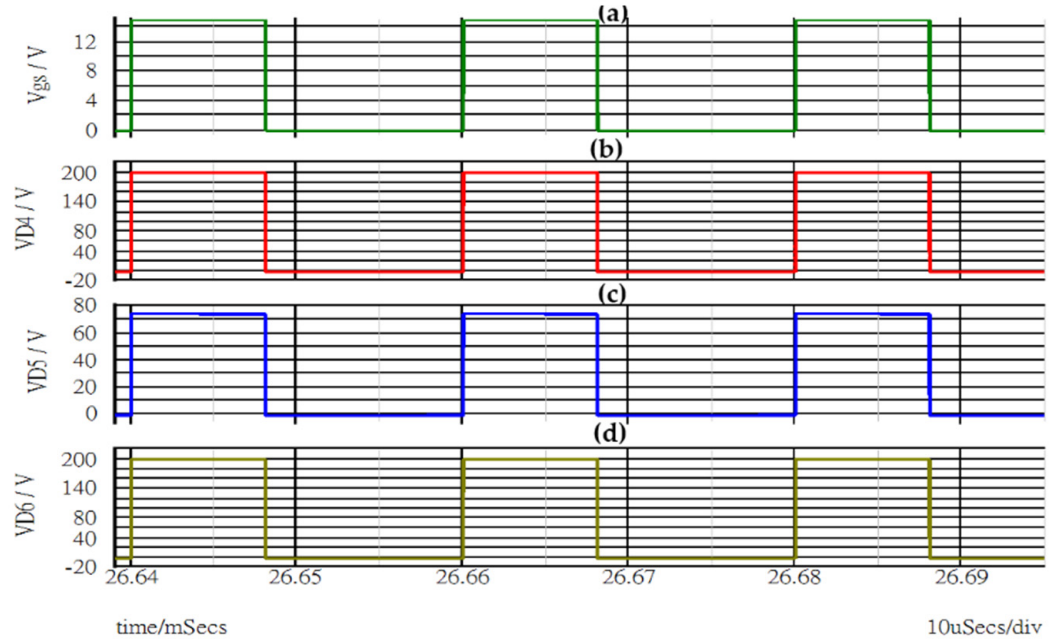

Figure 15. Simulated waveform of (**a**) duty cycle (V_{gs}) at duty d = 0.402, (**b**) Voltage stress of diode D4 (V_{D4}), (**c**) Voltage stress of diode D_5 (V_{D5}), and (**d**) Voltage stress of diode D_6 (V_{D6}).

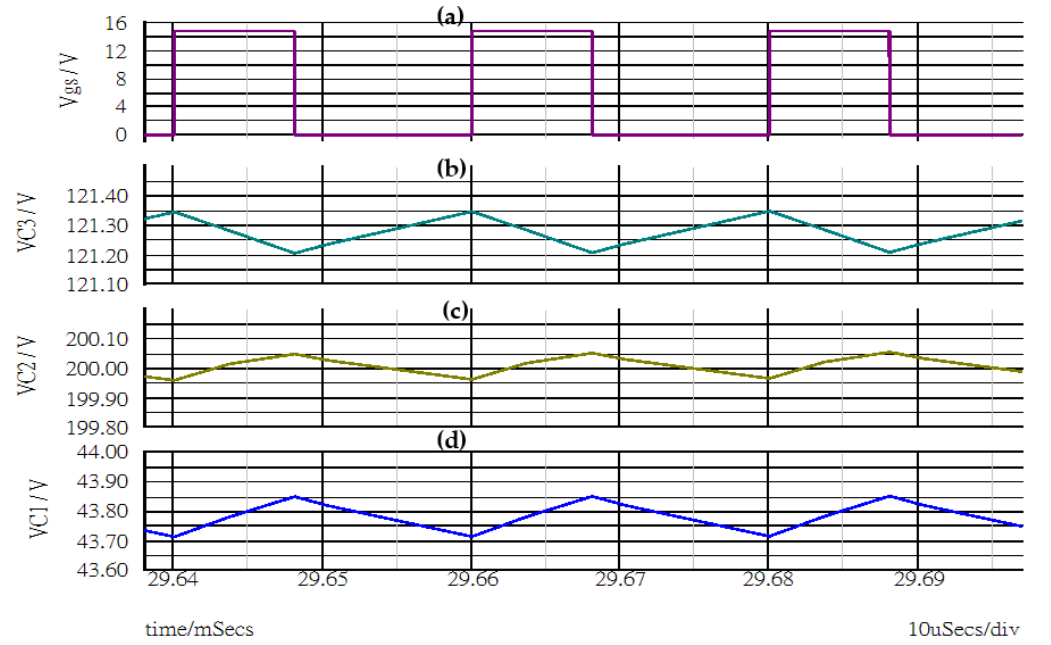

Figure 16. Simulated waveform of (**a**) duty cycle (V_{gs}) at duty d = 0.402, (**b**) Capacitor (C_3) voltage (V_{C3}), (**c**) Capacitor (C_2) voltage (V_{C2}), and (**d**) Capacitor (C_1) voltage (V_{C1}).

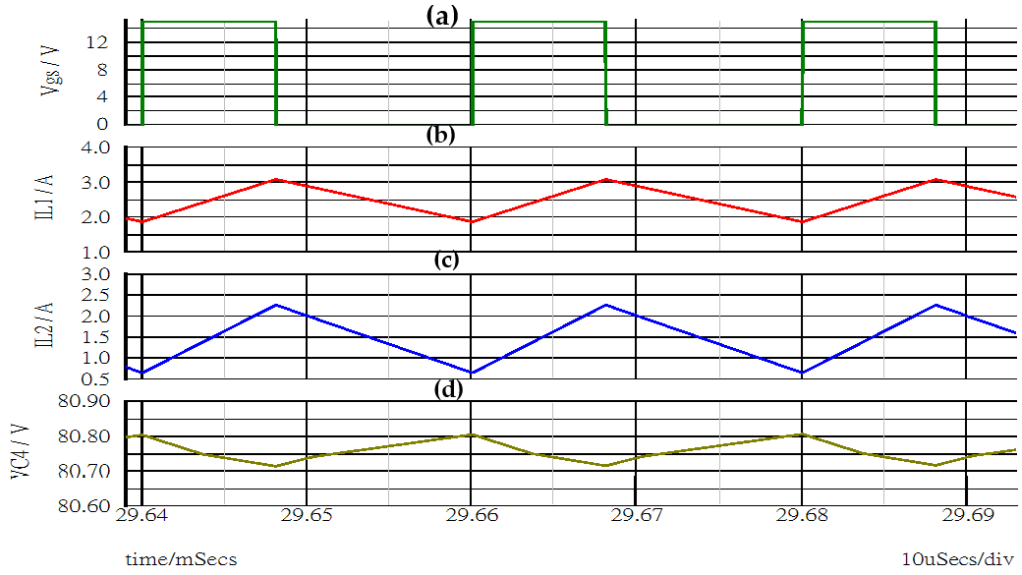

Figure 17. Simulated waveform of (**a**) duty cycle (V_{gs}) at duty d = 0.402, (**b**) Inductor (L_1) Current (I_{L1}), (**c**) Inductor (L_2) Current (I_{L2}), and (**d**) Capacitor (C_4) voltage (V_{C4}).

6.2. Experimental Results and Discussion

In this section, the experimental results are discussed. To validate the potential performance of the proposed converter, a prototype capable of providing 200 W output power was developed in our lab and was tested in the laboratory environment. The Hardware prototype is shown in Figure 18. The Experimental results for the 150 W output power were measured and they are thoroughly discussed in this section. The experimental waveform was obtained from the digital oscilloscope and is presented in the later section step by step.

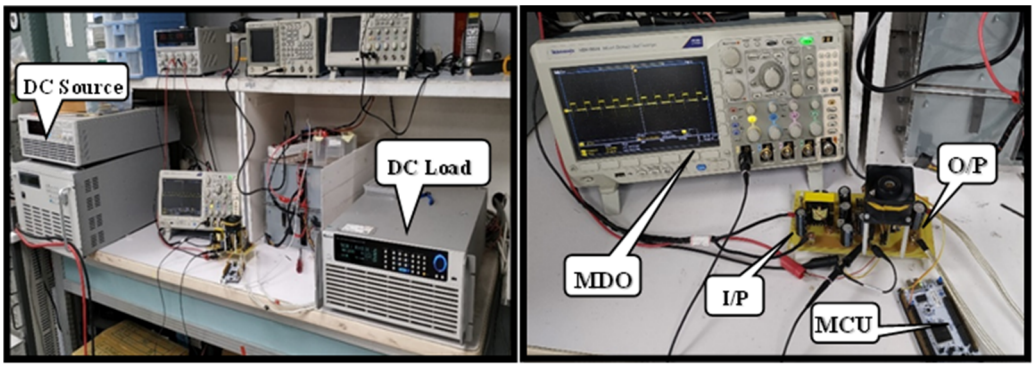

Figure 18. Hardware prototype developed in our lab.

The hardware parameters starting from passive components to the power MOSFET switch and power diodes have the same specification as in the simulation parameters and are shown in Table 2. This proposed study was tested by feeding 48 V DC input voltage and extracting 400 V DC of output voltage (i.e., range 395–405 V). The corresponding duty cycle's value was measured and then selected to obtain the desired output from the non-ideal gain voltage formula (i.e., Equation (31)). Referring to the non-ideal voltage gain Equation (31), the calculated duty cycle was 0.4 or 40%, which refers to the exact desired output voltage. The PWM signal generated from the STMicroelectronics microcontroller unit was directly fed to the MOSFET driver circuit using the driver IC (i.e., TLP 250H) mentioned in Table 3. The electronic DC load was used for taking all the measurements.

Table 3. Comparison table of voltage stress of simulated results and experimental results.

Components	Simulated Results	Experimental Results
Output voltage (V_0)	408 V	402 V
The voltage across the switch (V_{DS})	205 V	201 V
Voltage stress across diode D_1	76~76.5 V	75 V
Voltage stress across diode D_2	126 V	123 V
Voltage stress across diode D_3	203.5 V	202 V
Voltage stress across diode D_4	203.5 V	201 V
Voltage stress across diode D_5	76.3 V	75 V
Voltage stress across diode D_6	203 V	202 V

In Figure 19, the gate pulse, input voltage, switch's voltage stress, and output voltage are shown. A 402 V output voltage is measured at the load side experimentally and is shown in Figure 19. At duty 0.4, the actual output voltage gain is about 426 V, and, in this case, a reduction of 26 V can be seen in the experimental results, which is due to the diode's forward voltage (i.e., due to non-ideal voltage gain, Equation (31)) as well as including some small drops associated with passive components.

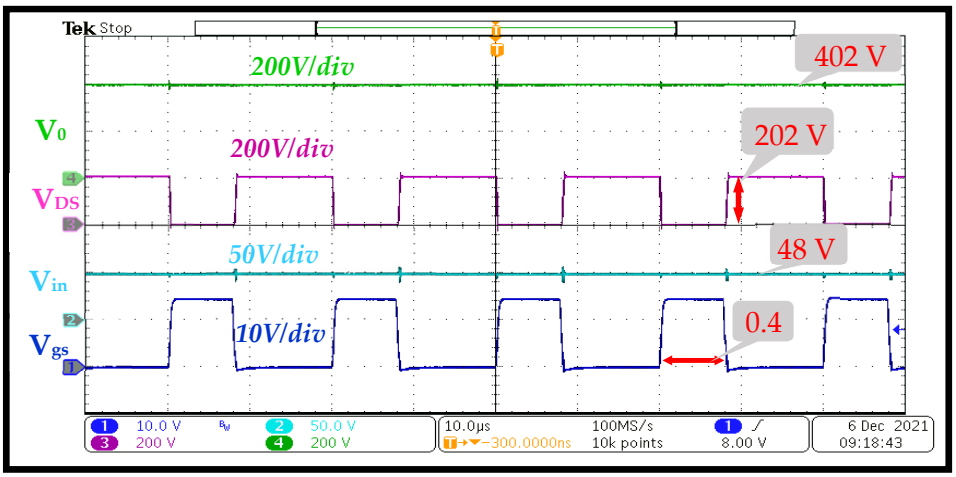

Figure 19. Experimental waveform of input voltage (V_{in}), (**1**) Duty cycle (V_{gs}) at d = 0.4, (**2**) Input Voltage (V_{in}), (**3**) Drain to Source voltage and (**4**) output voltage (V_0).

Figure 20 represents the voltage stress of diodes D_1, D_2, and D3. For the above-mentioned rated power rating, the corresponding voltage stress of the diodes are 75 V, 123 V, and 202 V, respectively. In Figure 21, the voltage stress across diodes D_4, D_5, and D_6 are plotted. The measured values are V_{D4} = 201 V, V_{D5} = 75 V, and V_{D6} = 202 V, respectively. The voltage across capacitors C_1, C_2, and C_3 are plotted in Figure 22. The corresponding measured voltages are V_{C1} = 47 V, V_{C2} = 200 V, and V_{C3} = 125 V.

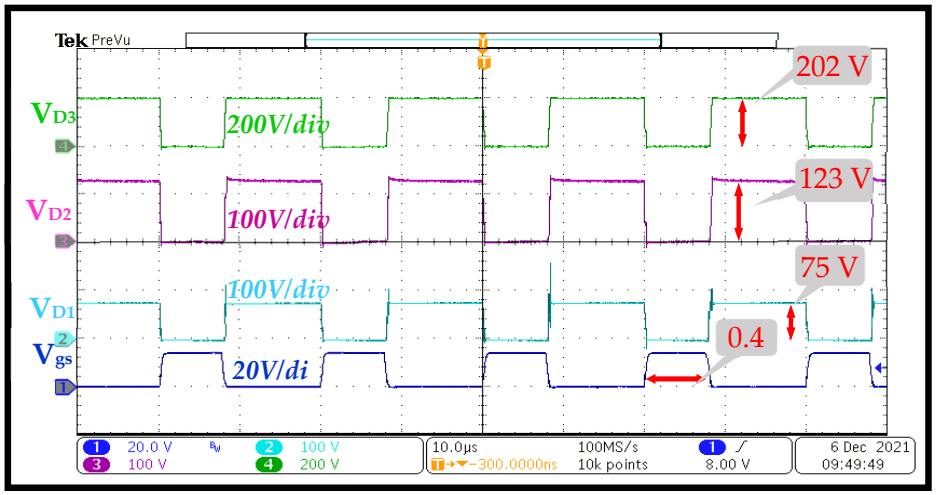

Figure 20. The experimental waveform of (**1**) Duty cycle (V_{gs}) at d = 0.4, (**2**) Diode (D_1) voltage (V_{D1}), (**3**) Diode (D_2) voltage (V_{D2}), and (**4**) Diode (D_3) Voltage (V_{D3}).

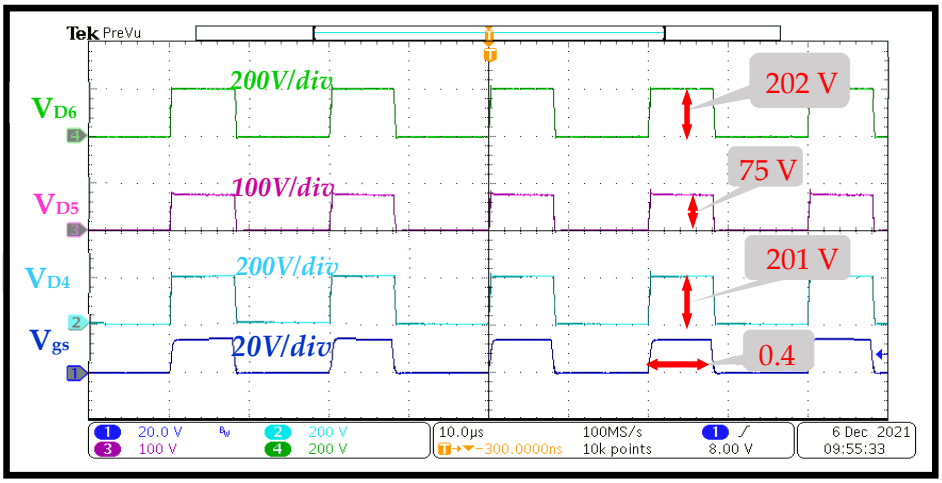

Figure 21. The experimental waveform of (**1**) Duty cycle (V_{gs}) at d = 0.4, (**2**) Diode (D_4) voltage (V_{D4}), (**3**) Diode (D_5) voltage (V_{D5}), and (**4**) Diode (D_6) Voltage (V_{D6}).

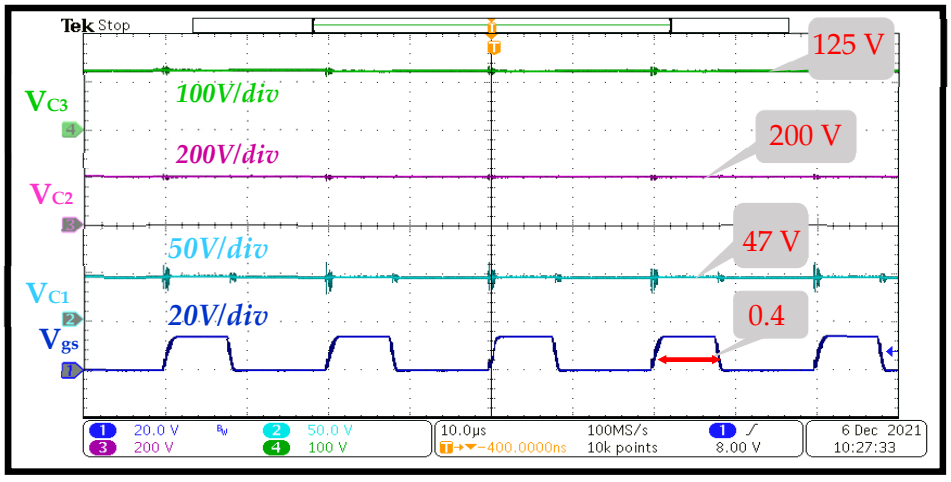

Figure 22. The experimental waveform of (**1**) Duty cycle (V_{gs}) at d = 0.4, (**2**) Capacitor (C_1) voltage (V_{C1}), (**3**) Capacitor (C_2) Voltage (V_{C2}), and (**4**) Capacitor (C_3) Voltage (V_{C3}).

The currents through both inductor L_1 and inductor L_2 are shown in Figure 23. The first inductor carries an average current of about 2.15 A, and the second inductor carries an average current of about 1.3 A for 150 W out power, which is in good agreement with the characteristics equation as described in Section 2. The average output current (i.e., 0.378 A) and the input current (i.e., 3.2 A) is experimentally measured and are shown in Figure 24, respectively.

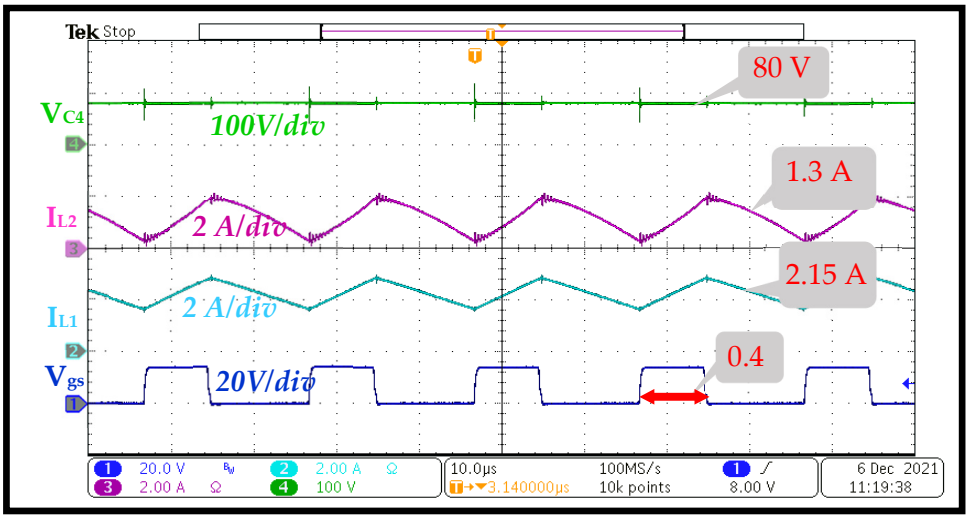

Figure 23. The experimental waveform of (**1**) Duty cycle (V_{gs}) at d = 0.4, (**2**) Inductor (L_1) Current (I_{L1}), (**3**) Inductor (L_2) Current (I_{L2}), and (**4**) Capacitor (C_4) voltage (V_{C4}).

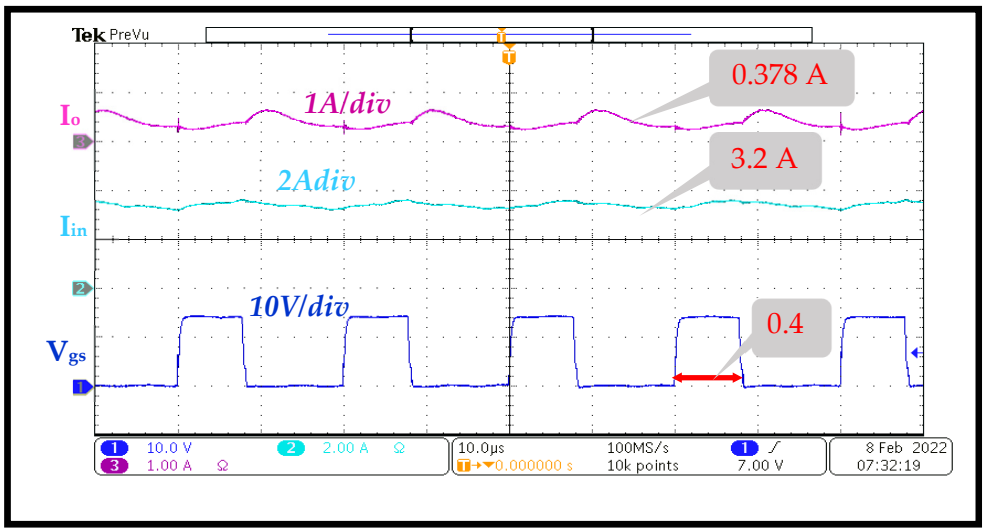

Figure 24. The experimental waveform of (**1**) Duty cycle (V_{gs}) at d = 0.4, (**2**) Input Current (I_{in}), (**3**) Output Current (I_0).

In Table 3 the comparison of the voltage stress across the power MOSFET switch and the power diodes from the simulated results and the experimental results are shown. Both the simulated and experimental results are verified by the characteristics formula for each component.

The efficiency of this proposed converter was measured experimentally by considering various loads, as is shown in Figure 25. All of the data points corresponding to each load were measured, and the duty was varied for the low input voltage to obtain the fixed output voltage (i.e., 400 V). The proposed topology was designed for 48 V input voltage and 400 V output voltage; as a result, the efficiency was reduced for lower input voltage for

the same load. Peak efficiency of about 94.5% was obtained at 150-W output power for this proposed high gain quadratic-based boost DC-DC topology.

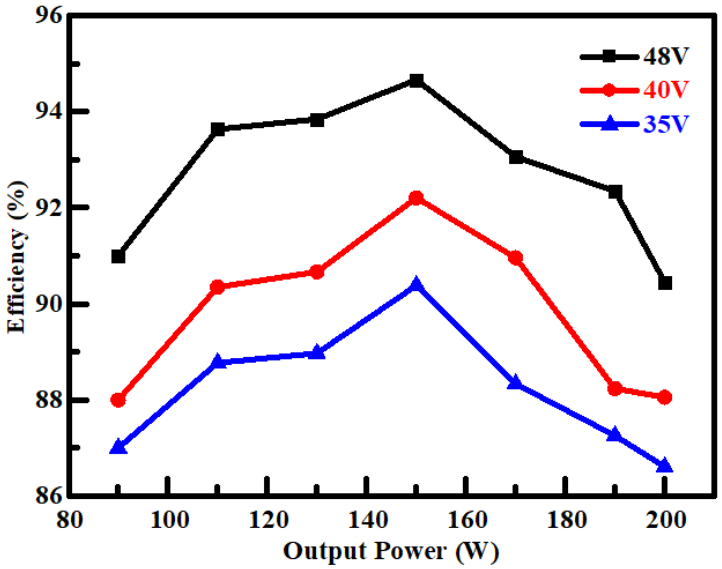

Figure 25. Experimentally measured efficiency plot with the variation of output load power with fixed 400 V output Voltage.

6.3. Stability Analysis

For stability analysis, the PSIM software is used to achieve the open-loop gain, and the phase plot of the system and is shown below. Figure 26 was generated using the PSIM simulation software.

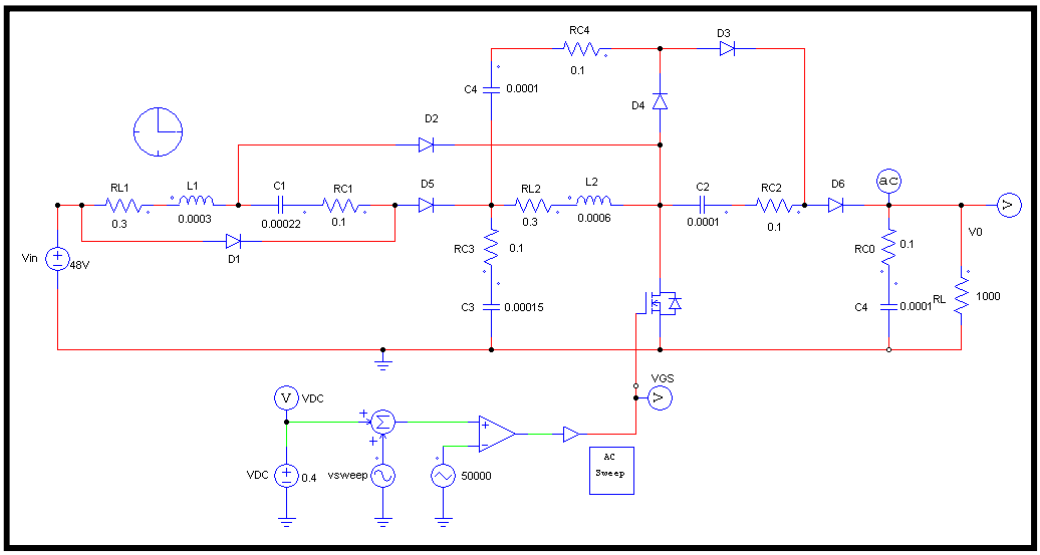

Figure 26. Circuit configuration simulated in PSIM for small signal analysis.

The circuit configuration is exactly constructed in PSIM considering the equivalent series resistance (ESR) of each component. The gain and phase plot of the system is obtained by applying small-signal perturbation with the gate signal. In Figure 27 the corresponding bode plot is shown.

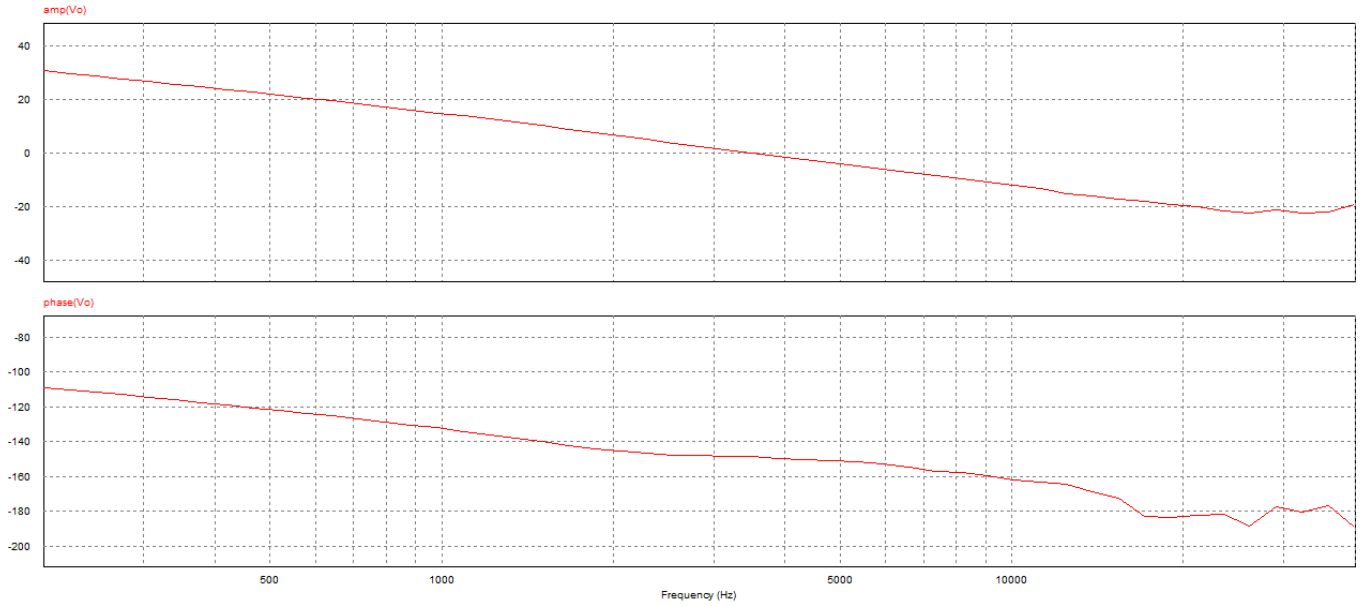

Figure 27. Open-loop Gain plot (in dB) and Phase plot (in Hz) vs. frequency.

Figure 27 demonstrates that the system had a positive gain margin and positive phase margin (i.e., GM 10 dB, PM 25 degree). So, the close loop control can be designed easily for this proposed circuit configuration.

7. Conclusions

In this study, a modified non-isolated high gain quadratic boost topology is proposed and studied, which can achieve high voltage gain with a lower duty ratio that enables its potential application in the renewable energy sector as well as other different applications. The obtainable voltage gain for this topology is verified by both the theoretical and experimental results (i.e., in this study Vin 48 V is stepped up to 400 V output voltage). A base 94.5% efficiency is achieved for 150-W output power from the prototype circuit. The performance of the proposed high gain quadratic boost converter is validated by the experimental prototype, which is also verified by the SIMPLIS software simulation results. The gain and phase plot of the system obtained from PSIM justify that the control can be easily implemented. Further, the efficiency can be improved by reducing the switching loss (i.e., using more efficient power MOSFET) and the loss due to the ESR of the passive component.

Author Contributions: Conceptualization, A.S.J.; Methodology, A.S.J.; software, A.S.J. and T.-H.K.; Validation, A.S.J.; Formal analysis, A.S.J.; PCB design, A.S.J. and T.-H.K.; Investigation, C.-H.L.; Resources, C.-H.L.; Data curation, A.S.J.; Writing—original draft preparation, A.S.J.; writing—review and editing, C.-H.L.; project administration, C.-H.L. and C.-H.C.; funding acquisition, C.-H.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Ministry of Science and Technology, Taiwan, R.O.C., grant number MOST 110-2221-E-011-081 and MOST 110-3116-F-011-002.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Acknowledgments: The authors sincerely appreciate the support from the Taiwan Building Technology Center from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education in Taiwan.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Meinshausen, M.; Meinshausen, N.; Hare, W.; Raper, S.C.; Frieler, K.; Knutti, R.; Frame, D.J.; Allen, M.R. Greenhouse-gas emission targets for limiting global warming to 2 °C. *Nature* **2009**, *458*, 1158–1162. [CrossRef] [PubMed]
2. Shrader-Frechette, K. Mortgaging the future: Dumping ethics with nuclear waste. *Sci. Eng. Ethics* **2005**, *11*, 518–520. [CrossRef] [PubMed]
3. Bagherian, M.A.; Mehranzamir, K. A comprehensive review on renewable energy integration for combined heat and power production. *Energy Convers. Manag.* **2020**, *224*, 113454. [CrossRef]
4. Calcabrini, A.; Muttillo, M.; Weegink, R.; Manganiello, P.; Zeman, M.; Isabella, O. A fully reconfigurable series-parallel photovoltaic module for higher energy yields in urban environments. *Renew. Energy* **2021**, *179*, 1–11. [CrossRef]
5. Sahu, B.; Rincon-Mora, G.A. A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications. *IEEE Trans. Power Electron.* **2004**, *19*, 443–452. [CrossRef]
6. Gaboriault, M.; Notman, A.; House, S.; Park, E. Buck-Boost DC-DC Converter. In Proceedings of the Asia-Pacific Economic Cooperation, Santiago, Chile, 17 November 2004. [CrossRef]
7. Hwu, K.I.; Peng, T.J. A novel buck-boost converter combining KY and buck converters. *IEEE Trans. Power Electron.* **2012**, *27*, 2236–2241. [CrossRef]
8. Ghosh, A. Possibilities and challenges for the inclusion of the electric vehicle (EV) to reduce the carbon footprint in the transport sector: A review. *Energies* **2020**, *13*, 2602. [CrossRef]
9. Emadi, A.; Lee, Y.J.; Rajashekara, K. Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2237–2245. [CrossRef]
10. Hu, X.; Gong, C. A high gain input-parallel output-series DC/DC converter with dual coupled inductors. *IEEE Trans. Power Electron.* **2015**, *30*, 1306–1317. [CrossRef]
11. Cecati, C.; Ciancetta, F.; Siano, P. A multilevel inverter for photovoltaic systems with fuzzy logic control. *IEEE Trans. Ind. Electron.* **2010**, *57*, 4115–4125. [CrossRef]
12. Fan, Z.; Kalogridis, G.; Efthymiou, C.; Sooriyabandara, M.; Serizawa, M.; McGeehan, J. The new frontier of communications research: Smart grid and smart metering. In Proceedings of the Energy-Efficient Computing and Networking: First International Conference, E-energy 2010, Athens, Greece, 14–15 October 2010. [CrossRef]
13. Amjadi, Z.; Williamson, S.S. Power-electronics-based solutions for plug-in hybrid electric vehicle energy storage and management systems. *IEEE Trans. Ind. Electron.* **2010**, *57*, 608–616. [CrossRef]
14. Barreto, L.H.S.C.; Praça, P.P.; Oliveira, D.S.; Silva, R.N.A.L. High-voltage gain boost converter based on three-state commutation cell for battery charging using PV panels in a single conversion stage. *IEEE Trans. Power Electron.* **2014**, *29*, 150–158. [CrossRef]
15. Rosas-Caro, J.C.; Mancilla-David, F.; Mayo-Maldonado, J.C.; Gonzalez-Lopez, J.M.; Torres-Espinosa, H.L.; Valdez-Resendiz, J.E. A transformer-less high-gain boost converter with input current ripple cancelation at a selectable duty cycle. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4492–4499. [CrossRef]
16. Rosas-Caro, J.C.; Ramirez, J.M.; Peng, F.Z.; Valderrabano, A. A DC-DC multilevel boost converter. *IET Power Electron.* **2010**, *3*, 129–137. [CrossRef]
17. Navamani, J.D.; Vijayakumar, K.; Jegatheesan, R. Non-isolated high gain DC-DC converter by quadratic boost converter and voltage multiplier cell. *Ain Shams Eng. J.* **2018**, *9*, 1397–1406. [CrossRef]
18. Hu, X.; Gong, C. A high voltage gain DC-DC converter integrating coupled-inductor and diode-capacitor techniques. *IEEE Trans. Power Electron.* **2014**, *29*, 789–800. [CrossRef]
19. Tang, Y.; Wang, T.; He, Y. A Switched-Capacitor-Based Active-Network. *IEEE Trans. Power Electron.* **2014**, *29*, 2959–2968. [CrossRef]
20. Nguyen, M.; Duong, T.; Lim, Y. Switched-Capacitor-Based Dual-Switch High-Boost. *IEEE Trans. Power Electron.* **2018**, *33*, 4181–4189. [CrossRef]
21. Tran, V.T.; Nguyen, M.K.; Choi, Y.O.; Cho, G.B. Switched-capacitor-based high boost DC-DC converter. *Energies* **2018**, *11*, 987. [CrossRef]
22. Park, K.B.; Moon, G.W.; Youn, M.J. Nonisolated high step-up boost converter integrated with sepic converter. *IEEE Trans. Power Electron.* **2010**, *25*, 2266–2275. [CrossRef]
23. Vazquez, N.; Estrada, L.; Hernandez, C.; Rodriguez, E. The Tapped-Inductor Boost Converter. *IEEE Int. Symp. Ind. Electron.* **2007**, 538–543. [CrossRef]
24. Deng, Y.; Rong, Q.; Li, W.; Zhao, Y.; Shi, J.; He, X. Single-switch high step-up converters with built-in transformer voltage multiplier cell. *IEEE Trans. Power Electron.* **2012**, *27*, 3557–3567. [CrossRef]
25. Dwari, S.; Parsa, L. An efficient high-step-up interleaved DC-DC converter with a common active clamp. *IEEE Trans. Power Electron.* **2011**, *26*, 66–78. [CrossRef]
26. Kim, J.H.; Kim, M.Y.; Yeon, C.O.; Moon, G.W. Analysis and design of Boost-LLC converter for high power density AC-DC adapter. In Proceedings of the 2013 IEEE ECCE ASIA DOWNUNDER: 5th IEEE Annual International Energy Conversion Congress and Exhibition: Crown Convention Centre, Melbourne, Australia, 3–6 June 2013. [CrossRef]
27. Lee, J.Y.; Jeong, Y.S.; Han, B.M. An isolated DC/DC converter using high-frequency unregulated LLC resonant converter for fuel cell applications. *IEEE Trans. Ind. Electron.* **2011**, *58*, 2926–2934. [CrossRef]

28. Lee, S.W.; Do, H.L. Quadratic Boost DC-DC Converter with High Voltage Gain and Reduced Voltage Stresses. *IEEE Trans. Power Electron.* **2019**, *34*, 2397–2404. [CrossRef]
29. Kadri, R.; Gaubert, J.P.; Champenois, G.; Mostefaï, M. Performance analysis of transformless single switch quadratic boost converter for grid connected photovoltaic systems. In Proceedings of the 19th International Conference on Electrical Machines, Rome, Italy, 6–8 December 2010. [CrossRef]
30. Shahir, F.M.; Babaei, E.; Farsadi, M. Extended Topology for a Boost DC-DC Converter. *IEEE Trans. Power Electron.* **2019**, *34*, 2375–2384. [CrossRef]
31. Barreto, L.H.S.C.; Coelho, E.A.A.; Farias, V.J.; DeFreitas, L.C.; Vieira, J.B. An optimal lossless commutation quadratic PWM Boost converter. In Proceedings of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 19–23 March 2002. [CrossRef]
32. Jahangiri, H.; Mohammadpour, S.; Ajami, A. A high step-up DC-DC boost converter with coupled inductor based on quadratic converters. In Proceedings of the 9th Annual International Power Electronics, Drive Systems and Technologies Conference, Tehran, Iran, 1–3 February 2018. [CrossRef]
33. Zhang, S.; Xu, J.; Yang, P. A single-switch high gain quadratic boost converter based on voltage-lift-technique. In Proceedings of the 2012 10th International Power & Energy Conference (IPEC), Ho Chi Minh City, Vietnam, 12–14 December 2012. [CrossRef]
34. Veerachary, M. Design and Analysis of a New Quadratic Boost Converter. In Proceedings of the 2017 National Power Electronics Conference (NPEC), Pune, India, 18–20 December 2017. [CrossRef]
35. Zaid, M.; Lin, C.H.; Khan, S.; Ahmad, J.; Tariq, M.; Mahmood, A.; Sarwar, A.; Alamri, B.; Alahmadi, A. A family of transformerless quadratic boost high gain dc-dc converters. *Energies* **2021**, *14*, 4372. [CrossRef]
36. Porselvi, T.; Arounassalame, M. A novel Single Switch High Gain DC-DC Converter. In Proceedings of the 7th India International Conference on Power Electronics (IICPE), Jaipur, India, 13–15 December 2018. [CrossRef]
37. Khan, S.; Mahmood, A.; Zaid, M.; Tariq, M.; Lin, C.-H.; Ahmad, J.; Alamri, B.; Alahmadi, A. A high step-up dc-dc converter based on the voltage lift technique for renewable energy applications. *Sustainability* **2021**, *13*, 11059. [CrossRef]
38. Fardoun, A.A.; Ismail, E.H. Ultra Step-Up DC–DC Converter With Reduced Switch Stress. *IEEE Trans. Ind. Appl.* **2010**, *6*, 2025–2034. [CrossRef]
39. Ahmad, J.; Zaid, M.; Sarwar, A.; Tariq, M.; Sarwer, Z. A New Transformerless Quadratic Boost Converter with High Voltage Gain. *Smart Sci.* **2020**, *8*, 163–183. [CrossRef]
40. Maroti, P.K.; Padmanaban, S.; Holm-Nielsen, J.B.; Bhaskar, M.S.; Meraj, M.; Iqbal, A. A New Structure of High Voltage Gain SEPIC Converter for Renewable Energy Applications. *IEEE Access* **2019**, *7*, 89857–89868. [CrossRef]
41. Gorji, S.A.; Mostaan, A.; My, H.T.; Ektesabi, M. Non-isolated buck–boost dc–dc converter with quadratic voltage gain ratio. *IET Power Electron.* **2019**, *12*, 1425–1433. [CrossRef]
42. Zhang, N.; Zhang, G.; See, K.W.; Zhang, B. A single-switch quadratic buck-boost converter with continuous input port current and continuous output port current. *IEEE Trans. Power Electron.* **2018**, *33*, 4157–4166. [CrossRef]
43. Rezaie, M.; Abbasi, V. Effective combination of quadratic boost converter with voltage multiplier cell to increase voltage gain. *IET Power Electron.* **2020**, *13*, 2322–2333. [CrossRef]