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An LLC Converter with Capacitive Insulation

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Abstract: Offline power converter products must apply for and pass the national electrical safety code before they can be marketed. The transformers of offline power converters must be made from certificated materials with a high voltage rating and high electrical insulation, which increases the volume of the transformers and the printed circuit boards. In most studies, the miniaturization of a power converter is usually achieved by increasing the conversion efficiency and reducing the heat sink, or by increasing the switching frequency to reduce the size of the transformers. In this paper, the insulation material is reduced to miniaturize the transformer of the LLC converter. The resonant capacitor of the LLC converter is used to meet the requirements of insulation voltage, leakage current, creepage, and clearance. A prototype with the specifications of 12 V and 10 A rated output was built to verify the proposed method.

Keywords: capacitive isolation; LLC converter; leakage current; touch current

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1. Introduction

Offline power converter products must apply for and pass the national electrical safety code before they can be marketed. That means the transformer must be designed and manufactured with certified materials with high voltage rating and high electrical insulation. Therefore, the volume of the transformer and the printed circuit board (PCB) increase. In this paper, the insulation material is reduced to miniaturize the volume of the transformer of the LLC converter. The resonant capacitor of the LLC converter is used to meet the requirements of the electrical safety regulations.

1.1. Safety Capacitors

Typically, for offline converters, safety capacitors are required to suppress the conducted interference due to the electromagnetic interference (EMI) in the alternating current (AC) input. The AC power input is divided into three terminals: line, neutral, and earth ground. The safety capacitors in the line–earth or neutral–earth and the primary side to the secondary side are referred to as Y capacitors, and these capacitors should be certified for safety certification [1].

Y capacitors can be divided into four classes, Y1 to Y4, according to different withstand voltage levels. The smaller the number is, the higher the safety level, as shown in Table 1. Briefly, class Y1 and class Y2 are more commonly used: the Y2 capacitor, called Y2-cap, is used on line–earth or neutral–earth, and the Y1 capacitor, called Y1-cap, should be used on the primary side to the secondary side. In addition, the Y1 capacitor is marked with a rated withstand voltage of 250 V or 275 V. However, the peak pulse withstand voltage of the Y1 capacitor is as high as 8 kV, and the peak pulse withstand voltage of the Y2 capacitor is as high as 5 kV, as shown in Table 1.

Many previous studies have presented circuit architectures using Class Y capacitors as isolation components and these capacitors replace transformers as energy transfer components. However, this is only for LED lighting [2–8] or electric vehicle chargers [9,10], and is characterized by the fact that the secondary side is not in contact with the human body.

Table 1. Classification of class Y capacitors.

Subclass	Type of Insulation Bridged	Range of Rated Voltages	Peak Impulse Voltage before Endurance Test
Y1	Double insulation or reinforced insulation	≤500 V	8.0 kV
Y2	Basic insulation or supplementary insulation	≥150 V ≤300 V	5.0 kV
Y3	Basic insulation or supplementary insulation	≥150 V ≤250 V	None
Y4	Basic insulation or supplementary insulation	≤150 V	2.5 kV

1.2. Test Methods and Requirements of Electrical Safety

For a commercial converter product, it is necessary to satisfy the requirements of the electrical safety test. There are two important certification items as shown in Figure 1: the dielectric strength test and touch current, which is also called the hipot test earth leakage current.

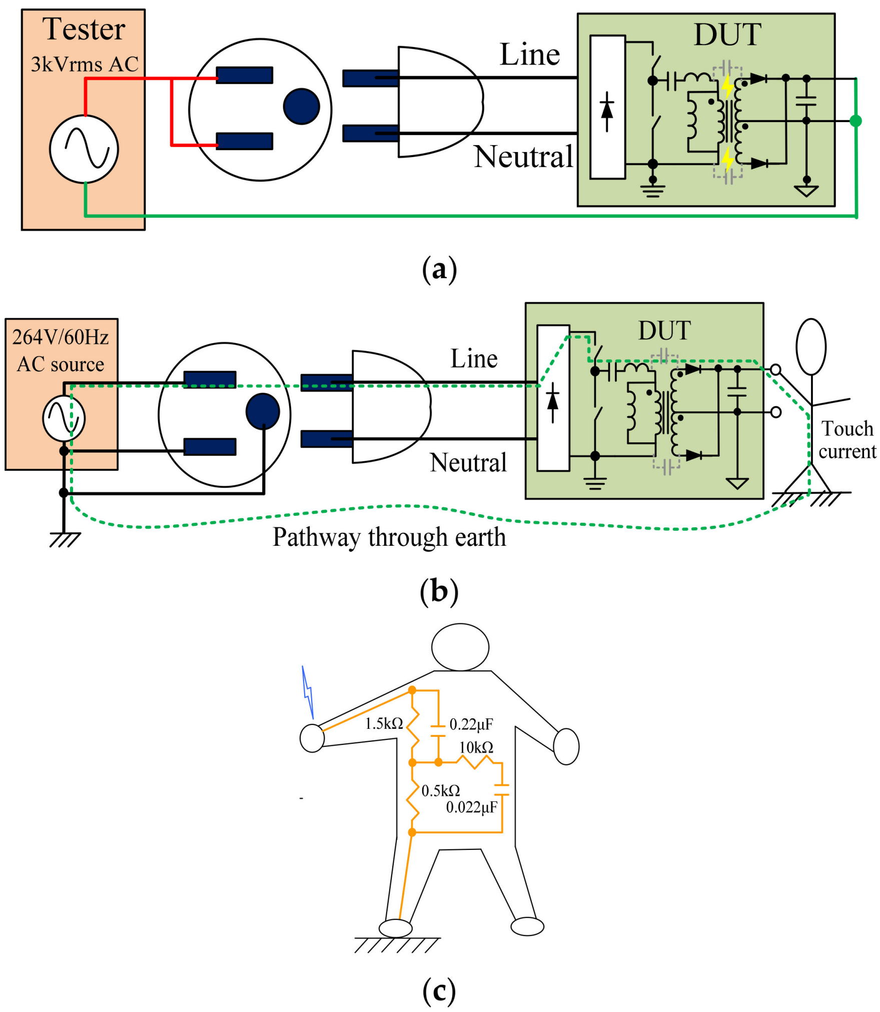


Figure 1. Electrical safety test: (**a**) hipot, (**b**) touch current, (**c**) human body model.

In the design process of a commercial converter product, it is important to satisfy the requirements of electrical safety. For example, for information and communication equipment products, the Underwriters Laboratories Inc. (UL), (Northbrook, IL, USA) and the International Electrotechnical Commission (IEC) define the standard documents of UL60950-1 [11] and IEC62368-1 [12], respectively. One of the requirements in these two standards is the dielectric strength test, commonly called a "dielectric withstand" or "hipot" test. The hipot test is a stress test of the insulation of a device under test (DUT).

As shown in Figure 1a, the hipot test applies a voltage that is much higher than the normal operating voltage to the DUT. For reinforced insulation products with a universal input voltage ranging from 85 Vac to 264 Vac, the required test voltages [11] may be 3000 Vac or equivalent to 4242 Vdc. When the equipment operates, the DUT is applied with a high voltage between the primary side and the secondary side or the earth ground to test its insulation breakdown status.

Table 2 and Figure 1b simply illustrate the touch current defined in the standards [11–13]. The touch current test simulates the effect of a person touching exposed metal parts of a product and detects whether or not the safe level of leakage current flows through the body to the earth. A high enough leakage current can cause an uncontrolled muscular spasm or shock. The equivalent circuit of the human body in [11–13] is defined in Figure 1c.

Table 2. Limitation of touch current.

Type of Equipment	Maximum Touch Current
Information equipment without earth ground connection	0.25 mA
Hand-held information equipment with earth ground connection	0.75 mA
Stationary, pluggable information equipment with earth ground connection	3.5 mA

Converters used in data centers or communication centers are defined as grounded products, so the maximum touch current is 3.5 mA. The maximum touch current for an ungrounded (2 pin plug) product is 0.25 mA.

The creepage distance and clearance distance are also specified in the standard documents [11,12,14], as shown in Table 3. In offline converters used in homes or businesses, components such as PCBs, photo couplers, Y capacitors, transformers, etc., are required to comply with the electrical insulation system standards specified in safety regulations [11,12,14], and must have sufficient clearance distance and creepage distance, as shown in Table 3. In general, the primary-side winding to the secondary-side winding adopts double insulation or reinforced insulation, and the primary-side winding to the core adopts basic insulation. In order to reach a high insulation voltage, the insulation materials [15,16] and internal structure of a transformer are critical. The transformer contains many insulating materials, such as insulation tape [15], bobbins, margin spacers, and triple insulation wire [16], and so the transformer is bulky.

Table 3. Creepage distance and clearance distance.

Insulation Level	Creepage Distance	Clearance Distance
Basic or supplementary insulation	3.2 mm	2.0 mm
Double or reinforced insulation	6.4 mm	4.0 mm

1.3. Prior Arts of Capacitive Insulation in Power Converters

As shown in Figure 2, a high-inductance common-mode choke in [17] works as a line-frequency low-pass filter to suppress touch current under the requirement limitations. However, the high-inductance common-mode choke on the DC output path usually induces lower conversion efficiency and higher cost. The experimental result of touch current is 0.734 mA. The hipot test is not discussed in [17]. In [18], there are two Y3 capacitors used as secondary-side switch zero voltage switching (ZVS) auxiliary components. Because the Y3 capacitors [19] cannot satisfy the requirement for reinforced or double insulation shown in Table 1, the main safety insulation and the energy transmission path are still via the transformer.

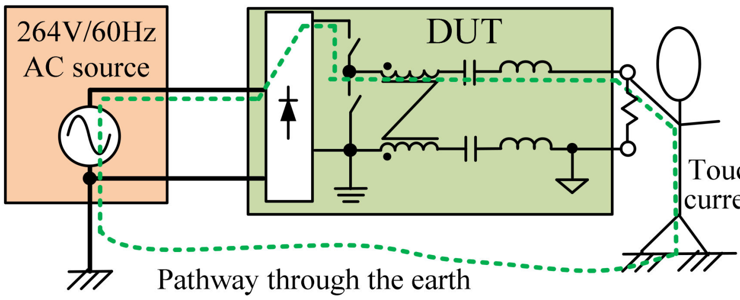
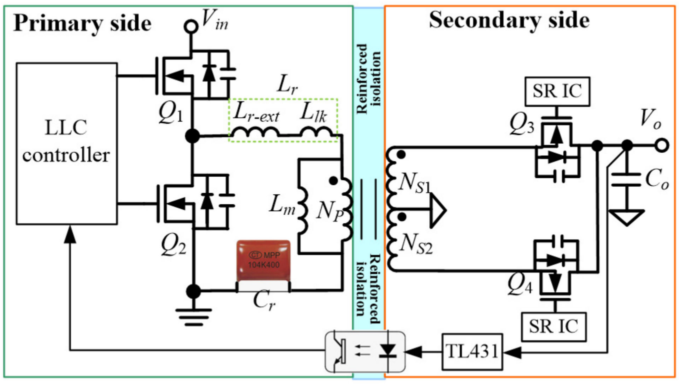
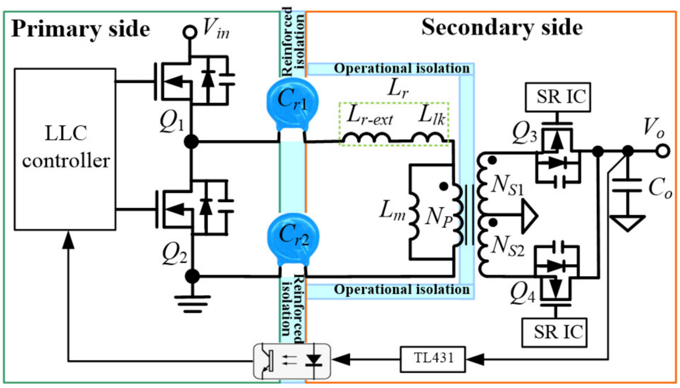


Figure 2. Conventional capacitor isolation converter.

The traditional LLC converter is widely used because of its simple circuit structure and ZVS function. The basic structure is shown in Figure 3a. The resonance between the capacitor C_r, the resonant inductor L_r, and the transformer magnetizing inductance L_m can realize the ZVS of the switches Q_1 and Q_2, achieving high conversion efficiency. In many low-power applications, the leakage inductance L_{lk} of the transformer is also used as the resonant inductor L_r. On the other hand, the resonant capacitor C_r generally adopts the plastic film capacitor, which is characterized by its high capacitance and low cost.



(**a**)



(**b**)

Figure 3. *Cont.*

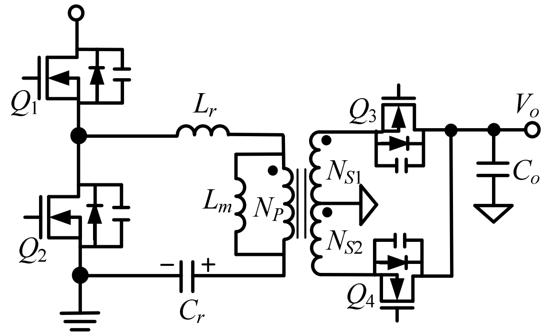


Figure 3. Circuit structures: (**a**) traditional LLC converter, (**b**) proposed architecture, (**c**) simplified architecture of (**a**,**b**).

In the LLC converter presented in [20], the resonant capacitor C_r is replaced by the Y1 capacitor [21] to meet the clearance and creepage isolation requirements defined by the safety regulations. However, considering the design of EMI common mode noise, insulation current, and LLC voltage gain curve, the transformer is retained, but the transformer does not need to adhere to the electrical isolation requirements. The transformer as a whole can be regarded as a secondary component and only requires a basic insulation grade. Therefore, this transformer does not use triple insulated wire, and can use high-efficiency wires such as Litz wire and flat wires that are not reinforced insulation grades to minimize the insulation material in the transformer. Hence, the transformer structure and volume can be reduced so that a compact design of the magnetic component can be achieved.

In addition, since the rated withstand voltage of a typical triple insulated wire is only 3 kVac, applications requiring higher-voltage insulation such as power supplies for industrial equipment requiring 4.2 kVac [22] or auxiliary power supplies for solid state transformer systems with an insulation voltage of 25 kV [23] require expensive transformer insulation materials, resulting in more volume and cost. The proposed method only requires increasing the number of Y-capacitors in series to achieve higher insulation voltage without redesigning the transformer design.

2. Proposed Circuit Configuration

Figure 3a shows the circuit structure of a typical LLC converter. The plastic film capacitor C_r works as a resonant capacitor, which is usually connected between the primary winding of the transformer and the primary side ground.

The proposed circuit is shown in Figure 3b. The single resonant capacitor is divided into two Y1 capacitors, named C_{r1} and C_{r2}, so that safety regulations can be met. In the proposed LLC converter, the transformer plays a role in the functions of the resonant tank, voltage gain design, and common mode touch current blocker. The transformer is necessary for the reasons above. However, the volume and power density of the transformer are still improved via the reduction in transformer insulation materials.

Since the proposed method can keep the original transformer and minimize the insulation material in the transformer, the touch current is solved by isolation and the size is reduced. The circuits in Figure 3a,b have the same equivalent circuit shown in Figure 3c.

Compared with the method in [24], the mathematical theory of the proposed method is the same as the conventional LLC converter, so it can be driven by existing LLC control ICs and can be easily implemented for industrial applications.

3. Design Considerations

For design convenience, the components are chosen based on the traditional LLC converter and then the capacitor equivalent theorem to obtain C_{r1} and C_{r2}. Table 4 shows the circuit specifications.

Table 4. Circuit specifications.

Parameter	Specification
Rated input voltage (V_{in})	370 V~390 V
Rated output voltage (V_o)	12 V
Rated output current (I_o)	10 A
Resonant frequency (f_s)	230 kHz
Minimum switching frequency ($f_{sw(\min)}$)	210 kHz
Magnetizing inductance divided by resonant inductance (k)	4
Maxima duty cycle (D_{max})	0.42
Estimated efficiency (η)	96%

3.1. Design of Transformer T_1

For the minimization of the LLC converter, the ferrite core LP22 with material JPP95 is chosen as T_1, with a saturation flux density of 0.35 T at 120 °C according to the data sheet. Considering the component tolerance and the de-rating operation for mass production, the maximum flux density is designed to be 0.28 T. The minimum primary turns of T_1 are designed as below:

$$N_{P(\min)} = \frac{V_{in} \cdot D_{max}}{4 \cdot B_{max} \cdot A_e \cdot f_{sw(\min)}} = 25.3 \text{ Turns}, \quad (1)$$

For the convenience of production of the windings, the secondary turns are set as N_{S1} = N_{S2} = 2. It is suitable to design the turn ratio of T_1 as an integer such that the value of N_P is chosen as 28 turns to obtain a turn ratio of 14.

3.2. Design of Resonant Tank

By considering the unpredictable parasitic impedance caused by PCB traces, in practice, the voltage gain operating point at full load is usually set to be slightly lower than 1, generally 0.98. Based on N_P = 28, the equivalent load impedance $R_{ac\text{-}FL}$ at full load and the equivalent load impedance $R_{ac\text{-}LL}$ at light load can be determined as follows:

$$R_{ac\text{-}FL} = \frac{8 \cdot N_P^2}{\pi^2} \cdot R_o = 190.6\ \Omega, \quad (2)$$

$$R_{ac\text{-}LL} = 10 \cdot \frac{8 \cdot N_P^2}{\pi^2} \cdot R_o = 1960.5\ \Omega, \quad (3)$$

Compared to conventional LLC converters, which generally use a film capacitor as a resonant capacitor, the capacitance of the film capacitor has a low temperature coefficient of $\pm 5\%$, so the capacitance can be considered a constant value when designing a conventional LLC converter. The proposed circuit uses Y1 capacitors for the resonant tank. Considering that the capacitance of the Z5U grade capacitor will change with the temperature, the higher the temperature is, the lower the capacitance. According to its data sheet [21], the capacitance variation curve is built in Figure 4 to establish that the capacitance of the 4.7 nF Y1 capacitor at a high temperature of 70 °C and 85 °C will decline by 35% and 50%, respectively, which is a critical point for designing the resonant tank.

The relationship between C_{r1}, C_{r2} and C_r is as follows:

$$C_{r1} = C_{r2} = 2C_r, \quad (4)$$

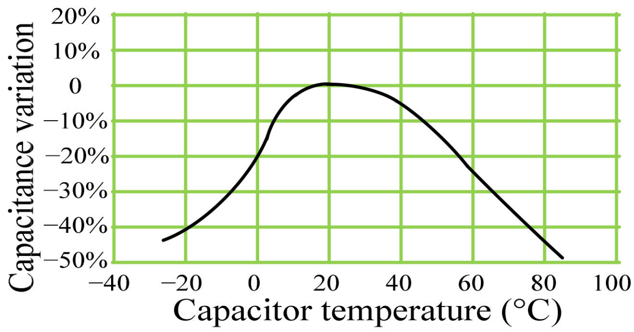


Figure 4. Capacitance change curve of C_{r1} and C_{r2}.

Since the maximum capacitance of the Y1 capacitor is 4.7 nF, considering the capacitance and volume, both C_{r1} and C_{r2} are designed as 9.4 nF (two 4.7 nF Y1 capacitors paralleled) in this prototype. Then, the value of L_r can be worked out as follows:

$$L_r = \frac{1}{2 \cdot \pi^2 \cdot f_r^2 \cdot C_r} = 160\ \mu\text{H}, \tag{5}$$

The value of L_m and the value of L_{lk} are as follows:

$$L_m = 4 \cdot L_r = 640\ \mu\text{H},\ L_{lk} = 17.6\ \mu\text{H}, \tag{6}$$

Eventually, the resonance frequencies f_s and f_p, and the corresponding quality factors can be calculated as follows:

$$f_s = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} = 229.7\ \text{kHz}, \tag{7}$$

$$f_p = \frac{1}{2\pi\sqrt{(L_m + L_r) \cdot C_r}} = 102.7\ \text{kHz}, \tag{8}$$

$$Q_{FL} = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac\text{-}FL}} = 1.211, \tag{9}$$

$$Q_{LL} = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac\text{-}LL}} = 0.1211, \tag{10}$$

3.3. Voltage Gain for Light and Full Load

As shown in Figure 5, the voltage gain curves at 10% load and 100% load can be obtained. From this figure, it can be seen that the minimum V_{in} at 100% load is 380 V/1.03 = 369 V, corresponding to the circuit specifications shown in Table 2. In addition, the full-load voltage gain and the light-load voltage gain can be expressed as follows, where $\omega = 2\pi f$:

$$M_{FL} = \left| \frac{\left(\frac{\omega^2}{\omega_p^2}\right) \cdot \frac{k}{1+k}}{\left(i \cdot \frac{\omega}{\omega_s} \cdot \left(1 - \frac{\omega^2}{\omega_s^2}\right) \cdot Q_{FL} \cdot k\right) + \left(1 - \frac{\omega^2}{\omega_p^2}\right)} \right|, \tag{11}$$

$$M_{LL} = \left| \frac{\left(\frac{\omega^2}{\omega_p^2}\right) \cdot \frac{k}{1+k}}{\left(i \cdot \frac{\omega}{\omega_s} \cdot \left(1 - \frac{\omega^2}{\omega_s^2}\right) \cdot Q_{LL} \cdot k\right) + \left(1 - \frac{\omega^2}{\omega_p^2}\right)} \right|, \tag{12}$$

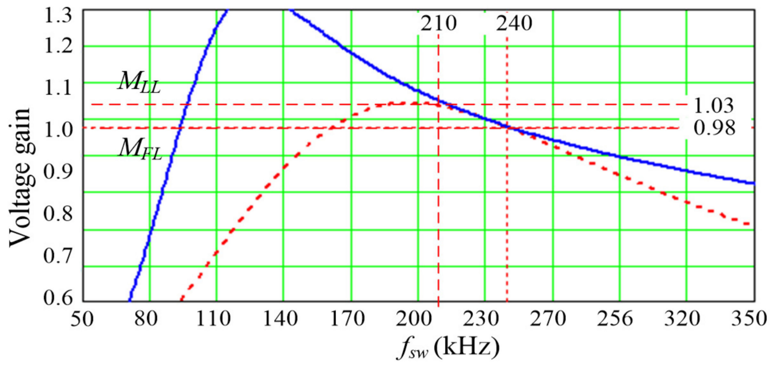


Figure 5. Voltage gain curves at 10% load and 100% load.

3.4. Loss Breakdown Analysis

The existing commercial 150 W LLC module from Asian Power Device Inc. (Taipei, Taiwan) is used as a reference in this paper. In order to make a fair comparison, the proposed prototype in this paper will adopt the same controller IC and MOSFETs as a reference. The proposed prototype only miniaturizes the magnetic component and replaces the resonant capacitor C_r using the film capacitor with high-side and low-side capacitors using Y1 capacitors. Due to the much lower capacitance of Y1 capacitors than that of film capacitors, the resonant tank parameter is redesigned to enhance the output power with higher switching frequency. The current of primary winding and the current of secondary winding can be calculated as follows:

$$i_{L(\mathrm{pk})} = \frac{n \cdot V_o}{4 \cdot L_m \cdot f_r} = 0.285\ \mathrm{A}, \tag{13}$$

$$i_{Lr(\mathrm{rms})} = \sqrt{\frac{V_o^2}{8} \cdot \left[\left(\frac{n}{2 \cdot L_m \cdot f_r} \right)^2 + \left(\frac{\pi}{n \cdot R_o} \right)^2 \right]} = 0.819\ \mathrm{A}, \tag{14}$$

$$i_{Ns1(\mathrm{rms})} = i_{Ns2(\mathrm{rms})} = I_o \cdot \frac{\pi}{4} = 3.535\ \mathrm{A}, \tag{15}$$

$$i_{Co(\mathrm{rms})} = \sqrt{\left(I_o \cdot \frac{\pi}{2\sqrt{2}} \right)^2 - I_o^2} = 4.838\ \mathrm{A}, \tag{16}$$

The magnetic flux of L_m also can be calculated as in (17).

$$B_{max\text{-}Lm} = \frac{L_m \cdot i_{Lm(\mathrm{pk})}}{N_P \cdot A_{e(T1)}} = 0.274\ \mathrm{T}, \tag{17}$$

Based on the manufacturability of the T_1, the N_P is determined to be made with 28 turns of Litz wire with a diameter of 0.1 mm and 30 strands. N_{S1} and N_{S2} are both made with two turns of Litz wire with a diameter of 0.1 mm and 120 strands.

Eventually, the DC resistance of each winding is measured to be DCR_{NP} = 9.2 mΩ and DCR_{NS1} = DCR_{NS2} = 164 µΩ so as to obtain the copper loss of T_1, as shown in (18) and (19). The core loss of T_1 is also obtained from (20) with core characteristics: $V_{e(T1)}$ = 2480 mm^3 and $P_{CV(T1)}$ = 1800 kW/m^3.

$$P_{copp\text{-}Np} = DCR_{Np} \left(\frac{i_{Lr(\mathrm{pk})}}{\sqrt{2}} \right)^2 = 6.16\ \mathrm{mW}, \tag{18}$$

$$P_{copp\text{-}Ns} = DCR_{Ns1} \left(i_{SR(\mathrm{rms})} \right)^2 + DCR_{Ns2} \left(i_{SR(\mathrm{rms})} \right)^2 = 17\ \mathrm{mW}, \tag{19}$$

$$P_{core\text{-}T1} = V_{e(T1)} \cdot P_{CV(T1)} = 4.464\ \mathrm{W}, \tag{20}$$

$$P_{T1} = P_{copp\text{-}Np} + P_{copp\text{-}Ns} + P_{core\text{-}T1} = 4.487 \text{ W}, \tag{21}$$

The voltage ratings of the resonant capacitors C_{r1} and C_{r2} are determined by (22) to (25):

$$v_{Cr(\min)} = V_{in} - n \cdot V_o - \sqrt{\frac{\left(\frac{I_o \cdot \pi}{2 \cdot n}\right)^2 - i^2_{L_m(\text{pk})}}{\frac{C_r}{L_r}}} = -65.4 \text{ V}, \tag{22}$$

$$v_{Cr1(\min)} = v_{Cr2(\min)} = \frac{1}{2} \cdot v_{Cr(\min)} = -32.7 \text{ V}, \tag{23}$$

$$v_{Cr(\max)} = V_{in} - v_{Cr(\min)} = 452 \text{ V}, \tag{24}$$

$$v_{Cr1(\max)} = v_{Cr2(\max)} = \frac{1}{2} \cdot v_{Cr(\max)} = 226 \text{ V}, \tag{25}$$

The peak current and the RMS current of $L_{r\text{-}ext}$ can be calculated as shown in (26) and (27):

$$i_{Lr(\text{pk})} = i_{Cr1(\text{pk})} = i_{Cr2(\text{pk})} = \left(V_{in} - n \cdot V_o - v_{Cr(\min)}\right) \cdot \sqrt{\frac{L_r}{C_r}} = 1.158 \text{ A}, \tag{26}$$

$$i_{Lr(\text{rms})} = i_{Cr1(\text{rms})} = i_{Cr2(\text{rms})}, \tag{27}$$

In (5), it is known that L_r is 160 μH and L_{lk} is 17.6 μH, and so the required value of $L_{r\text{-}ext}$ should be 142.4 μH. Hence, an RM6 ferrite core is chosen with material JPP95 with the following key characteristics: $A_{e(Lr\text{-}ext)}$ = 37.5 mm^2 and $V_{e(Lr\text{-}ext)}$ = 1090 mm^3. Set $B_{max\text{-}Lr}$ = 0.28 T; then, the minimum number of turns required is calculated as follows:

$$N_{Lr\text{-}ext} = \frac{L_{r\text{-}ext} \cdot i_{Lr(\text{pk})}}{B_{max} \cdot A_{e(Lr\text{-}ext)}} = 16.1 \text{ Turns}, \tag{28}$$

Based on the manufacturability of $L_{r\text{-}ext}$, N_P is determined to be made with 30 turns of Litz wire with a diameter of 0.1 mm and 20 strands. Finally, the measured DC resistance of $L_{r\text{-}ext}$ is DCR_{Lr} = 0.33 Ω to obtain the copper loss of $L_{r\text{-}ext}$, as shown in (29). The core loss of $L_{r\text{-}ext}$ is also obtained as shown in (31) with the following core characteristics: $A_{e(Lr\text{-}ext)}$ = 36.6 mm^2, $V_{e(Lr\text{-}ext)}$ = 1090 mm^3, and $P_{CV(Lr\text{-}ext)}$ = 500 kW/m^3:

$$P_{copp\text{-}Lr\text{-}ext} = DCR_{Lr}\left(\frac{i_{Lr(\text{pk})}}{\sqrt{2}}\right)^2 = 0.235 \text{ W}, \tag{29}$$

$$B_{max\text{-}Lr} = \frac{L_{r\text{-}ext} \cdot i_{Lr(\text{pk})}}{N_{Lr\text{-}ext} \cdot A_{e(Lr\text{-}ext)}} = 0.15 \text{ T}, \tag{30}$$

$$P_{core\text{-}Lr\text{-}ext} = V_{e(Lr\text{-}ext)} \cdot P_{CV(Lr\text{-}ext)} = 1.09 \text{ W}, \tag{31}$$

Finally, the total loss of $L_{r\text{-}ext}$ is 1.325 W, as shown in (32):

$$P_{Lr\text{-}ext} = P_{copp\text{-}Lr\text{-}ext} + P_{core\text{-}Lr\text{-}ext} = 1.325 \text{ W}, \tag{32}$$

Here, we set the key parameters as R_{on1} = R_{on2} = 0.33 Ω, Q_{g1} = Q_{g2} = 13 nC, and v_{gs1} = v_{gs2} = 11 V for Q_1 and Q_2 to design the driving loss and conduction loss, which can be calculated as shown in (33) and (34). Due to the ZVS turn-on function of the LLC converter, the switching loss is unnecessary to consider:

$$P_{driving(Q1,Q2)} = 2 \cdot Q_{g(Q1,Q2)} \cdot V_{gs(Q1,Q2)} \cdot f_r = 66 \text{ mW}, \tag{33}$$

$$P_{cond(Q1,Q2)} = 2 \cdot \frac{\left(R_{on(Q1,Q2)} \cdot i^2_{Lr(\text{rms})}\right)}{2} = 0.221 \text{ W}, \tag{34}$$

$$P_{Q1,Q2} = P_{cond(Q1,Q2)} + P_{driving(Q1,Q2)} = 0.287 \text{ W}, \quad (35)$$

Here, the key parameters, namely, $R_{on3} = R_{on4} = 2.65$ mΩ, $Q_{g3} = Q_{g4} = 37$ nC, and $v_{gs3} = v_{gs4} = 8$ V for Q_3 and Q_4, can be set to design the driving loss, and conduction loss can be determined as shown in (36) and (37). Due to the ZVS turn-on function of SR switches, the switching loss is unnecessary to consider. Two 470 µF/25 V solid capacitors are applied to the output capacitor C_o. The data sheet provided by the manufacturer shows that the ESR of this capacitor is 16 mΩ and the corresponding ripple current capability is 4.65 A. C_o needs to withstand the 4.83 A current ripple, as shown in (39). The combinational ESR_{Co} is 8 mΩ. Therefore, the loss of the C_o is shown in (40). Eventually, the total loss of the proposed LLC converter is shown in (41). Additionally, the estimated efficiency is 94.7%. The analysis of the loss breakdown is shown in Figure 6. The component list of the prototype is shown in Table 5.

$$P_{driving(SR)} = 2 \cdot Q_{g(SR)} \cdot V_{gs(SR)} \cdot f_r = 0.136 \text{ W}, \quad (36)$$

$$P_{cond(SR)} = 2 \cdot R_{on(SR)} \cdot i^2_{SR(\text{rms})} = 0.275 \text{ W}, \quad (37)$$

$$P_{SR} = P_{cond(SR)} + P_{driving(SR)} = 0.411 \text{ W}, \quad (38)$$

$$i_{C_o(\text{rms})} = \sqrt{i^2_{SR(\text{rms})} - I_o^2} = 4.83 \text{ A} \quad (39)$$

$$P_{Co} = \left(i_{Co(\text{rms})}\right)^2 \cdot ESR_{Co} = 0.187 \text{ W} \quad (40)$$

$$P_{total} = P_{T1} + P_{Lr\text{-}ext} + P_{Q1,Q2} + P_{SR} + P_{Co} = 6.697 \text{ W} \quad (41)$$

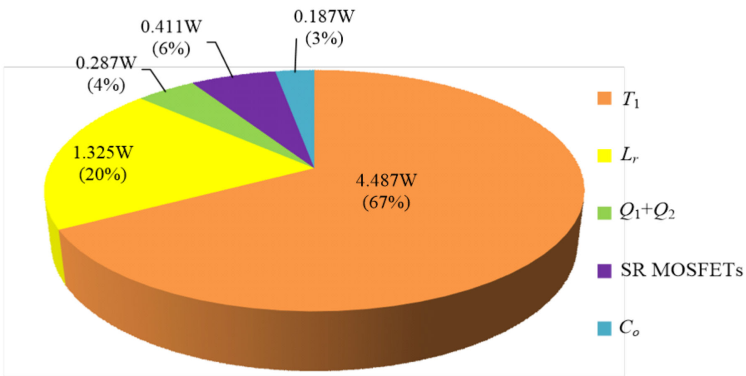


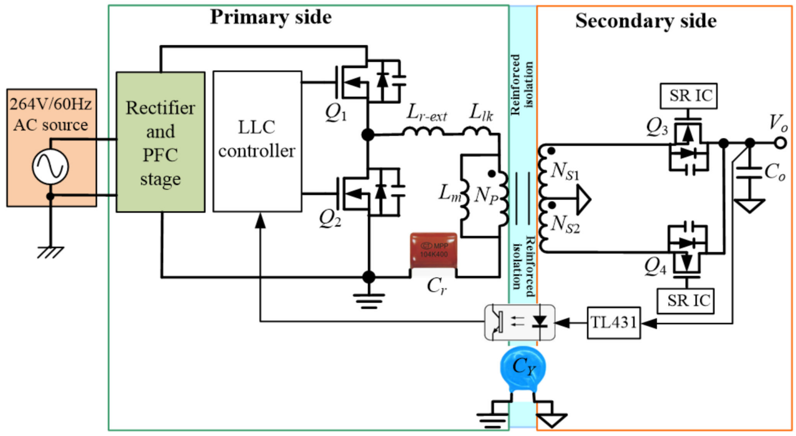
Figure 6. Loss breakdown analysis.

Table 5. Component specifications.

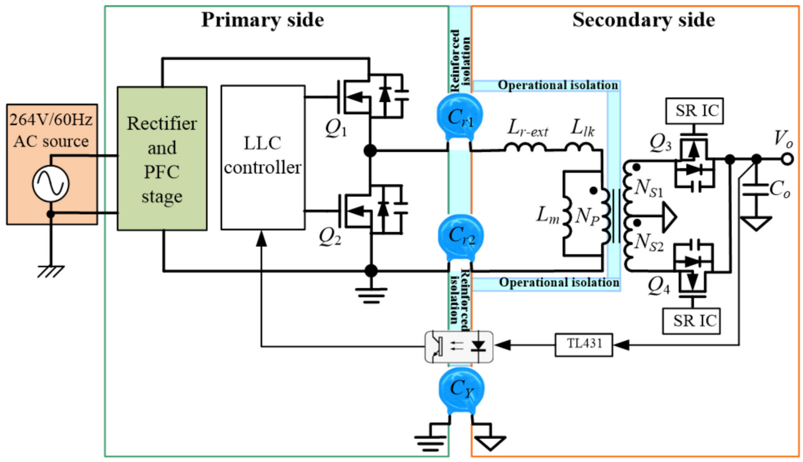
Symbols	Description
C_{r1}, C_{r2}	4.7 nF//4.7 nF, DE1E3KX472M, Murata, Kyoto, Japan, 300 Vac Class Y1 Reinforced Insulation Capacitors with IEC384-14 Safety Recognized
$L_{r\text{-}ext}$	RM6, 142.4 µH, JPP95, A-core Inc., Jiangmen, China
T_1	LP22, 640 µH, 28:2:2, JPP95, A-core Inc., Jiangmen, China
Q_1, Q_2	IPD60R360P7S, DPAK, Infineon AG, Warstein, Germany
Q_3, Q_4	BSC028N06NS, TDSON8, Infineon AG, Warstein, Germany
C_o	470 µF//470 µF; Conductive Polymer Aluminum Cap, APAQ Co., Maioli, Taiwan
LLC Controller IC	HR1001A, Monolithic Power Systems Inc., Kirkland, WA, USA
SR Controller IC	MP6924, Monolithic Power Systems Inc., Kirkland, WA, USA

4. Experimental Results

The traditional circuit shown in Figure 7a and the proposed circuit shown in Figure 7b adopt individual Y1 capacitors, named C_Y, to remove common-mode EMI without affecting circuit behavior. These two have the same input voltage, output voltage, primary-side LLC controller IC, secondary-side SR controller IC, and MOSFETs, except for resonant parameters and transformer parameters.



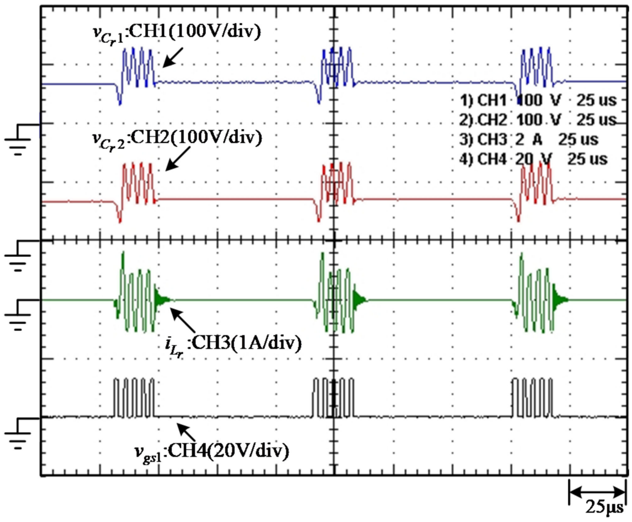
(**a**)



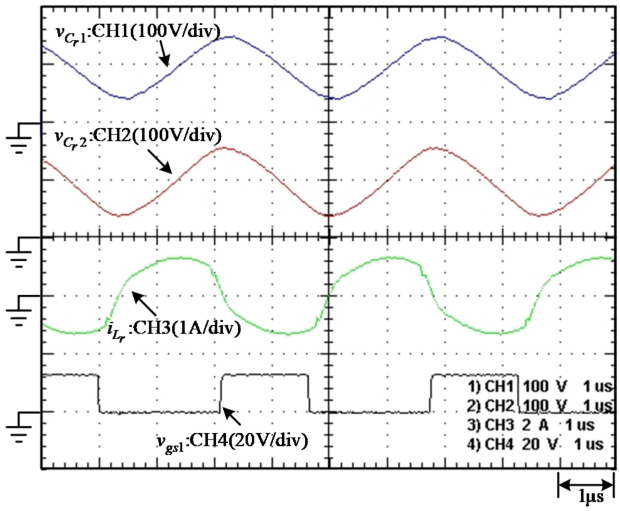
(**b**)

Figure 7. Actual circuit structure: (**a**) traditional; (**b**) proposed.

Figure 8a–c present the measured waveforms of v_{cr1}, v_{cr2}, i_{Lr}, and v_{gs2} at 10%, 50%, and 100% load, respectively. It can be seen that when the load is lower than 40%, the converter enters burst mode operation, which is a common technology that improves the efficiency of the LLC at a light load for the commercial LLC IC in industry applications. As the load current increases, the amplitudes of v_{Cr1}, v_{Cr2}, and i_{Lr} will increase. It can be observed that the operation of the burst mode allows the light-load frequency to be reduced to maintain a relatively high i_{Lr}, so that the resonant tank has enough energy for the output capacitance C_{oss} of the MOSFET to be charged and discharged, as well as to obtain near-ZVS. As the load increases, i_{Lr} increases, and complete ZVS can be achieved. Figure 9a–c show the measured waveforms of v_{gs1}, v_{gs2}, v_{ds1}, and v_{ds2} at 10%, 50, and 100% load, respectively. Both switches are near-ZVS or ZVS.



(**a**)



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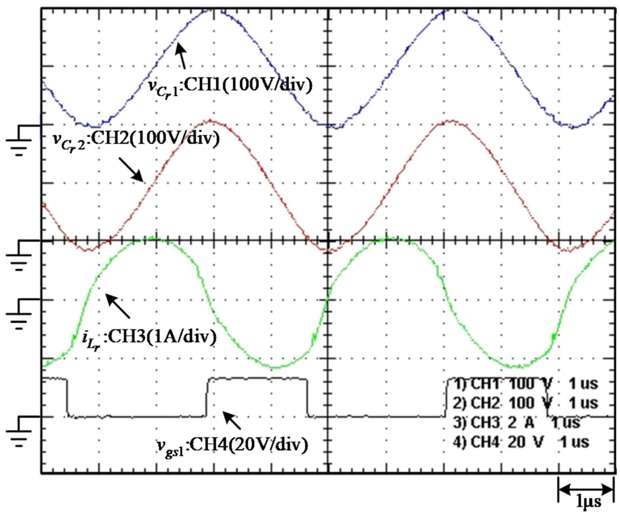
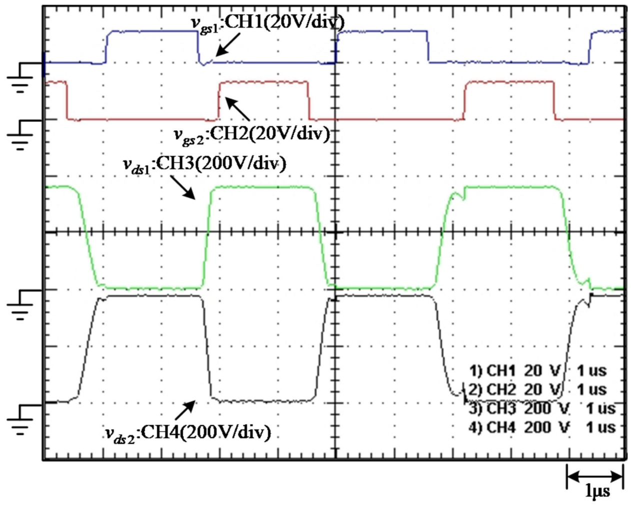
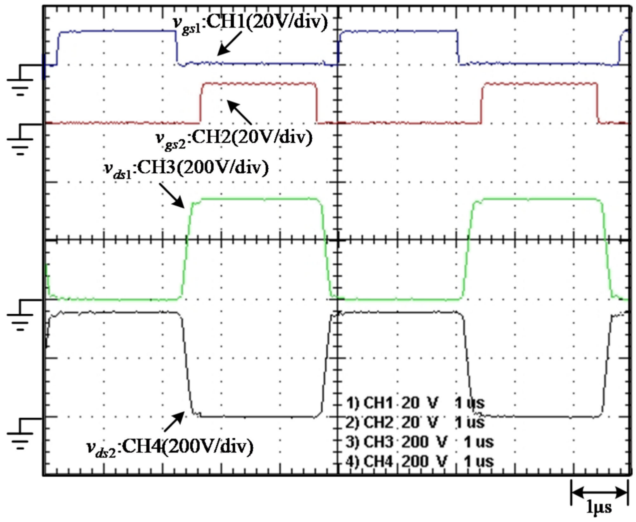


(**c**)

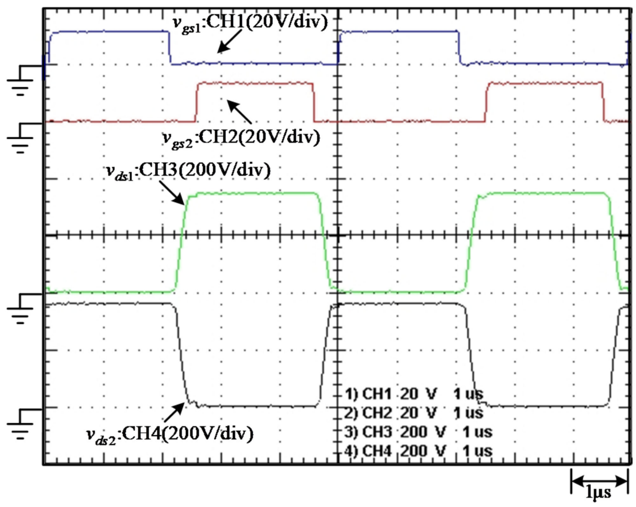
Figure 8. Measured waveforms: v_{cr1}, v_{cr2}, i_{Lr}, and v_{gs2} under (**a**) 10% load, (**b**) 50% load, and (**c**) 100% load.



(**a**)



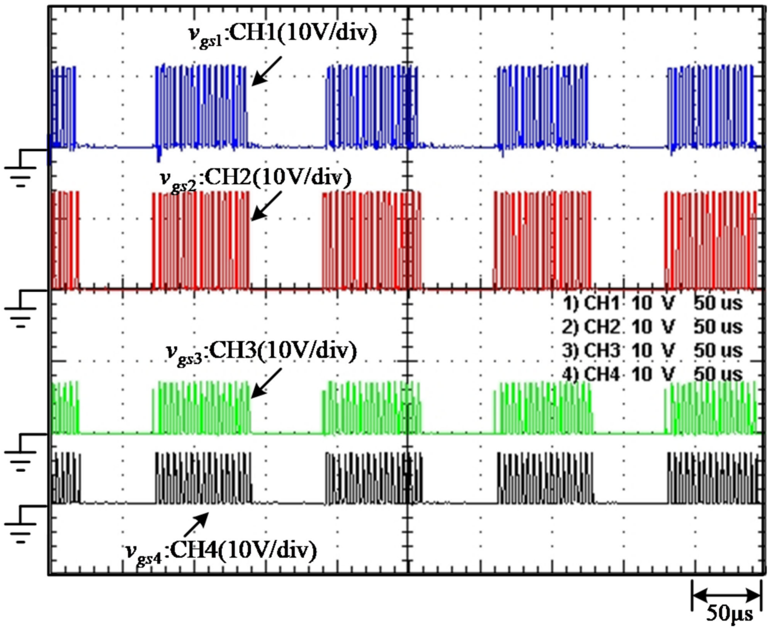
(**b**)



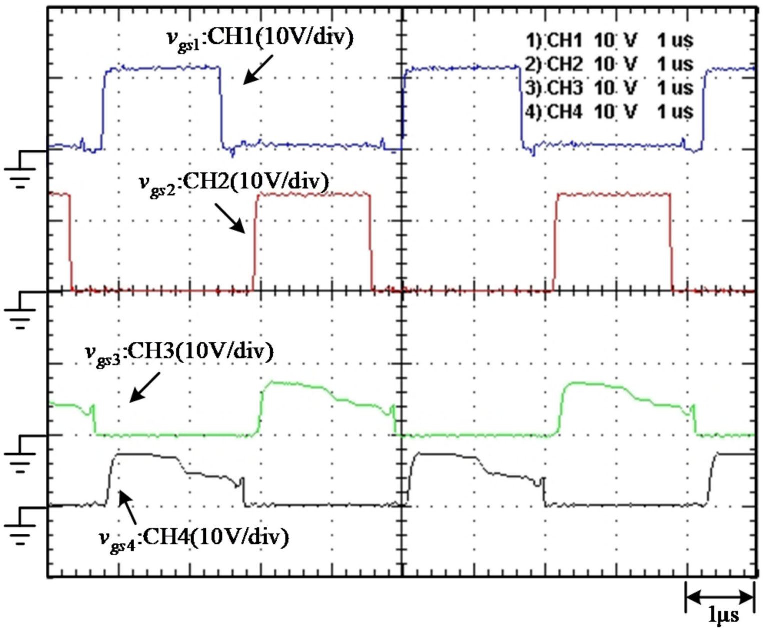
(**c**)

Figure 9. Measured waveforms: v_{gs1}, v_{gs2}, v_{ds1}, and v_{ds2} under (**a**) 10% load, (**b**) 50% load, and (**c**) 100% load.

Figure 10a–c display the measured waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and v_{gs4} at 10%, 50%, and 100% load, respectively. All the switches operate as the traditional LLC converter. The reduction in the voltages on v_{gs3} and v_{gs4} is a patented driving mechanism [25]. This mechanism can keep v_{ds3} and v_{ds4} at around −40 mV, even when the current through the MOSFET is low. This function puts the gate driving voltage at a low level when the synchronous MOSFET is turned off, which shortens the turn-off time. When v_{ds3} or v_{ds4} rises to trigger the turn-off threshold of +40 mV, the gate driving voltage drops to zero rapidly.

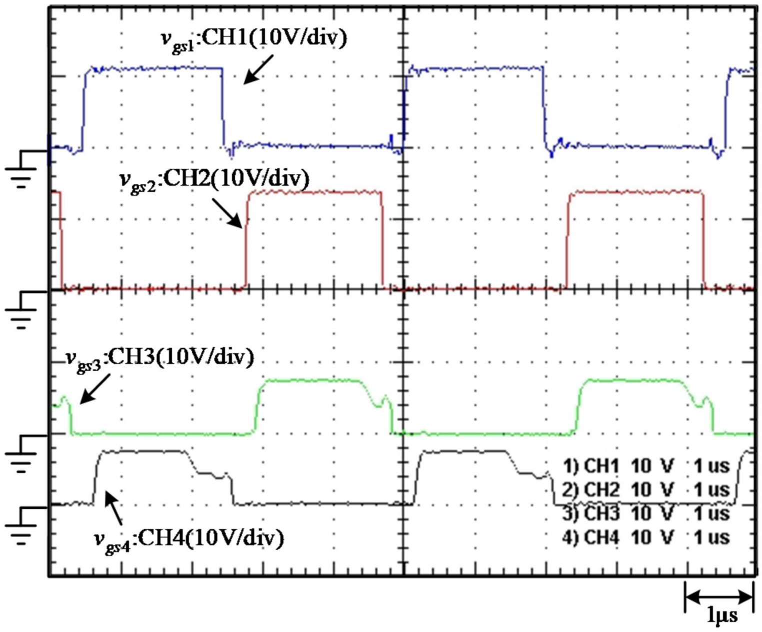


(**a**)



(**b**)

Figure 10. *Cont*.



(**c**)

Figure 10. Measured waveforms: v_{gs1}, v_{gs2}, v_{gs3}, and v_{gs4} under (**a**) 10% load, (**b**) 50% load, and (**c**) 100% load.

All the measured efficiency results do not include the front-end bridge rectifier and power factor correction stage. From Figure 11, it can be observed that the efficiency throughout the load range is above 87.5% and can be up to 95%. Even though the prototype is designed with a specification of DC input voltage from 370 V to 390 V, the final prototype can still work with lower input voltage down to 340 V DC and perform similar conversion efficiency, which is helpful to extend the hold-up time further.

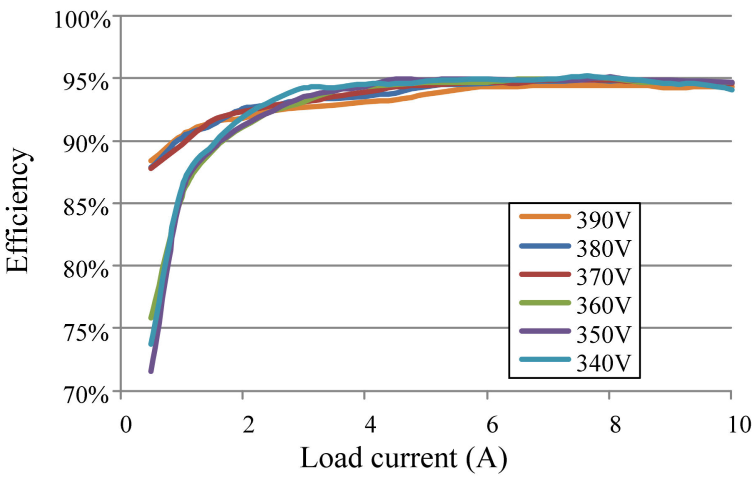


Figure 11. Curves of efficiency versus load current.

The proposed prototype is compared with the 150 W LLC DC-DC module product from Asian Power Device Inc. (Taipei, Taiwan). Their LLC controller, primary-side switches, and SR switches are all the same.

As shown as Figure 12, the former LLC DC-DC module is a 150 W product from Asian Power Device Inc. with a power density of 1.81 W/cm^3, and the latter is a 120 W product with a power density of 2.71 W/cm^3. The proposed prototype has a higher power density than the traditional circuit due to the reduction in the size of the transformer.

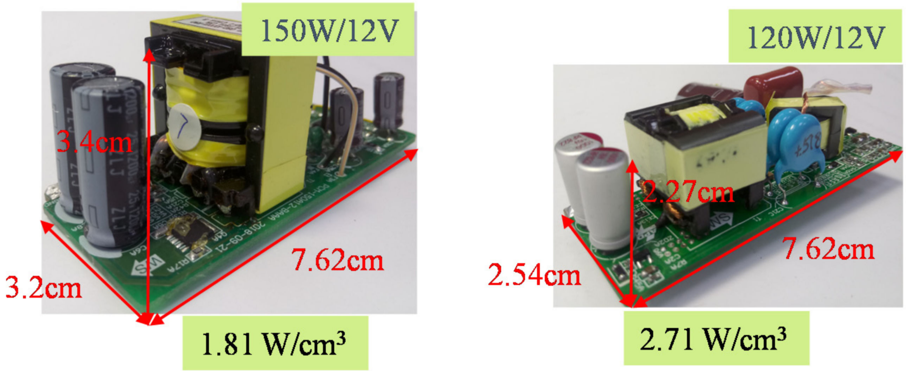


Figure 12. Power density comparison.

The efficiency comparison is shown in Figure 13. The proposed prototype has the same efficiency performance when the load current is above 4 A. The prototype has higher efficiency under light load conditions due to the burst mode setting point at 40% load.

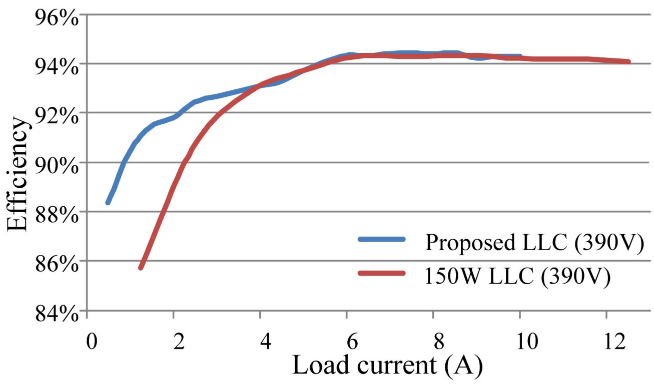
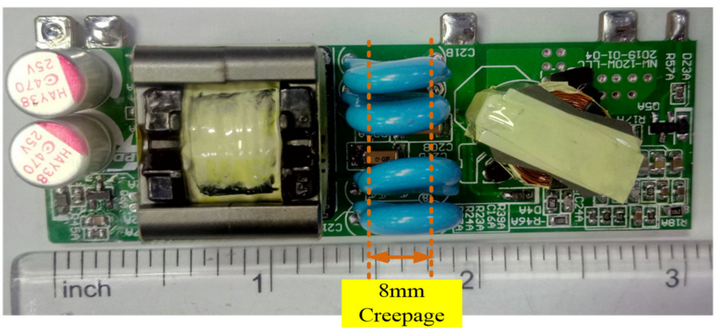


Figure 13. Curves of efficiency versus load current for proposed LLC and 150 W LLC.

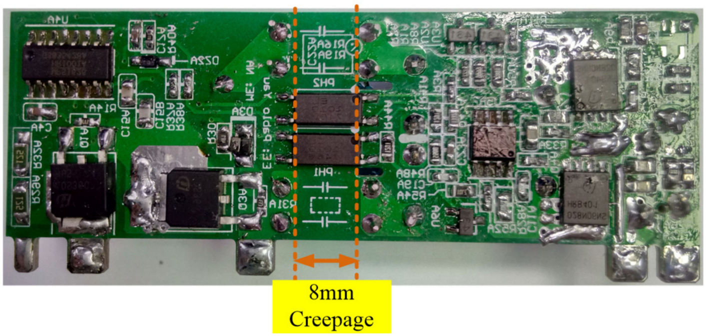
The experimental setup of the safety test method is shown in Figures 1 and 7. The front-end bridge rectifier and the power factor correction stage are included during the safety test. Finally, the leakage current of the proposed circuit with 3 kV/60 Hz hipot test conditions is 80 µA. The leakage current test is operated with a working DUT with an input voltage of 264 V/60 Hz and full load conditions. The experimental leakage current of the proposed circuit is only 10 µA, which is far below the limitation of 0.5 mA.

Figure 14a,b show the photos from the top view and bottom view, respectively. The resonant capacitors C_{r1} and C_{r2} provide 8 mm creepage to meet the reinforced insulation requirements [13,14,26]. The two photo couplers work as signal isolators on the feedback path.



(**a**)

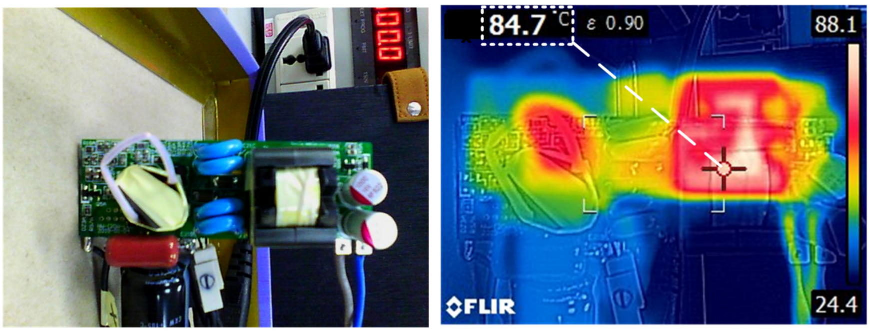
Figure 14. *Cont.*



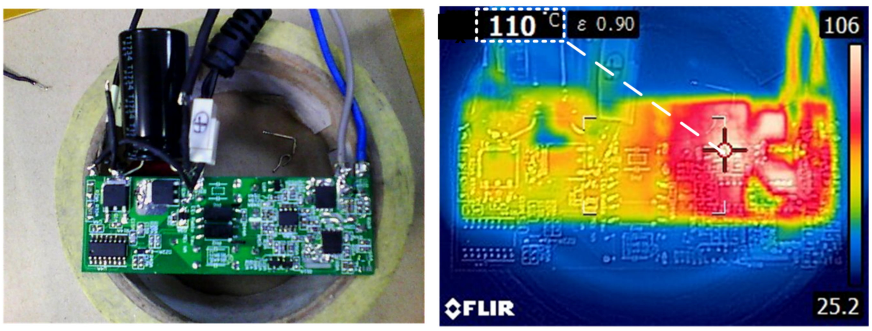
(b)

Figure 14. Photos of the proposed prototype: (**a**) top view, (**b**) bottom view.

The resonant capacitors used in this paper are ceramic capacitors, which generally have a high temperature coefficient, so the capacitance value is affected by component temperature, and this should be taken into consideration in the circuit design. Figure 15a,b correspondingly show the thermography photos from the top view and bottom view under full load operation and natural convection, respectively. As shown as Figure 15, the actual operation of C_{r1} and C_{r2} is around 56 °C to obtain capacitance variation of −20%. The hotpot is at the SR control IC, which is located too close to the heat sources of T_1, Q_3, and Q_4.



(**a**)



(**b**)

Figure 15. Thermography photos of the proposed prototype: (**a**) top view, (**b**) bottom view.

In a conventional LLC converter design, the switching frequency decreases as the output load increases, and the switching frequency shifts to region II to increase the voltage gain. The higher the output power, the higher the thermal radiation from L_r and T_1, the higher the temperature of C_{r1} and C_{r2}, the lower the capacitance of C_{r1} and C_{r2}, and the higher the f_s will rise, causing the f_{sw} to move to region II. When the rate of increase in f_s due to the decrease in capacitance is equal to the decrease in f_{sw} due to the increase in the output load, it can be observed that the f_{sw} decreases insignificantly after the half load of the proposed circuit, as shown in Figure 16.

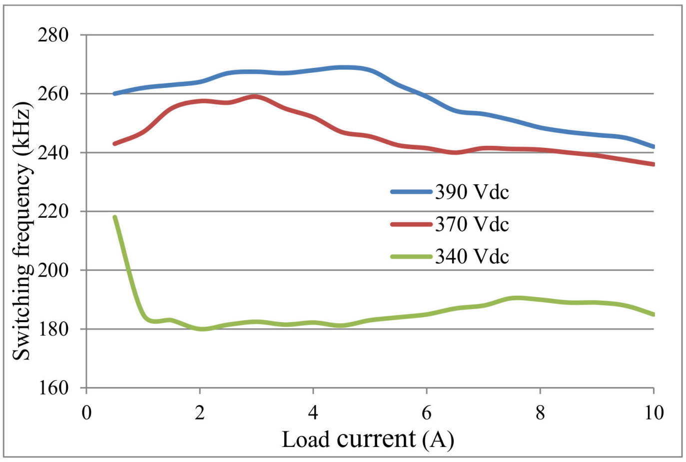


Figure 16. Measured curves of switching frequency.

In terms of circuit design, the temperature of the components can be obtained from the heat flow simulations by the mechanical engineer, and then the temperature change curve provided by the data sheet can be used to estimate the change in capacitance caused by the temperature. In addition, during the period of the PCB layout, the capacitor should be placed upwind of the cooling air flow to avoid being close to heat-generating components such as switch devices or magnetic components to reduce the temperature rise.

If a more stable capacitance value is required, the X7R grade capacitor [27,28] is recommended, with a capacitance variation of less than 15% and 20% over the temperature range of −55 °C to +125 °C, respectively.

Table 6 shows the comparison between the proposed and the existing methods. It can be found that the proposed method can satisfy the safety requirement of the IEC60950-1 standard and achieve higher conversion efficiency and power density.

Table 6. Comparison of the proposed and conventional methods.

	[18]	[17]	Conventional LLC	Proposed Method
Rated power	36 W (12 V, 3 A)	85 W (165 V, 0.51 A)	150 W (12 V, 12.5 A)	120 W (12 V, 10 A)
Efficiency at full load	94.5%	85.5%	94.1%	94.3%
Efficiency at half load	94.5%	84%	94.3%	93.7%
Switching frequency at full load	1.4 MHz	65 kHz	~100 kHz	~240 kHz
Active switches	GaN FET	Si-MOSFET	Si-MOSFET	Si-MOSFET
Power density	18.3 W/cm^3	Not available	1.81 W/cm^3	2.71 W/cm^3
Touch current test (264 Vac, 60 Hz)	Not available	734 µA	10 µA	80 µA
High pot test (3 kVac, 60 Hz, 60 s)	Fail (Y3 cap)	Not available	Pass	Pass

Figure 17 shows the four possible derivative circuits of the proposed circuit in this research. Because they all have the same operating principles, they are considered to have high feasibility.

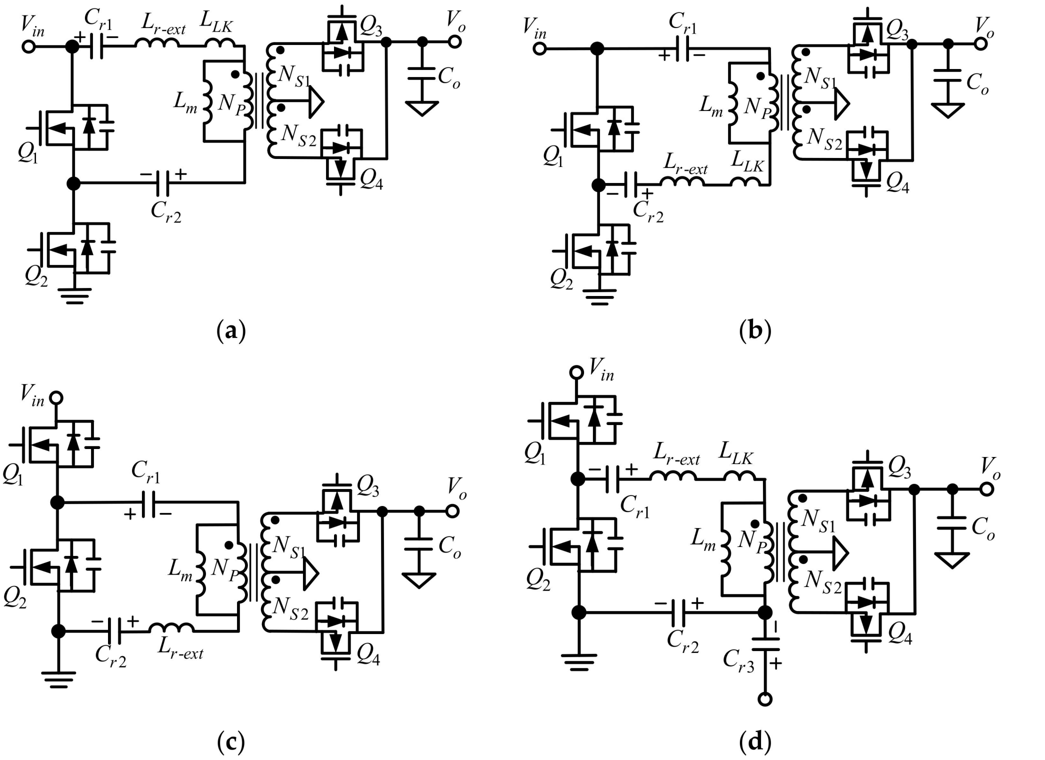


Figure 17. Derivation of the proposed circuit structure: (**a**) Type 1, (**b**) Type 2, (**c**) Type 3, (**d**) Type 4.

5. Conclusions

In this paper, the resonant capacitor is cut into two resonant capacitors, which are used to share the isolation capacity of the transformer. The benefits of the proposed method are as follows. First, the creepage of the transformer is effectively transferred to the Y1 capacitor by the proposed method. The volume of the transformer is significantly reduced. The proposed converter has a higher power density than the traditional converter. The proposed prototype with 120 W was briefly compared with the traditional prototype with 150 W to verify the feasibility of the proposed isolated structure. Second, the rated insulation voltage of a normal three-layer insulated wire is only 3 kVac. However, some applications require higher insulation voltage, such as power supplies for industrial equipment or the auxiliary power supplies for solid state transformer systems, where the insulation voltage required is up to 25 kV. The proposed approach only requires an increase in the number of Y-capacitors in series to achieve a higher insulation voltage without modifying the transformer design.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

Q_1, Q_2	Main switches
Q_3, Q_4	SR switches
C_o	Output capacitor
T_1	Main transformer
N_P	Primary winding of T_1
N_{S1}, N_{S2}	Secondary windings of T_1
n	Turn ration of T_1
L_r	Resonance inductor
L_{lk}	Leakage inductance of N_p of T_1
$L_{r\text{-}ext}$	Additional resonance inductor
C_r	Resonant capacitor
C_{r1}	High-side resonant capacitor
C_{r2}	Low-side resonant capacitor
D_{max}	Maxima duty cycle
B_{max}	Maxima flux density of T_1
f_p	Resonant frequency of L_r, L_m, and C_r
f_s	Resonant frequency of L_r and C_r
f_{sw}	Switching frequency (Hz)
Q_{FL}, Q_{LL}	Quality factor of full load and light load, respectively
R_o	Equivalent resistance of output load
$R_{ac\text{-}FL}$, $R_{ac\text{-}LL}$	Reflected load resistance of output load at full load and light load, respectively
ω	Switching frequency (rad/sec)
ω_p	Resonance frequency of parallel resonant converter
ω_s	Resonance frequency of series resonant converter
M_{FL}, M_{LL}	Voltage gain of the output and input at full load and light load, respectively
A_e	Effective core area
v_{Cr}	Voltage cross C_r
$v_{Cr(\min)}$	Minima voltage of C_r
$v_{Cr(\max)}$	Maxima voltage of C_r
$i_{Cr1(\text{pk})}$	Peak current of C_{r1}
v_{Cr1}	Voltage cross C_{r1}
$v_{Cr1(\min)}$	Minima voltage of C_{r1}
$v_{Cr1(\max)}$	Maxima voltage of C_{r1}
$i_{Cr2(\text{pk})}$	Peak current of C_{r2}
v_{Cr2}	Voltage cross C_{r2}
$v_{Cr2(\min)}$	Minima voltage of C_{r2}
$v_{Cr2(\max)}$	Maxima voltage of C_{r2}
$N_{p(\min)}$	Minima required turns of N_p
$i_{Np(\text{rms})}$	RMS current of N_p
$i_{Ns1(\text{rms})}$, $i_{Ns2(\text{rms})}$	RMS current of N_{s1} and N_{s2}, respectively
$B_{max\text{-}Lm}$	Maxima flux density of L_m
$i_{Lm(\text{pk})}$	Peak current of L_m
DCR_{Np}	DCR_{Np} resistance of N_p
DCR_{Ns1}, DCR_{Ns2}	DCR_{Np} resistance of N_{s1} *and* N_{s2}
$A_{e(T1)}$	Effective core area of T_1
$V_{e(T1)}$	Effective core volume of T_1
$P_{copp\text{-}Np}$	Copper loss of N_p
$P_{copp\text{-}Ns}$	Copper loss of N_s
$P_{core\text{-}T1}$	Core loss of T_1
$P_{CV(T1)}$	Unit core loss of T_1
P_{T1}	Total loss of T_1
$i_{Lr(\text{pk})}$	Peak current of L_r
$N_{Lr\text{-}ext}$	Winding turns of $L_{r\text{-}ext}$
$L_{r\text{-}ext}$	Additional resonant inductor
$A_{e(Lr\text{-}ext)}$	Effective core area of $L_{r\text{-}ext}$
$B_{max\text{-}Lr}$	Maxima flux density of $L_{r\text{-}ext}$

$V_{e(Lr\text{-}ext)}$	Effective core volume of $L_{r\text{-}ext}$
$P_{CV(Lr\text{-}ext)}$	Core loss of unit volume of $L_{r\text{-}ext}$
DCR_{Lr}	DC resistance of $L_{r\text{-}ext}$
$i_{Lr(\mathrm{rms})}$	RMS current of $L_{r\text{-}ext}$
$P_{core\text{-}Lr\text{-}ext}$	Core loss of $L_{r\text{-}ext}$
$P_{copp\text{-}Lr\text{-}ext}$	Copper loss of $L_{r\text{-}ext}$
$P_{Lr\text{-}ext}$	Total loss of $L_{r\text{-}ext}$
$R_{on(Q1,Q2)}$	Conduction resistance of Q_1 and Q_2
$P_{cond(Q1,Q2)}$	Conduction loss of Q_1 and Q_2
$V_{gs(Q1,Q2)}$	Maxima driving voltage of Q_1 and Q_2
$Q_{g(Q1,Q2)}$	Gate charge of Q_1 and Q_2
$P_{driving(Q1,Q2)}$	Driving loss of Q_1 and Q_2
$P_{Q1,Q2}$	Total loss of Q_1 and Q_2
$R_{on(SR)}$	Conduction resistance of Q_3 and Q_4
$i_{SR(\mathrm{rms})}$	RMS current of Q_3 and Q_4
$P_{cond(SR)}$	Conduction loss of Q_3 and Q_4
$Q_{g(SR)}$	Gate charge of Q_3 and Q_4
$V_{gs(SR)}$	Maximum driving voltage of Q_3 and Q_4
$P_{driving(SR)}$	Driving loss of Q_3 and Q_4
$P_{cond(SR)}$	Conduction loss of Q_3 and Q_4
P_{SR}	Total loss of Q_3 and Q_4
$i_{Co(\mathrm{rms})}$	RMS ripple current of C_o at low line and high line V_{in}
ESR_{Co}	Equivalent series resistance of C_o
P_{Co}	Total loss of C_o
P_{total}	Total loss of system

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