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Power Factor Correction Application Based on Independent Double-Boost Interleaved Converter (IDBIC)

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Abstract: In this paper, a Power Factor Correction (PFC) application, based on the novel power stage topology named Independent Double-Boost Interleaved Converter (IDBIC), has been analyzed. The novelty of the proposed PFC rectifier is based on the sum of capabilities, such as supplying three independent output voltage levels with interleaved operation at the input and high voltage gain. The hardware used within this application consists of an AC input L-C-L filter, a single-phase bridge rectifier, the IDBIC power stage, output capacitors group and a group of variable high-power rheostats (resistors) group as DC load. The main purpose of the carried study was to highlight the advantages and disadvantages of the novel power stage topology in the context of a green and modern AC to DC conversion solution. Nowadays, a high level of the efficiency and power factor have become a mandatory feature for the AC to DC conversion solutions to satisfy the international electrical standards. Thus, considering the modern electrical standards and recommendations, the current study tries to better depict the working steps and principles of the modern power stage topology within an AC to DC conversion application. The behavior of the considered power stage described in different detailed working steps (such as the Discontinuous Conduction Mode and Continuous Conduction Mode) may help understand how the energy conversions process of AC to DC becomes more efficient. The high output voltage gain of the considered power stage is the key feature in the Power Factor Correction process. With such a feature, the AC to DC conversion solution/application can also operate at lower input AC voltages (such as 90 [V] and 110 [V]). The proposed solution can be successfully used in the electric vehicle (automotive field) and high-power electrical traction (e.g., trains, high power electrical machines and drives). The same solution can also be used successfully in fast battery charging applications and chemical electrolysis processes.

Keywords: Power Factor Correction (PFC); Independent Double-Boost Interleaved Converter (IDBIC); high voltage gain; low input voltage; electrical traction; electric vehicle; fast battery charging

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1. Introduction

Modern applications such as smart houses, hybrid microgrids, renewable energy, electric vehicles and energy storage systems demand an increase in quality for their infrastructure, as different policies regarding energy efficiency have been internationally introduced [1–3]. Concerning energy conversion systems and external power supplies, the European Union (EU) Commission has also established efficiency criteria that aims to improve power quality [4]. Since AC/DC converters have become a component of almost all electronic devices used daily, the AC distribution grid may be subjected to poor performance due to the behavior and low power quality of such equipment. Often single-phase rectifiers are required to operate over a wide supply voltage range, with low input current ripple and near-unity power factor in order to meet the present-day standards and market

needs [5,6]. Usually, if bidirectional power flow is not required, a common solution is the boost PFC rectifier. In order to improve the performance of this type of converter, reducing the input current ripple and minimizing the volume of passive devices in the interleaved topology are considered to be among the best practice. Studies and analyses have been made in developing and improving the performance and efficiency of such converter topology. In [7], a method for analyzing the input and output currents in the converter is proposed and derives the specific time functions. A coupled inductor approach is presented in [8–11] to improve the inductor current ripple and power density of the interleaved PFC bridge rectifier. In [12], a hybrid topology comprised of a conventional boost PFC rectifier and a semi-bridgeless PFC interleaved rectifier is presented, claiming better efficiency and performance than that of the traditional interleaved boost PFC. Bridgeless configurations, as mentioned in [13], can present an interleaved topology that offers better performance and reduces the size of the magnetic devices needed. Improved efficiency through the soft switching operation of all switching devices is analyzed in [14]. Here, a snubber circuit is integrated into an interleaved PFC converter. Lighting applications [15,16], connected to the mains grid or industrial, can be provided with a voltage driver which in term has PFC features realized with an interleaved boost rectifier topology. Other applications such as electric vehicle chargers [17–19] are also being studied.

The novelty of the proposed PFC rectifier is the capability of supplying three output voltage levels with interleaved operation at the input. The so-called "three-level PWM rectifiers" [20,21] have been studied for their high efficiency power conversion (>98%) [22], large voltage gain and low stress on the semiconductor devices [23], but they lack the interleaved functionality. More, the concept of bipolar DC microgrids used in distributed generation systems [24,25] presents an increasing interest because of its benefits in energy saving, power quality and power electronics control [26]. Hence, the proposed PFC rectifier can easily interconnect a single-phase AC grid with a multilevel DC microgrid, also assuring the interleaved behavior, and it can be successfully used as a solution in the development of distributed generation.

2. Converter Topology Analysis

2.1. General Representation of the Switching States

The proposed PFC application consists of a novel DC–DC power-stage topology named Independent Double Boost Interleaved Converter (IDBIC). The current topology is based on a patent application in reference [27] that describes its operation in DC–DC systems through paper [28]. The basic PFC converter topology is presented in Figure 1, while the characteristic waveforms during operation are introduced in Figure 2, where the continuous conduction mode (CCM) is exemplified for a duty cycle D larger than 0.5 by means of switching states S1, S4 and S5, respectively, for a duty cycle smaller than 0.5 with the help of switching states S1, S2, S3 and S5.

The main operating stages of the converter for positive alternation are shown in Figure 3, where the diodes D_{r1} and D_{r4} are in conduction and five independent switching states (S1–S5) are highlighted. For the negative alternation, the operating stages are the same on the DC stage; the only difference is that the input current flows through the D_{r2} and D_{r3} diodes.

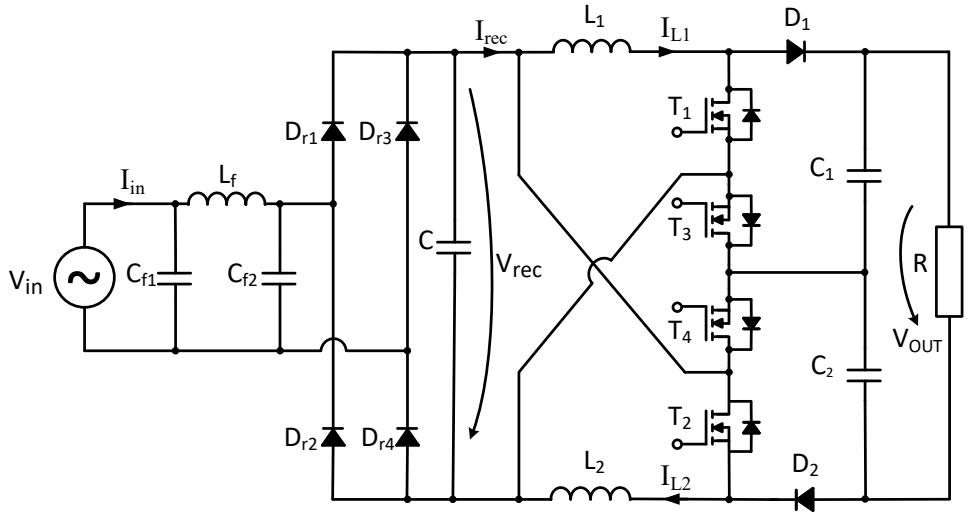
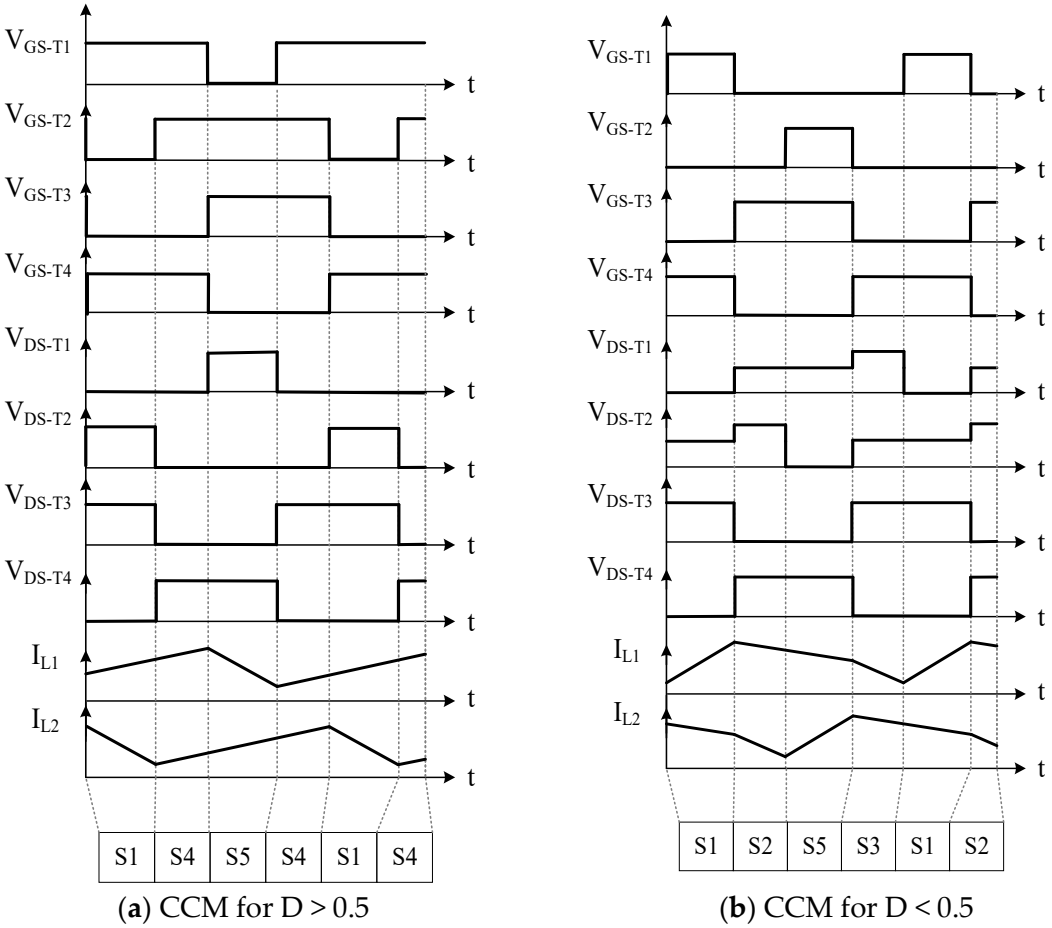
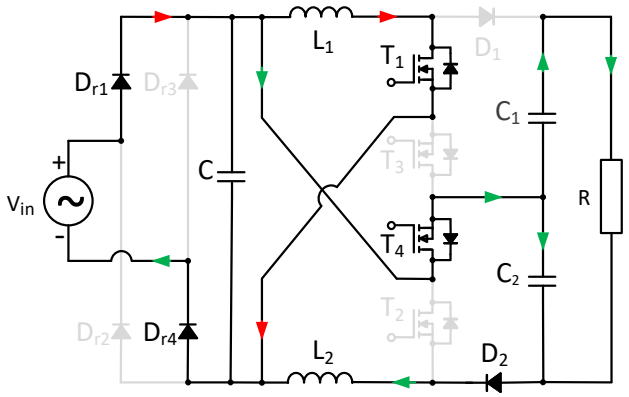


Figure 1. The electronic schematic of the proposed converter. V_{in}—main input voltage; V_{rec}—rectified voltage; V_{out}—DC output voltage; I_{rec}—rectified current; I_{in}—input current; and I_{L1} and I_{L2}–L_1 and L_2 inductor currents.

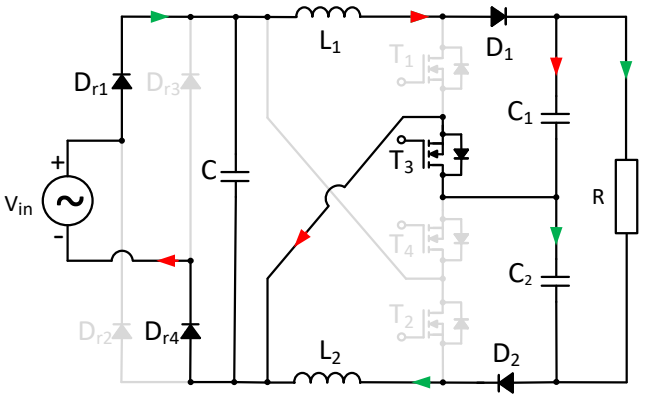


(**a**) CCM for D > 0.5 (**b**) CCM for D < 0.5

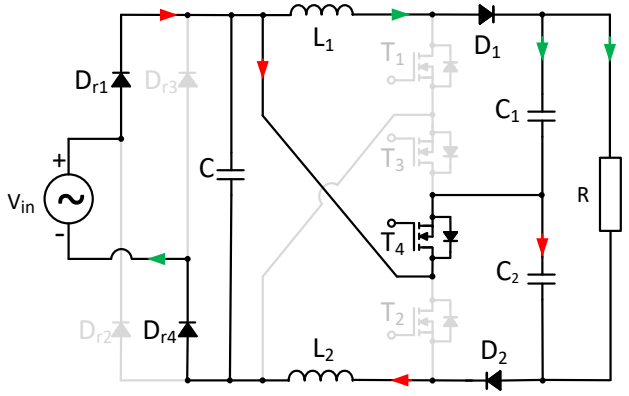
Figure 2. Presumptive functioning waveform and switching stages correlations. V_{GS-T1}, V_{GS-T2}, V_{GS-T3} and V_{GS-T4}—Gate-Source voltage for T_1–T_4 transistors; V_{DS-T1}, V_{DS-T2}, V_{DS-T3} and V_{DS-T4}—Drain-Source voltage for T_1–T_4 transistors; I_{L1} and I_{L2}–L_1 and L_2 inductor currents; D—Duty Cycle; CCM—continuous conduction mode; S1–S5—switching stages from Figure 2.



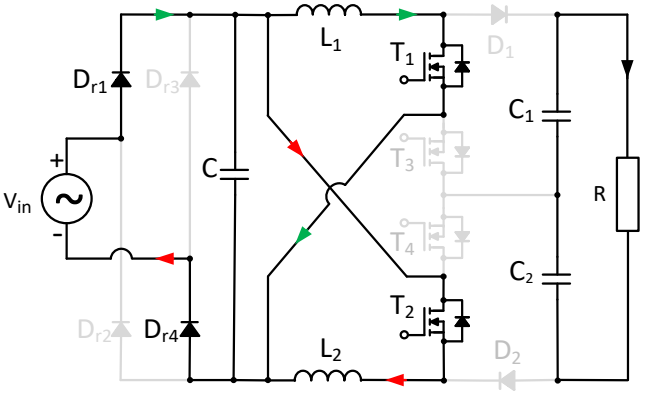
S1–Charging L_1; Discharging L_2.



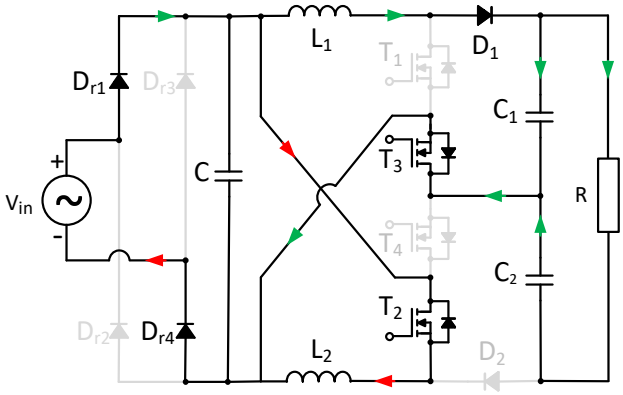
S2–Discharging L_1; Discharging L_2.



S3—Discharging L_1; Discharging L_2.



S4—Charging L_1; Charging L_2.



S5—Discharging L_1; Charging L_2.

Figure 3. Switching stages for the proposed PFC converter.

2.2. State-Space Modeling of the Converter

Observing the switching states presented in Figure 3, the state-space analysis of the proposed converter has been made [29]. Thus, the expressions that describe the behavior of the converter at CCM were first derived for the operation at a duty cycle smaller than 0.5.

This operation is characterized by the switching stated S1–S2–S5–S3, as can be observed in Figure 2b. Therefore, for the switching state S1, will result:

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{1}{L_1} v_{\text{rec}} \\ \dfrac{di_{L2}}{dt} = \dfrac{1}{L_2} v_{\text{rec}} - \dfrac{1}{L_2} v_{C2} \\ \dfrac{dv_{C1}}{dt} = \dfrac{-1}{RC_1} v_{C2} - \dfrac{1}{RC_1} v_{C1} \\ \dfrac{dv_{C2}}{dt} = \dfrac{1}{C_2} i_{L2} - \dfrac{1}{RC_2} v_{C1} - \dfrac{1}{RC_2} v_{C2} \end{cases} \tag{1}$$

Considering the next switching state, S2, when operating at the specified conditions, the equations will be:

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{-1}{L_1} v_{C1} + \dfrac{1}{L_1} v_{rec} \\ \dfrac{di_{L2}}{dt} = \dfrac{-1}{L_2} v_{C2} \\ \dfrac{dv_{C1}}{dt} = \dfrac{-1}{C_1} i_{L1} + \dfrac{1}{RC_1} v_{C1} + \dfrac{1}{RC_1} v_{C2} \\ \dfrac{dv_{C2}}{dt} = \dfrac{1}{C_2} i_{L2} - \dfrac{1}{RC_2} v_{C1} - \dfrac{1}{RC_2} v_{C2} \end{cases} \tag{2}$$

For the switching states S5 and S3, the resulted expressions can be written as:

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{-1}{L_1} v_{C1} + \dfrac{1}{L_1} v_0 \\ \dfrac{di_{L2}}{dt} = \dfrac{1}{L_2} v_0 \\ \dfrac{dv_{C1}}{dt} = \dfrac{1}{C_1} i_{L1} - \dfrac{1}{RC_1} v_{C1} - \dfrac{1}{RC_1} v_{C2} \\ \dfrac{dv_{C2}}{dt} = \dfrac{-1}{RC_2} v_{C1} - \dfrac{1}{RC_2} v_{C2} \end{cases} \tag{3}$$

Respectively,

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{-1}{L_1} v_{C1} \\ \dfrac{di_{L2}}{dt} = \dfrac{-1}{L_2} v_{C2} + \dfrac{1}{L_2} v_0 \\ \dfrac{dv_{C1}}{dt} = \dfrac{1}{C_1} i_{L1} - \dfrac{1}{RC_1} v_{C1} - \dfrac{1}{RC_1} v_{C2} \\ \dfrac{dv_{C2}}{dt} = \dfrac{-1}{C_2} i_{L2} + \dfrac{1}{RC_2} v_{C1} + \dfrac{1}{RC_2} v_{C2} \end{cases} \tag{4}$$

The general state space representation of the modeled system will be:

$$\begin{cases} \dot{x} = A_i x + B_i u \\ y = C_i x \end{cases} \tag{5}$$

where $\dot{x} = \left[\dot{i_{L1}}\ \dot{i_{L2}}\ \dot{v_{C1}}\ \dot{v_{C2}}\right]$; $x = [i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}]$; $u = v_{rec}$.

Thus, from relation (1), the state-space system for the S1 switching configuration is characterized by the matrices:

$$A_{S1} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & \frac{-1}{RC_1} & \frac{-1}{RC_1} \\ 0 & \frac{1}{C_2} & \frac{-1}{RC_2} & \frac{-1}{RC_2} \end{bmatrix}; \; B_{S1} = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix} \tag{6}$$

The representation of relation (2) under state matrices will yield:

$$A_{S2} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{-1}{C_1} & 0 & \frac{1}{RC_1} & \frac{1}{RC_1} \\ 0 & \frac{1}{C_2} & \frac{-1}{RC_2} & \frac{-1}{RC_2} \end{bmatrix}; \; B_{S2} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{7}$$

For the expressions in (3) and (4), corelated with the switching states S5 and S3, the state-space matrices will be:

$$A_{S5} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & \frac{-1}{RC_1} & \frac{-1}{RC_1} \\ 0 & 0 & \frac{-1}{RC_2} & \frac{-1}{RC_2} \end{bmatrix}; \; B_{S5} = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix} \tag{8}$$

and

$$A_{S3} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & \frac{-1}{RC_1} & \frac{-1}{RC_1} \\ 0 & \frac{-1}{C_2} & \frac{1}{RC_2} & \frac{1}{RC_2} \end{bmatrix}; \; B_{S3} = \begin{bmatrix} 0 \\ \frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix} \tag{9}$$

while

$$C_{S1} = C_{S2} = C_{S5} = C_{S3} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{10}$$

Considering the representation from Figure 2b and the duty cycle as d, the state matrices averaged over one switching period will result the following:

$$\begin{aligned} A_{av} &= A_{S1}\, d + A_{S2}(0.5 - d) + A_{S5}\, d + A_{S3}(0.5 - d) \\ B_{av} &= B_{S1}\, d + B_{S2}(0.5 - d) + B_{S5}\, d + B_{S3}(0.5 - d) \\ C_{av} &= C_{S1}\, d + C_{S2}(0.5 - d) + C_{S5}\, d + C_{S3}(0.5 - d) \end{aligned} \tag{11}$$

To obtain the expressions depicting the continuous, linear behavior of the converter, the small signal analysis is implied to the linearized model. Small variations of the input variables, $\widetilde{v}_{rec}$ and duty cycle $\widetilde{d}$, around the quiescent operating point of the converter will result in small variations of the output variables $\widetilde{i}_{L1}$, $\widetilde{i}_{L2}$, $\widetilde{v}_{C1}$ and $\widetilde{v}_{C2}$.

$$\begin{cases} \dot{\widetilde{x}} = A_{av}\,\widetilde{x} + B_{av}\,\widetilde{v}_{rec} + E_{av}\,\widetilde{d} \\ \widetilde{y} = C_{av}\,\widetilde{x} \end{cases} \tag{12}$$

where $E_{av} = [(A_{S1} + A_{S5}) - (A_{S2} + A_{S3})]X + [(B_{S1} + B_{S5}) - (B_{S2} + B_{S3})]V_{rec}$.

After specific algebraic operation, the Laplace domain solutions of the state vectors will determine the output to input transfer functions. Thus, the solution for the output to input voltage transfer function will be:

$$\frac{\widetilde{Y}}{\widetilde{V}_{rec}} = C_{av}\,(sI - A_{av})^{-1}\cdot B_{av} \tag{13}$$

and for the output to duty cycle variation:

$$\frac{\widetilde{Y}}{\widetilde{D}} = C_{av}\,(sI - A_{av})^{-1}\cdot E_{av} \tag{14}$$

The steady-state values of the state variables can be determined as:

$$Y = -C_{av}\,(A_{av})^{-1}\cdot B_{av}\,V_{rec} \tag{15}$$

Concerning the operation at a duty cycle greater than 0.5, the switching states from Figure 2a are partially similar with the ones described by (1) and (3). The only particular switching state for this mode of operation is S4, which is characterized by the equations:

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{1}{L_1}v_0 \\ \dfrac{di_{L2}}{dt} = \dfrac{1}{L_2}v_0 \\ \dfrac{dv_{C1}}{dt} = \dfrac{-1}{RC_1}v_{C2} - \dfrac{1}{RC_1}v_{C1} \\ \dfrac{dv_{C2}}{dt} = \dfrac{-1}{RC_2}v_{C1} - \dfrac{1}{RC_2}v_{C2} \end{cases} \tag{16}$$

from which will result the following state matrices:

$$A_{S4} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{-1}{RC_1} & \dfrac{-1}{RC_1} \\ 0 & 0 & \dfrac{-1}{RC_2} & \dfrac{-1}{RC_2} \end{bmatrix};\ B_{S4} = \begin{bmatrix} \dfrac{1}{L_1} \\ \dfrac{1}{L_2} \\ 0 \\ 0 \end{bmatrix} \tag{17}$$

Having obtained the state-space model of the converter, a suitable control strategy can be developed.

3. Simulation Results

The simulation was performed based on a MATLAB Simulink model of the described PFC solution within this paper. The whole structure is depicted in Figure 4.

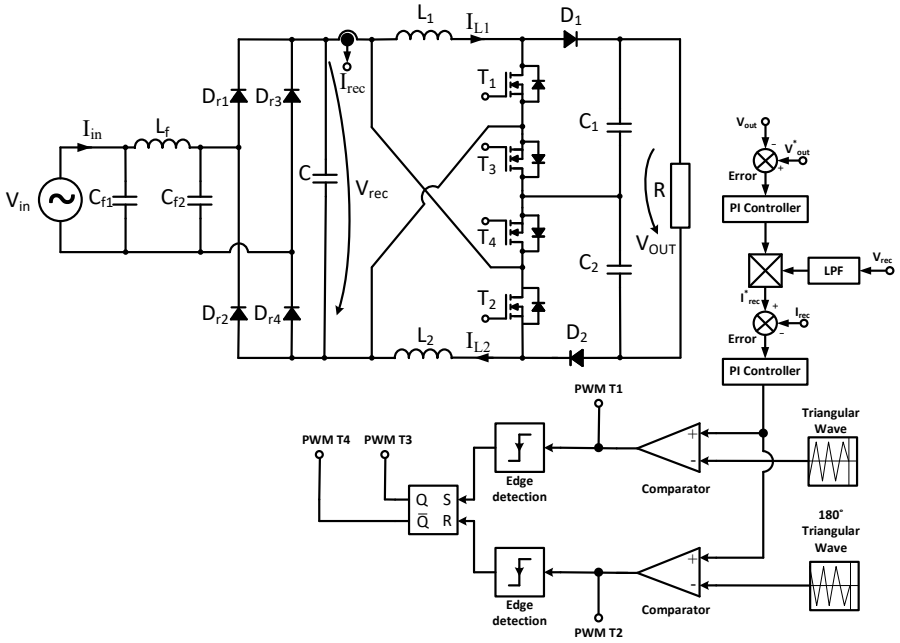


Figure 4. The generic output voltage control loop and PWM generator. V_{in}—AC input voltage; V_{rec}—rectified voltage; V_{out}—DC output voltage; V^*_{out}—reference DC output voltage; I_{rec}—rectified current; I^*_{rec}—reference rectified current; I_{in}—input current; PWM T1, PWM T2, PWM T3 and PWM T4 — Gate-Source voltage for T_1–T_4 transistors.

The "PFC" sub-system represented in Figure 5 contains the control law of the power stage [30]. The reference rectified voltage was obtained from the input voltage waveform by reversing the negative half-cycle. Based on two proportional–integrator (PI) regulators, the control law was implemented, and the output "Duty_Cycle" drive signal was computed as result. The "Voltage_PI" regulator maintains the output DC voltage constant, and the "Current_PI" regulator limits and shapes the input current.

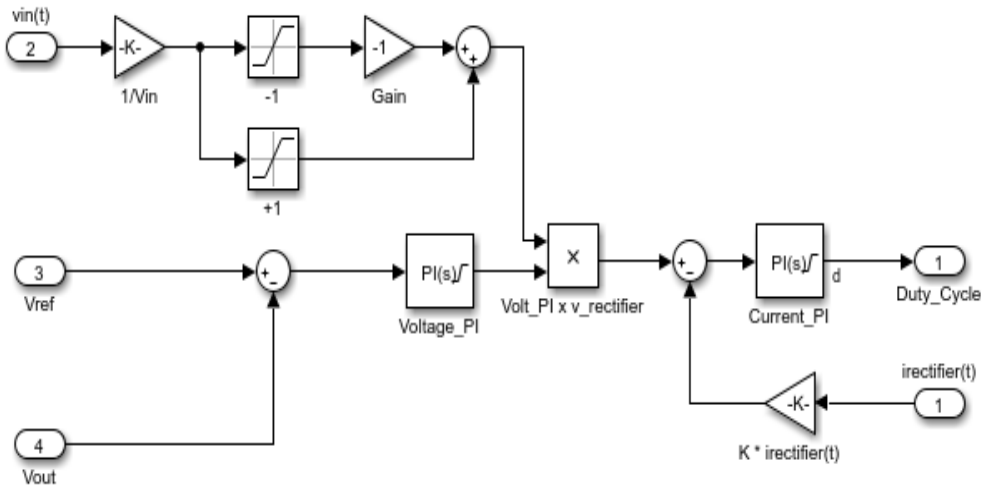


Figure 5. MATLAB Simulink inside "PFC" sub-system. K—Current calibration factor.

Figure 6 represents the sub-system of the "PWM_generator" which, depending on the signals received by the "PFC" subsystem, realizes the control logic of the four transistors.

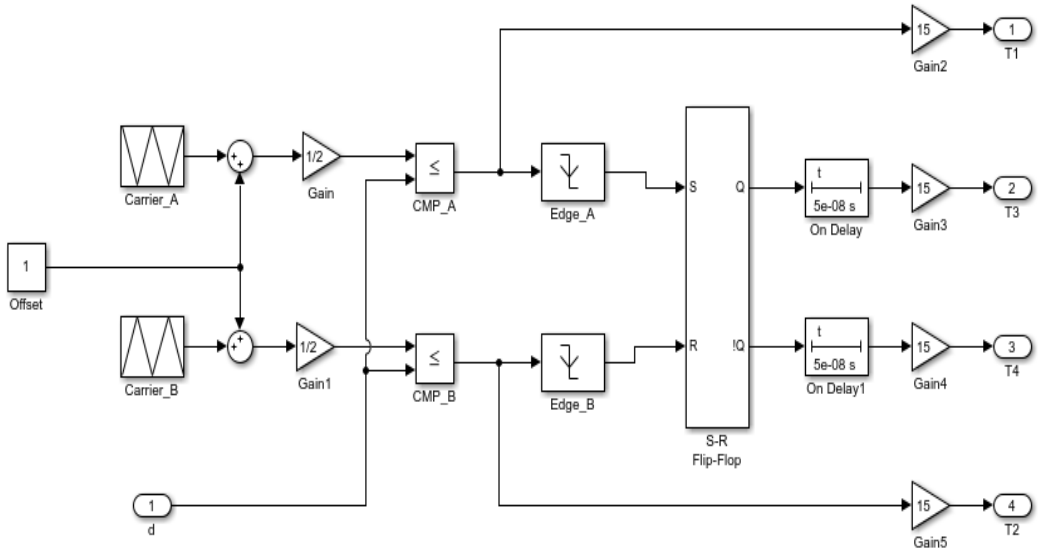


Figure 6. MATLAB Simulink inside "PWM_generator" sub-system.

Following Figure 7, the input current (I_{in}) and voltage (V_{in}) can be analyzed in conjunction with the output voltage (V_{out}). Additionally, the inductor L_1 and L_2 currents (i_{L1} and i_{L2}) synchronized at low frequency are represented, followed by the rectified input voltage (V_{rec}), all these signals being introduced in Figure 4.

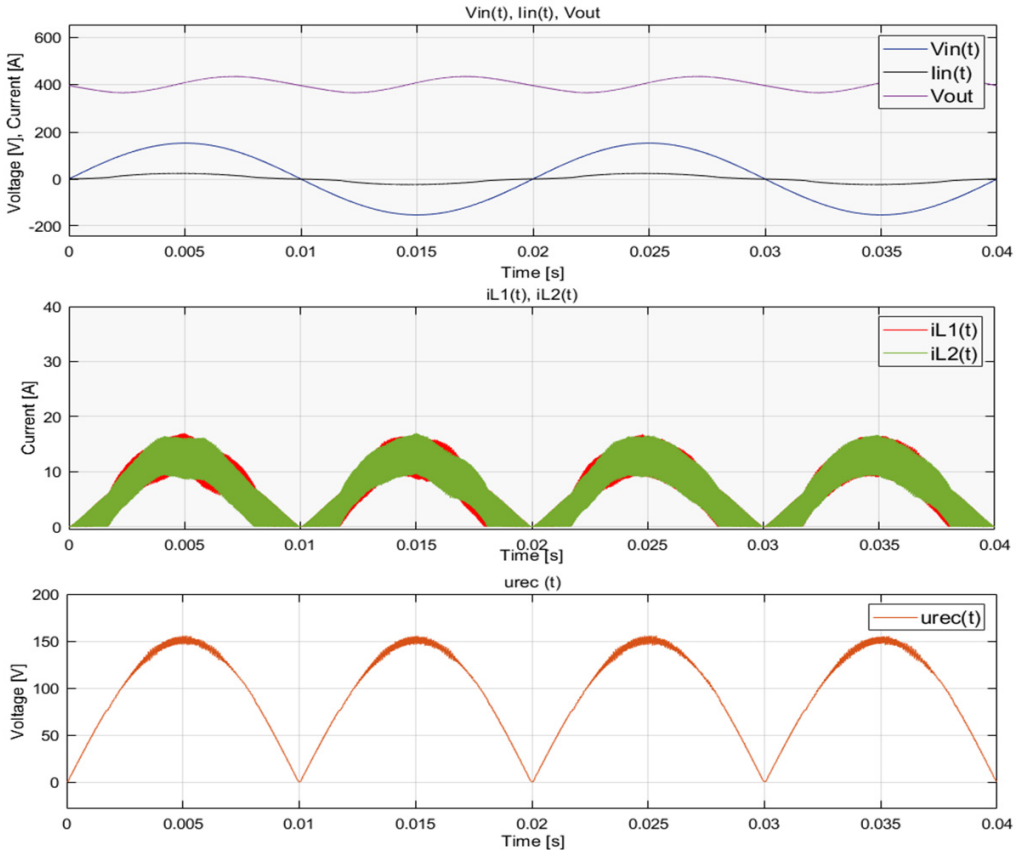


Figure 7. Low—frequency waveforms representation of the input voltage (Vin), input current (Iin), output voltage (V_{out}), inductor L_1 and L_2 currents (iL_1, iL_2) and the input rectified voltage (Vrec).

Figure 8 shows the L_1 and L_2 coils' current evolution at both low- and high-frequency representations. One can see that during a low-frequency cycle, the boost converters are

working from DCM (Figure 8a) and BCM (boundary conduction mode, Figure 8b) to CCM. In CCM, two current waveforms can be noticed at duty cycles bigger then 0.5 (Figure 8c) or smaller then 0.5 (Figure 8d).

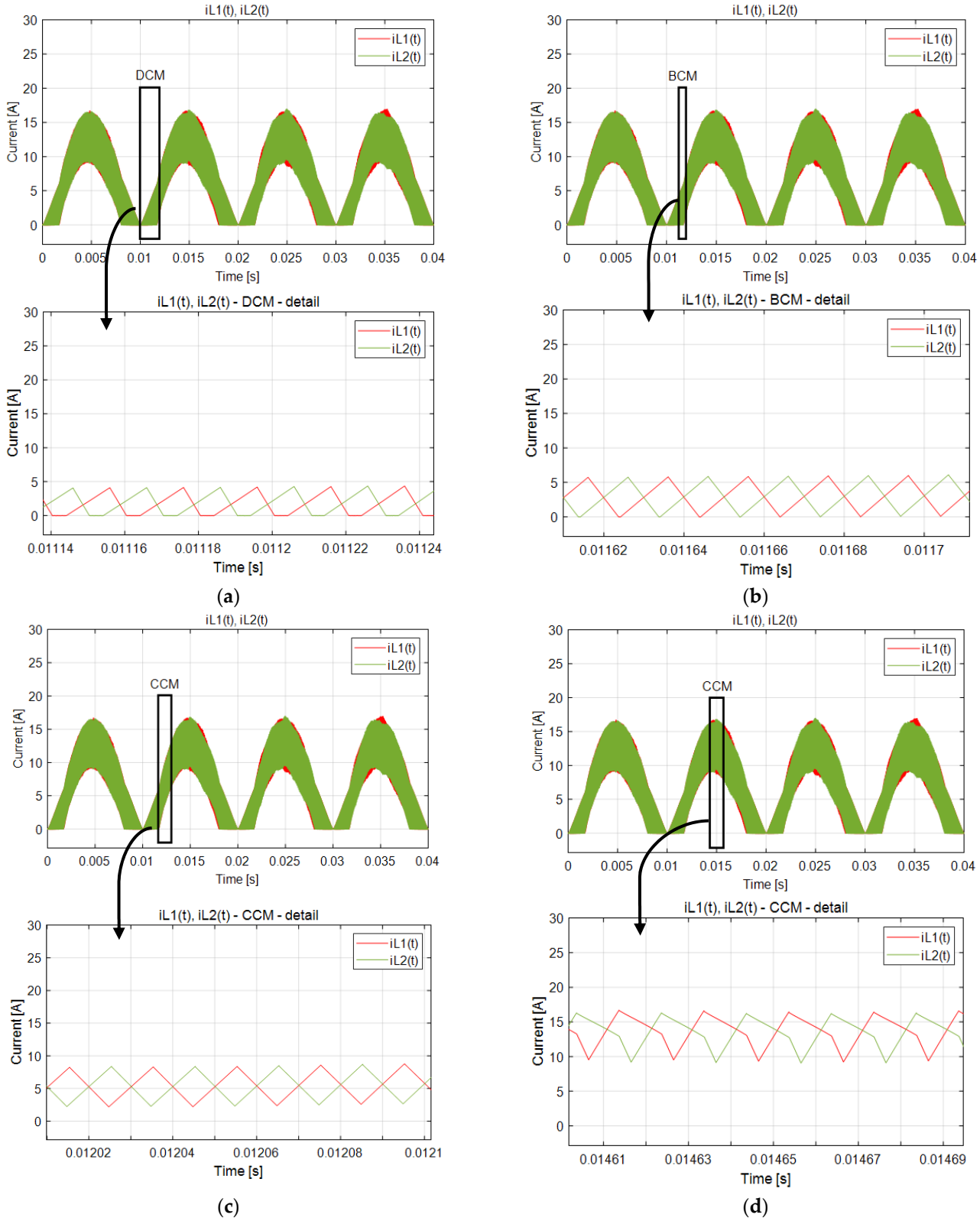


Figure 8. L_1 and L_2 inductor currents' (I_{L1}, I_{L2}) representation at low and high frequency representations; (**a**) DCM; (**b**) BCM; (**c**) CCM for D > 0.5; (**d**) CCM for D < 0.5.

4. Experimental Implementation

The experimental implementation was based on the schematic represented in Figure 4. In this figure, both the control loop and the gate signal generator block structure was depicted. The resultant PWM gate signals are used to drive the four IDBIC power stage transistors (MOSFET IPW60R099CPFKSA1, 600 [V], 31 [A]). This scheme is suitable for a symmetrical control of the two integrated boost converters in which a single reference voltage is used for both, so that each will work independently but identically. In view of this, the voltage on the output capacitors C_1 and C_2 will be regulated at the same value, and there is no need for a further balancing mechanism. For the considered power factor application, in which the total output voltage V_{out} must be regulated, the symmetrical approach of the control loop is sufficient, which means that only a PI controller and a voltage reference V_{ref} are required for the output voltage control loop.

If a three-voltage-levels approach is desired at the output, the asymmetric control of the converter can be applied, in which two reference voltages must be entered and the two integrated boost converters will operate independently and potentially with different duty cycles.

The laboratory test settings are shown in Figure 9. Based on an application with AC input voltages of 90 [V], 110 [V] and 130 [V] and a 350 [V] DC output voltage, the total harmonic distortion (THD) and power factor (PF), performed with the Tektronix PA3000 power analyzer, are illustrated in Figures 10 and 11. The main waveforms taken with the Tektronix MDO3024 oscilloscope are shown in Figure 12, while in Figure 13 one can notice the efficiency measurements.

In Table 1, a comparison is made of the proposed solution with similar converter topologies. Limited three-level boost converter topologies are available for power factor correction applications; thus, the comparison is made also with similar topologies used in the DC–DC converter application.

Table 1. Comparison of the proposed topology with similar approaches.

Ref.	Converter Application	Voltage Stress On		Maximum Efficiency	Components S*/D*/L*/C*/C.I*/T*
		Switches V_S/V_O	Diodes V_D/V_O		
[27]	DC–DC	(M + 1)/2 M	(M + 1)/2 M	91.7	2/2/2/4/2/-
[28]	DC–DC	0.5	0.5	95.9	4/2/2/3/-/-
[29]	DC–DC	0.5	0.5	95	2/3/2/3/-/-
[30]	DC–DC	(M + 1)/4 M (M − 1)/2 M	(M + 1)2 M	95.85	3/4/2/3/-/-
[31]	DC–DC	(1 + 5 M)/6 M	(M + 1)/M	95.9	6/9/6/1/-/-
[32]	DC–DC	0.5	-	94.3	4/0/1/4/-/-
[33]	DC–DC	0.33	0.33	93.9	1/5/1/5/0/-
[34]	DC–DC	(M + 1)/4 M	(M + 1)/2 M	96	2/3/-/3/1/-
[35]	Boost PFC	0.5	0.5	95.8	2/6/1/2/-/-
[36]	Boost PFC	0.5	0.5	94.8	2/4/1/2/-/-
[37]	Boost PFC	$V_{dc}/2$; V_{dc}; $V_O/2$	-	95.1	6/6/2/5/-/1
[38]	Boost PFC	$V_{dc}/2$; $V_O/2$	-	94.2	6/8/2/6/-/1
Proposed	Boost PFC	1/M + 0.5 1/M	0.5	95.8	4/6/2/2/-/-

S*: switch, D*: diode, L*: inductor, C*: capacitor, C.I*: coupled inductor, T*: transformer, V_O: output voltage, V_S: switch voltage, V_D: diode voltage, V_{in}: input voltage, M: voltage gain (V_o/V_{in}), V_{dc}: primary stage DC voltage.

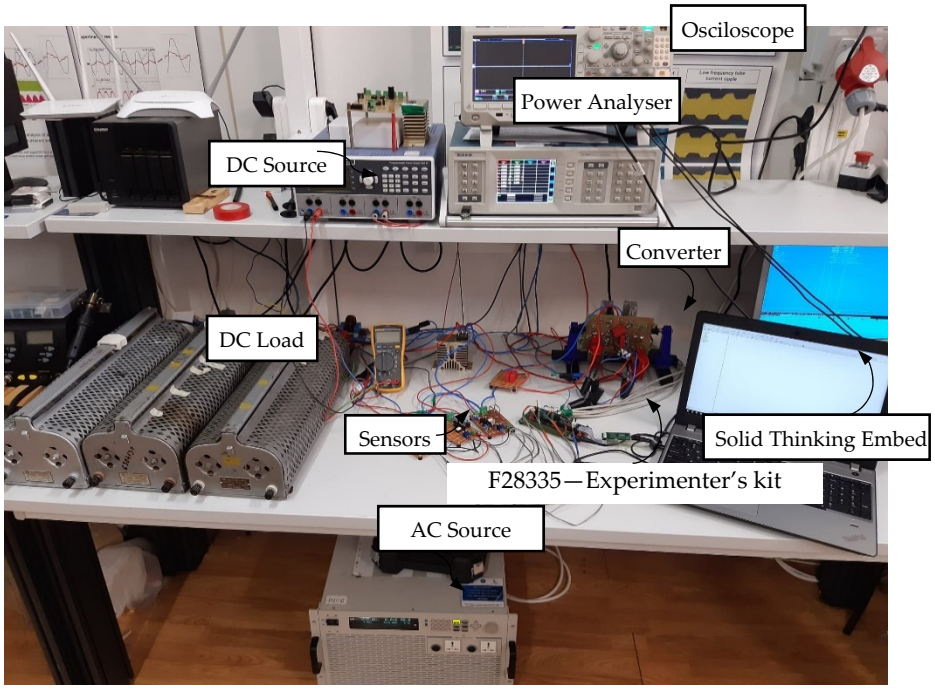


Figure 9. Laboratory test setup.

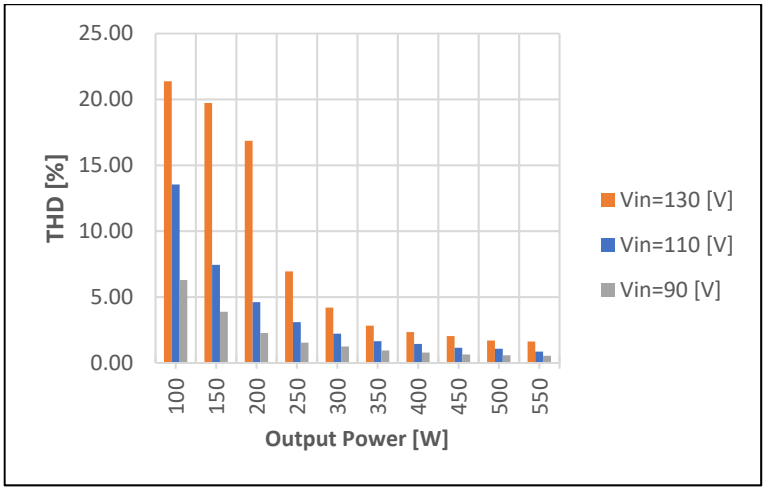


Figure 10. Laboratory practical total harmonic distortion measurements.

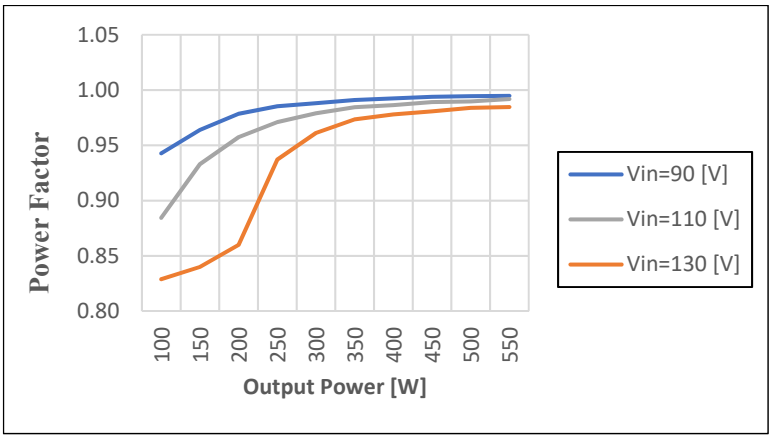


Figure 11. Laboratory practical power factor measurements.

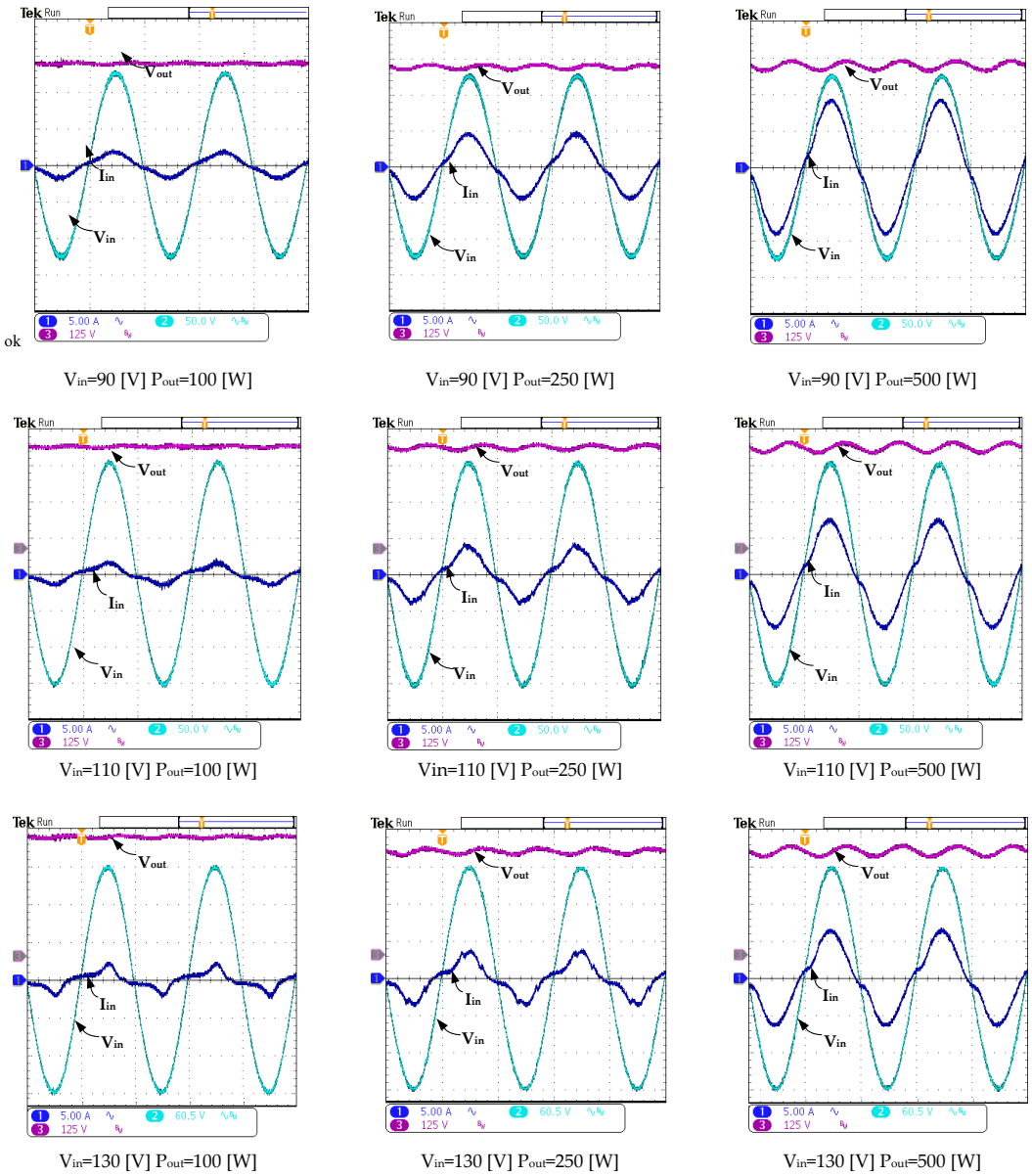


Figure 12. Practical measurements of the proposed converter at different input voltages and different output powers. V_{in}—main input voltage; V_{out}—DC output voltage and I_{in} input current.

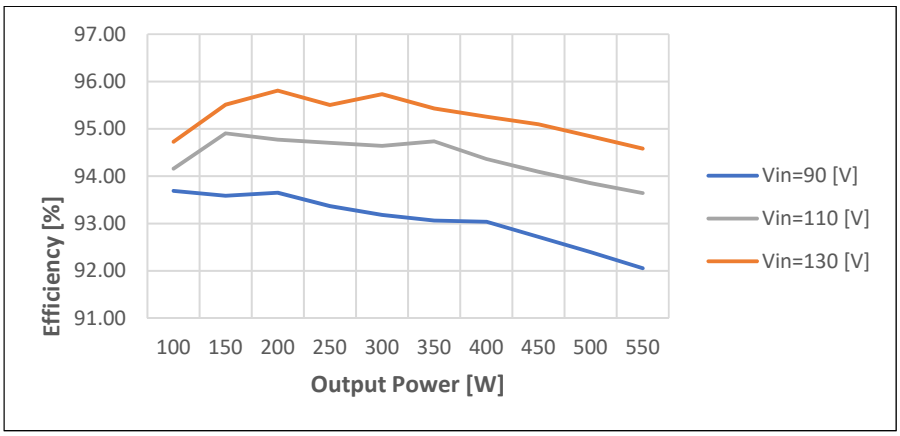


Figure 13. Laboratory practical efficiency measurements.

5. Conclusions

The paper proposes a new type of converter for active Power Factor Correction applications, combining some key functions in one solution. The three voltage levels at the output together with the high gain capability could be favorable assets for future integration in bipolar symmetric/asymmetric DC microgrids. Likewise, the input interleaved operation and low voltage stress on the power semiconductors can be beneficial for efficiency improvements and high-power/high-voltage applications.

The proposed converter has been analyzed through theoretical, simulated and practical approaches to highlight the overall impact of the solution. From the simulation results, the operation of the new converter meets the analytical description presented, where the mathematical model of the converter was developed to help tuning the control loop. According to the experimental part, near the converter rated power, the obtained results in terms of THD and power factor are improving. Another phenomenon that can be observed is that the converter has better performance, in terms of power quality, at higher voltage gains. In terms of efficiency, on the other hand, it has been observed that at low supply voltage, the efficiency is lower. Therefore, the performance is decreasing with the increasing of the converter's gain. In this matter, for future optimization iterations, this tradeoff must be considered, but with the remark that these are common facts in boost PFC applications.

Regarding the converter overall performance attained, the results are promising, considering that this is the first prototype developed, which is not optimized in terms of switching and passive elements criteria. In view of this, future developments are mandatory for power and control optimizations, and more close analyses are needed on the implementation of the converter topology in market applications.

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