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A Full Load Range ZVS Isolated Three-Level DC/DC Converter with Active Commutation Auxiliary Circuit Suitable for Electric Vehicle Charging Application

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Abstract: The isolated three-level DC/DC converter (ITLDC) can be used to charge electric vehicles. During the constant current charging stage, the ITLDC can be designed to realize nature zero voltage switching (ZVS). However, during the constant voltage charging stage, the charging current is small; thus, nature ZVS cannot be realized. This paper presents an active commutation auxiliary circuit (ACAC) for the ITLDC to realize the full load range ZVS. With the proposed ACACs, all the main switches achieve zero-voltage turn-on and quasi zero-voltage turn-off, and the auxiliary switches realize zero current turn-on and zero-voltage turn-off; thus, the efficiency will be high. The auxiliary currents generated by the ACACs are controllable. During the constant current charging stage, the ITLDC realizes nature ZVS and the auxiliary currents are controlled to zero; thus, the ACACs do not result in high current stress or bring in additional losses, and the efficiency will be high. During the constant voltage charging stage, the charging current decreases with charging time and the charging current is too small to realize nature ZVS. Thus, the ITLDC can work with the proposed ACACs and the auxiliary currents can be controlled within a suitable value to realize ZVS. With the proposed ACACs, the ITLDC can realize ZVS during the whole charging process; thus, the efficiency will be high. The structure and operating principle of the ITLDC with ACACs are introduced and the performance of the proposed TLDC is experimentally verified on a 1.5 kW prototype converter.

Keywords: isolated three-level DC/DC converter; zero-voltage switching; active commutation auxiliary circuit; electric vehicle charger

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1. Introduction

With the characteristics of being environmentally friendly and reducing fuel consumption, electric vehicles (EVs) are becoming popular. The chargers of EVs can be categorized into two classes—slow charging and fast charging. The fast chargers are usually installed in highway rest areas and city refueling points [1]. The slow chargers are usually installed in community parking sites or located on-board. Usually, these chargers include an AC/DC converter followed by a second-stage DC/DC converter [2] or one-stage DC/DC converter powered by a high-voltage DC bus [3]. Some AC/DC converters can be used to charge the EVs directly. However, the control is complex [4]. Usually, DC/DC converters are used in chargers and the input voltage of these DC/DC converters is high. To reduce the voltage stress, the DC/DC converter can be implemented by an isolated three-level DC/DC converter (ITLDC) [5,6]. A four-switch ITLDC was proposed in [7], which has the simplest structure. Many research works focusing on the four-switch ITLDC have been conducted to achieve high efficiency and reliability. To ensure the reliability of the ITLDC, the voltages of the input capacitors and the current of switches should be balanced. The pulse wide modulation methods are proposed in [8,9] to achieve perfect voltage balancing results. The periodically swapping modulation strategy is proposed in [10] to achieve balanced switch

currents. To achieve high efficiency in an ITLDC, soft switching should be realized. This paper will focus on the zero-voltage switching (ZVS) of the four-switch ITLDC.

There are many research works focusing on the ZVS of the diode clamping ITLDC. For example, in [11,12], the ZVS is realized with a large load range and reduced circulating loss; in [13,14], the ZVZCS methods are proposed, and some switches realize zero-current turn-on and other switches realize zero-voltage turn-on. However, the research works focusing on the ZVS of the four-switch ITLDC are relatively few and these research works are as follows. The ITLDC will achieve natural ZVS with a high output current and the natural ZVS range can be extended by increasing the leakage inductance of the transformer or adding an external inductor in series with the primary winding of the transformer [11]. However, a too large leakage inductance will result in high duty cycle loss and high circulating loss [11,15]. In [16], a combined DC/DC converter is proposed to realize wide load range ZVS, two ITLDCs' parallel operation and share two switches of the down bridge; thus, the current stress of the down bridge switches will be high. A wide load range ZVZCS ITLDC with two main switches realized ZVS and another two main switches realized zero-current switching (ZCS) in [17]. However, when the ITLDC is implemented with MOSFETs, the switching losses will not be substantially reduced with ZCS, due to the large output capacitance of MOSFETs. In [6], a zero-voltage switching PWM strategy with capacitor current-balancing control is proposed; the ZVS achievement conditions of the upper bridge switches and the down bridge switches are shifted towards each other in every two switching periods; thus, the switching losses caused by the hard switching at the light load situation can be distributed evenly among the four power switches. However, the soft switching range is not extended with this ZVS method. In [18], a ZVS non-isolated bidirectional DC/DC converter with transient current build-up technique is proposed with a small average auxiliary current, which can be used in ITLDC to realize full load range ZVS. However, this ZVS method needs two auxiliary switches for each bridge and the auxiliary switches are turned off under hard switching conditions.

To extend the ZVS range of the ITLDC, a commutation auxiliary circuit (CAC) can be added. A CAC with one inductance and two capacitances is proposed in [19]. The CAC can be used in different ITLDCs, and also in the four-switch ITLDC, as shown in Figure 1a. However, this CAC will not perform well when the ITLDC is used as an EV charger. According to [20,21], the constant-current and constant-voltage charging strategy is used to charge lithium-ion batteries. In the first charging stage, the batteries are charged with a constant current and, then, the charging process will switch to a constant-voltage stage. During the constant-current stage, the duty cycle of the ITLDC will increase with the increase in battery voltage. During the constant-voltage stage, the output current of the ITLDC will decrease with the charging process time. The maximum value of the auxiliary current i_A is i_{A_peak}, which will change with the duty cycle. The maximum value i_{A_peak} can be expressed as (1) [17] and the change in i_{A_peak} with duty cycle is shown in Figure 1b.

$$i_{A\_peak} = \frac{D(1-D)V_{in}T_s}{4L_A} \quad (1)$$

where D is the duty, T_s is the period, V_{in} is the input voltage, and L_A is the auxiliary inductor of the CAC.

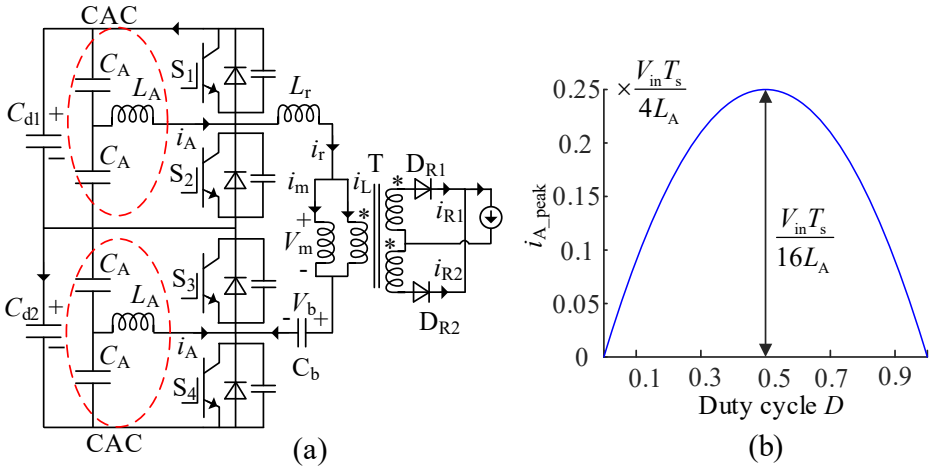

Figure 1. (**a**) ITLDC with the CAC. (**b**) Auxiliary current changes with duty cycle. Where the * represents the dotted terminal of the transformer and the circuits in the red circles are the CACs.

As shown in Figure 1b, to achieve ZVS at a small duty cycle, the auxiliary inductor L_A should be designed with a small value. However, the auxiliary current will be large when the duty cycle is large. The auxiliary current will result in high conduction losses and high current stress of the main switches. Moreover, during the constant-current charging stage, the output current is large enough to realize ZVS naturally, and then the CAC is unwanted. A controllable CAC is required to generate a controllable commutation auxiliary current, which does not change with the duty cycle and can be controlled to zero when the ITLDC realizes ZVS naturally.

This paper proposes an active commutation auxiliary circuit (ACAC) with controllable commutation auxiliary current, which will realize a full load range ZVS of the ITLDC. The ACACs can be left unused when the ITLDC realizes natural ZVS, which will result in high efficiency. Since the ACACs will not work when the current of the ITLDC is large enough to realize natural ZVS, the ACACs do not increase the current stress of the main switches. The auxiliary switch achieves zero-current turn-on and zero-voltage turn-off and the switching loss of the auxiliary switch is quite small. The structure and operating principle of the ITLDC with ACACs are introduced and the performance of the proposed ITLDC is experimentally verified on a 1.5 kW prototype converter.

2. Proposed Topology and Working Principle

The topology of the proposed ITLDC is shown in Figure 2. The ACAC consists of a small auxiliary inductor L_A, an auxiliary capacitor C_A and an auxiliary switch S_A. Two ACACs are applied to the ITLDC's upper bridge and down bridge, respectively. The auxiliary capacitor C_A is large enough so that the voltage of C_A remains unchanged in one period. L_r is the leakage inductance of the transformer and C_b is the DC-blocking capacitor, which is large enough to act as a DC voltage source. C_1~C_4 are the equivalent parallel capacitors, which will achieve a quasi-zero-voltage turn-off condition for the main switches. V_{S1}~V_{S4} are the drain source voltages of the main switches S_1~S_4. The main switches S_1, S_2 are driven by a complementary PWM with dead time and S_3, S_4 are also driven by a complementary PWM with dead time. The PWM phases of S_1 and S_3 are shifted by π degrees.

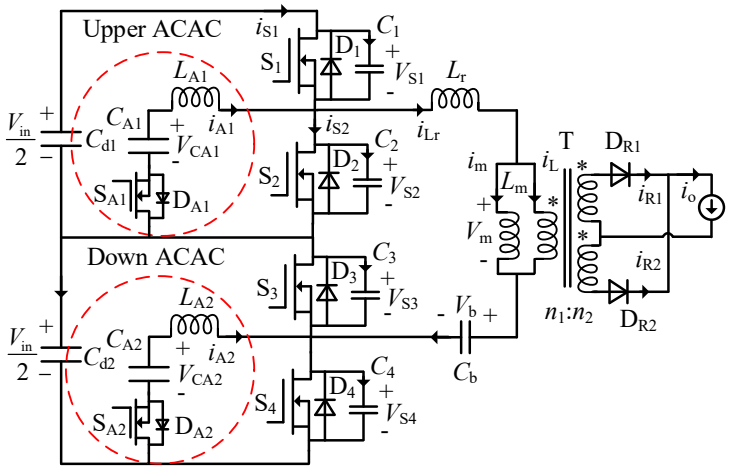

Figure 2. The ITLDC with proposed ACACs. Where the * represents the dotted terminal of the transformer and the circuits in the red circles are the proposed ACACs.

The operating principle and auxiliary current of the upper ACAC are shown in Figure 3 and the operating principle of the down ACAC is the same as the upper one. Before the switch S_2 is turned off, the auxiliary switch S_{A1} is turned on, the voltage V_{CA1} is applied to L_{A1} and the current i_{A1} will increase linearly from zero. The auxiliary switch S_{A1} is turned on at the zero-current condition. The auxiliary current i_{A1} can be expressed as in (2).

$$i_{A1}(t) = \frac{V_{CA1}}{L_{A1}} t \tag{2}$$

where V_{CA1} is the voltage of the auxiliary capacitor C_{A1}, and L_{A1} is the auxiliary inductance.

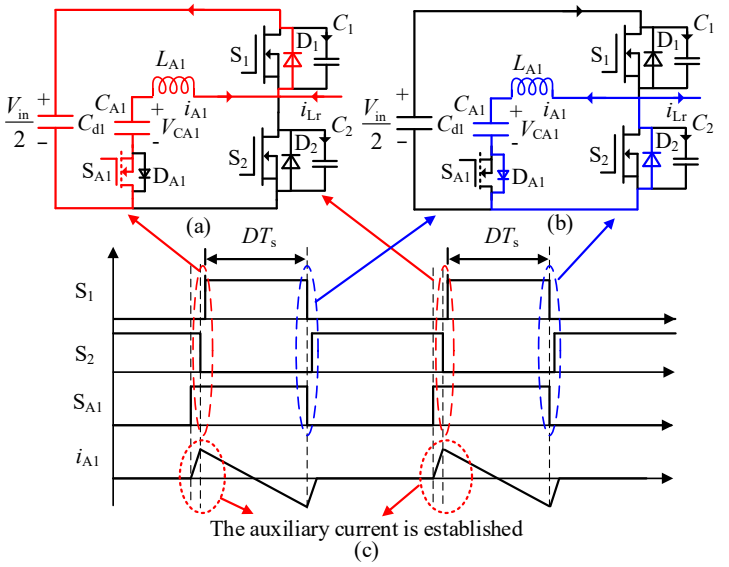

Figure 3. Working principle and the auxiliary current of the upper ACAC. (**a**) ZVS turn on condition for S_1. (**b**) ZVS turn on condition for S_2. (**c**) Theoretical waveforms.

The current i_{A1} will increase linearly until the main switch S_2 is turned off. When S_2 is turned off, the auxiliary current i_{A1} increases to i_{A_peak}, which will be used to achieve the ZVS turn-on of S_1. The auxiliary current i_{A1} will discharge the equivalent parallel capacitor C_1 and charge C_2. Once the voltage of C_1 decreases to zero, the antiparallel freewheeling diode D_1 is conducted and the zero-voltage turn-on condition of S_1 is ready, as shown in Figure 3a. The energy to realize ZVS is taken from L_{A1} and C_{A1}, which are large enough to maintain the zero-voltage condition throughout the entire dead time. After

S_1 is turned on at zero-voltage condition, the current i_{A1} will decrease linearly, which can be expressed as (3). The current i_{A1} will decrease to negative until S_1 is turned off. When S_1 is turned off, the switch S_{A1} is also turned off. The negative current of i_{A1} will flow through the antiparallel freewheeling diode D_{A1} and the auxiliary switch S_{A1} is turned off at zero-voltage condition. The negative current of i_{A1} will discharge the equivalent parallel capacitor C_2 and charge C_1. Once the voltage of C_2 decreases to zero, the antiparallel freewheeling diode D_2 is conducted and the zero-voltage turn-on condition of S_2 is ready, as shown in Figure 3b.

$$i_{A1}(t) = i_{A\_peak} - \frac{V_{in} - 2V_{CA1}}{2L_A}t \tag{3}$$

where i_{A_peak} is the peak value of the auxiliary current, $0 < t \leq DT_s$ and D is the duty cycle, and T_s is the PWM period.

With the proposed ACACs, all the main switches realized zero-voltage turn-on even at no load condition, and the auxiliary switch realized zero current turn-on and zero-voltage turn-off. The auxiliary current i_{A1} is controllable by adjusting the turn-on time of the auxiliary switch S_A, and the auxiliary current i_{A1} will be zero if the auxiliary switch S_{A1} is not turned on. If the load is heavy enough, the ACACs will not work and the ITLDC achieves natural ZVS. When the load is light, the auxiliary current i_{A1} can be controlled to a suitable value to realize ZVS. Then, a full load range ZVS of the ITLDC can be realized; thus, the efficiency will be high. The detailed working process is analyzed as follows. The main theoretical waveforms of the ITLDC with ACACs are shown in Figure 4, and the positive directions of currents and voltages are marked in Figure 2. Since the working principle of the ITLDC has already been described in [7], here, we focus on the realization of ZVS. One switching period is divided into ten time intervals and the equivalent circuits for each time interval are shown in Figure 5. Before the analysis, the following assumptions are made: (1) the output inductor L_o is large enough, and thus the output current i_o can be assumed to be constant; (2) the magnetizing current is negligibly small; (3) the equivalent parallel capacitors have the same value, i.e., $C_1 = C_2 = C_3 = C_4 = C_s$; (4) the auxiliary inductors have the same value, i.e., $L_{A1} = L_{A2} = L_A$. Detailed analysis for each time interval is described as follows.

Interval 1 (Figure 5a, t_0~t_1): During this interval, the auxiliary current i_{A1} will decrease from the maximum value i_{A_peak} to $-i_{A\_peak}$, which can be expressed as (3). The current i_{S1} flows though the main switch S_1 and the value of i_{S1} is equal to $(i_{Lr} - i_{A1})$.

Interval 2 (Figure 5b, t_1~t_2): At t_1, the main switch S_1 is turned off and the auxiliary current i_{A1} reaches the peak value $-i_{A\_peak}$. The current i_{A1} and i_{Lr} will charge C_1 and discharge C_2 until the voltage of C_2 reaches zero; thus, the zero-voltage turn-on condition for the switch S_2 is realized. At t_1, the auxiliary switch S_{A1} is turned off at zero-voltage condition.

Interval 3 (Figure 5c, t_2~t_3): At t_2, the switch S_2 is turned on at zero-voltage condition and the converter reaches a freewheeling stage. At t_2, the current i_{A1} reaches $-i_{A\_peak}$. Since the voltage of V_{CA1} is assumed to be constant, the charge variation of the capacitance C_{A1} should be zero. The voltage V_{CA1} is applied to the auxiliary inductance; thus, the auxiliary current i_{A1} increases linearly, which can be expressed as (4). The current i_{A1} will reach zero quickly.

$$i_{A1}(t) = -i_{A\_peak} + \frac{V_{CA1}}{L_A}t \tag{4}$$

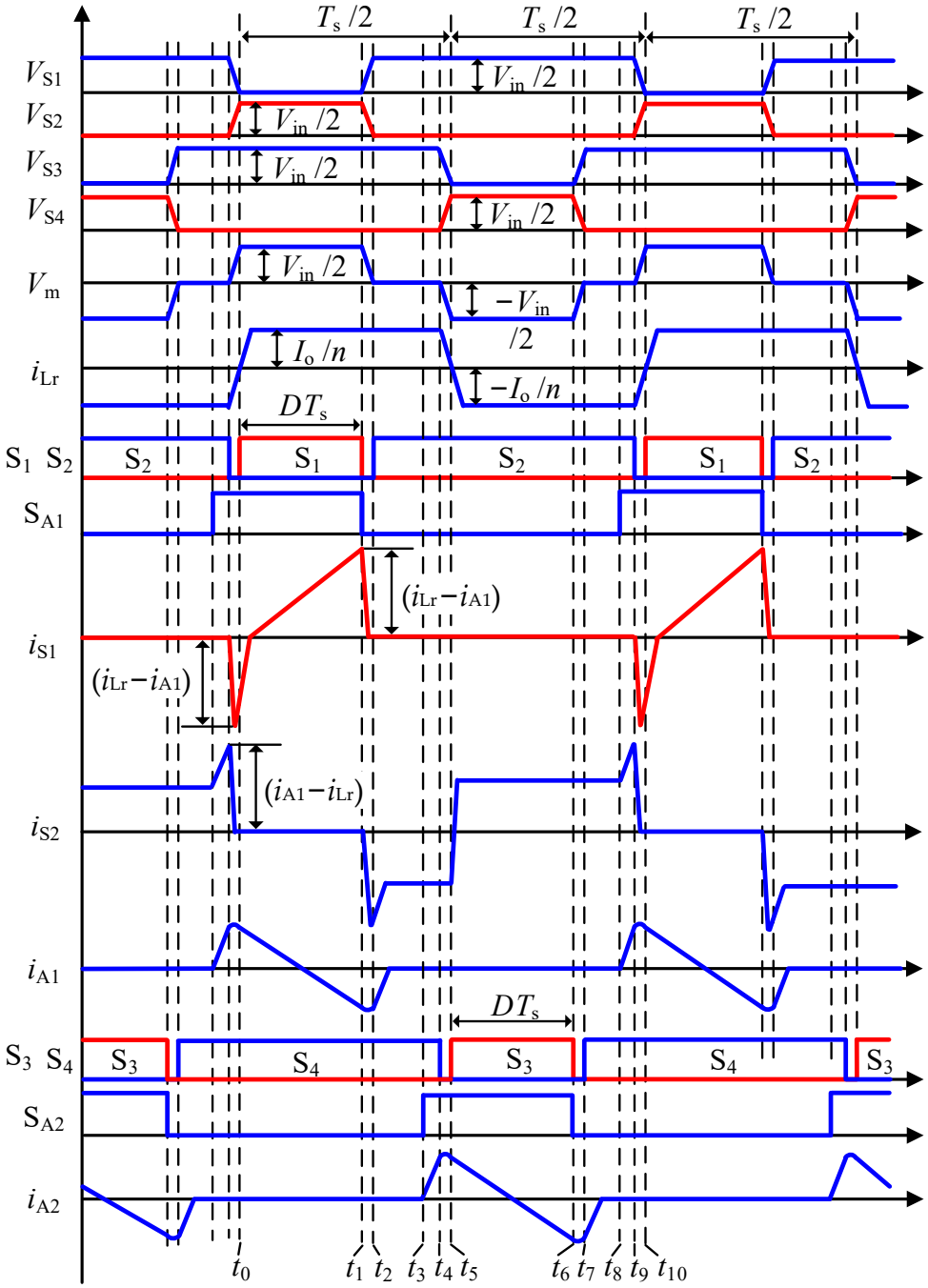

Figure 4. Theoretical waveforms of the ITLDC with proposed ACACs.

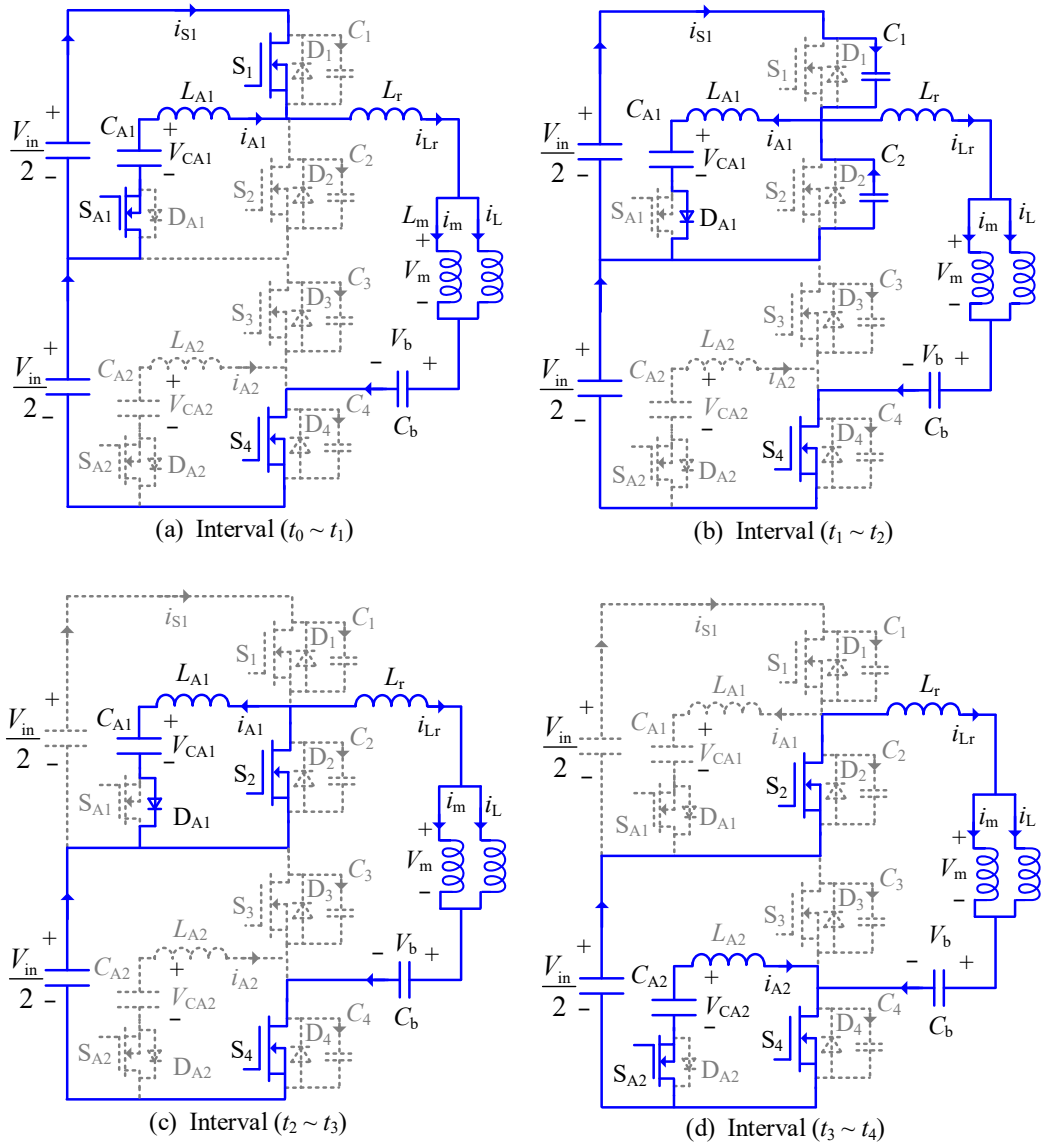

Figure 5. *Cont.*

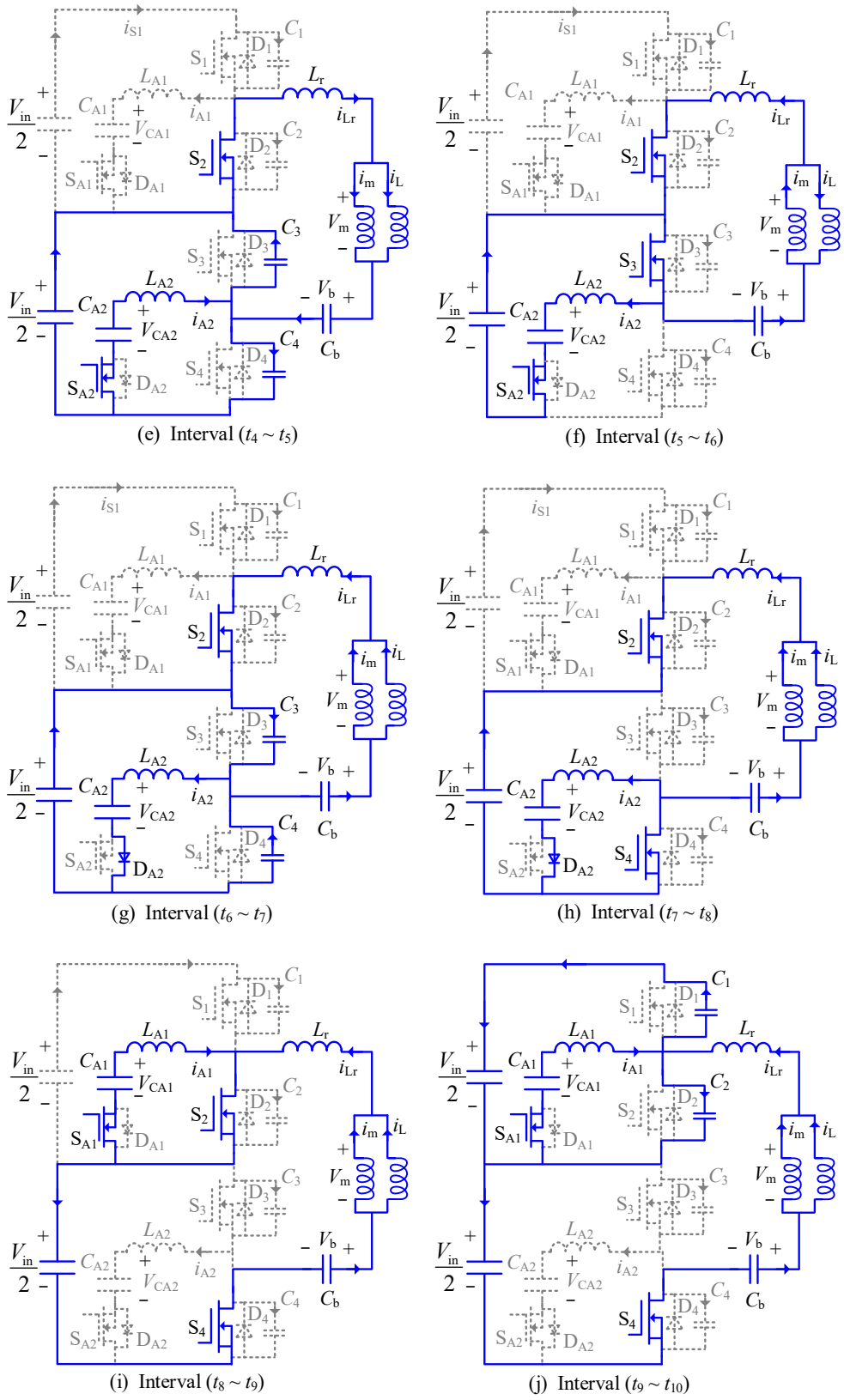

Figure 5. Equivalent circuits for each time interval. (**a–j**) are the equivalent circuits of interval 1–interval 10 respectively.

Interval 4 (Figure 5d, t_3~t_4): The auxiliary switch S_{A2} is turned on at zero-current condition and the auxiliary current i_{A2} is built up in a short time. The auxiliary current

increases from zero; thus, the auxiliary switch S_{A2} realizes zero-current turn-on. At t_4, the main switch S_4 is turned off and the current i_{A2} reaches the maximum value i_{A_peak}.

Interval 5 (Figure 5e, t_4~t_5): At t_4, the main switch S_4 is turned off, and the current i_{A2} and i_{Lr} will charge C_4 and discharge C_3 until the voltage of C_3 reaches zero; thus, the zero-voltage turn-on condition for the switch S_3 is realized.

Interval 6 (Figure 5f, t_5~t_6): At t_5, the main switch S_3 is turned on at zero-voltage condition. The current i_{A2} will decrease until S_3 is turned off. During this interval, current i_{A2} will decrease from the maximum value i_{A_peak} to $-i_{A\_peak}$. The power is transferred from the block capacitor C_b to the load.

Interval 7 (Figure 5g, t_6~t_7): At t_6, the main switch S_3 and the auxiliary switch S_{A2} are turned off simultaneously and S_{A2} is turned off at zero-voltage condition. The current i_{A2} and i_{Lr} will charge C_3 and discharge C_4 until the voltage of C_4 reaches zero; thus, the zero-voltage turn-on condition for the switch S_4 is realized.

Interval 8 (Figure 5h, t_7~t_8): At t_7, the main switch S_4 is turned on at zero-voltage condition and the converter reaches a freewheeling stage. The auxiliary current i_{A2} increases linearly and will reach zero quickly.

Interval 9 (Figure 5i, t_8~t_9): At t_8, the auxiliary switch S_{A1} is turned on at zero-current condition and the current i_{A1} will be built up quickly. At t_9, the main switch S_2 is turned off and the current i_{A1} reaches the maximum value i_{A_peak}.

Interval 10 (Figure 5j, t_9~t_{10}): At t_9, the main switch S_2 is turned off and the current i_{A1} and i_{Lr} will discharge C_1 and charge C_2 until the voltage of C_1 reaches zero; thus, the zero-voltage turn-on condition for the switch S_1 is realized. At t_{10}, the main switch S_1 is turned on at zero-voltage condition and a new cycle begins.

With the ACACs, all the main switches achieved zero-voltage turn-on. Considering that the equivalent parallel capacitors C_1~C_4 limit the rising slope of the voltages across the main switches, the main switches are turned off at quasi zero-voltage condition. The auxiliary switches realized zero-current turn-on and zero-voltage turn-off. The auxiliary current is controllable by adjusting the turn-on time of the auxiliary switch S_A. As shown in Figure 4, the intervals (t_3~t_4) and (t_8~t_9) are used to build the auxiliary current; these intervals can be marked as t_{A_build}. During the constant-current stage, the charging current is large enough to realize ZVS naturally, the auxiliary switch S_A will not turn-on and the auxiliary circuit does not work. During the constant-voltage stage, the charging current is small, and the auxiliary circuit will work to realize ZVS of the main switches; thus, the full load range ZVS can be realized.

3. Discussion of the Proposed ZVS ITLDC

3.1. Design of the Proposed ACAC

3.1.1. The Auxiliary Current i_{A_peak}

To avoid the shoot-through of the bridges, a proper dead time t_{dead} between the PWM drivers is needed and the dead time t_{dead} can be designed according to [22]. The dead time will affect the ZVS operation, as shown in Figure 6a; although the collector-emitter voltage of S_1 reaches zero during the dead time t_{dead}, the zero-voltage condition will not be maintained till the end of the dead time. When the current i_{S1} increases to zero and changes to positive, the equivalent parallel capacitor of S_1 will be charged and V_{S1} will increase; then, the zero-voltage condition does not exist. To maintain the zero-voltage condition, the auxiliary current should be large enough. As shown in Figure 6b, with a large auxiliary current, the zero-voltage condition is maintained throughout the dead time interval.

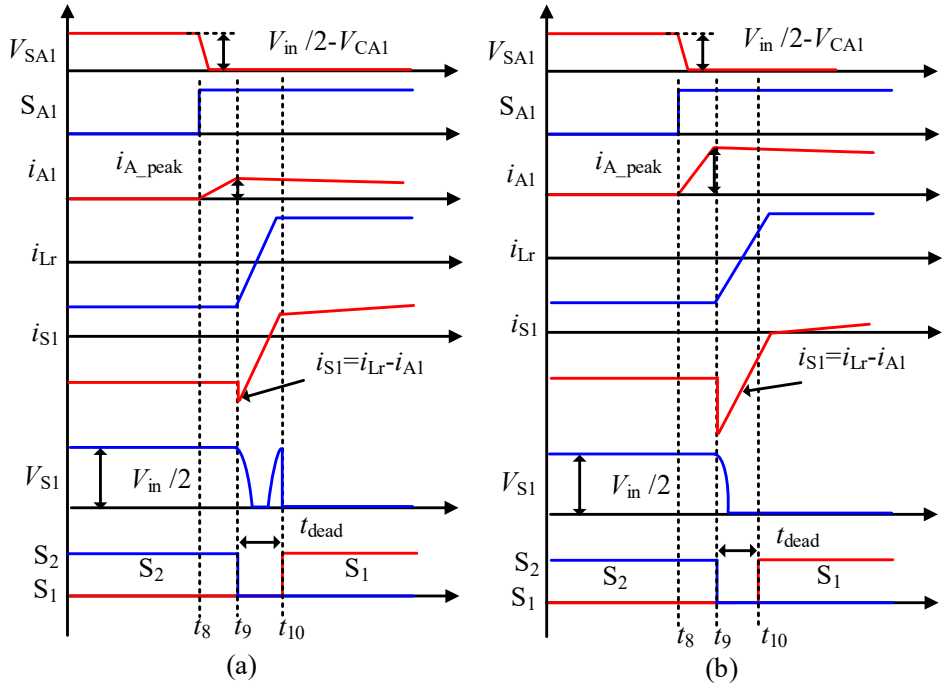

Figure 6. The turn-on process of the main switch S_1 (**a**) with small auxiliary current, (**b**) with large auxiliary current.

Due to the large auxiliary inductor, the current i_{A1} is equal to i_{A_peak} throughout the dead time interval. When the ITLDC works with no load, the peak value of the auxiliary current i_{A_peak} reaches the minimum. The voltage of the equivalent parallel capacitors should be discharged to zero in the dead time interval; thus, the minimum value of i_{A_peak} can be expressed as (5). When the output current is not zero, the auxiliary current i_{A_peak} should be larger than $I_o/2n$ (n is the transformation ratio). When the output current is large enough, the current of the leakage inductance will continue not crossing zero throughout the dead time interval. The voltage applied to the leakage inductance is $V_{in}/2$; thus, the critical value of the output current to realize natural ZVS can be expressed as (6). When the converter realizes natural ZVS, the auxiliary circuit does not work, and i_{A_peak} is zero. The minimum value of the auxiliary current's peak value i_{A_peak} can be designed as in Figure 7.

$$i_{A\_peak\_min} = \frac{C_s V_{in}}{t_{dead}} \tag{5}$$

where C_s is the equivalent parallel capacitor of the main switch, V_{in} is the input voltage of the ITLDC, and t_{dead} is the dead time.

$$\frac{I_{o\_naturalZVS}}{n} = \frac{V_{in}}{2L_r} t_{dead} \tag{6}$$

where L_r is the leakage inductance of the transformer, and n is the transformation ratio.

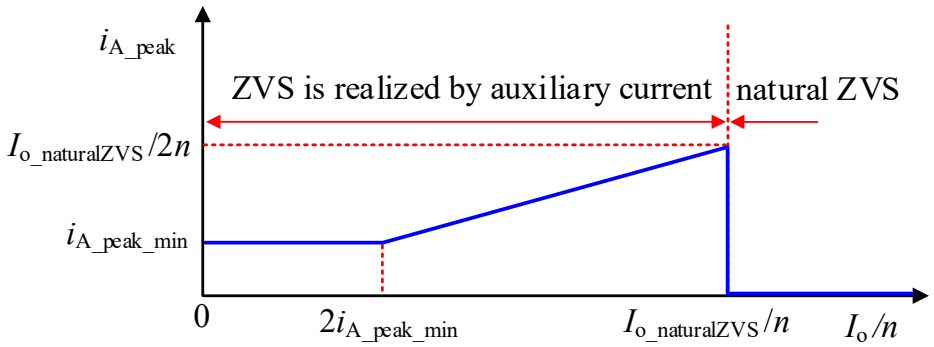

Figure 7. The designed value of i_{A_peak}.

3.1.2. The Auxiliary Inductor L_A

When the auxiliary current i_A is positive, the capacitor C_A is discharged, and when the current i_A is negative, the capacitor C_A is discharged. When the ITLDC reaches steady state, the voltage of C_A remains unchanged during one period. Thus, the charge variation of C_A in one period should be zero. According to Figure 4, during the time interval t_0~t_1, the auxiliary current i_{A1} decreases from i_{A_peak} to $-i_{A\_peak}$, the voltage $(V_{CA} - V_{in}/2)$ is applied to the auxiliary inductance L_{A1} and the time is DT_S; thus, the voltage of the auxiliary capacitor C_A can be expressed as (7).

According to Figure 4, in the time interval t_8~t_9, the auxiliary current is built up. The voltage V_{CA} is applied to the auxiliary inductance L_{A1}. At t9, the auxiliary current reaches the peak value i_{A_peak}; thus, the time to build up the auxiliary current can be expressed as (8). According to (7), the voltage V_{CA} changes with the duty cycle and the minimum voltage of V_{CA} will occur at the minimum duty cycle D_{min}. The maximum value of the time t_{A_build} should be smaller than $(1 - D_{min})T_s$, i.e., $t_{A\_build} < (1 - D_{min})T_s$. Considering that t_{A_build} can be expressed as (8) and the voltage V_{CA} can be expressed as (7), the maximum value of the auxiliary inductor L_A can be calculated as (9). Large L_A will result in large conduction losses and large ripple voltage of the auxiliary capacitor C_A; thus, the auxiliary inductor L_A can be selected with a small value but much greater than the leakage inductance L_r.

$$V_{CA} = \frac{1}{2}V_{in} - \frac{2i_{A\_peak}L_A}{DT_s} \tag{7}$$

$$t_{A\_build} = \frac{L_A i_{A\_peak}}{V_{CA}} \tag{8}$$

$$L_A < \frac{D_{min}(1 - D_{min})V_{in}T_s}{2(2 - D_{min})i_{A\_peak}} \tag{9}$$

3.1.3. The Auxiliary Capacitor C_A

When the auxiliary current i_A is positive, the auxiliary capacitor C_A is discharged. According to Figure 4, the time when the auxiliary current is positive is $(t_{A\_build} + DT_s/2)$ and the peak value of the auxiliary current is i_{A_peak}. As the auxiliary current is triangular, the charge variation during the discharge process can be calculated as (10). The charge variation will cause a voltage drop and the voltage drop can be calculated as $\Delta Q/C_A$. The maximum voltage drop will occur at D_{max} and D_{max} is equal to 0.5. If the maximum ripple of the voltage V_{CA} is set to 5%, (11) can be obtained. Considering that ΔQ can be expressed as (10) and V_{CA} can be expressed as (7), the minimum value of the auxiliary capacitor C_A can be calculated as in (12).

$$\Delta Q = \frac{1}{2}(t_{A\_build} + \frac{DT_s}{2})i_{A\_peak} = \frac{1}{2}(\frac{L_A i_{A\_peak}}{V_{CA}} + \frac{DT_s}{2})i_{A\_peak} \tag{10}$$

$$\Delta V_{CA} = \frac{\Delta Q(D_{max})}{C_A} < 5\% V_{CA}(D_{max}) \tag{11}$$

$$C_A > \frac{\Delta Q(D_{max})}{5\% V_{CA}(D_{max})} = \frac{(D_{max} T_s)^3 V_{in} i_{A\_peak}}{0.1(D_{max} T_s V_{in} - 4 L_A i_{A\_peak})^2} \tag{12}$$

3.2. Voltage and Current Stress Analysis

The circuit of the proposed ACAC does not operate in a resonance mode, the voltage of the auxiliary capacitor C_A is stable and the current of auxiliary inductor L_A is controllable. Thus, the proposed ACAC added to the ITLDC will not result in additional voltage stress. The voltage stress of the main switches S_1~S_4 is equal to $V_{in}/2$ and the voltage stress of the auxiliary switches is equal to V_{CA}. When the output current is large enough to realize natural ZVS, the auxiliary circuit does not work; thus, the ACACs do not increase the current stress of the main switches in the ITLDC. The current stress of the main switches is equal to I_{oN}/n, where I_{oN} is the designed maximum output current. The current stress of the auxiliary switches is equal to $I_{o\_naturalZVS}/2n$, which can be calculated from (6).

The voltage and current stress of the main switches do not increase with the proposed ACACs. The voltage and current stress of the auxiliary switches are smaller than the stress of the main switches.

3.3. Design of Snubber Capacitor

The snubber capacitor C_s will reduce the dv/dt and the turn-off losses of switches. According to [23], the minimum value of C_s can be expressed as (13), where I_{oN} is the rated current, and t_f is the turn-off fall time of the switches. To ensure the zero-voltage turn-off condition, the authors suggest that the snubber capacitor is designed slightly greater than the minimum value C_{smin}, 1.5 C_{smin}~2 C_{smin}, for example.

$$C_s > \frac{I_{oN} t_f}{n V_{in}} = C_{smin} \tag{13}$$

3.4. Loss Analysis

The proposed ACACs will result in power losses, including the core loss of the auxiliary inductance, conduction losses and switching losses of the auxiliary switch. With the ACACs the main switches realize zero-voltage turn-on and quasi-zero-voltage turn-off. Thus, the switching losses are reduced. The added losses and reduced losses will also be discussed.

3.4.1. The Losses Reduced by the ACAC

The turn-on and turn-off losses of the main switches are reduced. The turn-on losses can be expressed as (14), which consist of the loss caused by the output current and the loss caused by the equivalent output parallel with the main switches.

$$P_{SW\_on} = \left(\frac{V_{DS} I_o}{n} \frac{t_r + t_{fu}}{2} + \frac{1}{2} C_s V_{DS}^2\right) f_s \tag{14}$$

where V_{DS} is the drain-source voltage; t_r is the current rise time, which can be found in the datasheet; t_{fu} is the drain-source voltage fall time, which can be calculated according to [24]; C_s is the equivalent output parallel with the main switch, which consists of the added snubber capacitor and the energy-related effective output capacitance C_{o_er}, which can be found in the datasheet; and f_s is the switching frequency.

The turn-off losses can be expressed as (15), and they are mainly caused by the output current.

$$P_{SW\_off} = \frac{V_{DS} I_o}{n} \frac{t_f + t_{ru}}{2} f_s \tag{15}$$

where t_f is the current fall time, which can be found in the datasheet; t_{ru} is the drain-source voltage rise time, which can be calculated according to [25].

3.4.2. The Losses Resulting from the ACAC

The losses resulting from the ACAC include the core losses of the auxiliary inductor, conduction losses and switching losses of the auxiliary switch. According to [25], the core losses can be expressed as (16). Since the auxiliary current build-up time is very short, the conduction losses during the auxiliary current build-up process can be neglected; thus, the conduction loss is mainly generated during the DT_s interval, which can be calculated as (17). Since the auxiliary switch realizes zero-current turn-on and zero-voltage turn-off, the switching loss of the auxiliary switch can be expressed as (18).

$$P_{core} = aB_{pk}^{b} f^{c} \times V \tag{16}$$

where the constants a, b and c are determined from curve fitting, which can be obtained from the datasheet of the core. V is the volume of the magnetic core. B_{pk} is defined as half the AC flux swing, which can be calculated from the BH curve.

$$P_{Conduction} = I_{RMS}^2 R_{ESR} = \frac{1}{3} D i_{A\_peak}^2 R_{ESR} \tag{17}$$

where I_{RMS} is the RMS value of the auxiliary current; $R_{L,ESR}$ is the equivalent series resistance of the auxiliary inductor and drain source on state resistance.

$$P_{SAW\_on} = \frac{1}{2} C_{o\_er} V_{DS}^2 f_s = \frac{1}{2} C_{o\_er} {V_{CA}}^2 f_s \tag{18}$$

4. Experimental Results

To verify the proposed ZVS ITLDC, a 1.5 kW prototype ITLDC with ACACs is utilized with the specifications shown in Table 1. When the proposed ITLDC is used to charge EVs, the ACACs mainly play a role in the constant-voltage charging stage. During the constant-voltage charging stage, the charging current changes with charging time and the charging current is relatively small. Then, the ITLDC cannot realize natural ZVS soft switching during the constant-voltage charging stage; thus, the ACACs will work to realize ZVS soft switching. In this experiment, the input voltage is 400 V, which is powered by a programmable DC voltage source. The variable resistor with 80 Ω maximum resistance is used as a load and the output voltage is controlled to 150 V. The snubber capacitors C_s are added in parallel with the main switches, and the equivalent parallel capacitors C_1~C_4 are increased; thus, the main switches are turned off at quasi-zero-voltage condition. A photograph of the experimental platform is shown in Figure 8.

Table 1. The specifications of the prototype ITLDC.

Items	Value
Input voltage V_{in}	400 V
Output voltage V_{out}	150 V
Maximum output current I_o	10 A
Main switches	IPW65R041CFD
Auxiliary switches	IXFH22N65X2
Diode D_{R1}, D_{R2}	DSEI60-06A
Switching frequency f	40 kHz
Transformer ratio n	1:1
Magnetizing inductances L_m	1.22 mH

Table 1. *Cont.*

Items	Value
DC-blocking capacitor C_b	40 μF
Leakage inductance L_r	1.8 μH
Added snubber capacitor	1000 pF
Dead time t_{dead}	0.35 μs
Filter inductance L_o	0.5 mH
Auxiliary inductor L_A	18 μH
Auxiliary capacitor C_A	9.4 μF

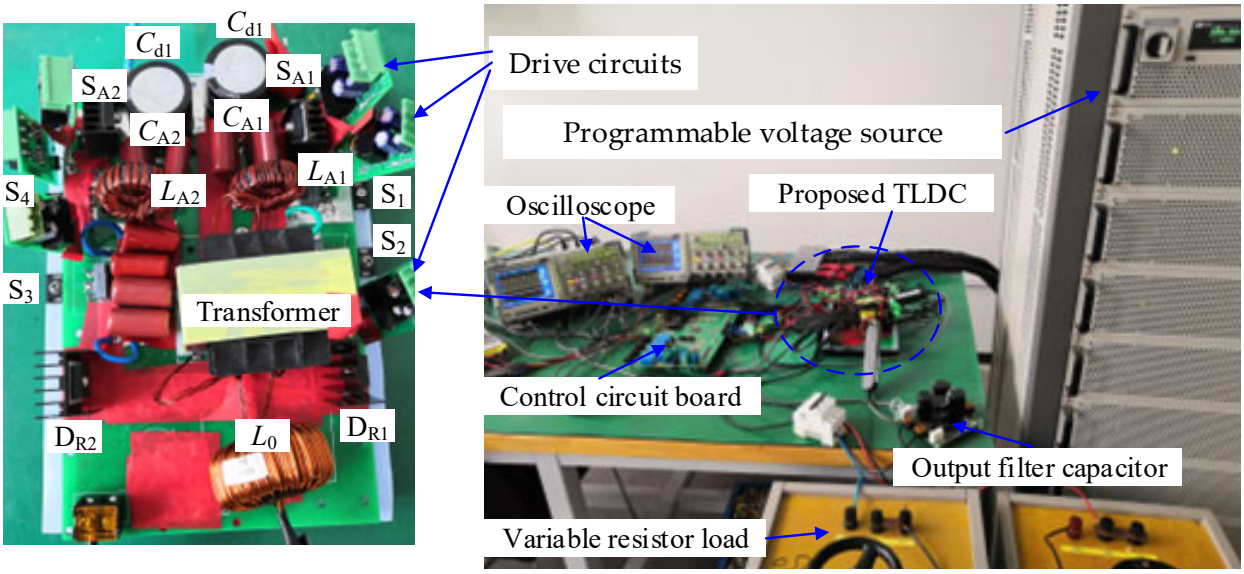

Figure 8. A photograph of the experimental platform.

The main waveforms measured are shown in Figure 9, where V_{DS1} is the drain-source voltage of the main switch S_1, G_{S1} is the drive of S_1, i_o is the output current, i_{Lr} is the current of the primary winding of the transformer, V_{CA1} is the voltage of the auxiliary capacitance C_{A1}, G_{S2} is the drive of S_2, G_{SA1} is the drive of S_{A1}, and i_{A1} is the auxiliary current flowing through L_{A1}. The turn-on process of the main switch S_1 without ACACs is shown in Figure 9a,b. As shown in Figure 9a, the output current i_o is 2 A, and before S_1 is turned on, the voltage V_{DS1} is discharged from 200 V to 150 V. As shown in Figure 9b, the output current i_o is 10 A, and before S_1 is turned on, the voltage V_{DS1} is discharged from 200 V to 40 V firstly; however, V_{DS1} increases to 160 V quickly. In Figure 9a,b, the zero-voltage turn-on condition of the main switch S_1 is unrealized. However, as shown in Figure 9c, the main switch S_1 is turned off at quasi-zero-voltage condition. This is because the equivalent parallel capacitors C_1~C_4 limit the rising slope of the voltage across the main switches. In this experiment, 1000 pF snubber capacitors are added in parallel with the main switches and the time-related effective output capacitance of the main switch is 1485 pF (documented in the data sheet); thus, the snubber capacitors C_s of the main switches are equal to 2485 pF.

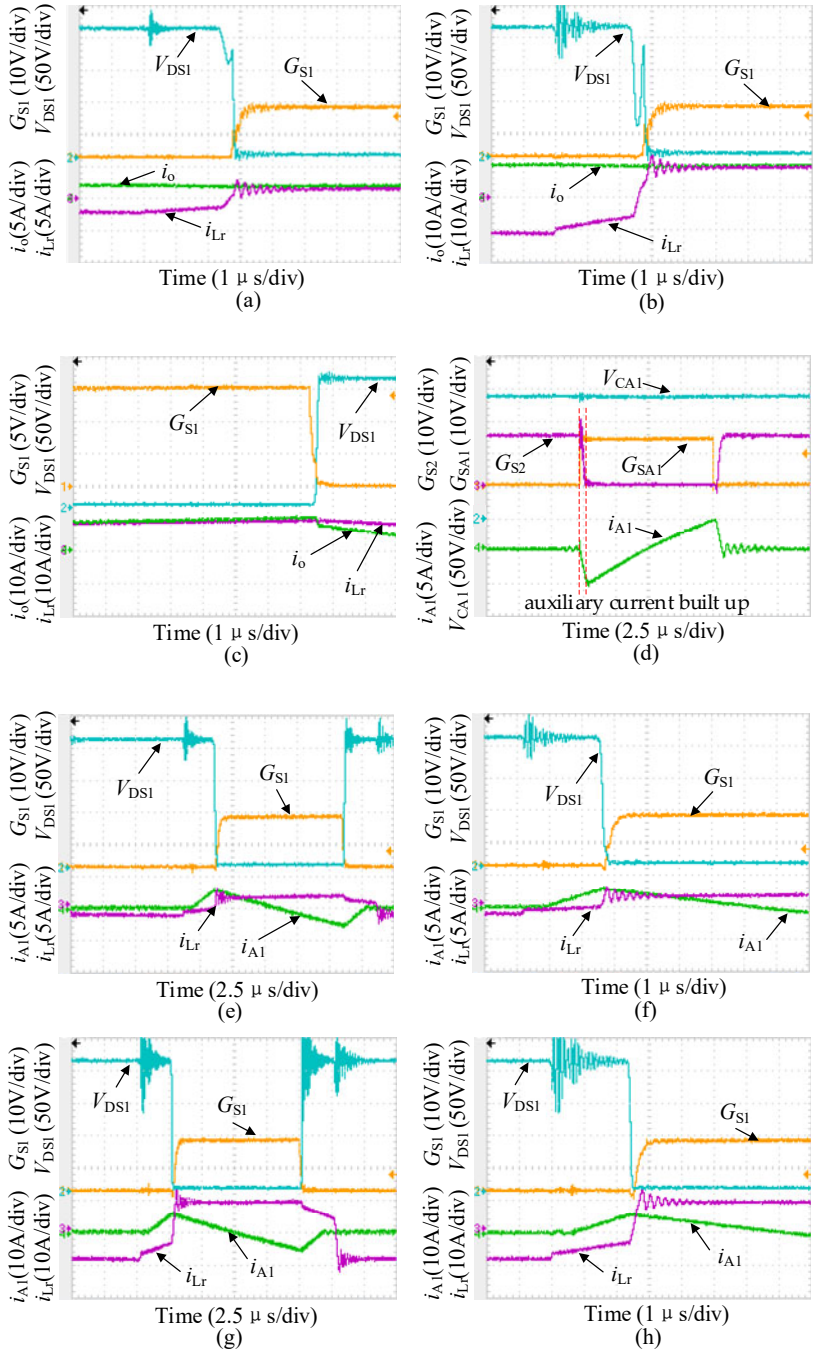

Figure 9. Main experimental waveforms of the ITLDC: (**a**) turn on process of S_1 without ACACs, I_o = 2 A, (**b**) turn on process of S_1 without ACACs, I_o = 10 A, (**c**) turn-off process of S_1, (**d**) auxiliary current build-up process, (**e**,**f**) switching process of S_1 with ACACs, I_o = 2 A, (**g**,**h**) switching process of S_1 with ACACs, I_o = 10 A.

In fact, according to (6), to realize natural ZVS, the output current i_o should be larger than 38.9 A. When the output current is not large enough to realize natural ZVS, the proposed ACACs can be used to realize ZVS. As shown in Figure 9d, before S_2 is turned off, the auxiliary switch S_{A1} is turned on and the auxiliary current i_{A1} increases rapidly from 0 A; thus, the auxiliary switch realizes zero-current turn-on. When S_2 is turned off, the auxiliary current i_{A1} reaches the maximum value. The voltage of the auxiliary capacitance C_{A1} is steady and the value of V_{CA1} is approximately 190 V, which is consistent with the theoretical calculation value. According to (5), to realize zero-voltage turn-on of the main switch, the minimum value of the auxiliary current $i_{A\_peak\_min}$ should be 2.8 A. According

to Figure 7, when the output current is 2 A, the auxiliary current should be larger than 2.8 A; in this experiment, the auxiliary current i_{A_peak} is 3 A. As shown in Figure 9e,f, with the auxiliary current, the main switch realized zero-voltage turn-on. When the output current is 10 A, the auxiliary current should be larger than 5 A; in this experiment, the auxiliary current i_{A_peak} is 6 A. As shown in Figure 9g,h, with the auxiliary current, the main switch realized zero-voltage turn-on. With the proposed ACACs, the main switches of the ITLDC realized zero-voltage turn-on. To verify the efficiency, the efficiency of the ITLDC with the proposed ACACs and without ACACs is measured by a HIOKI power analyzer PW6001 and the efficiency changes with the output power are shown in Figure 10. When the output power is small, the efficiency of the ITLDC with ACACs is slightly higher than that of the ITLDC without ACACs, and when the output power is large, the efficiency of the ITLDC with ACACs is much higher than that of the ITLDC without ACACs.

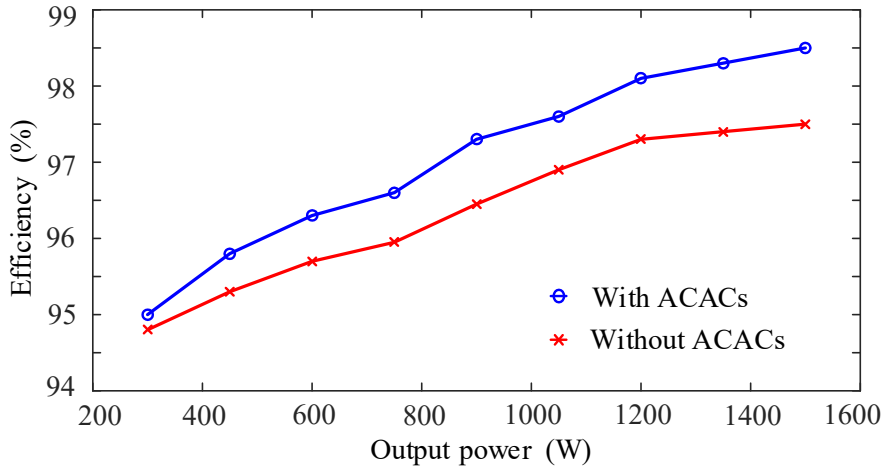

Figure 10. The efficiency of the ITLDC.

It is interesting to compare the proposed ZVS method and the state-of-the-art ZVS methods for the four-switch ITLDC. The comparison results are summarized in Table 2. The auxiliary circuits, soft switching of the switches, soft switching range and current/voltage stress are employed to evaluate the ZVS methods. Each ZVS method has its own advantages. For example, in [16,20], wide load range ZVS turn-on and turn-off for all switches is realized; in [17], wide load range soft switching is realized by the auxiliary circuit with only two switches; in [19], the ZVS is realized with no auxiliary circuits. However, most of them do not realize the full load range ZVS; thus, with the light load situation—for example, the battery floating charge stage—the converter has to work with hard switching. Many ZVS methods realize wide load range ZVS; however, the ZVS range will decrease when considering the dead time between switches. Although two ACACs are added in the proposed ZVS converter, the full load range ZVS of the main switches is realized. Furthermore, the auxiliary switches realized zero current turn-on and zero-voltage turn-off, and this ZVS method does not increase the current stress of the switches.

Table 2. Comparison of the proposed ZVS method with the state-of-the-art ZVS methods.

Converter	Auxiliary Circuits	Soft Switching of the Switches	Soft Switching Range	Current/Voltage Stress
In [16]	Combined converter	ZVS turn-on and turn-off for all switches	Wide load range	$2I_o/n$, $V_{in}/2$
In [17]	Two switches	Q_2, Q_4 ZVS turn-on and ZCS turn-off, Q_1, Q_3, Q_{a1}, Q_{a2} ZCS turn-on and ZVS turn-off	Wide load range	I_o/n, slightly higher than $V_{in}/2$
In [18]	No auxiliary circuits	ZVS turn-on and turn-off for all switches	Traditional load range	I_o/n, $V_{in}/2$
In [20]	Two CACs	ZVS turn-on and turn-off for all switches	Wide load range	higher than I_o/n, $V_{in}/2$
Proposed	Two ACACs	ZVS turn-on and turn-off for all the main switches, ZCS turn-on and ZVS turn-off for the auxiliary switches	Full load range	I_o/n, $V_{in}/2$

5. Conclusions

This paper has presented an ACAC for the ITLDC to realize full load range ZVS. With the proposed ACACs, all the main switches achieved zero-voltage turn-on and the auxiliary switches realized zero-current turn-on and zero-voltage turn-off; thus, the efficiency will be high. The auxiliary current generated by the ACAC is controllable, and the ACACs will not work when the current of the ITLDC is large enough to realize natural ZVS; thus, the ACACs do not increase the current stress of the switches in the ITLDC. The ITLDC with the proposed ACACs is suitable for electric vehicle charging applications; during the constant-current charging stage, the ITLDC can be designed to realize nature ZVS; during the constant-voltage charging stage, the charging current will decrease, and the ITLDC can work with ACACs to realize ZVS; thus, high efficiency can be achieved during the whole charging process.

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References

1. Danese, A.; Torsæter, B.N.; Sumper, A.; Garau, M. Planning of high-power charging stations for electric vehicles: A review. *Appl. Sci.* **2022**, *12*, 3214. [CrossRef]
2. Liu, C.; Fang, J. Analysis and design of inertia for grid-tied electric vehicle chargers operating as virtual synchronous machines. *Appl. Sci.* **2022**, *12*, 2194. [CrossRef]
3. Fan, S.; Sun, L.; Duan, J.; Zhang, K. Improved active clamped ZVS buck converter with freewheeling current transfer circuit. *IET Power Electron.* **2019**, *12*, 1341–1348. [CrossRef]
4. Nassary, M.; Vidal-Idiarte, E.; Calvente, J. Analysis of non-minimum phase system for AC/DC battery charger power factor correction converter. *Appl. Sci.* **2022**, *12*, 868. [CrossRef]
5. Tan, L.; Wu, B.; Yaramasu, V.; Rivera, S.; Guo, X. Effective voltage balance control for bipolar-DC-bus fed EV charging station with three-level DC-DC fast charger. *IEEE Trans. Ind. Electron.* **2016**, *63*, 4031–4041. [CrossRef]

6. Haga, H.; Kurokawa, F. A novel modulation method of the full bridge three-level LLC resonant converter for battery charger of electrical vehicles. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, 20–24 September 2015; pp. 5498–5504. [CrossRef]
7. Barbi, I.; Gules, R.; Redl, R.; Sokal, N.O. DC–DC converter: Four switches Vpk = Vin/2, capacitive turn-off snubbing, ZV turn-On. *IEEE Trans. Power Electron.* **2004**, *19*, 918–927. [CrossRef]
8. Liu, D.; Deng, F.; Zhang, Q.; Chen, Z. Zero-voltage switching PWM strategy based capacitor current-balancing control for half-bridge three-level DC/DC converter. *IEEE Trans. Power Electron.* **2018**, *33*, 357–369. [CrossRef]
9. Liu, W.; Jin, H.; Yao, W.; Lu, Z. An interleaved PWM method with better voltage-balancing ability for half-bridge three-level DC/DC converter. *IEEE Trans. Power Electron.* **2018**, *33*, 4594–4598. [CrossRef]
10. Liu, D.; Deng, F.; Zhang, Q.; Chen, Z. Periodically Swapping Modulation (PSM) strategy for Three-Level (TL) DC/DC converters with balanced switch currents. *IEEE Trans. Ind. Electron.* **2018**, *65*, 412–423. [CrossRef]
11. Guo, Z.; Sun, K.; Sha, D. Improved ZVS three-level DC–DC converter with reduced circulating loss. *IEEE Trans. Power Electron.* **2016**, *31*, 6394–6404. [CrossRef]
12. Sha, D.; Chen, D.; Zhang, J. A Bidirectional three-level DC–DC converter with reduced circulating loss and fully ZVS achievement for battery charging/discharging. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 993–1003. [CrossRef]
13. Liu, D.; Wang, Y.; Zhang, Q.; Chen, Z. ZVZCS full-bridge three-level DC/DC converter with reduced device count. *IEEE Trans. Power Electron.* **2020**, *35*, 9965–9970. [CrossRef]
14. Azeem, S.W.; Chen, W.; Tariq, I.; Ye, H.; Kaija, D. A hybrid resonant ZVZCS three-level converter suitable for photovoltaic power DC distribution system. *IEEE Access* **2020**, *8*, 114981–114990. [CrossRef]
15. Das, P.; Pahlevaninezhad, M.; Singh, A.K. A novel load adaptive ZVS auxiliary circuit for PWM three-level DC–DC converters. *IEEE Trans. Power Electron.* **2015**, *30*, 2108–2126. [CrossRef]
16. Shi, Y.; Yang, X. Wide-range soft-switching PWM three-level combined DC–DC converter without added primary clamping devices. *IEEE Trans. Power Electron.* **2014**, *29*, 5157–5171. [CrossRef]
17. Shi, Y.; Wang, X.; Xi, J.; Gui, X.; Yang, X. Wide load range ZVZCS three-level DC–DC converter with compact structure. *IEEE Trans. Power Electron.* **2019**, *34*, 5032–5037. [CrossRef]
18. Fan, S.; He, H.; Chen, S.; Duan, J.; You, J.; Bai, L. Zero voltage switching non-isolated bidirectional DC–DC converter with transient current built-up technique. *J. Power Electron.* **2022**, *22*, 764–772. [CrossRef]
19. Shi, Y.; Yang, X. Wide range soft switching PWM three-level DC–DC converters suitable for industrial applications. *IEEE Trans. Power Electron.* **2014**, *29*, 603–616. [CrossRef]
20. Urtasun, A.; Berrueta, A.; Sanchis, P.; Marroyo, L. Parameter-independent control for battery chargers based on virtual impedance emulation. *IEEE Trans. Power Electron.* **2018**, *33*, 8848–8858. [CrossRef]
21. Safayatullah, M.; Elrais, M.T.; Ghosh, S.; Rezaii, R.; Batarseh, I. A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications. *IEEE Access* **2022**, *10*, 40753–40793. [CrossRef]
22. Qiu, W.; Mercer, S.; Liang, Z.; Miller, G. Driver deadtime control and its impact on system stability of syn-Chronous buck voltage regulator. *IEEE Trans. Power Electron.* **2008**, *23*, 163–171. [CrossRef]
23. Choe, H.J.; Chung, Y.C.; Sung, C.H.; Yun, J.J.; Kang, B. Passive snubber for reducing switching power losses of IGBT in dc-dc boost converter. *IEEE Trans. Power Electron.* **2014**, *29*, 6332–6341. [CrossRef]
24. Graovac, D.; Pürschel, M.; Andreas, K. MOSFET power losses calculation using the data-sheet parameters. *Infineon Appl. Note* **2006**, *1*, 1–23.
25. Barg, S.; Ammous, K.; Mejbri, H.; Ammous, A.; Hanen, M. An improved empirical formulation for magnetic core losses estimation under Nonsinusoidal induction. *IEEE Trans. Power Electron.* **2017**, *32*, 2146–2154. [CrossRef]