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A Single-Bit Incremental Second-Order Delta-Sigma Modulator with Coarse-Fine Input Buffer

Mookyoung Yoo, Kyeongsik Nam, Gyuri Choi, Sanggyun Kang, Byeongkwan Jin, Hyeoktae Son, Kyounghwan Kim and Hyoungho Ko *

Department of Electronics Engineering, Chungnam National University, Daejeon 34134, Republic of Korea
* Correspondence: hhko@cnu.ac.kr

Featured Application: Low noise circuit, delta-sigma modulator, analog to digital converter.

Abstract: This paper presents an incremental second-order delta-sigma modulator with a coarse-fine input buffer in 180-nm CMOS. The modulator's architecture was implemented as a second-order cascade of integrators with a feedback structure. The switched-capacitor integrator was operated in discrete time, with high-gain amplifiers required to achieve improved performance during the integration phase. The amplifier comprised rail-to-rail input and gain-boosted cascode intermediate stages, thus achieving a high gain and wide input voltage range. The circuit adopts a coarse-fine buffer for higher performance. The coarse buffer is operated first to enable fast settling through a high slew rate, followed by the fine buffer to satisfy the low-noise and high-accuracy characteristics. The fine buffer has a smaller current consumption with higher power efficiency. The experiment results show that the proposed input buffer achieved a 13.14 effective number of bits and an 80.87 dB signal-to-noise and distortion ratio. The modulator operates a single bit and sampling clock at 125 kHz. The proposed delta-sigma modulator was operated at 1.8 V. The proposed circuit was designed using a standard 0.18-µm CMOS process with an active area of 1.06 mm^2. The total current consumption with the coarse-fine buffer was 1.374 mA.

Keywords: coarse-fine input buffer; pre-charge buffer; low-noise amplifier; delta-sigma modulator; incremental delta-sigma modulator

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1. Introduction

Analog-to-digital converters (ADCs) have attracted considerable attention for their potential in applications that require high resolution, such as wearable bio-signal sensors [1] or biosensor arrays [2,3]. Delta-sigma modulation (DSM) ADCs are often chosen for processing low-frequency signals, which are within a few kilohertz [4]. Many high-precision sensors were reported with high-resolution DSM, such as the Hall sensor [5], electrochemical sensor [6], bridge sensor [7], and so on. Among the various DSM architectures, the incremental DSM [8,9] is widely used for multiplexing between multichannel inputs [10–12]. To achieve high resolution, the DSMs with second or higher-order noise shaping have been employed for achieving high-resolution [13,14]. The delta-sigma input stage is designed for continuous time (CT) or discrete time (DT) [15]. Oversampling and noise shaping are widely used to realize low-noise characteristics, so the input stage of the DSM acts as the high-frequency switching load at the point of the input buffer view. Assuming tens to thousands of oversampling rates (OSRs), the input buffer inside the DSM should operate as fast as the OSR times the output rate of the DSM. Fast operations cause higher power consumption, making the implementation of the buffer design a challenge in high-resolution ADC design. Moreover, when converting an analog input signal, the input signal is often corrupted by kickback noise [16] from the conversion. To prevent signal degradation, an input buffer with precise settling characteristics within the desired sampling period is highly desired.

Figure 1 shows the conventional and proposed input buffer schemes. In the conventional input buffer scheme, the input buffer drives the input-switching loads of the DSM input stage. A buffer is required to drive the input stage, and a high slew rate, power, and speed are required to achieve high-resolution performance. High power is required to drive the CT and DT input stages using a single buffer. As shown in Figure 1a, a pre-charge scheme has been reported to relax buffer requirements [17,18]. The internal pre-charge buffer relaxes the external buffer specifications [19,20]. Fast charging has been performed with the assistance of a pre-charge buffer [17–20]; the external buffer settled only a small voltage to the final desired value. In [21], the low noise fully differential amplifier (THP210, Texas Instruments, Dallas, TX, USA) drives the DSM (ADS127L11, Texas Instruments, Dallas, TX, USA), which includes the pre-charge buffer, and the current consumption of the driving amplifier is 950 uA. In this paper, a single-bit incremental second-order DSM with a coarse-fine input buffer is proposed.

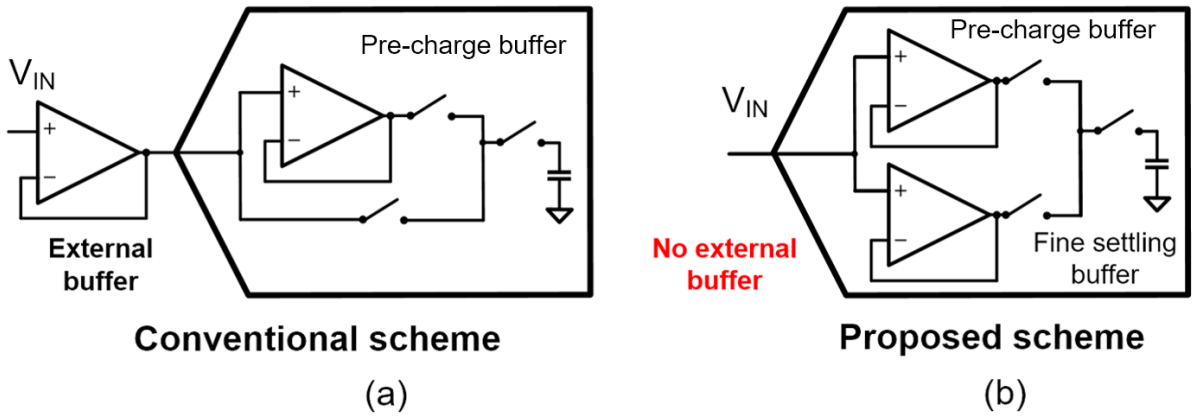


Figure 1. Conventional and proposed input buffer scheme: (**a**) Conventional external input buffer with internal pre-charge buffer; (**b**) Proposed internal coarse-fine dual input buffer.

The proposed input buffer with a parallel coarse fine buffer scheme is shown in Figure 1b. In existing technologies, DSM performance is limited by the driving ability of the external fine buffer. In the proposed scheme, the coarse-fine input buffer is integrated; thus, no external buffer is required. The coarse-fine input buffer includes two buffers: a pre-charge buffer and a fine settling buffer. Using the coarse-fine input buffer, both the fast settling and low noise characteristics can be achieved. Considering the circuit area and power consumption of the external buffer in the conventional scheme, the area and power consumption penalty of the proposed coarse-fine buffer is negligible. In our proposed DSM ADC, the input buffer and secondary DT DSM are integrated.

The operational concept of the coarse-fine buffer-based input buffer circuit is shown in Figure 2. In this paper, the pre-charge and fine paths were placed in parallel; coarse pre-charge was performed by the pre-charge path buffer according to the timing, and then fine settling was performed by the low-noise fine buffer. A fast buffer that drives the coarse path and a low-noise fine path buffer were built in parallel, and the internal voltage was precisely settled with the fine buffer after charging most of the voltage with the coarse buffer. The proposed scheme integrates the buffer and DSM to achieve stable performance without an external buffer. The circuit designed in this research can be applied to precise measurement requiring low-noise analog signal processing without a separate external buffer.

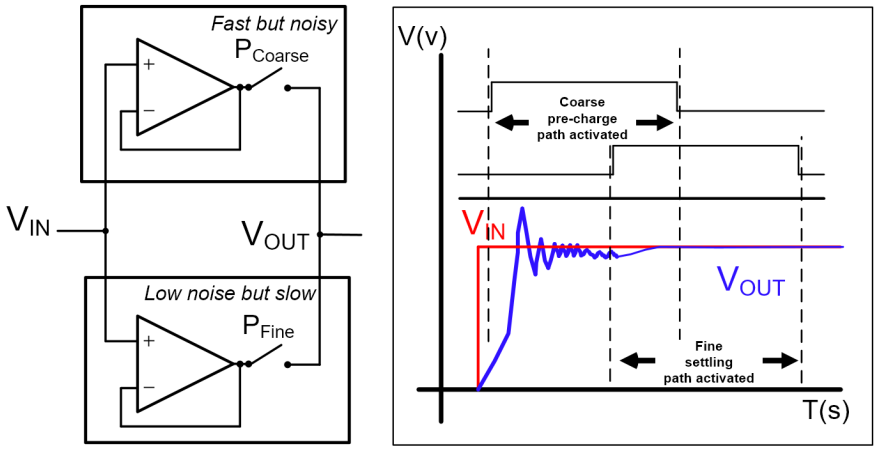


Figure 2. Working process of coarse-fine input buffer.

2. Proposed Delta Sigma Modulator with Coarse-Fine Input Buffer

The block diagram of the proposed circuit is shown in Figure 3. The circuit comprises two main parts: a coarse-fine, pre-charged buffer that acquires analog signals and a DSM that post-processes it. Both circuits require timing circuits to optimize their performance. The operational times of the coarse and fine buffers are partially shared. The input buffer internal chopper clock uses a frequency of 16 kHz. The unintended noise in the low-frequency band can be significantly reduced through chopper modulation. The sampling signal used was 125 kHz, higher than the chopper frequency, and the oversampling rate was set at 512. The circuit characteristics can be controlled by externally adjusting the resistor through a serial peripheral interface (SPI). Through SPI logic manipulation, modulator and buffer blocks can be enabled or disabled, and the performance of each block is tested.

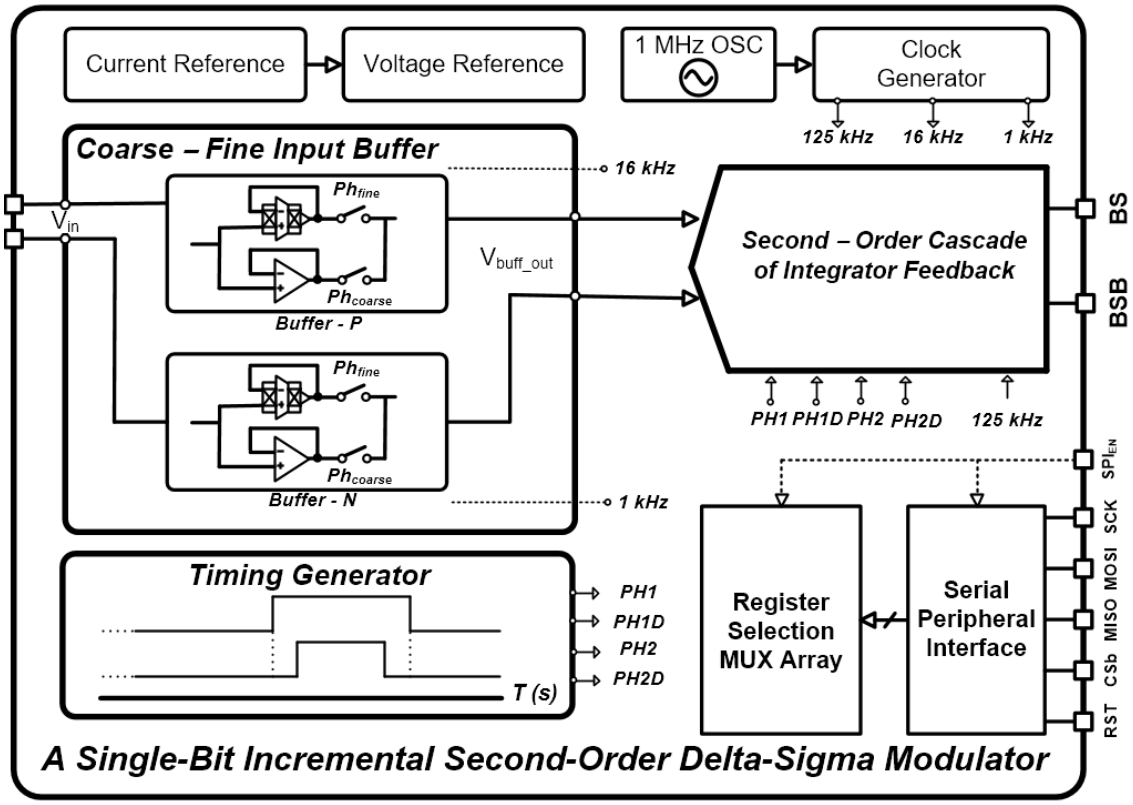


Figure 3. Block diagram of the proposed circuit.

2.1. Coarse-Fine Input Buffer

A coarse-fine input buffer was used for fast, low-noise, characteristic-based analog signal acquisition. As shown in Figure 4, the input buffer comprises a parallel connection between the coarse and fine buffers and a timing circuit. The main characteristics of coarse circuits are that they are faster and noisier than fine buffers. To compensate for this, a low-noise but slow fine buffer was connected in parallel. The acquisition of analog signals with high speed and low noise can be achieved through two complementary and timing circuits. The circuit had two inputs and two outputs; the output was fed to a DSM for the post-processing of the acquired analog signal. For low-noise characteristics, a fine buffer must have high voltage gain characteristics.

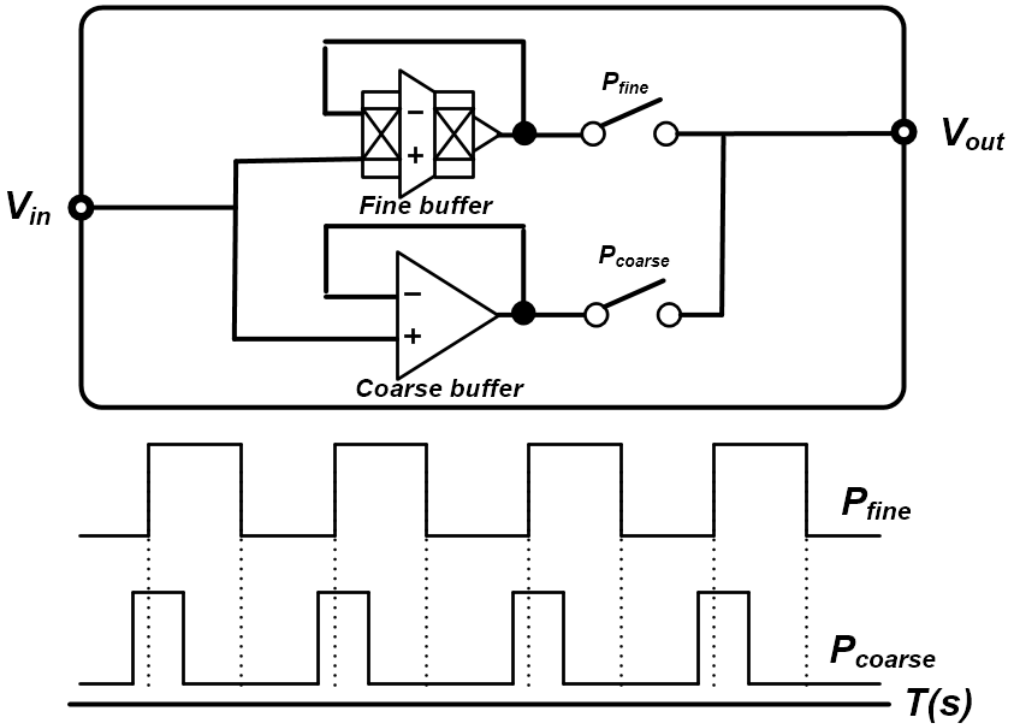


Figure 4. Schematic of coarse-fine input buffer.

The chopper technique was used to reduce flicker noise in the low-frequency band [22,23] in the fine buffer. The input chopper modulates the input signal to a higher frequency and prevents degradation due to the low-frequency noise. The output chopper demodulates the input signal to the baseband and also modulates the low-frequency noise of the amplifier to the high-frequency band; thus, a high signal-to-noise ratio can be achieved.

The coarse buffer was designed to operate with the unit-gain bandwidth of 3 MHz. The bandwidth of the fine buffer is limited by the chopper frequency. The chopper is operated at 16 kHz. The output stage of the fine and coarse buffers is designed using the Monticelli-style class-AB amplifier circuit [24] to enhance the driving capability of the switching load.

The amplifier used for the coarse buffer is shown in Figure 5. The circuit was a single-ended Monticelli amplifier circuit. A rail-to-rail input output-type circuit was used for a wide range of analog signal inputs and outputs. A Miller compensation capacitor is used from the class-AB output terminal for the stable operation of the circuit.

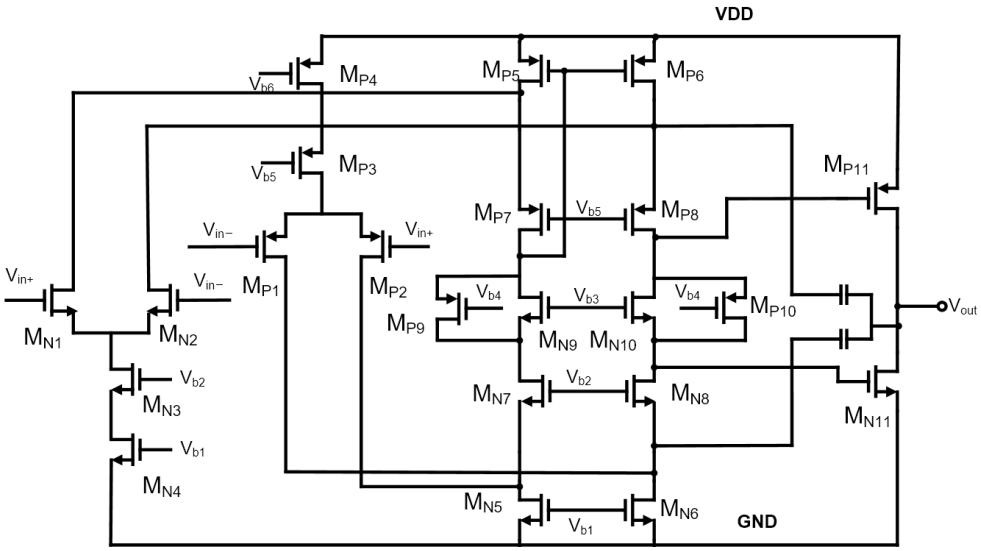


Figure 5. Schematic of the coarse input buffer.

The amplifier used in the fine buffer is shown in Figure 6. The circuit structure is similar to that of the coarse buffer circuit. However, a chopper is used between the input and output stages to focus on the low-noise characteristics. In the input stage, the signal was modulated using a chopper, and the folded cascode stage was demodulated. There is a difference in the total amount of current compared to the coarse buffer. Low-noise characteristics can be achieved by adjusting the input differential amplifier stage and the folded-cascode stage current ratio. To optimize the g_m value, which is important for optimizing low-noise characteristics, a fine buffer can achieve low-noise characteristics. Coarse and fine buffers have similar circuit structures but complementary characteristics. The coarse buffer is responsible for operating characteristics over a wide frequency range, while the fine buffer has high voltage gain and low noise characteristics. Figure 7 shows the transient simulation results for the optimal timing of each buffer. The enable time of the coarse buffer is slightly shorter than that of the fine buffer. Two buffer enable times of approximately 1 µs were shared. Both enable the signals to operate at a frequency of 125 kHz. The signal is stabilized by the fine buffer after the pre-charge of the coarse buffer with a fast settling time.

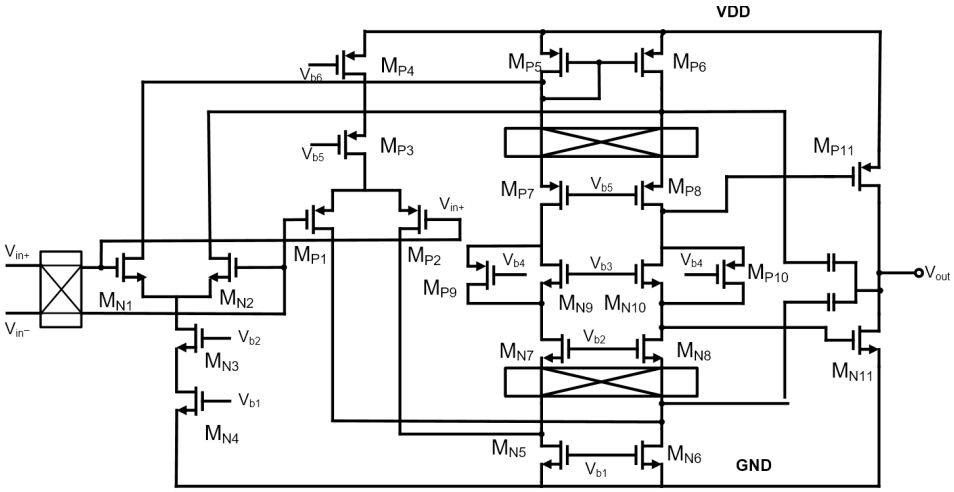


Figure 6. Schematic of the fine input buffer.

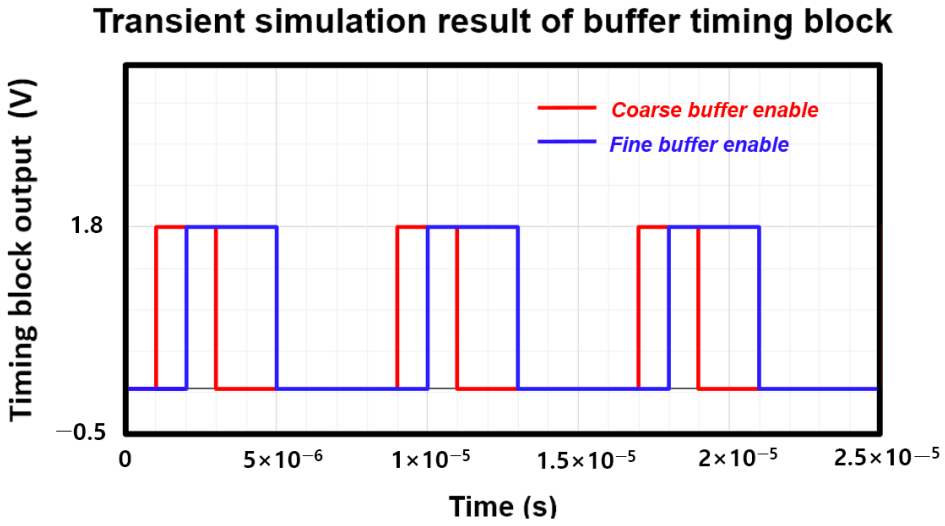


Figure 7. Transient simulation result of the buffer's enable timing diagram.

2.2. Second-Order Incremental Cascade of Integrator Feedback

The DSM circuit is designed as a second-order cascade of an integrator with feedback (CIFB). Figure 8a shows the block diagram of the secondary CIFB circuit. Figure 8b shows the schematic of the modulator. The OSR in the secondary modulator circuit is assumed to be 512. Moreover, the sampling frequency was set to 125 kHz, and the passband frequency was given to 122.07 Hz. From the assumed parameters, the noise transfer function (*NTF*) and signal transfer function (*STF*) are expressed as follows:

$$NTF = \frac{(z-1)^2}{(z^2 - 1.225z + 0.4415)} \tag{1}$$

$$STF = \frac{0.21637}{(z^2 - 1.225z + 0.4415)} \tag{2}$$

The coefficients a_1, a_2, b_1, and c_1 are designed to satisfy the following relationship (3) when the supply voltage of the circuit (V_{dd}) was at 1.8 V:

$$a_1 = \frac{C_1 V_{dd}}{C_2},\ a_2 = \frac{C_4 V_{dd}}{C_5},\ b_1 = \frac{C_1 V_{dd}}{C_2},\ c_1 = \frac{C_3}{C_5} \tag{3}$$

The coefficients are calculated using the MATLAB behavioral model and approximated according to the design rule of the metal-insulator-metal (MIM) capacitors. The coefficients are summarized in Table 1.

The amplifier used in the DSM integrator is shown in Figure 9. The circuit was designed as a fully differential amplifier (FDA) with rail-to-rail input and output to maximize the voltage input and output. A Miller compensation capacitor was used to stabilize the frequency band of the circuit. A gain-boosting technique was used to optimize the voltage gain. In the folded cascode amplification circuit, electrical signals are input from the sources of M_{P6} and M_{P7}, and of M_{N6} and M_{N7}. The amplified electrical signal is then outputted to the gates. M_{P12}, M_{P13}, M_{P14}, M_{P15}, M_{N13}, and M_{N14} were used as common-mode feedback circuits.

Figure 10 shows the loop gain simulation of the FDA used as an integrator. The DC gain, unit gain bandwidth, and phase margin are 180 dB, 1.8 MHz, and 60°, respectively. The FDA draws approximately 210 µA at a voltage supply of 1.8 V.

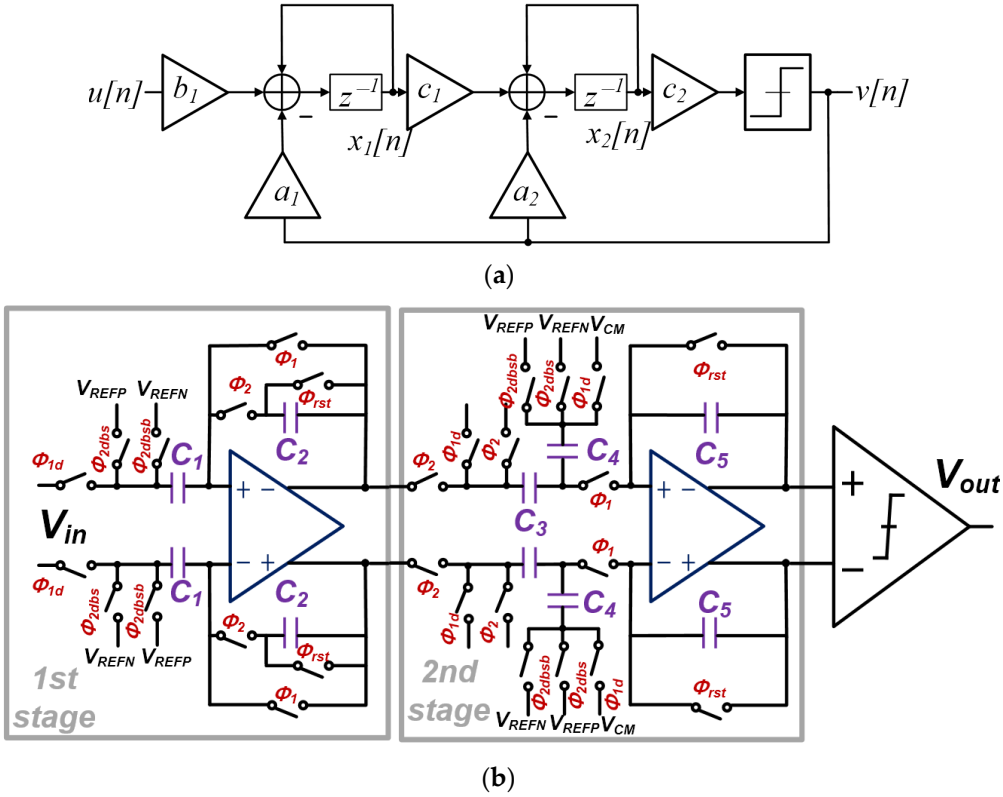


Figure 8. (**a**) Block diagram; (**b**) Schematic of second-order delta-sigma modulator.

Table 1. Comparison of simulated ideal coefficients and actual coefficients designed with MIM capacitors.

Coefficient	Ideal Value	Real Value
a1	0.1125	0.1112
a2	0.18	0.1776
b1	0.1125	0.1112
c1	0.45	0.4365

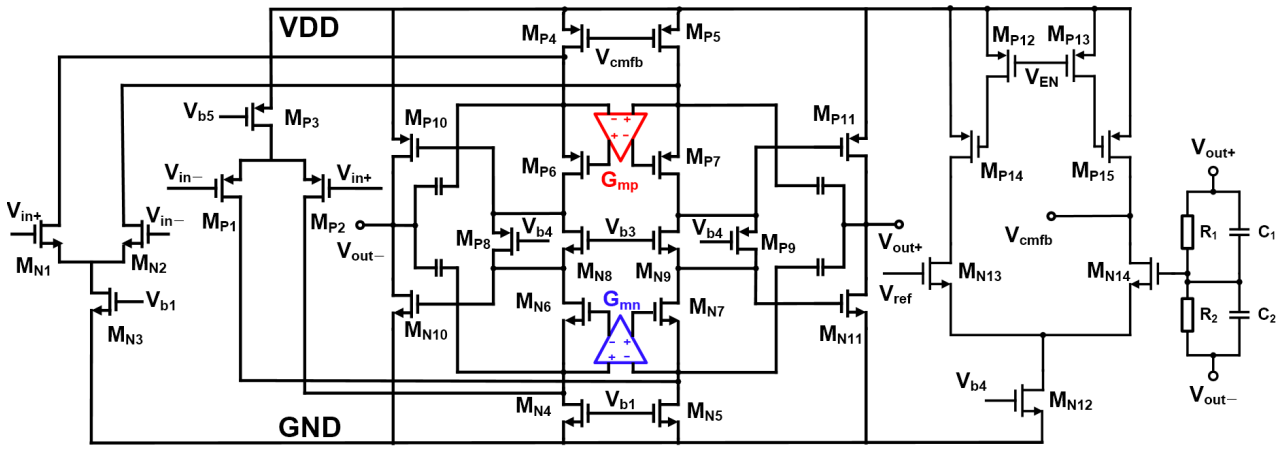


Figure 9. Fully differential amplifier for integrator.

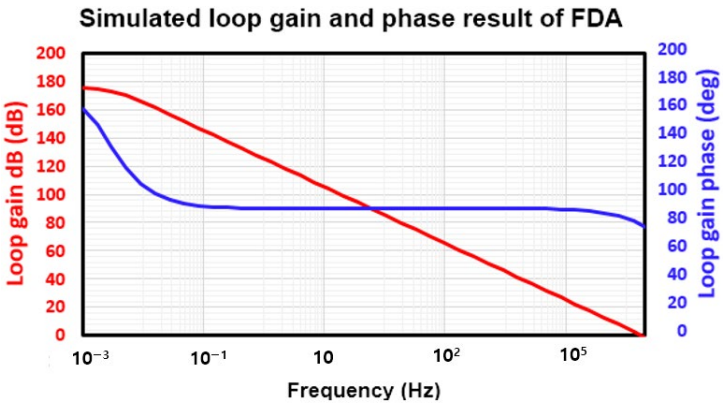
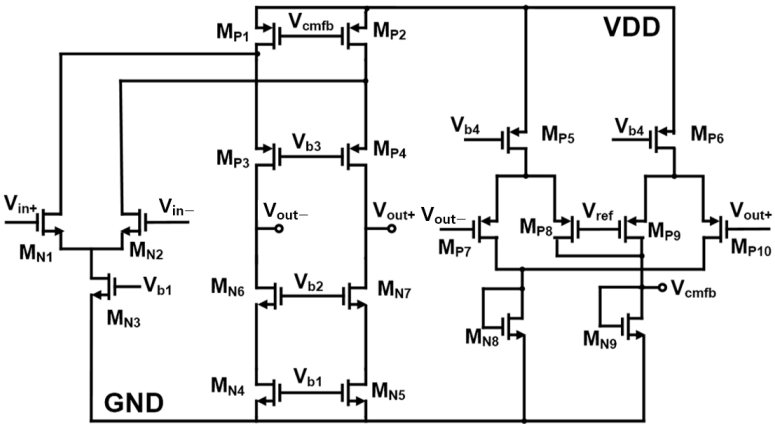


Figure 10. FDA loop gain simulation result in integrator.

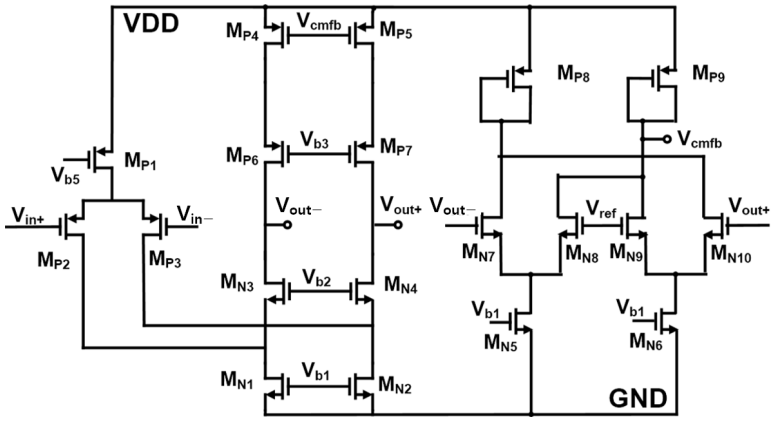
The PMOS and NMOS gain-boosting circuits are shown in Figure 11a,b, respectively. These circuits are used for G_{mn} and G_{mp} in Figure 9. The G_{mn} and G_{mp} are designed using a folded-cascode amplifier configuration. The G_{mn} and G_{mp} provide the boosted gain of Equations (4) and (5), respectively.

$$G_{mn} = g_{mn1}(r_{on1} \,||\, r_{op1})(g_{mp3}r_{op3}) \,||\, (g_{mn8}r_{on8}r_{on4}) \tag{4}$$

$$G_{mp} = g_{mp2}(r_{op2} \,||\, r_{on1})(g_{mn3}r_{on3}) \,||\, (g_{mp6}r_{op6}r_{op4}) \tag{5}$$



(**a**)



(**b**)

Figure 11. Gain boosting amplifier of G_{mp} (**a**) and G_{mn} (**b**).

The two-stage comparator at the end of the modulator stage is shown in Figure 12. The pre-amplifier stage is designed using the PMOS input stage and the gain-enhanced positive feedback NMOS loads (M_{N2} and M_{N3}) and diode-connected loads (M_{N1} and M_{N4}). The second stage is designed using the dynamic latch and the following SR-latch.

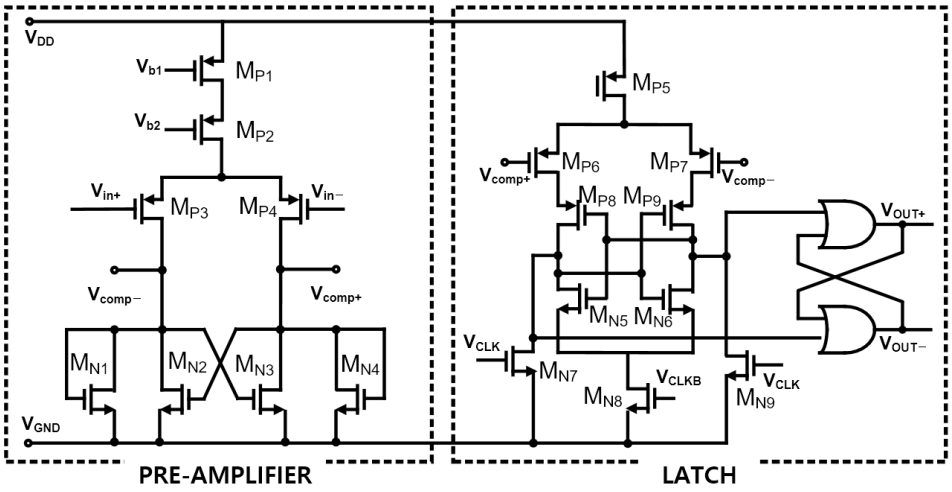


Figure 12. Schematic of the two-stage comparator.

3. Results and Discussion

A chip die photograph of the circuit is shown in Figure 13. The circuit was fabricated using the TSMC 180 nm process. The supply voltage operates at 1.8 V, and the supply current is 1.4 mA. The active area of the circuit is 1.06 mm^2.

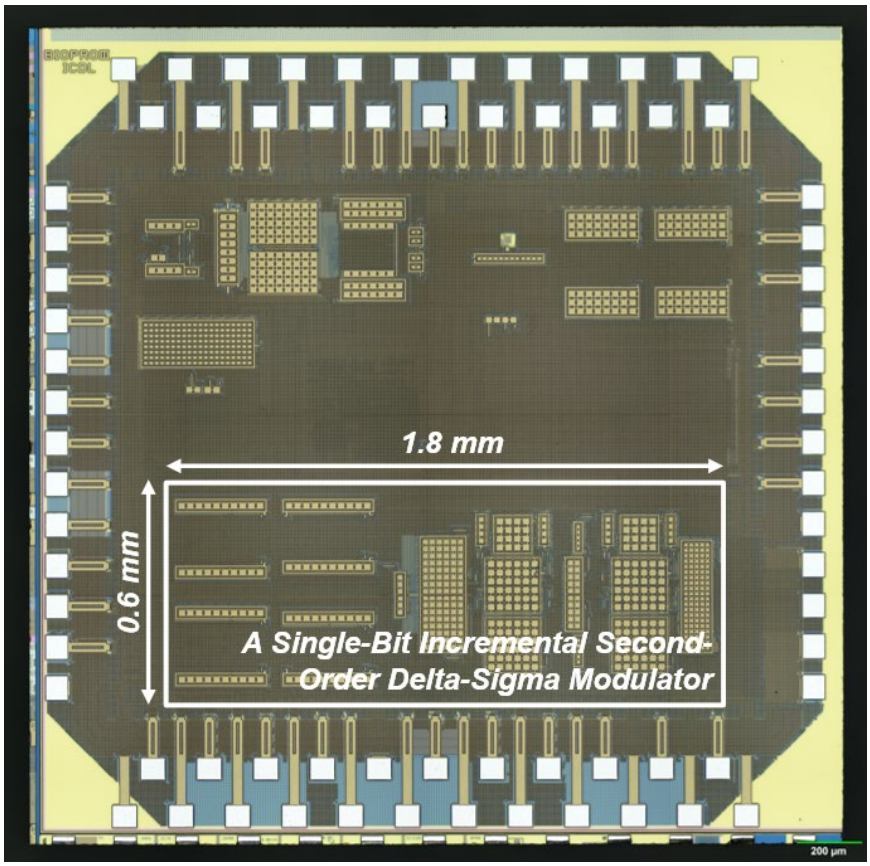


Figure 13. Die photograph of the proposed circuit.

Figure 14 shows the output transient measurement results for the buffer according to the sinusoidal input. The activation timings of the coarse buffer and fine buffer are shown in Figure 15. The coarse-fine buffer can drive the input switching load of the DSM.

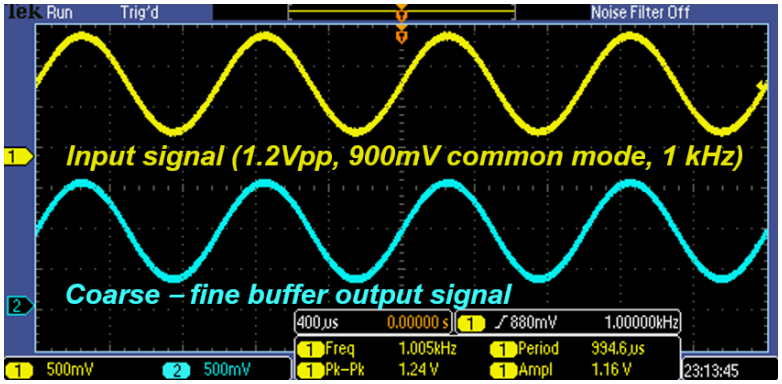


Figure 14. Transient measurement result of coarse-fine input buffer.

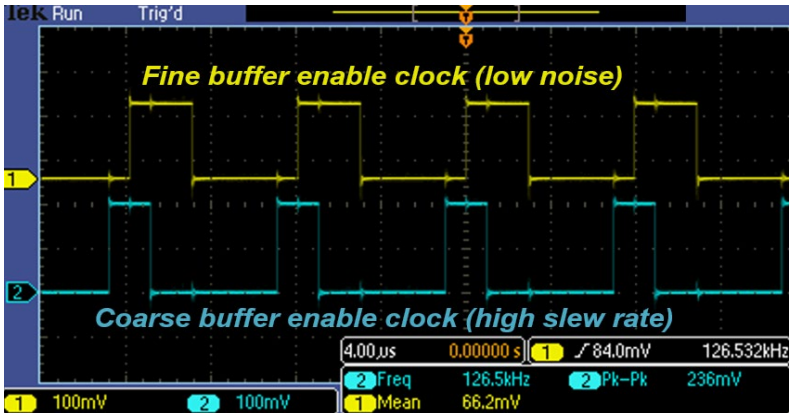


Figure 15. Enable timing signal measurement of coarse and fine buffers.

To measure the slew rate of the input buffer, the step input with the magnitude of 200 mV, from 800 mV to 1 V, is applied. The slew rate was 2.13 V/µs for the voltage arrival times from 10% to 90% of signal amplitude.

Figure 16 shows the input-referred noise measurement results for the coarse and fine buffers. To measure the buffer noise, the output of the buffer was amplified using the low-noise voltage amplifier SR560 (Stanford Research Systems, Sunnyvale, CA, USA). The input-referred noise floor of the coarse buffer was measured to be 36 nV/rtHz 100 Hz, and that of the fine buffer was measured to be 17 nV/rtHz. The coarse and fine buffers used currents of approximately 225 and 270 µA, respectively. As shown in Figures 16 and 17, it is possible to achieve a fast settling time and low noise characteristics simultaneously through coarse and fine buffers.

Figure 18 shows the sampling clock and bitstream output results as functions of the sinusoidal input. The frequency of the input sine wave was applied at 100 Hz, 1.2 V_{pp}, and 900 mV common mode voltage. The sampling clock was set to 125 kHz, and the OSR was set to 512 during the design process. It was observed that the bitstream output changed according to high and low sine waves. The result of the pulse density modulation (PDM) FFT analysis based on the bitstream output result is shown in Figure 19. Analysis of the PDM signal was performed using an APX500 (Audio Precision, 5750 SW Arctic Dr, Beaverton, OR 97005, NA). The passband frequency was determined from the Nyquist frequency of the sampling frequency and oversampling rate, which was 122.07 Hz. Performance indicators such as ENOB, SINAD, and the spurious free dynamic range of the modulator were calculated based on the above, with the average noise floor at −113 dB.

Based on this, we calculated the RMS value of the noise up to the passband, wherein the signal's amplitude was −10 dB. The calculated SINAD and ENOB were 80.87 dB and 13.14 bits, respectively.

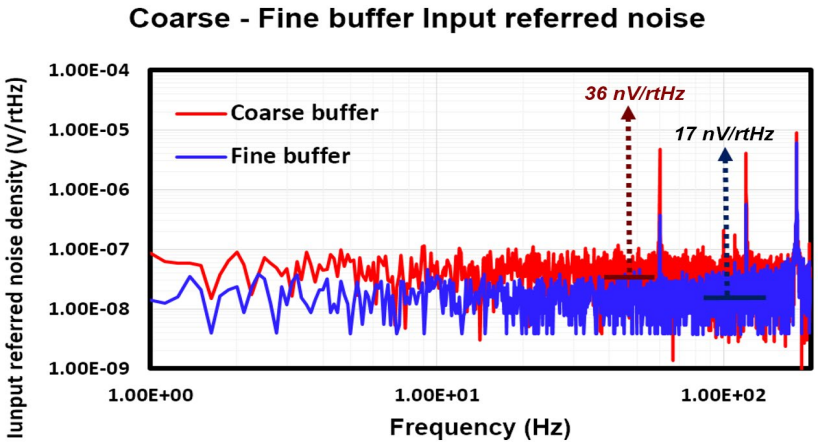


Figure 16. Noise measurement result of coarse and fine buffers.

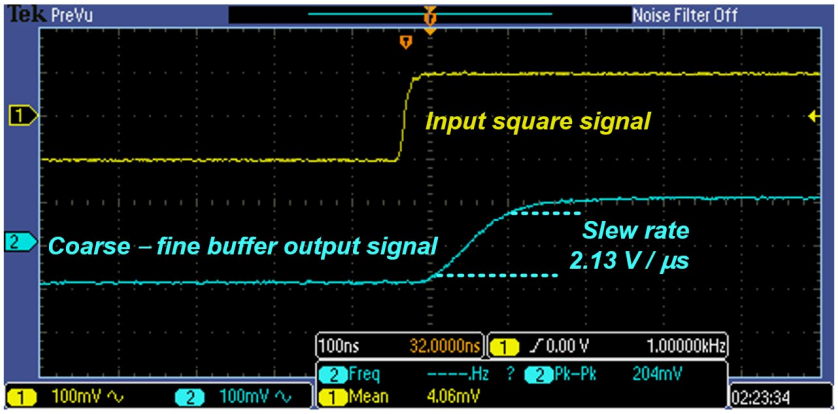


Figure 17. Transient measurement results of square input signal and output signal of buffer.

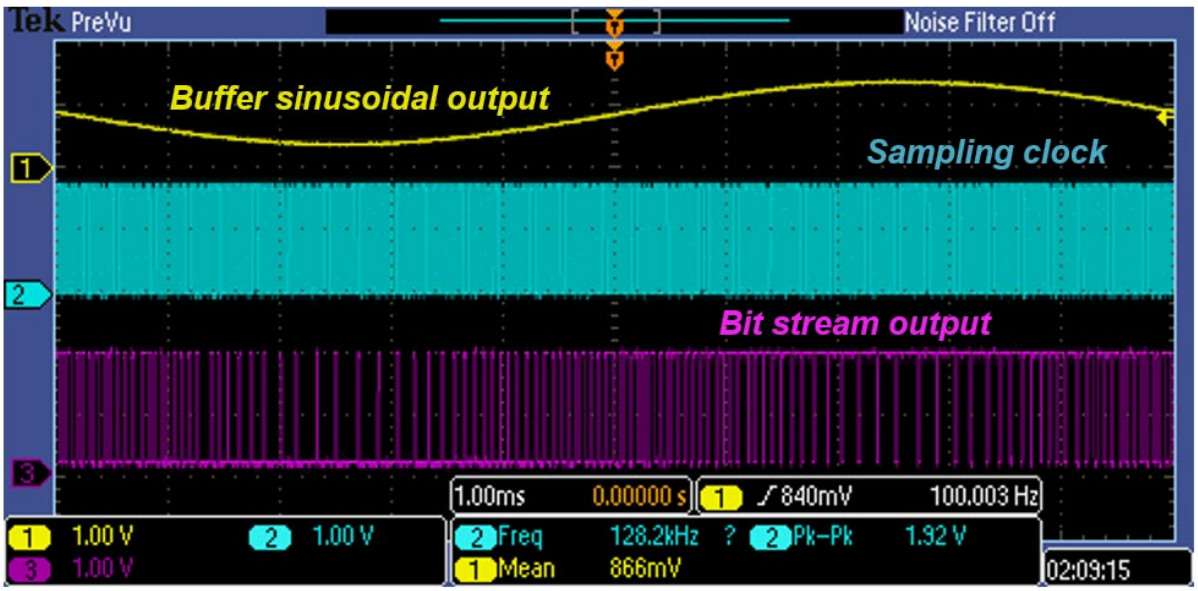


Figure 18. Sinusoidal signal of buffer output and bitstream output.

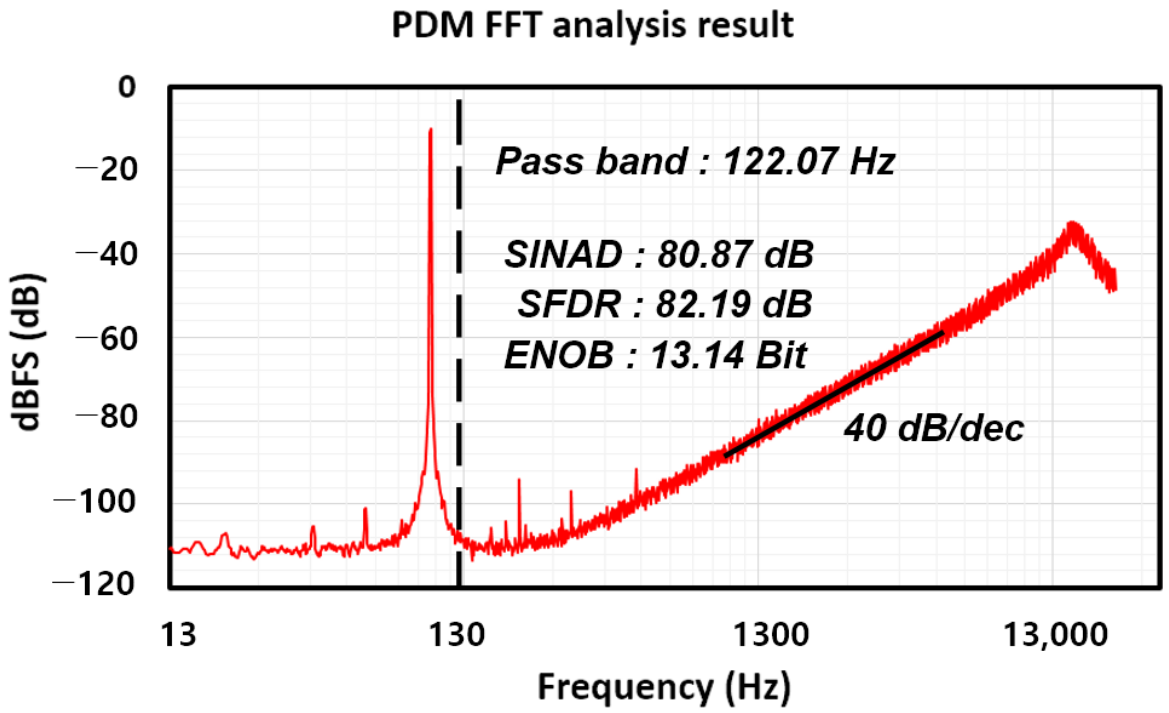


Figure 19. Sinusoidal input signal and bitstream output.

4. Conclusions

A summary of the performance achievements of this research is shown in Table 2. In the DSM operated with high OSRs, high-speed input buffers are required to drive the input stage of the DSM. The overall performances of the DSMs are highly dependent on the characteristics of the input buffers. The pre-charge scheme can relax the requirement of the input buffers. However, still low noise input buffers are required. Moreover, it is hard to optimize the power consumption and performance of the system using the commercial-off-the-shelf (COTS) components. In this paper, a single-bit incremental second-order DSM with a fully integrated coarse-fine input buffer without an external buffer was presented. In the coarse-fine input buffer, two parallel buffers, the pre-charge buffer and fine-settling buffer, are included. Using the coarse-fine input buffer, both the fast settling and low noise characteristics can be achieved. The proposed input buffer achieved an ENOB and SINAD of 13.14 and 80.87 dB, respectively. The modulator operates a single bit and sampling clock at 125 kHz. The proposed DSM was operated at 1.8 V. The proposed circuit was designed using a standard 0.18-µm CMOS process with an active area of 1.06 mm^2. The total current consumption with the coarse-fine buffer was 1.374 mA.

Table 2. Performance summary comparison between the proposed delta-sigma modulator with previous studies.

	This Work	ISCAS 2021 [25]	ISSCC 2022 [26]	IEICE 2018 [27]	BIOCAS 2018 [28]
Process(µm)	0.18	0.18	0.065	0.18	0.18
Supply voltage (V)	1.8	1.8	1.2	1.8	1.8
Current consumption (A)	1.374 m	480 µ	61.9 µ	81.5 µ	14 µ
Oversampling rate	512	128	5	-	256
Order of modulator	2nd	4th	4th	-	-
DT/CT	DT	DT	CT	DT	CT
SINAD (dB)	80.87	97.7	84.1	64.6	80
ENOB (bits)	13.14	15.97	13.67	10.34	13
Sampling frequency (Hz)	125 k	6.144 M	5 M	10 k	1 M
Pass band frequency (Hz)	122.07	24 k	500 k	-	4 k
Buffer usage (Y/N)	Y	Y	Y	Y	N
Settling time (s)	130 n	-	-	134 n	-

Author Contributions: Conceptualization and supervision, H.K.; circuit design, measurement, and draft preparation, M.Y.; investigation, K.N.; visualization, G.C.; methodology, S.K.; writing—review and editing, B.J.; format analysis, H.S.; conceptualization, K.K.; project administration, H.K.; funding acquisition, H.K. All authors have read and agreed to the published version of the manuscript.

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Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

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Conflicts of Interest: The authors declare no conflict of interest.

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