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Performance Analysis of Modular Multilevel Converter with NPC Sub-Modules in Photovoltaic Grid-Integration

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Abstract: In this article, a three-phase modular multilevel converter (MMC) with three-level neutral point clamped converter (NPC) sub-modules (SMs) along with the placement of transformers in place of arm inductors is proposed for PV grid integration. Compared to the traditional MMCs, the proposed configuration reduces the voltage and power rating for the switches and the requirement of a high capacitor bank. In order to analyze the performance of the proposed converter arrangement, we have implemented four pulse width modulation schemes, such as Sine PWM with phase-level shifted carrier (SPWMLSC), Sine PWM with a phase-shifted carrier (SPWMPSC), Sine with the third harmonic injected level-shifted carrier (STHILSC), and Sine with the third harmonic injected phase-shifted carrier (STHIPSC). The proposed converter was simulated in the MATLAB/Simulink platform. Under normal and faulty operation, the results were presented with their performance indices of voltage and current harmonic distortion and sub-module capacitor voltage ripples at various modulation indices.

Keywords: modular multilevel converter (MMC); fault-tolerant; voltage source modular multilevel converter (VSMMC); SPWMLSC; SPWMPSC; STHILSC; STHIPSC

Citation: Mikkili, S.; Krishna, R.V.; Bonthagorla, P.K.; Senjyu, T. Performance Analysis of Modular Multilevel Converter with NPC Sub-Modules in Photovoltaic Grid-Integration. *Appl. Sci.* **2022**, *12*, 1219. https://doi.org/10.3390/app12031219

Academic Editor: Giovanni Petrone

Received: 6 December 2021
Accepted: 21 January 2022
Published: 24 January 2022

1. Introduction

In order to achieve lower harmonic content in the output waveforms and lower filtering requirements at the grid side, multi-level inverters would have been the future trend in grid integration applications. To boost the efficiency and performance of grid-connected systems, multi-level inverters would have been integrated into renewable energy applications. Recently, a topology, that is, the modular multilevel converter (MMC) evolved from the multi-level family that has a profound application in photovoltaics, offshore, onshore wind energy, and medium voltage motor drives STATCOM, and UPQC, etc. The advantages of MMC are handled for high voltage applications, compact construction, stability, and reliability, whereas the PV is integrated into the grid. We could see some special characteristics like peak power capacity, fault ride-through, power quality, and higher redundancy capabilities popularly in MMC PV-based inverters [1]. One of the key topics that has been in current research is how to improve the efficiency and performance of photo-voltaic systems in the field of advanced power electronics for the energy conversion stages. There are various publications directed toward improvements and future implementation areas of before and after MMC studies. Many of those studies mostly focused on the various sub-module arrangements. The idea of a unidirectional sub-module has been explored in [2]. The efficiency of the MMC has been tested and compared to traditional two-level cells using various cell configurations, such as neutral point clamped and flying capacitor topologies. DC-MMC-based systems have been used as PV conversion systems with two stages with MMC-based HVDC [3,4], where high irradiance is available at longer distances from the consumption centers. Generally, in some MMC-based PV systems, it is

required to provide each dc-dc converter without independent MPPT to supply for the SM capacitor balance, which in turn helps in constant production of output required voltage levels without any power fluctuations [5]. Having said that, by maintaining lossless energy conversion, we have had MV grid integration of PV using MMC [6], because the individual MPPT arrangement in MMC and multi-string central inverter have lower MPPT losses when compared to a central inverter. In addition, a high-power hybrid-MMC was used for PV grid integration to provide reliable performance, even though under partial shading condition, because of the presence of individual MPPTs in each SM [7]. Thus, some of the MMC-based PV-BESs (photovoltaic-battery energy storage systems) [8] and energy distribution areas [9] had also been potential options for handling power mismatches and smoothening the output power. In addition, for applications where high power and medium voltage requirements, we can have some topologies of inverters without any need for the line-frequency transformer are given in [10]. The organization of the paper is as follows: Section 1 deals with the introduction. Section 2 explains the MMC and its sub-module variants. Section 3 details the control of MMC. Section 4 illustrates the modulation strategies for MMC. Section 5 discusses the results. Finally, the paper is concluded in Section 6.

2. Modular Multilevel Converter and Sub Module Variants

Figure 1a is a three-phase MMC, and it consists of the top arm (Tarm) and the bottom arm (Barm). This arrangement generally could have an N-number of SM in each arm [11]. Each phase consists of arm inductors (Larm) and the submodules to provide better arm-currents without circulating harmonics and fault currents. Submodule (SM) or power cell represents a topological connection of IGBTs and could be of any voltage level. Generally, this SM is half-bridge (HBSM) or full-bridge (FBSM), but some researchers [12] started using SM with high levels. The SMs in the arms must be identical to get a symmetrical output wave. In the basic operation of the MMC, there is a chance of two events—sub-module insertion or by-passing state—whenever all the sub-modules are inserted in series and would result in arm voltages, respectively, and in turn produces a multilevel output. During the insertion processes, the SM capacitors were charged to their rated voltage magnitudes in the blocking mode based on the SM variants. The DC-link energy was equally divided among the SM capacitors; otherwise, there would be an unbalance of voltages and circulating currents within the phases. Figure 1b is a single-phase equivalent representation of a conventional MMC. The top and bottom arms' SM's total voltage magnitudes constitute V au and Val, respectively. For many applications, like motor drive, the number of SMs drastically increased day by day. The ongoing developer has structurally connected multi-level SM topologies to have dc fault handling capability, dimension reduction, and a higher number of voltage levels. Table 1 here provides us with the topological variants of SMs. Two-level SMs: Figure 2a shows the half-bridge submodule (HBSM) to produce the unipolar voltage by chopping the dc-link voltage. It consists of two IGBTs and a capacitor [13]. It can produce two levels of voltages 0, +VC1 when bypassed and inserted. In the HBSM, the dc voltage component will be present in the MMC arms [14]. Figure 2b is unipolar voltage FBSM [12], and this is similar to FBSM but with a slight replacement of a S3 switch with D3 of the FBSM (Figure 3a); it would be suitable for dc-fault handling capability. Another two-level variant is the unidirectional SM [15], and it has fewer semiconducting switches, as shown in Figure 2c. The clamp single submodule (CSSM) configuration is another configuration [16], which is shown in Figure 2d. The CSSM is derived from the three-level flying capacitor submodules (TLFCSM) for providing dc-fault handling capability during unidirectional operation.

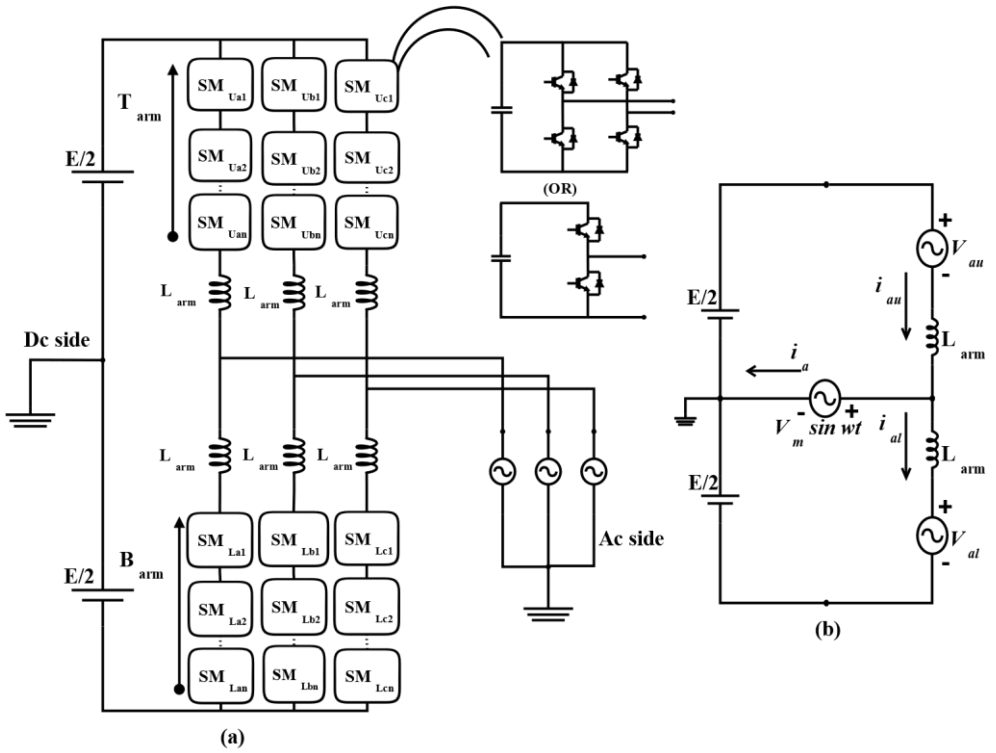

Figure 1. (**a**) Configuration of three-phase MMC, (**b**) single-phase equivalent circuit of conventional MMC.

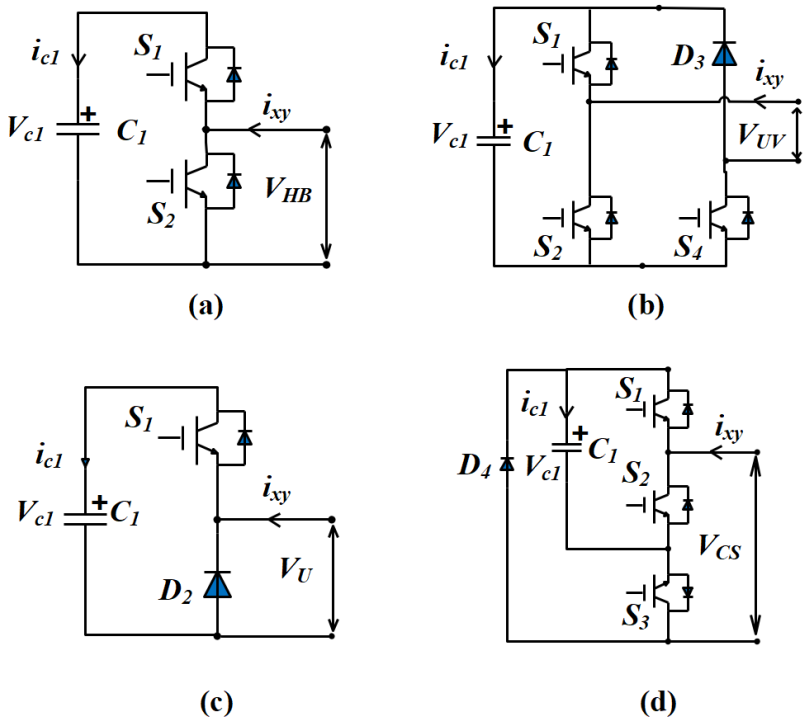

Figure 2. Two-level submodule variants (**a**) Half-bridge (**b**) Unipolar voltage full-bridge (**c**) Unidirectional SM (**d**) Clamp single SM.

Table 1. Comparison of different submodules [13–20].

Sub-Module (SM)	NVL	Voltage Level	NS	MNSC	MBV	Bipolar	DC-Fault Handling
Two-Level SMs							
HBSM	2	$0, +V_{C1}$	2	1	V_{C1}	No	No
Unipolar SM	2	$0, +V_{C1}$	3	1	V_{C1}	No	Yes
Unidirectional	2	$0, +V_{C1}$	1	1	V_{C1}	No	No
CSSM	2	$0, +V_{C1}$	3	2	V_{C1}	No	Yes
Three-Level SMs							
FBSM	3	$0, +V_{C1}, -V_{C1}$	4	2	V_{C1}	Yes	Yes
TLFCSM	3	$0, +V_{C2}, +(V_{C1} + V_{C2})$	4	2	$V_{C1} + V_{C2}$	No	No
TLNPC-1	3	$0, +V_{C2}, +(V_{C1} + V_{C2})$	4	2	$V_{C1} + V_{C2}$	No	No
TLNPC-2	3	$0, +V_{C2}, +(V_{C1} + V_{C2})$	6	2	$V_{C1} + V_{C2}$	No	No
TLNPC-3	3	$0, +V_{C2}, +(V_{C1} + V_{C2})$	4	2	$V_{C1} + V_{C2}$	No	No
DSM	3	$0, +V_{C2}, +(V_{C1} + V_{C2})$	8	4	$V_{C1} + V_{C2}$	No	Yes
TLCCSM	3	$0, +V_{C2}, +(V_{C1} + V_{C2})$	5	3	$V_{C1} + V_{C2}$	No	Yes
DBSM	3	$0, +V_{C1}, -V_{C2}$	2	1	V_{C1}	Yes	Yes
IHSM	3	$0, +V_{C1}, +(V_{C1} + V_{C2})$	5	3	$V_{C1} + V_{C2}$	No	Yes
Four-Level SMs							
CDSM-1	4	$0, +V_{C1}, +(V_{C1} + V_{C2})$	5	3	$V_{C1} + V_{C2}$	Yes	Yes
CDSM-2	4	$0, +V_{C2}, +(V_{C1} + V_{C2})$	7	3	$V_{C1} + V_{C2}$	Yes	Yes
Asymmetrical	4	$0, +V_{C2}, +(V_{C1} + V_{C2})$	4	2	$V_{C1} + V_{C2}$	Yes	Yes
Mixed SM	4	$0, +V_{C2}, +(V_{C1} + V_{C2})$	6	3	$V_{C1} + V_{C2}$	Yes	Yes
SDSM	4	$0, +V_{C2}, +(V_{C1} + V_{C2})$	5	3	$V_{C1} + V_{C2}$	Yes	Yes
Five-Level SMs							
FLCCSM	5	$0, +V_{C1}, +V_{C2}, \pm(VC_1 + V_{C2})$	6	3	$V_{C1} + V_{C2}$	Yes	Yes
CCSM	5	$0, +V_{C1}, +V_{C2}, \pm(VC_1 + V_{C2})$	8	4	$V_{C1} + V_{C2}$	Yes	Yes
PCSM	5	$0, +V_{C1}, +V_{C2}, \pm(VC_1 + V_{C2})$	8	4	$V_{C1} + V_{C2}$	Yes	Yes

Note: SM—Submodule, NVLs—Number of Voltage Levels, NSs—Number of Switches, MNSC—Maximum Number of Switches in the Conduction Path.

Three-level SMs: The well-known FBSM [16] is depicted in Figure 3a, and it generates bipolar output voltage levels, and we can use this for bipolar operation systems [17]. Moreover, if we connect two FBSMs in parallel, we could have a four-quadrant operation [18]. From Figure 3e, we can see that the three-level flying capacitor sub-module (TLFCSM) [14,15,18] has two capacitors—C1 which is twice in voltage rating with C2. This configuration does not have dc-fault handling and computationally complex control [19,20]. We see a three-level neutral point clamped submodules (TLNPC) in Figure 3b,d,g [14,18,21]. SMs in Figure 3d and TLFCSM are structurally close and produce 0, +VC2, and +(VC1 + VC2) magnitudes; SM in Figure 3b contains four switches, two capacitors, and two diodes, whereas SM in Figure 3g has six switches and two capacitors. Figure 3d, SM will be formed by the two-series combination of commutation circuits, while Figure 3b can be possible with the T-connection of switches; the midpoint switch here can block the voltages in both directions [22].

Even though it has more components, it lacks the dc-link short circuit handling capability, which results in severe control losses [17]. Two FBSMs are connected, as shown in Figure 3c, for improving the capacitor voltage performance, while keeping their SM's power level the same. This configuration [23] double-submodule (DSM) can improve the

functionality of the SM without an increment in the semiconducting device's cost. With this capacitor, voltage ripples at low frequencies could also be reduced. However, it lacks the presence of bipolar operation. In [12], another three-level cross-connected SM (TL-CCSM,) formed by connecting two HBSMs back-to-back with switch and diode, is shown in Figure 3f. Making the connection like this, we could produce voltage magnitudes 0, VC1, and (VC1 + VC2). The diagonal-bridge SM (DBSM), shown in Figure 3i, is another variant that is similar to FBSM but with two diagonal switches that are replaced by diodes [24].

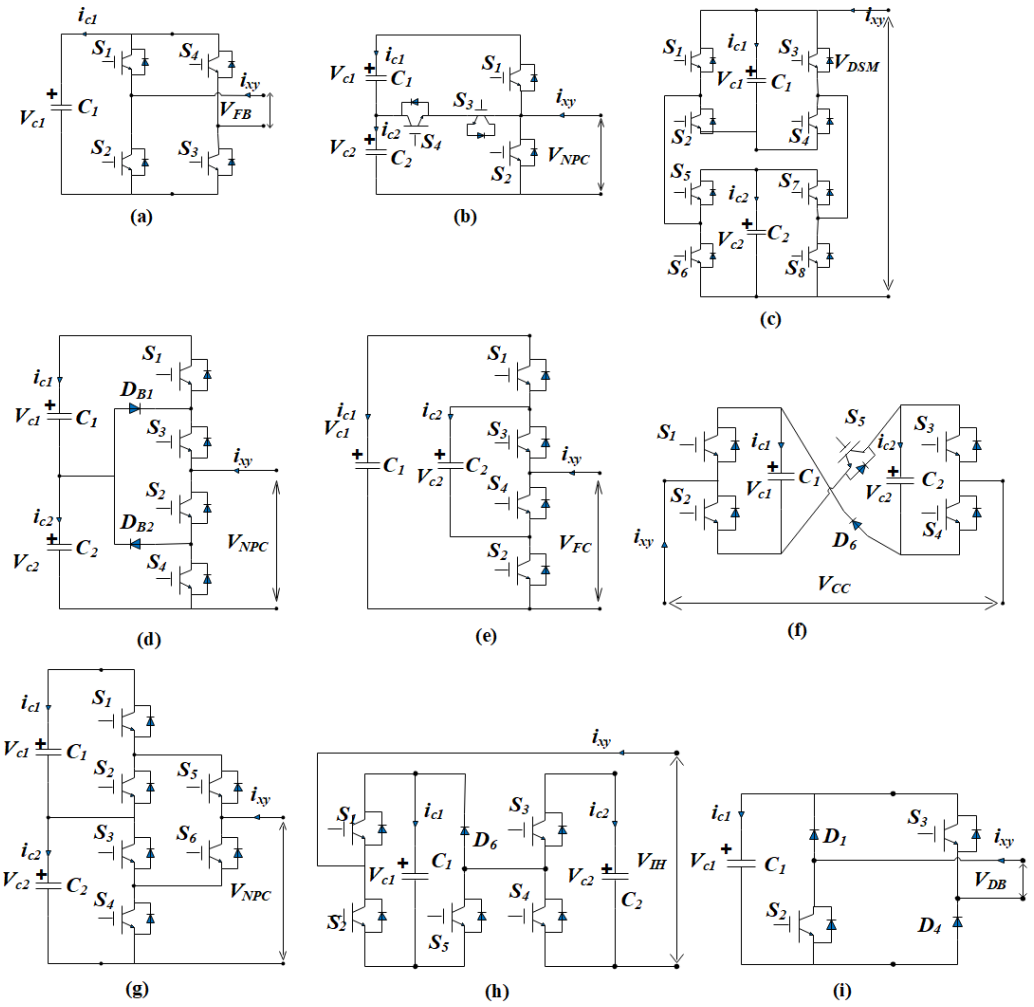

Figure 3. Three-level submodule variants (**a**) Full-bridge SM (**b**) Three-level flying capacitor submodule (TLFCSM) (**c**) TLNPC-1 (**d**) TLNPC-2 (**e**) TLNPC-3 (**f**) double-submodule (DSM) (**g**) three-level cross-connected (TLCCSM) (**h**) Improved hybrid SM(IHSM) (**i**) Diagonal-bridge SM (DBSM).

The last one is the three-level SM that is an improved hybrid SM (IHSM) [14], which has maximum voltage blocking of (VC1 + VC2), as depicted in Figure 3h. Four-level SMs: Figure 4a,b shows two kinds of double clamp submodules (CDSM) [12,14,21]. These configurations are the combination of two HBSMs connected in series. Here the switch S5 is on continuously, so it becomes two HBSMs connected in series under normal operating conditions. When the IGBTs are in blocking mode, both capacitors form either series or parallel connections in this CDSM. Further, this SM, operated as FBSM, has undergone different capacitor voltages as paralleled. To prevent this paralleling issue, diodes presented in that path could be replaced with IGBT switches. They would make another configuration, as shown in Figure 4b (CDSM); so far as losses are considered, CDSM is the combination of HBSM and FBSM. The alternate way of arranging commutation cells is shown in Figure 4c. This arrangement could be able to provide a dc-fault handling capability and can generate

four voltage magnitudes. A combination of FBSM and HBSM would result in forming a hybrid submodule termed an asymmetrical SM [25], and it can perform both unipolar and bipolar operations, as shown in Figure 4d. The series connected double SM(SDSM) in shown in Figure 4e, which is obtained by connecting two HBSMs with S5 and D6 [26]. It has the capability of arc extension whenever a short circuit has taken place, and it could protect MMCs even when zero impedance current would have been taken place. Five-level SMs: As shown in Figure 5a, five-level cross-connected SM (FLCCSM) is the same as CDSM. Structurally FLCCSM is designed with two HBSMs in back-to-back cross-connection with the help of S5 and S6 [21,27]. Due to the two capacitors of the SM being connected in series, a blocking effect on the dc-fault current can be created. A different cross-connected SM (CCSM) [27] is shown in Figure 5b. It has a balanced bipolar voltage output, which could achieve greater voltage [28]. Similarly, if FBSMs are connected as parallel-connected SMs [29], which is shown in Figure 5c, they would give a reduced capacitor ripple.

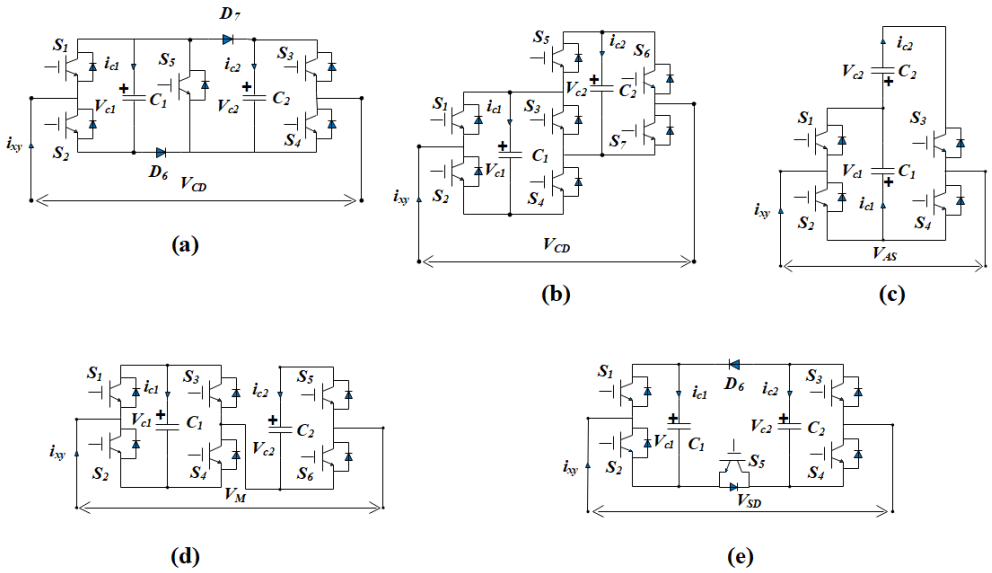

Figure 4. Four-level submodule variants (**a**) Clamp Double Submodules (CDSM), (**b**) Clamp Double Submodules (CDSM), (**c**) Mixed SM, (**d**) Asymmetrical SM, (**e**) Series Connected Double SM (SDSM).

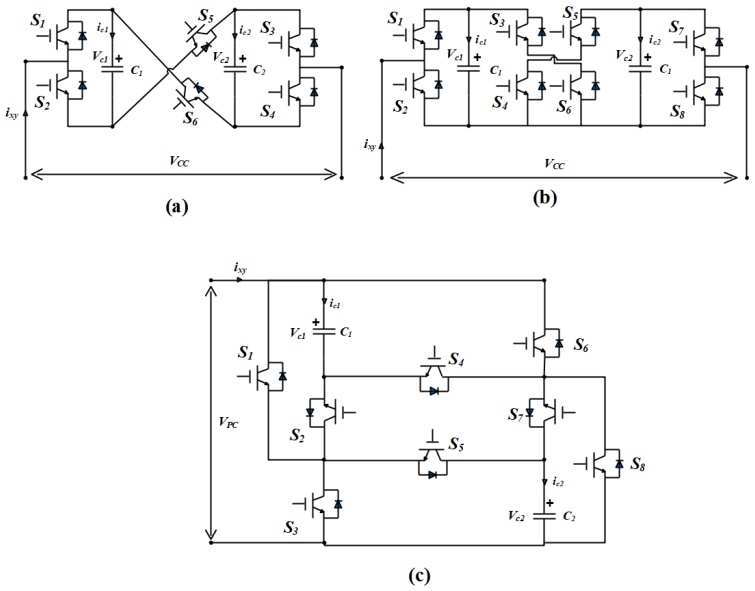

Figure 5. Five-level submodule variants (**a**) Five-Level Cross-Connected SM(FLCCSM), (**b**) Cross-Connected SM(CCSM), (**c**) Parallel-Connected SM.

3. Control Strategy of the Proposed MMC

The main part is the SM, which is may be a DC-DC or DC-AC power converter. Selection of better SM can provide fair control complexity, voltage blocking capability, and bipolar operation at a minimal cost. A new circuit performance of MMC with HB-SM is discussed in [2] by interchanging inductors with a transformer and also it offers twice the DC-AC voltage gain. The conventional MMC is having the advantage of power devices voltage ratings are halved, and the capacitor size of the SM is also lessened.

This paper uses neutral point clamped (NPC) SMs for the converter arrangement. The schematic (Figure 6) of the proposed MMC has slightly changed the SM with NPC SM with every single PV-panel, and the DC-DC converter and the DC-link to the MMC has been maintained by the PV array followed with the DC-DC converter. Figure 7 shows the controlling structure. For this controller implementation, initially, we are sensing the line-to-line three-phase voltages, and then these are transformed to two-phase voltage quantities by *alpha-beta* park's transformation. Using these *alpha-beta* voltages, PLL is implemented, *alpha-beta* voltages are then converted into *dq* voltages using Clark's transformation. Now from here, we are sensing the inverter side currents for the controller implementation. These currents are then transformed to the *alpha-beta* domain using park's transformation and then transformed to the *dq* domain using Clark's transformation. Here, *Id* corresponds to active current, and *Iq* corresponds to reactive current. Later *Id*&*Iq* are then subtracted from reference currents to find the error, and the error is fed to the *PI* controller to produce *Eq and Ed*. It is then transformed to *abc* voltages to get the references for PWM generation and, finally, we get the PWM generation block.

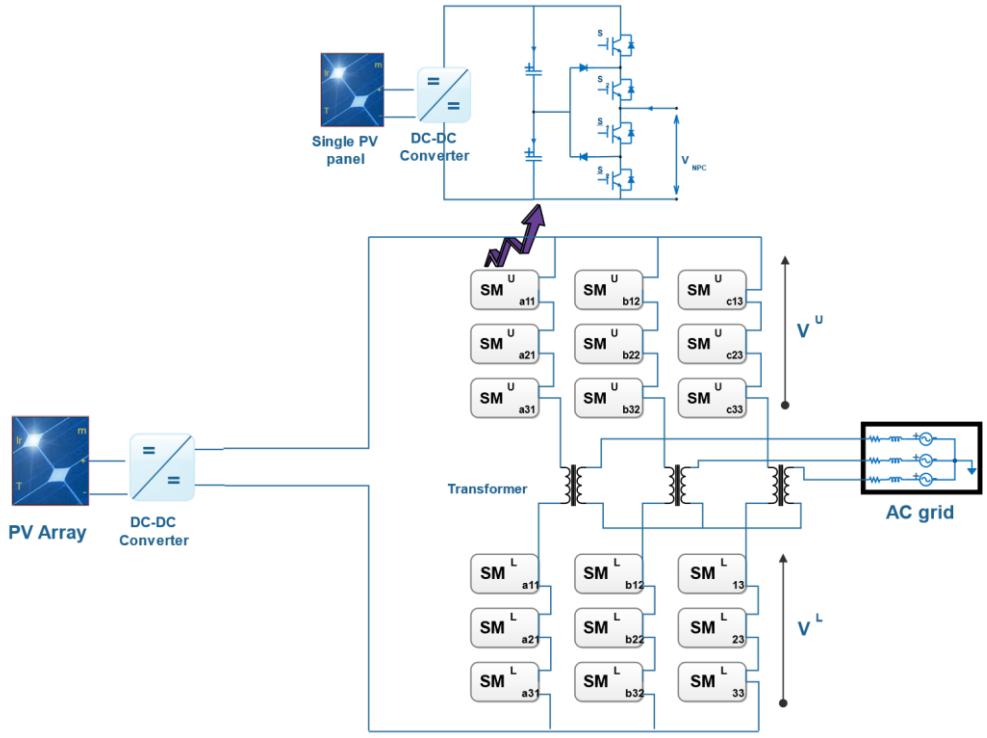

Figure 6. Schematic of the proposed modular multilevel converter.

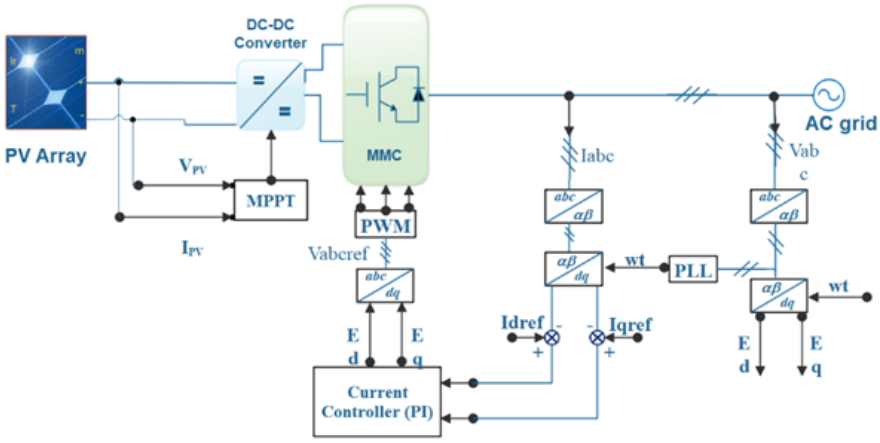

Figure 7. Control block diagram.

Generally, arm components in the traditional MMC are designed using the following equations.

$$L_{arm} \cdot C_{arm} = \frac{1}{\omega^2} \left\{ \frac{2(h^2-1) + m^2h^2}{8h^2(h^2-1)} \right\} \quad (1)$$

$$C_{arm} = \frac{1}{L_{arm} \cdot \omega^2} \left\{ \frac{2(h^2-1) + m^2h^2}{8h^2(h^2-1)} \right\} \quad (2)$$

where ω is the operating frequency, h is the harmonic order, and m is the modulation index.

However, in the proposed strategy, we use the transformers instead of arm inductors in the traditional MMC.

$$(L_{arm} + mutual\ inducance) \cdot C_{arm} = \frac{1}{\omega^2} \left\{ \frac{2(h^2-1) + m^2h^2}{8h^2(h^2-1)} \right\} \quad (3)$$

From Equations (1) and (3), the inductance component is more in the proposed strategy, because of the mutual inductance of the transformer when compared to the traditional MMC for the same harmonic order and modulation index. Hence, from Equations (2) and (4), the proposed system requires a lesser value of capacitance when compared to the traditional MMC.

4. Modulation Strategies

Pulse width modulation (PWM) is generally used for regulating the power converter AC output voltage. The desired (reference) AC output voltage is achieved by regulating the duty cycle of the switching equipment. PWM methods were intended to eliminate harmonic components in the output voltage and increase the magnitude of the output voltage at any switching frequency. Figure 8 demonstrates the classification of various pulse width modulation techniques commonly used in multilevel converters. These are the PWM techniques adopted in VSC applications based on the switching frequency requirements. Figure 9 shows the simulation results with the (a) Sine PWM with the level-shifted carrier (SPWMLSC), (b) Sine PWM with the phase-shifted carrier (SPWMPSC), (c) Sine with the third harmonic injected level-shifted carrier (STHILSC), and (d) Sine with the third harmonic injected phase-shifted carrier (STHIPSC).

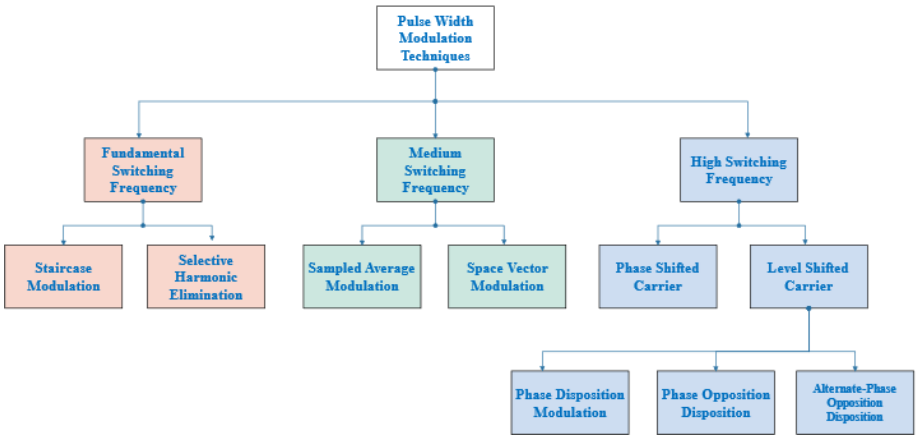

Figure 8. General pulse width modulation classification based on switching frequency.

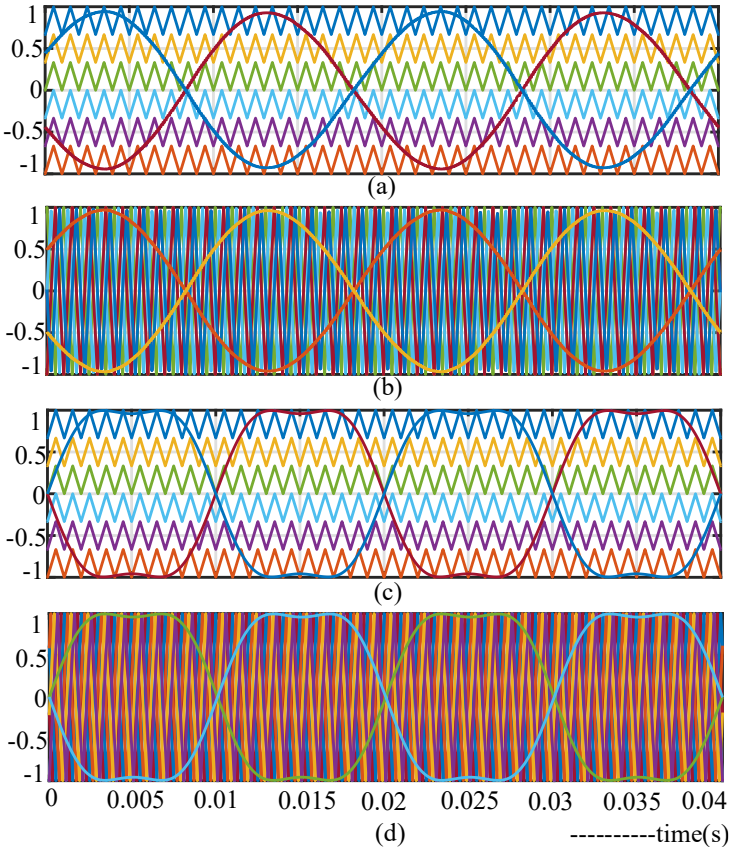

Figure 9. Modulation schemes conducted on this converter. (**a**) Sine PWM with level-shifted carrier (SPWMLSC); (**b**) Sine PWM with phase-shifted carrier (SPWMPSC); (**c**) Sine with third harmonic injected level-shifted carrier (STHILSC); and (**d**) Sine with third harmonic injected phase-shifted carrier (STHIPSC).

5. Results and Discussion

The simulation results of the proposed converter with various PWM schemes are clearly explained in this section. The parameters chosen for the simulation are given in Table 2. From Figure 10, we can see that the converter is operated with a modulation index (MI) of 0.5 from t = 0.8 s to t = 1.2 s, and it is operated with M = 0.95 from t = 0.8 s to t = 1.2 s. It is observed from Figure 10a,k that the THD in line voltage of the converter with d-q control and SPWMLSC is 2.58% at 50 Hz. respectively. In addition, from Figure 10b,m, the THD in line voltage of the converter with d-q control and SPWMPSC is 1.63%. Similarly, the

THD in line current with d-q control and SPWMLSC is 12.20% and with SPWMPSC is 6.64% at 50 Hz, as shown in Figure 10c,l, respectively. Figure 10e,g shows the capacitor voltages of upper arm phase-a SM-1 and lower arm phase-a SM-1 with SPWMLSC modulation scheme. Figure 10f,h shows the capacitor voltages of the upper arm phase-a SM-1 and lower arm phase-a SM-1 with SPWMPSC modulation scheme. Figure 10i,j shows the transformer primary and secondary phase-a currents for both PWM techniques, respectively.

Table 2. Simulated converter parameters.

Number of Cells in Each Arm	**3**
Ac line inductor	3 μH
Carrier frequency	1 KHz
Transformer resistance	74 m-ohm
Transformer inductor	3.48 mH
Cell capacitance	1000 μF

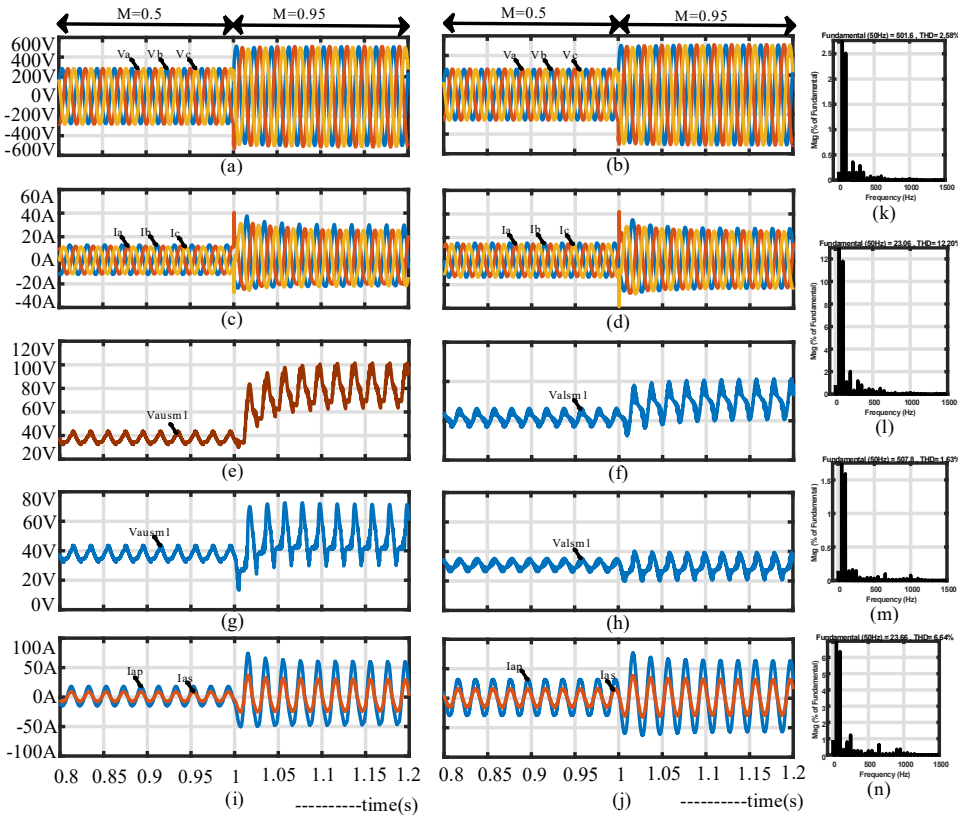

Figure 10. Change in modulation index. (**a**) Line voltages of converter with d-q control and SPWMLSC, (**b**) line voltages of converter with d-q control and SPWMPSC, (**c**) Line currents of converter with d-q control and SPWMLSC, (**d**) line currents of converter with d-q control and SPWMPSC, (**e**) SPWMLSC implemented upper arm phase-a SM-1 capacitor voltage, (**f**) SPWMPSC implemented upper arm phase-a SM-1 capacitor voltage, (**g**) SPWMLSC implemented lower arm phase-a SM-1 capacitor voltage, (**h**) SPWMPSC implemented lower arm phase-a SM-1 capacitor voltage, (**i**) primary and secondary phase-a transformer currents when SPWMLSC is implemented, (**j**) primary and secondary phase-a transformer currents when SPWMPSC is implemented, (**k**) SPWMLSC implemented line voltage THD, (**l**) SPWMLSC implemented line current THD, (**m**) SPWMPSC implemented line voltage THD, and (**n**) SPWMPSC implemented line current THD.

Further, the converter's dynamic performance is analyzed when there is a step-change from time t = 1 s to t = 1.2 s in the current magnitude of I = 7.25 A to I = 17.5 A at 50 Hz

frequency. It is observed from Figure 11a,k that the THD in line voltage of the converter with d-q control and STHILSC is 1.26% at 50 Hz, respectively, and from Figure 11b,m the THD in line voltage of the converter with d-q control and STHIPSC is 1.18%. Similarly, the THD in line current with d-q control and STHILSC is 10.26% and with STHIPSC is 8.84% at 50 Hz, as is shown in Figure 11c,l and Figure 11d,n respectively. Figure 11e,g shows the capacitor voltages of upper arm phase-a SM-1 and lower arm phase-a SM-1 with STHILSC modulation scheme. Figure 11f,h shows the capacitor voltages of upper arm phase-a SM-1 and lower arm phase-a SM-1 with STHIPSC modulation scheme. Figure 11i,j shows the transformer primary and secondary phase-a currents for both STHILSC and STHIPSC PWM techniques, respectively.

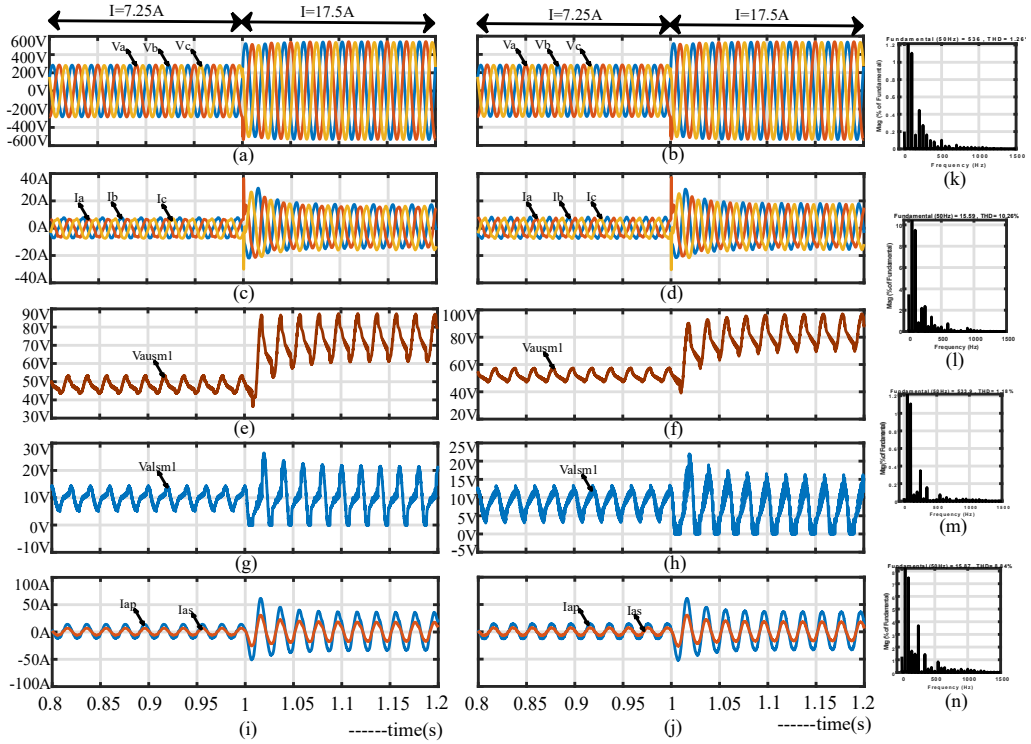

Figure 11. Change in current. (**a**) Line voltages of converter with d-q control and STHILSC, (**b**) line voltages of converter with d-q control and STHIPSC, (**c**) line currents of converter with d-q control and STHILSC, (**d**) line currents of converter with d-q control and STHIPSC, (**e**) STHILSC implemented upper arm phase-a SM-1 capacitor voltage, (**f**) STHIPSC implemented upper arm phase-a SM-1 capacitor voltage, (**g**) STHILSC implemented lower arm phase-a SM-1 capacitor voltage, (**h**) STHIPSC implemented lower arm phase-a SM-1 capacitor voltage, (**i**) primary and secondary phase-a transformer currents when STHILSC is implemented, (**j**) primary and secondary phase-a transformer currents when STHIPSC is implemented, (**k**) STHILSC implemented line voltage THD, (**l**) STHILSC implemented line current THD, (**m**) STHIPSC implemented line voltage THD, and (**n**) STHIPSC implemented line current THD.

Now, the performance of the MMC is analyzed when it is operating in open and short circuit conditions. The Figure 12a,b shows the line voltages with d-q control and SPWMLSC and SPWMPSC respectively, when one of the phases is open-circuited from time t = 1 s to t = 1.2 s at 50 Hz frequency. Figure 12c,d is the line currents with d-q control and SPWMLSC and SPWMPSC. During the faulty open-circuited operation, Figure 12e–h shows the capacitor voltages of the upper arm and lower arm of phase-a SM-1 with SPWMLSC and SPWMPSC modulation schemes, respectively. Further, the primary and secondary phase-a transformer currents, when SPWMLSC and SPWMPSC schemes are implemented, are shown, respectively, in Figure 12i,j. Similarly, Figure 13a,b shows the line voltages with d-q control and STHILSC and STHIPSC respectively, when one of the

phases is open-circuited from time t = 1 s to t = 1.2 s at 50 Hz. Figure 13c,d shows the line currents with d-q control and STHILSC and STHIPSC respectively. During the faulty open circuit condition, Figure 13e–h shows the STHILSC implemented upper arm and lower arm phase-a SM-1 capacitor voltages, respectively, and STHIPSC implemented upper arm and lower arm phase-a SM-1 capacitor voltages, respectively. The primary and secondary phase-a transformer currents when implementing STHILSC STHIPSC are shown in Figure 13i,j. Further, the short circuit condition is created from time t = 1 s to t = 1.2 s. At this time interval, the converter performance is visualized, with simulation results shown in Figure 14. Figure 14a,b shows the line voltages with d-q control and SPWMLSC and SPWMPSC respectively. Furthermore, Figure 14c,d shows the line currents with d-q control and SPWMLSC and SPWMPSC respectively. During the faulty short circuit condition, Figure 14e–h shows the upper arm mad lower arm phase-a SM-1 capacitor voltages with SPWMPSC and SPWMLSC schemes, respectively. Furthermore, the primary and secondary phase-a transformer currents SPWMLSC and SPWMPSC modulation schemes are shown in Figure 14i,j, respectively.

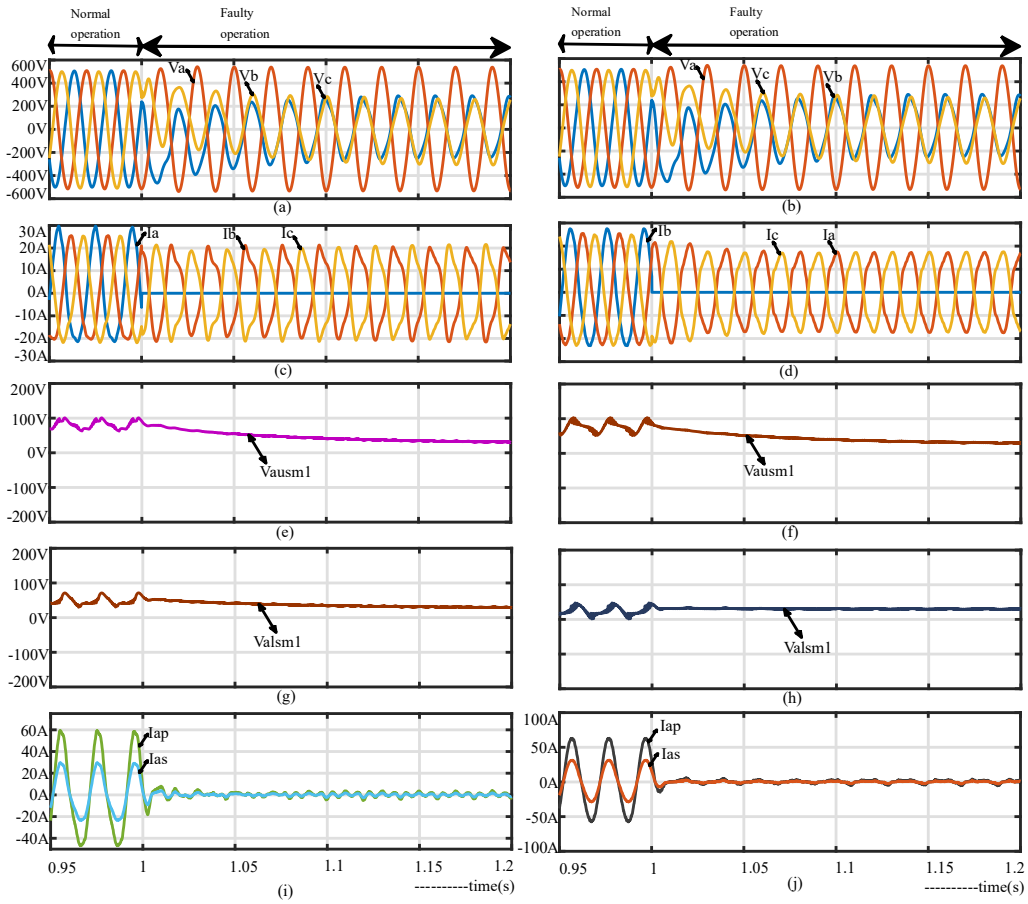

Figure 12. Converter when one phase is open circuited. (**a**) Line voltages of converter with d-q control and SPWMLSC, (**b**) line voltages of converter with d-q control and SPWMPSC, (**c**) line currents of converter with d-q control and SPWMLSC, (**d**) line currents of converter with d-q control and SPWMPSC, (**e**) SPWMLSC implemented upper arm phase-a SM-1 capacitor voltage, (**f**) SPWMPSC implemented upper arm phase-a SM-1 capacitor voltage, (**g**) SPWMLSC implemented lower arm phase-a SM-1 capacitor voltage, (**h**) SPWMPSC implemented lower arm phase-a SM-1 capacitor voltage, (**i**) primary and secondary phase-a transformer currents when SPWMLSC is implemented, (**j**) primary and secondary phase-a transformer currents when SPWMPSC is implemented.

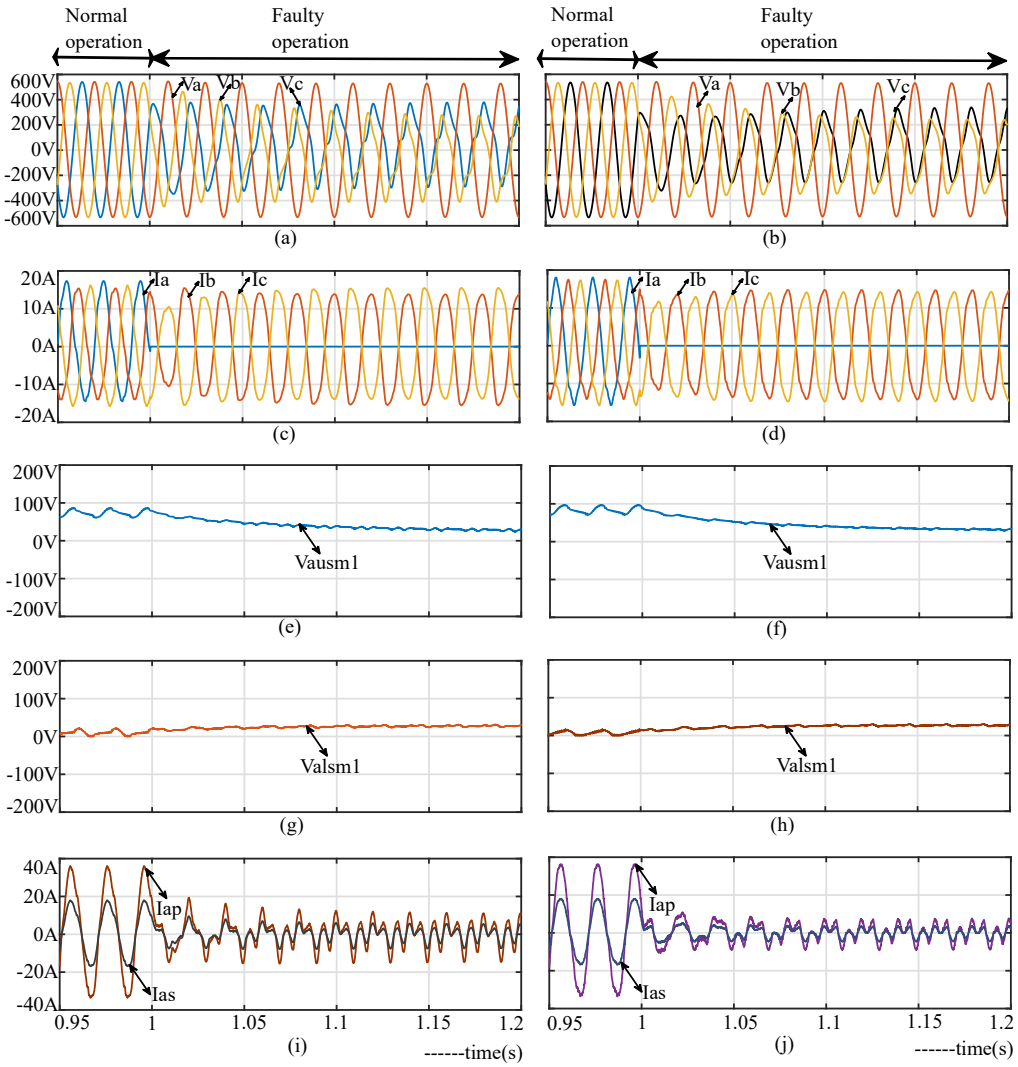

Figure 13. Converter when one phase is open circuited. (**a**) Line voltages of converter with d-q control and STHILSC, (**b**) line voltages of converter with d-q control and STHIPSC, (**c**) line currents of converter with d-q control and STHILSC, (**d**) line currents of converter with d-q control and STHIPSC, (**e**) STHILSC implemented upper arm phase-a SM-1 capacitor voltage, (**f**) STHIPSC implemented upper arm phase-a SM-1 capacitor voltage, (**g**) STHILSC implemented lower arm phase-a SM-1 capacitor voltage, (**h**) STHIPSC implemented lower arm phase-a SM-1 capacitor voltage, (**i**) primary and secondary phase-a transformer currents when STHILSC is implemented, (**j**) primary and secondary phase-a transformer currents when STHIPSC is implemented.

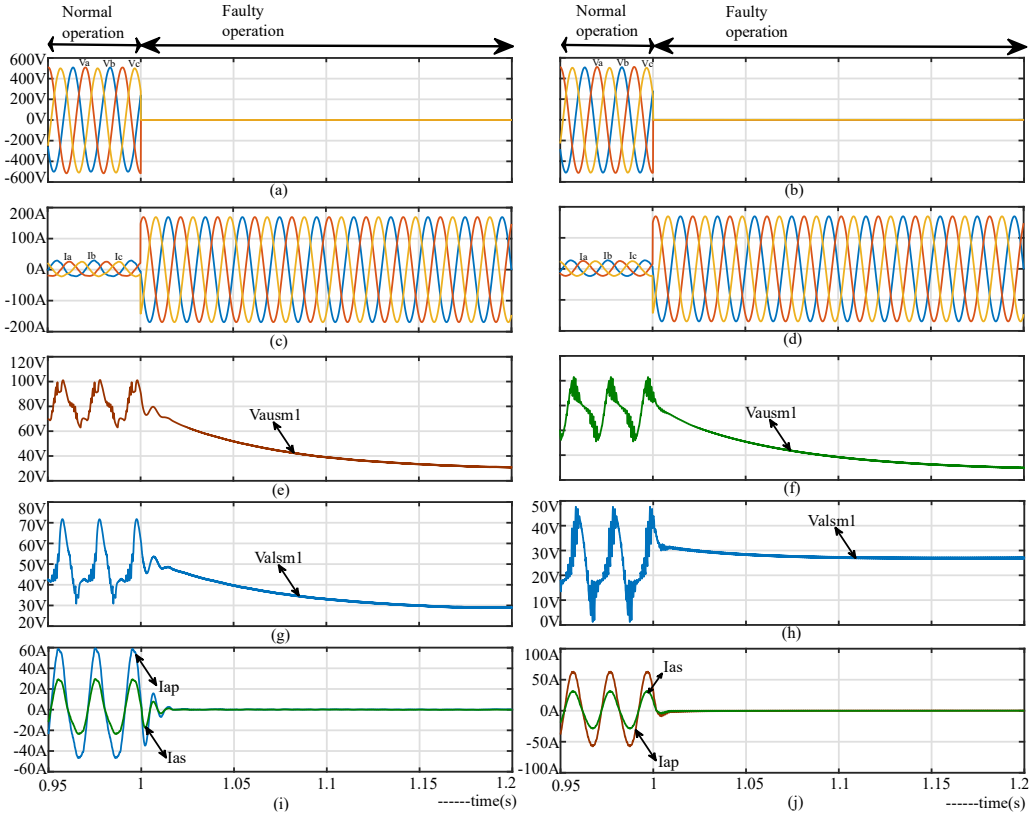

Figure 14. Converter during short circuited condition. (**a**) Line voltages of converter with d-q control and SPWMLSC, (**b**) line voltages of converter with d-q control and SPWMPSC, (**c**) line currents of converter with d-q control and SPWMLSC, (**d**) line currents of converter with d-q control and SPWMPSC, (**e**) SPWMLSC implemented upper arm phase-a SM-1 capacitor voltage, (**f**) SPWMPSC implemented upper arm phase-a SM-1 capacitor voltage, (**g**) SPWMLSC implemented lower arm phase-a SM-1 capacitor voltage, (**h**) SPWMPSC implemented lower arm phase-a SM-1 capacitor voltage, (**i**) primary and secondary phase-a transformer currents when SPWMLSC is implemented, (**j**) primary and secondary phase-a transformer currents when SPWMPSC is implemented.

Here, the proposed converter's performance is analyzed with sin third harmonic injection for both levels—shifted and phase-shifted PWM schemes—when the converter has been short-circuited from t = 1 s to t = 1.2 s at 50 Hz. Figure 15a,b shows the line voltages with d-q control and STHILSC and STHIPSC respectively. Figure 15c,d shows the line currents with d-q control and STHILSC and STHIPSC respectively. During short-circuited operation, Figure 15e–h shows the capacitor voltages of the upper arm and lower arm phase-a SM-1 with STHILSC modulation scheme. The primary and secondary phase-a transformer currents with STHILSC and STHIPSC schemes are shown in Figure 15i,j respectively.

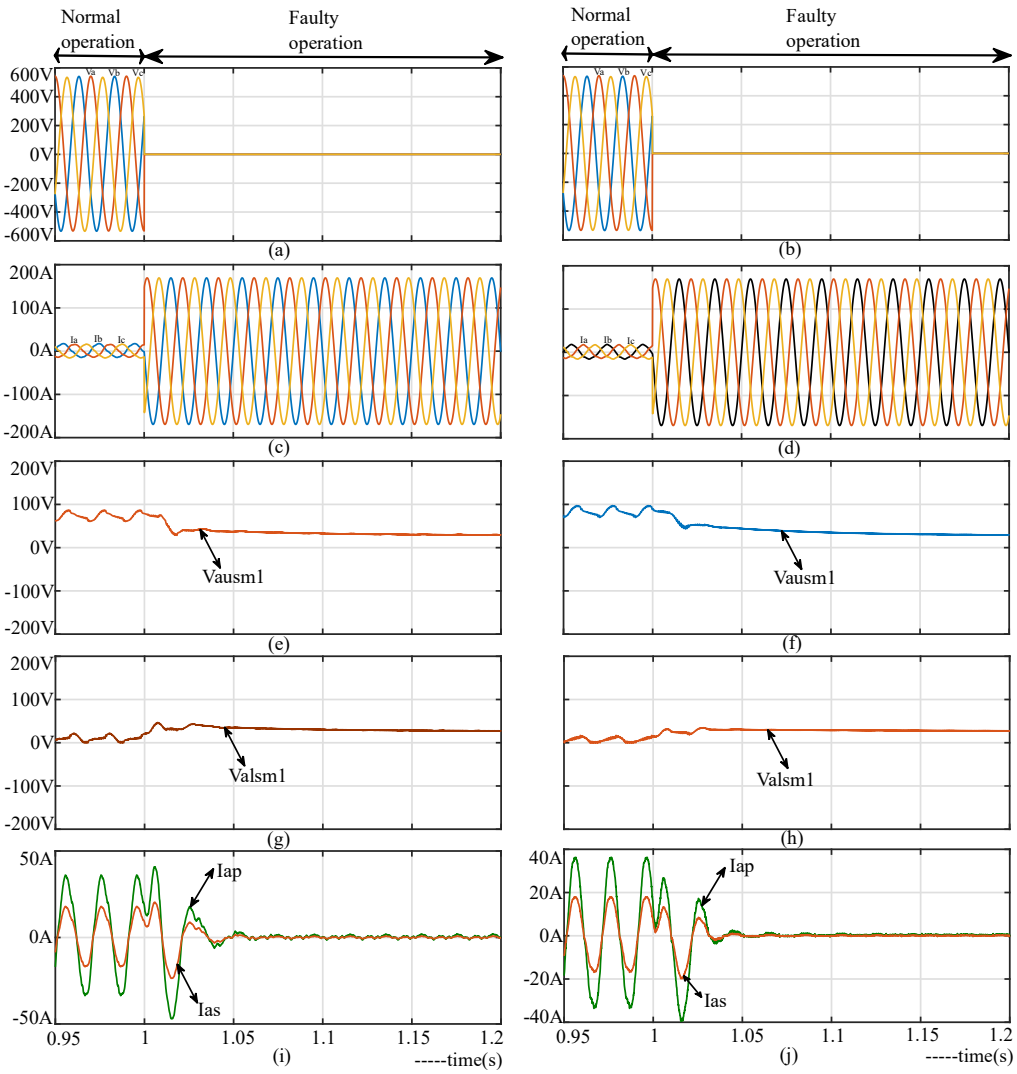

Figure 15. Converter during short circuited condition. (**a**) Line voltages of converter with d-q control and STHILSC, (**b**) line voltages of converter with d-q control and STHIPSC, (**c**) line currents of converter with d-q control and STHILSC, (**d**) line currents of converter with d-q control and STHIPSC, (**e**) STHILSC implemented upper arm phase-a SM-1 capacitor voltage, (**f**) STHIPSC implemented upper arm phase-a SM-1 capacitor voltage, (**g**) STHILSC implemented lower arm phase-a SM-1 capacitor voltage, (**h**) STHIPSC implemented lower arm phase-a SM-1 capacitor voltage, (**i**) primary and secondary phase-a transformer currents when STHILSC is implemented, (**j**) primary and secondary phase-a transformer currents when STHIPSC is implemented.

6. Conclusions

In this paper the performance of the proposed MMC with NPC sub-modules in PV grid-connected applications was investigated under steady and transient conditions by employing various PWM techniques. The proposed MMC with NPC sub-modules with various SPWMLSC, SPWMPSC, STHILSC, and STHIPSC modulation techniques reports the voltage THDs were 2.58%, 1.63%, 1.26%, and 1.18%, and the current THDs were 12.20%, 6.64%, 10.26%, and 8.84%, respectively. The phase-shifted carrier modulation scheme has features like a low computational burden, can manage fault tolerance, and provides superior voltage balance under abnormal conditions when it comes to the digital controllers. From the results it is clearly revealed that the modulation schemes, such as STHILSC and STHIPSC, give superior performance in terms of lower output voltage and current harmonic distortions. The proposed arrangement achieves any volage level with lower rating of power switches when compared to the conventional neutral point clamped

converter. This strategy can also significantly reduce the requirement of the high rating capacitor bank due to the presence of the mutual inductance component in the transformers, which is not present in the traditional MMC. Hence it can used for many high-power and medium-voltage grid-connected applications.

Author Contributions: Conceptualization—S.M. and R.V.K; Methodology, Software, Validation—S.M., R.V.K., P.V.B., and T.S.; Investigation, Resources, Writing—Original Draft Preparation, Writing—Review and Editing, Visualization; Supervision; Project Administration, S.M., R.V.K., P.V.B., and T.S. All authors have read and agreed to the published version of the manuscript.

Funding: The authors gratefully acknowledge the support offered by the Science and Engineering Research Board (SERB), Department of Science and Technology, Government of India, under the Grant number: ECR/2017/000316 for this research work.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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