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Design Considerations of Multi-Phase Buck DC-DC Converter

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Abstract: The main objective of this article is to propose a rational methodology for designing multi-phase step-down DC-DC converters, which can find applications both in engineering practice and in power electronics education. This study discusses the main types of losses in the multi-phase synchronous buck converter circuit (transistors' conduction losses, high-side MOSFET's switching losses, reverse recovery losses in the body diode, dead time losses, output capacitance losses in the MOSFETs, gate charge losses in MOSFETs, conduction losses in the inductor, and losses in the input and output capacitors) and provides analytical dependencies for their calculation. Based on the control examples for applications characterized by low voltage and high output current, the multi-phase buck converter's output and input current ripples are analyzed and compared analytically and graphically (3D plots). Furthermore, graphical results of the converter efficiency at different numbers of phases (N = 2, 4, 6, 8, and 12) are presented. An analysis of the impact of various parameters on power losses is conducted. Thus, a discussion on assessing the factors influencing the selection of the number of phases in the multi-phase synchronous buck converter is presented. The proposed systematized approach, which offers a fast and accurate method for calculating power losses and overall converter efficiency, reduces the need for extensive preliminary computational procedures and achieves optimized solutions. Simulation results for investigating power losses in 8-phase multi-phase synchronous buck converters are also presented. The relative error between analytical and simulation results does not exceed 4%.

Keywords: DC-DC converter; design considerations; energy efficiency; multi-phase converter; power electronics

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1. Introduction

Power electronic converters and systems convert electrical energy with various parameters. They have a variety of applications, such as highly efficient intelligent drives; implementation of industrial processes; energy storage systems; decentralized production of electricity based on alternative energy sources; supply of sensitive consumers; and others. Their requirements may vary depending on the specific application and standards. However, in practice, there are some general requirements and aspects that must be taken into account in the development and use of power electronic converters and systems [1–5]:

1. Energy conversion efficiency: Power electronic converters are expected to exhibit high energy conversion efficiency, with minimal losses during the process. Enhanced energy efficiency not only reduces energy and cooling expenses but also alleviates the loading of cooling systems.
2. Stability and Adjustability: Converters are required to maintain a stable output voltage and/or current, typically in the presence of varying input conditions and loads. The capability for adjustment and precision in control is essential, especially in applications requiring precise control.

3. Protection and Safety: Equipping converters with robust protection mechanisms against overload, short circuits, disconnections, and other electrical faults is crucial. This is important to prevent damage to the converter and related components and devices that are powered.
4. Electromagnetic Compatibility (EMC): Compliance with electromagnetic compatibility standards is essential for converters. This ensures the prevention of electrical interference with other systems and devices while guaranteeing seamless operation in environments characterized by electromagnetic disturbances.
5. Heat Dissipation and Cooling: Converters generate heat during their operation. Applying adequate cooling and heat dissipation mechanisms is necessary to prevent overheating and component damage.
6. Reliability and Long Life: The converters must be designed and built with high reliability, guaranteeing a long product life and reducing the need for repairs and replacements. This approach facilitates sustained cost-effectiveness throughout the operational phase and the entire lifecycle of the devices.
7. Size and Weight: Depending on the application, the size and weight of converters can hold critical importance. For instance, achieving a compact and lightweight design is significant in the automotive sector, particularly for mobile or portable devices.
8. System Compatibility: Converters must exhibit compatibility with other system components with which they are integrated, including control systems, sensors, and various other peripherals.
9. Effective Control and Communication: Most applications require the ability to control, monitor and communicate with the converters, which may include analogue or digital interfaces. In this way, the devices and controllers' diagnostics, training, and self-learning processes are carried out.
10. Certifications and Standards: Depending on the industry and application, converters must meet specific standards and certifications for safety and compliance.

However, despite the many general properties that modern power electronic devices and systems need to possess, it is essential to note that there are always some specific requirements that are formed and individualized depending on the specific application and industry. In this context, the development of power electronic converters and systems requires, on the one hand, a careful analysis of the needs and conditions of the specific application, as well as compliance with the relevant specific standards and regulations, on the other.

Multi-phase converters represent one approach to enhancing energy density, elevating reliability, and attaining cost-effective power electronic device configurations. These multi-phase DC-DC converters utilize multiple switching phases to facilitate power conversion, offering distinct advantages and disadvantages compared to conventional single-phase DC-DC converters [6–8].

The main advantages of multi-phase converters are as follows:

- Reduced output current and voltage ripple: Multi-phase converters combine ripples from all phases, resulting in smoother output current and voltage than single-phase configuration.
- Improved thermal distribution: Effective power distribution across multiple phases ensures a more uniform heat distribution among components, enhancing overall thermal management.
- Ability to increase the total power: By adding additional phases, the total output power of the converter can be increased.
- Enhanced reliability: If one of the phases fails, the remaining phases can continue operation, although the device has a reduced efficiency compared to the mode when all phases work.
- Faster response to load changes: The presence of multiple phases enables the converter to exhibit fast dynamic responses to fluctuations in load conditions, ensuring stable performance.

- Ability to use modular and typical structures. Multi-phase converters offer the flexibility to utilize both modular and conventional configurations, thus optimizing the cost-effectiveness, reliability, and commercial viability of the device.

Naturally, multi-phase systems are also characterized by several disadvantages:

- Complexity: The design and control of multi-phase converters are more complex than single-phase ones.
- Increased number of components: more switching elements, drivers, and other components need to be used, which can increase the cost and size of the system.
- More complex control: Managing the phase difference and synchronization between different phases requires the use of a more complex controller.

Despite their shortcomings, multi-phase DC-DC converters have established themselves as irreplaceable in several fields and applications, such as:

- Microprocessor power supplies: Polyphase converters can provide high currents at low voltages, which is often required by modern microprocessors.
- In energy storage systems: Multi-phase converters naturally realize the management of energy flows between the elements making up the battery stack and support the realization of BMS.
- Electric and hybrid cars: These systems often require high power and flexible energy management.
- Photovoltaic systems: Multi-phase converters can optimize the energy conversion from solar panels.
- Server power supplies: High efficiency and the ability to handle high currents are critical for power supplies in data centers and server rooms.

In conclusion, multi-phase DC-DC converters offer a range of advantages, making them suitable for specific applications. However, they are also characterized by additional requirements regarding their design and control. The above-mentioned factors contribute to a significant interest in the research of multi-phase DC-DC converters. In [9], a method is proposed to improve the efficiency of a bi-directional, multi-phase (6-phase) Buck DC-DC converter with application in hybrid electric vehicles (HEV) or fuel cell electric vehicles (FCV). The control of the converter is synthesized by using modulation in constant switching frequency operation. The circuit is designed via optimization based on an objective function to achieve minimal losses in the power semiconductors and the inductor. The authors of [10] proposed a modified pulse-width modulation (PWM) method that achieves good harmonic composition and low noise. The Wrapped-Around Phase-Shift (WAPS) control is used for the RWAPPM-type multiphase converter, which achieves a significant reduction in the output ripple noise voltage compared to other control algorithms. This is proven on the basis of numerical experiments with a model of a three-phase converter. Their analysis shows that the multi-phase RWAPPM with the proposed WAPS control method (RWAPPM + WAPS) is characterized in addition to low output voltage ripple noise and very low peak spectral power of input current harmonics compared to using a standard PWM under the same conditions. In [11], a new multiphase PWM DC-DC converter is designed to meet the power requirements of a new generation microprocessor that requires 40–100 A currents, lower voltage, and better current dynamic transient response. In this regard, in the multiphase converter, it is very important to balance the currents in each phase, and current sharing in the master-slave control method is an effective way to do this. In [12], the interface between the energy storage system and the inverter is considered. The main objective of the manuscript is the analysis, design, and comparison of four interleaved boost DC-DC converter topologies. In this aspect, an evaluation of the effect of using a magnetic four-phase coupled inductor coupling in multiphase and modular circuits is made. As a development of the research, a new topology for a four-phase coupled inductor is presented. These DC-DC converters are designed to determine the proper placement of components to achieve the best performance. Synthesis control of multi-phase DC-DC converters has a number of features compared to that of classical schemes.

In [13], a method for synthesis control of multiphase DC-DC converters is presented by identifying an automated digital system. The results of the identification were used to tune the controller, which was achieved without previously known parameters of the power circuit. The authors of [14] presented a multiphase synchronous step-down converter (MSBC). Due to its higher efficiency, smaller passive component sizes, bi-directional power flow, and reduced output current ripple, this device finds wide application for electric vehicle charging. (EV). In order to achieve high reliability, the management of faults in the power circuit was performed by detecting a fault of a separate semiconductor switch, switching off the faulty phase, and corresponding reconfiguration of the PWM signals for the working phases. This prevents circulating current in the device and high output current ripple. The main contribution of the manuscript is the fault management method by detecting defective semiconductor switches and reconfiguring healthy phases using DSP. The method is validated via simulations and experiments. In [15,16], the design features of the magnetic components applied in multiphase DC-DC converters are considered. The authors of [15] proposed a procedure for the optimal design of a high-efficiency multiphase step-down converter implemented by a solenoid inductor, and [16] a method for designing a coupled inductor applied to a multiphase interleaved boost converter, which is a more efficient topology, compared to the classic multiphase boost converter. The authors of [17] present research on a series-arranged multiphase topology. It is well suited for high-voltage, high-power DC-DC conversion applications. The multi-phase structure used in the proposed converter helps to increase the power level and improve reliability by using a modular structure and minimizing the requirements on filter elements. The authors of [18] present the implementation and validation of a tool for analyzing multiphase-coupled inductor converters. In this type of converter, the equivalent inductance reduced to each phase changes significantly within one switching cycle and thus the number of equivalent inductances increases significantly as the number of phases increases. The proposed tool not only considers the design of the coupled inductor with symmetrical inductances and coupling coefficients but also the asymmetrical design parameters.

Ref. [19] proposed a new type of DC-DC converter with gallium nitride (GaN) transistors. By using additional soft switching circuits, the converter can operate with ZVS and ZCS. Thus, it allows operation at a very high frequency and has a higher efficiency compared to the classic buck–boost converter. To realize the modular design of the device, the technology of multiphase interlacing of magnetic integration is used. Ref. [20] addresses the concept of multiphase hybrid buck–boost converters, showing two types (MP-HBUC and MP-HBOC) for this purpose. Due to the use of single-phase hybrid buck–boost converters (HBUC and HBOC) in their structure, the MP-HBUC and MP-HBOC topologies are characterized based on significantly reduced conduction losses compared to conventional buck–boost converters (CBUC and CBOC). In this sense, even at high load levels, MP-HBUC and MP-HBOC type converters are highly efficient.

The authors of [21] present a new method for controlling multiphase step-down converters by operating with variable switching frequency. In operation, for each phase with the control frequency in the MHz range, the digital cycle-by-cycle converter control of both current and voltage results in fast transient dynamic response and correspondingly fast interference suppression. In this case, the main challenge in operating the device is adding phases or increasing the operating frequency. For this purpose, it is necessary to realize a feedback voltage measurement without the presence of disturbances from dynamic switching transients. Ref. [22] introduced a new design approach for multiphase non-isolated DC-DC topology. It is based on a new generic hybrid cell composed of a capacitor and an inductor. This approach contributed to a high degree of modularity of the obtained converters, and in this way, high conversion coefficients are achieved with higher efficiency compared to classical structures. The interaction between the capacitor and the inductor gives rise to resonant processes and leads to modes with soft commutations, which reduces losses and contributes to a higher efficiency of the converter. This method was used to construct a multiphase voltage regulator module VRM.

The steady in [23], a converter designed to deliver 1 kW of power at a 42 V output voltage, is proposed to fulfill the demands of the 14/42 power system widely employed in automotive applications. The paper covers designing, analyzing, and simulating a multi-phase interleaved DC-DC boost converter tailored for 42 V power systems. This converter comprises six-phase boost converters designed to operate in the discontinuous conduction mode (DCM), effectively providing 1 kW of output power. The influence of changing the parameters on the converter's performance is also described. In [24], an enhanced fixed-frequency current-following-based digital control strategy is introduced for low-voltage, high-current multi-phase DC-DC converters that necessitate rapid transient response. The paper presents dynamic ramp compensation methods to enhance stability while maintaining high-performance levels. It has been observed recently that data center energy consumption is on the rise, primarily due to the increasing number of Internet users, the proliferation of cloud computing, and the widespread use of multi-core processors. In order to reduce the losses in the DC bus and the power distribution network, data centers follow a trend of increasing the bus voltage from 12 V to 48 V.

In [25], a DC-DC converter is introduced to provide the interface between the 48 V bus and the existing 12 V server modules. This paper primarily focuses on the design of a 1.5 kW two-stage polyphase switched capacitor converter characterized based on high efficiency (above 98%) and high power density. The authors of [26] propose a methodology for sizing magnetic components and devising a novel multi-phase split-duty-cycle variant integrated with a cascaded converter. This configuration is well-suited for bidirectional operation, particularly when the low-voltage port requires a multi-phase step-down stage. The validity of the chosen magnetic components in the coupled inductor is confirmed through a combination of simulation and experimental results.

A four-phase interleaved buck–boost converter with changed load connection (CLC-FIBC) for fuel cell (FC) application is proposed, analyzed, and designed in [27]. A simple structure, a wide range of input current change, high input, and output current levels, and low ripple characterize the proposed structure. In [28], a novel multi-phase synchronous zero-voltage step-down converter (ZVT) with pulse-width modulation (PWM) is presented. With an auxiliary circuit, all buck converter switches can operate under soft-switching conditions. A 2 kW two-phase ZVT-PWM synchronous step-down converter is verified, and the experimental efficiency is given compared to a conventional two-phase step-down converter.

In [29], a detailed design and analysis of a multi-phase step-down converter based on a magnetic core solenoid inductor is observed. Additionally, it introduces an optimization framework for efficiently designing multi-phase step-down converters with magnetic core solenoid inductors tailored to specific specifications. Simulation results demonstrate that the multi-phase converter designed using the proposed methodology achieves 92.8% efficiency and 0.5 mV voltage ripple. In [30], a multi-phase interleaved bidirectional DC-DC converter structure is proposed. This structure brings about reductions in input current ripple, switch voltage, output voltage ripple, and passive component sizes. Improved transient dynamic response and enhanced reliability are notable advantages of using such a structure.

The steady in [31] presents a novel multi-phase DC-DC converter characterized by modularity, simple control and structure, additional gain, continuous input current, and low normalized switch/diode voltage. This configuration is particularly well-suited for tracking the maximum power point in photovoltaic (PV) power generation applications. The authors of [32] present a comparative study of single-phase and multi-phase DC-DC converters for controlling Li-Fi systems. The comparison includes the converter design, efficiency, and maximum achievable bitrates of each topology.

From the comprehensive analysis of the state of research in the field of multi-phase DC-DC converters, it is evident that this topic remains highly relevant, driven by a continually expanding array of applications. The enhancement of converter characteristics and the assurance of their performance metrics are primarily founded on several key methodologies:

optimal synthesis of control (most often digital); use of new topologies with better qualities compared to classical ones; optimal design of the magnetic components; and optimal design of the entire power circuit. However, it is worth noting that the published sources lack studies that determine the optimal number of phases for multi-phase buck converters and the associated relationships between converter efficiency, the number of phases, and the specific input–output parameters of the design task.

In this regard, the present work aims to present a rational methodology for determining the optimal number of phases of multi-phase step-down DC-DC converters depending on specific needs. The work is organized as follows: In Section 2, the main types of losses in the circuit of the studied converter are considered and analytical dependences for their calculation are presented. The output and input current ripples in the multi-phase converter are analyzed. In Section 3, design considerations of multi-phase buck DC-DC converters are presented. A discussion of the optimum phase numbers for some common input and output voltages is also presented. In Section 4, an analytical and simulation study of power losses in 8-phase synchronous buck converters is performed.

2. Power Losses in the Multi-Phase Synchronous Buck Converter

This article discusses the configuration based on the synchronous buck converter since this circuit is characterized by a higher converter efficiency compared to the conventional buck converter, especially in applications characterized by low voltage and high output current. Furthermore, a Schottky diode is typically placed in parallel to the low-side MOSFET, further reducing the reverse recovery losses during dead time, which is introduced to prevent shoot-through between transistors. Figure 1 presents the N-phase synchronous buck converter. For the purposes of the study the transistors $Q1 \div Q1N$ are denoted as high-side (HS) MOSFETs and transistors $Q2 \div Q2N$ are denoted as low-side (LS) MOSFETs. The following notations are used: Uin—input voltage; U_0—output voltage; N—number of phases; output capacitor $Cout$; input capacitor Cin; $ESRout$ equivalent series resistance of $Cout$; $ESRin$ equivalent series resistance of $Cout$; output inductances $L1 \div LN$; $DCR1 \div DCRN$ equivalent series resistances of the output inductances.

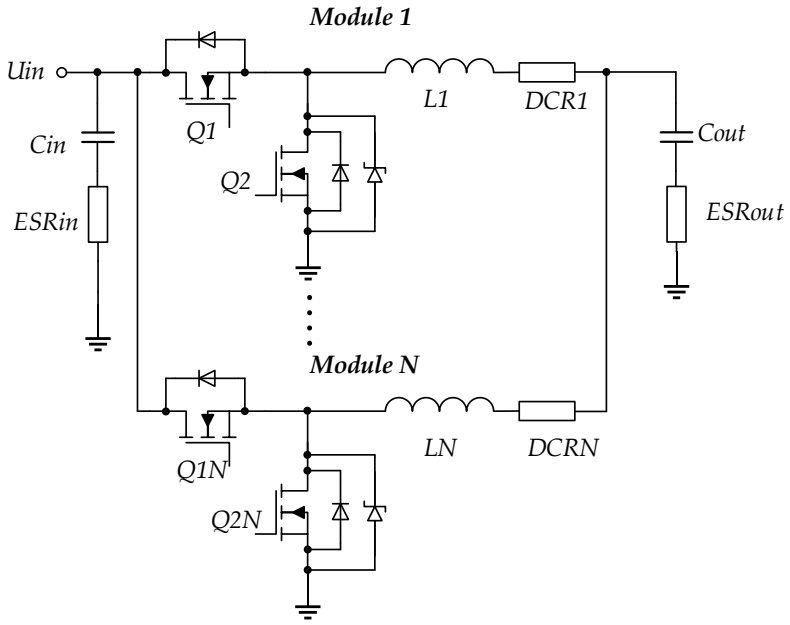

Figure 1. A multi-phase synchronous buck converter.

The power losses associated with MOSFETs in synchronous buck converters generally consist of conduction losses and switching losses. In the present study, the power losses in one stage of the multi-phase synchronous buck converter are divided into the following categories [33]:

1. Conduction losses P_{Qon_H} of the high-side MOSFET and conduction losses P_{Qon_L} of the low-side MOSFET;
2. Switching losses in the high-side MOSFET P_{QSW_H};
3. Reverse recovery losses in the body diode $P_{D(RR)}$;
4. Dead time losses P_{QL_td};
5. Output capacitance losses in the MOSFETs $P_{C_{OSS}}$;
6. Gate charge losses in MOSFETs P_G;
7. Conduction losses in the inductor P_L;
8. Losses in the input and output capacitors P_{Cin} and P_{Cout}.

The switching losses of the low-side MOSFET, in the considered applications, are small and are neglected since the transistor is turned on and off with a drain-source voltage equal to the forward voltage of the body diode [34]. In addition, there is no freewheeling current through *Q1*. Hence, there would not exist any body-diode losses. Also, the gate driver losses are not considered in this study due to the wide variety of control drivers.

There are two types of power losses in the inductor: conduction losses caused by the resistance and core losses determined by magnetic properties. Since calculating core losses requires manufacturer-provided data on the core material, which may only sometimes be available, this article does not describe it.

The considered methodology includes dependencies discussed in [33–38].

The ripple current through the inductance in the one buck stage is given by

$$\Delta I_L = \frac{U_0(1-D)}{Lf_{SW}}, \tag{1}$$

where $L1 = L2 = \ldots = LN = L$; duty cycle $D = U_0/U_{in}$ and f_{SW} is the switching frequency.

The RMS value of the input current I_{IN_rms} in the multiphase converter is expressed by

$$I_{IN\_rms} = \sqrt{\left(D - \frac{m}{N}\right)\left(\frac{1+m}{N} - D\right)I_0^2 + \frac{N\Delta I_L^2}{12D^2}\left[(m+1)^2\left(D - \frac{m}{N}\right)^3 + m^2\left(\frac{1+m}{N} - D\right)^3\right]} \tag{2}$$

where $m = floor(N \cdot D)$ provides the greatest integer that is smaller than or equal to $(N \cdot D)$ [34] and I_0 is the output current.

The optimum number of phases should be evaluated over the whole range of variations of the duty cycle. Figure 2a shows the dependence of the RMS input ripple current in normalized form versus the output current I_{IN_rms}/I_0 for different phase configurations and duty cycle range variation.

Output ripple current peak-to-peak amplitude ΔI_{Cout} in an N-phase converter is given by

$$\Delta I_{Cout} = \frac{U_0}{f_{SW}L}\frac{N}{D}\left(D - \frac{m}{N}\right)\left(\frac{1+m}{N} - D\right). \tag{3}$$

The graphical representation of (3) in normalized form $\Delta I_{Coutn} = \Delta I_{Cout}/\frac{U_0}{f_{SW}L}$ is plotted in Figure 2b.

For the RMS current I_{QH_rms} through an HS transistor, the following relation is valid:

$$I_{QH\_rms} = \sqrt{\left[\left(\frac{I_0}{N}\right)^2 + \left(\frac{\Delta I_L^2}{12}\right)\right]D}. \tag{4}$$

Hence, the conduction losses of P_{Qon_H} of the HS transistor can be written as follows:

$$P_{Qon\_H} = I^2_{QH\_rms}R_{DSon\_H} = \left[\left(\frac{I_0}{N}\right)^2 + \left(\frac{\Delta I_L^2}{12}\right)\right]DR_{DSon\_H}. \tag{5}$$

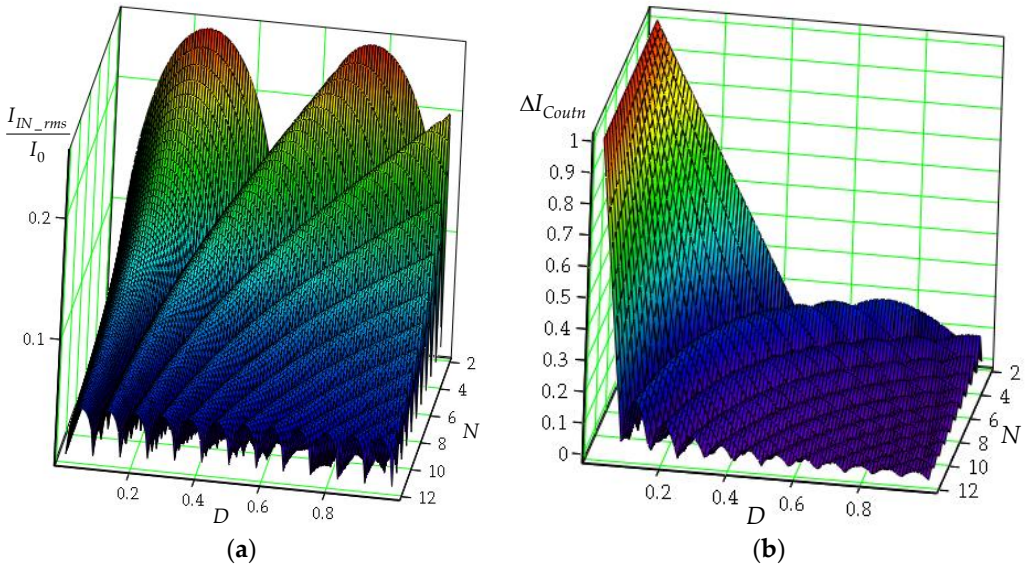

Figure 2. Normalized ripple currents in an N-phase converter: (**a**) Normalized input ripple current I_{IN_rms}/I_0; (**b**) normalized output ripple current peak-to-peak amplitude ΔI_{Coutn}.

Switching losses P_{QSW_H} in the high-side MOSFET are given by

$$P_{QSW\_H} = \frac{1}{2} U_{IN} f_{SW} \left[\left(\frac{I_0}{N} + \frac{\Delta I_L}{2} \right) t_{r\_H} + \left(\frac{I_0}{N} - \frac{\Delta I_L}{2} \right) t_{f\_H} \right]. \quad (6)$$

where t_{r_H} is the rise time and t_{f_H} is the fall time of the high-side MOSFET.

For the RMS current I_{QL_rms} through an LS transistor, the following relation is valid:

$$I_{QL\_rms} = \sqrt{\left[\left(\frac{I_0}{N} \right)^2 + \left(\frac{\Delta I_L^2}{12} \right) \right] (1 - D)}. \quad (7)$$

The conduction losses of P_{Qon_L} of the LS transistor are given by

$$P_{Qon\_L} = I^2{}_{QL\_rms} R_{DSon\_L} = \left[\left(\frac{I_0}{N} \right)^2 + \left(\frac{\Delta I_L^2}{12} \right) \right] (1 - D) R_{DSon\_L}. \quad (8)$$

At the beginning and the end of lower MOSFET's conduction intervals, losses in the freewheeling diode must be considered during the dead time intervals.

Furthermore, dead time conduction losses in the body diode P_{QL_td} are expressed as follows:

$$P_{QL\_td} \approx U_{SD} f_{SW} \left[\left(\frac{I_0}{N} + \frac{\Delta I_{Cout}}{2} \right) t_{d1} + \left(\frac{I_0}{N} - \frac{\Delta I_{Cout}}{2} \right) t_{d2} \right]. \quad (9)$$

where U_{SD} is the body diode voltage, and t_{d1} and t_{d2} indicate dead time for rising and dead time for falling, respectively. These losses depend on the duration of the dead time (t_{d1} and t_{d2}), switching frequency f_{SW}, diode forward voltage U_{SD}, and current I_0/N.

Reverse recovery losses of the low-side MOSFET are expressed as follows:

$$P_{D(RR)} = UinQ_{RR} f_{SW}. \quad (10)$$

where Q_{RR} is the body diode reverse recovery charge.

In the discussed circuit there are also other types of losses, such as gate charge losses and output capacitance losses in the MOSFETs, which are typically much smaller than the losses considered previously.

Gate charge losses P_{GH} of the transistor $Q1$ can be expressed by

$$P_{GH} = U_{GS} Q_{GH} f_{SW}. \tag{11}$$

where U_{GS} is the gate-source voltage and Q_{GH} is the gate charge of the high-side MOSFET.

Output capacitance losses in the high-side MOSFET $P_{C_{OSS\_H}}$ are given by

$$P_{C_{OSS\_H}} = \frac{1}{2} U_{in}^2 f_{SW} C_{OSS\_H}. \tag{12}$$

where C_{OSS_H} is the output capacitances of the high-side MOSFET.

The total losses in the HS transistor, in one stage, are the sum of the losses determined by (5), (6), (10), (11), and (12), and are calculated using the following [38]:

$$P_{QH} = P_{Qon\_H} + P_{QSW\_H} + P_{D(RR)} + P_{GH} + P_{C_{OSS\_H}}. \tag{13}$$

The total losses in the HS MOSFETs P_{QHN} in an N-phase synchronous buck converter is N times P_{QH}.

Gate charge losses P_{GL} of the transistor $Q2$ can be expressed by

$$P_{GL} = U_{GS} Q_{GL} f_{SW}. \tag{14}$$

where U_{GS} is the gate-source voltage and Q_{GL} is the gate charge of the low-side MOSFET.

Output capacitance losses in the low-side MOSFET $P_{C_{OSS\_L}}$ are given by

$$P_{C_{OSS\_L}} = \frac{1}{2} U_{in}^2 f_{SW} C_{OSS\_L}. \tag{15}$$

where C_{OSS_L} is the output capacitance of the low-side MOSFET.

Furthermore, the total losses in the LS transistor P_{QL}, in the one buck stage, are the sum of the losses determined by (8), (9), (14), and (15), and can be found in [38]:

$$P_{QL} = P_{Qon\_L} + P_{QL\_td} + P_{GL} + P_{C_{OSS\_L}}. \tag{16}$$

The total losses in the LS MOSFETs P_{QLN} in an N-phase synchronous buck converter is N times P_{QL}.

The conduction loss is caused by the DC resistance (DCR) of the winding forming the inductor [33]. The current amplitude and the switching frequency of the load determine the choice of inductors. The RMS current I_{L_rms}, through the inductance per phase, is given by

$$I_{L\_rms} = \sqrt{\left(\frac{I_0}{N}\right)^2 + \left(\frac{\Delta I_L^2}{12}\right)}. \tag{17}$$

Hence, the conduction losses in the inductor per phase can be expressed by

$$P_L = {I^2}_{L\_rms} DSR, \tag{18}$$

where $DCR1 = DCR2 = \ldots = DCRN = DCR$. Conduction losses P_{LN} in the inductors in an N-phase synchronous buck converter is N times P_L.

Power losses in the input capacitor P_{Cin} become

$$P_{Cin} = I_{IN\_rms}^2 ESRin. \tag{19}$$

The current through the output capacitor $Cout$ is the sum of the ripple currents of each individual stage. Moreover, the RMS value I_{Cout_rms} is given by

$$I_{Cout\_rms} = \sqrt{\frac{I^2_{Cout\_rip}}{12}}. \quad (20)$$

Thus, the power losses P_{Cout} in the output capacitor become

$$P_{Cout} = I^2_{Cout\_rms} ESRout. \quad (21)$$

The total losses P_{out} in the N-phase synchronous buck converter can be found using

$$P_{out} = P_{QHN} + P_{QLN} + P_{LN} + P_{Cin} + P_{Cout} \quad (22)$$

For the efficiency of a multi-phase synchronous buck converter, the following relation is used:

$$\eta = \frac{U_0 I_0}{U_0 I_0 + P_{out}} \times 100, \%. \quad (23)$$

3. Design Considerations of Multi-Phase Buck DC-DC Converters

Optimum Phase Numbers for Some Common Input and Output Voltages

The growing necessity for rapid and accurate phase number prediction in designing multi-phase buck converters, so as to minimize the ripple currents and achieve high efficiency is of particular importance to power supply designers. For this purpose, using the results from different control examples, this section discusses the selection of the optimum phase numbers for various common input and output voltages. Analytical examples (with an application in modern microprocessors) are based on the following parameters:

- *Uin* = 12 V, *Uout* = 1.6 V/3.3 V/5 V, f_{SW} = 75 kHz ÷ 300 kHz, I_0 = 5÷ 200 A, t_d = 100 ns;

To increase the efficiency of the multi-phase synchronous buck converter, transistors with small reverse recovery charge Qrr and R_{DSon}. are selected. Table 1 presents the MOSFET data used in the considered examples [39–43].

Table 1. N-Channel Power MOSFETs—typical values.

Part Number	V_{DS}, V	Id @ Tc = 25 °C, A	R_{DSon} @Tj = 25 °C, mΩ	Coss, pF	Q_G, nC (Vgs = 10 V)	Qrr, nC	trr @ Tj = 25 °C, ns	V_{SD}, V
SiRA10BDP	30	60	2.3	655	24.1	36	38	0.75
SiRC10DP (SkyFET with monolithic Schottky diode)	30	60	2.9	760	24.0	27	35	0.51
SiRC06DP	30	60	2.2	350	38.5	19	31	0.47
CSD17581Q3A	30	60	3.2	342	41.0	10.2	9.8	0.80
CSD17581Q5A	30	60	2.9	342	41.0	13	11	0.80

The used capacitors *Cout* and *Cin* (Figure 1) have equivalent series resistances *ESRout* = *ESRin* = 0.8 mΩ. The value of the used inductances *L1* = . . . = *LN* = *L* = 1.9 uH and the equivalent series resistances of the output inductances *DCR1* = . . . = *DCRN* = *DCR* = 0.62 mΩ (high current shielded power inductors AGM2222 [44]). A proper starting point is to select an inductor such that its ripple current amplitude is about 40% of the maximum channel current [35].

It is well known that increasing the number of units helps to reduce the maximum ripple current [32–38]. Also, the ripple output current and output voltage will reach zero if the duty cycle is equal to one of the following critical points:

$$D_{crit} = i/N \; i = 1, 2, N - 1. \quad (24)$$

For the considered examples, based on (2) and (3) the presented results in Tables 2 and 3 are for the RMS value of input current I_{IN_rms} and the output ripple current peak-to-peak amplitude ΔI_{Cout} of the multi-phase buck converter. The used transistors are SiRA10BDP (*Q1*) and SiRC10DP (*Q2*).

Table 2. Multi-phase buck converter output ripple current peak-to-peak amplitude ΔI_{Cout}.

ΔI_{Cout}, A - *Uin* = 12 V, f_{SW} = 200 kHz					ΔI_{Cout}, A - *Uin* = 12 V, f_{SW} = 300 kHz				
***Uout*, V**	***N* = 4**	***N* = 6**	***N* = 8**	***N* = 12**	***Uout*, V**	***N* = 4**	***N* = 6**	***N* = 8**	***N* = 12**
1.6	1.965	0.842	0.246	0.632	1.6	1.31	0.561	0.164	0.421
3.3	0.711	1.197	0.632	0.553	3.3	0.474	0.798	0.421	0.368
5	1.754	1.316	0.877	0	5	1.17	0.877	0.585	0

Table 3. Multi-phase buck converter RMS value of input current I_{IN_rms}.

I_{IN_rms}, A - *Uin* = 12 V, f_{SW} = 200 kHz						I_{IN_rms}, A - *Uin* = 12 V, f_{SW} = 300 kHz					
	Uout	***N* = 4**	***N* = 6**	***N* = 8**	***N* = 12**		***Uout***	***N* = 4**	***N* = 6**	***N* = 8**	***N* = 12**
I_0 = 45 A	1.6 V	5.665	3.144	1.662	1.944	I_0 = 45 A	1.6 V	5.636	3.065	1.524	1.885
	3.3 V	3.659	3.766	2.551	2.005		3.3 V	3.504	3.662	2.389	1.851
	5 V	5.503	3.916	2.911	2.216		5 V	5.393	3.825	2.770	1.477
I_0 = 100 A	1.6 V	12.496	6.733	3.243	4.131	I_0 = 100 A	1.6 V	12.483	6.696	3.174	4.104
	3.3 V	7.632	8.036	5.143	3.956		3.3 V	7.559	7.988	5.064	3.880
	5 V	11.876	8.410	6.014	2.216		5 V	11.826	8.367	5.947	1.477
I_0 = 150 A	1.6 V	18.724	10.044	4.761	6.156	I_0 = 150 A	1.6 V	18.715	10.02	4.715	6.138
	3.3 V	11.339	11.982	7.596	5.821		3.3 V	11.289	11.95	7.543	5.769
	5 V	17.739	12.551	8.920	2.216		5 V	17.705	12.523	8.875	1.477
I_0 = 200 A	1.6 V	24.956	13.367	6.299	8.190	I_0 = 200 A	1.6 V	24.95	13.348	6.264	8.176
	3.3 V	15.067	15.942	10.072	7.707		3.3 V	15.03	15.918	10.032	7.669
	5 V	23.616	16.705	11.846	2.216		5 V	23.591	16.684	11.812	1.477

It can be seen that, for all N, the RMS value of the input current I_{IN_rms} and the peak-to-peak ripple current amplitude ΔI_{Cout} decrease as the frequency increases. Furthermore, at *Uout* = 5 V and N = 12, the output ripple current will be zero. Therefore, theoretically, the output filter capacitor can be eliminated in the circuit. Thus, the size of the converter can be reduced significantly, and the response time will be faster. However, from a practical point of view, most of the converters operate with a variable duty cycle due to compatibility considerations with varied power supplies, and eliminating the output capacitor is impossible. However, providing less ripple current contributes to the use of less bulky capacitors.

Another crucial criterion in selecting the optimal number of phases is the circuit's efficiency. Figure 3a,b provide a graphical representation of efficiency η evaluated by (-23) for the control examples with the following parameters: *Uin* = 12 V, *Uout* = 1.6 V, f_{SW} = 200 kHz/f_{SW} = 300 kHz, $I_0 = 5 \div 200$ A, t_d = 100 ns.

Figure 3c,d present the graphical representation of efficiency η evaluated by (-23) for the next control examples: *Uin* = 12 V, *Uout* = 3.3 V, f_{SW} = 200 kHz/f_{SW} = 300 kHz, $I_0 = 5 \div 200$ A, t_d = 100 ns. Furthermore, in Figure 3e,f are plotted (23) for the control examples with the following parameters: *Uin* = 12 V, *Uout* = 5 V, f_{SW} = 200 kHz/f_{SW} = 300 kHz, $I_0 = 5 \div 200$ A, t_d = 100 ns.

Based on Figure 3a, it can be concluded that at the output current values $I_0 < 20$ A the multi-phase synchronous buck converter with N = 2 has the highest efficiency (90.8%). For output current values in the range of 20 A < I_0 < 35 A, the highest efficiency η has a circuit with N = 4 (η = 90.77%). For output current values in the range of 35 A < I_0 < 45 A, the circuit with N = 6 has the highest efficiency (η = 90.792%). On the other hand, at I_0 = 40 A the efficiency of a circuit with N = 4 is η = 90.58%, whereas for N = 6 it is η = 90.79%, or in other words, the efficiency is 0.21% less than that of N = 6. By analyzing the efficiency for N = 4 and I_0 = 45 A, it is observed that η = 90.44%. Therefore, for this range of variation in output current I_0, the efficiency decreases by 0.25% compared to the N = 6 configuration.

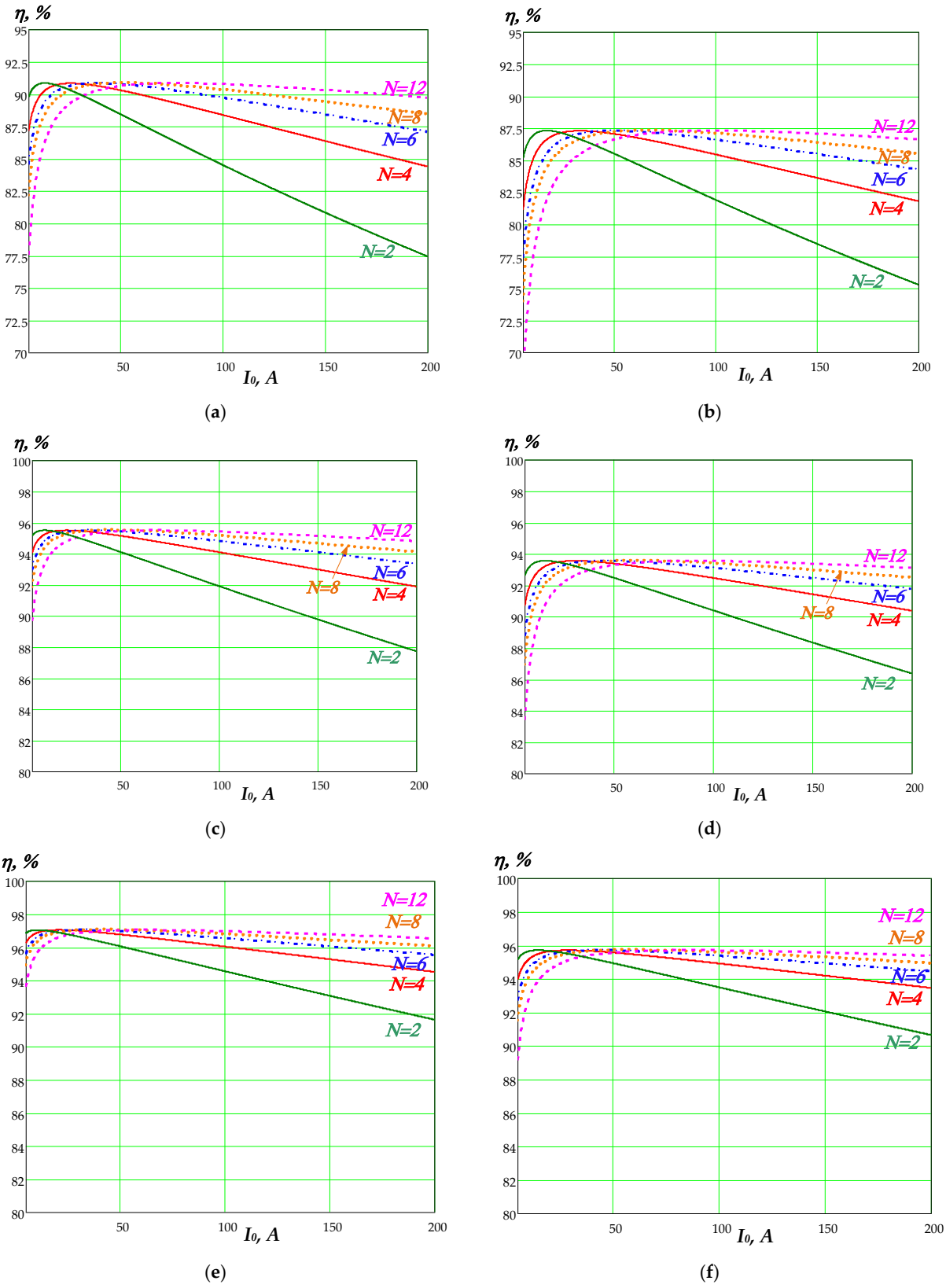

Figure 3. Multi-phase synchronous buck converter efficiency η vs. output current I_0: (**a**) Duty cycle D = 0.133, f_{SW} = 200 kHz; (**b**) duty cycle D = 0.133, f_{SW} = 300 kHz. (**c**) duty cycle D = 0.275, f_{SW} = 200 kHz; (**d**) duty cycle D = 0.275, f_{SW} = 300 kHz; (**e**) duty cycle D = 0.417, f_{SW} = 200 kHz; (**f**) duty cycle D = 0.417, f_{SW} = 300 kHz.

The results from Figure 3a–d are summarized and presented in Tables 4 and 5.

Table 4. Multi-phase buck converter efficiency η - *Uin* = 12 V, *Uout* = 1.6 V.

	η, %, f_{SW} = 200 kHz				η, %, f_{SW} = 300 kHz			
	***N* = 4**	***N* = 6**	***N* = 8**	***N* = 12**	***N* = 4**	***N* = 6**	***N* = 8**	***N* = 12**
I_0 = 45 A	90.44	90.77	90.77	90.4	87.14	87.25	87.03	86.29
I_0 = 100 A	88.41	89.73	90.31	90.74	85.48	86.61	87.07	87.27
I_0 = 150 A	86.43	88.45	89.43	90.31	83.68	85.51	86.37	87.07
I_0 = 200 A	84.48	87.13	88.47	89.74	81.88	84.32	85.53	86.62

Table 5. Multi-phase buck converter efficiency η - *Uin* = 12 V, *Uout* = 3.3 V.

	η, %, f_{SW} = 200 kHz				η, %, f_{SW} = 300 kHz			
	***N* = 4**	***N* = 6**	***N* = 8**	***N* = 12**	***N* = 4**	***N* = 6**	***N* = 8**	***N* = 12**
I_0 = 45 A	95.23	95.43	95.46	95.34	93.44	93.52	93.49	93.1
I_0 = 100 A	94.14	94.83	95.15	95.40	92.5	93.13	93.38	93.52
I_0 = 150 A	93.06	94.13	94.66	95.15	91.49	92.49	92.98	93.38
I_0 = 200 A	91.99	93.41	94.14	94.83	90.47	91.82	92.50	93.12

These results indicate that when selecting the optimal number of phases, a comprehensive approach should be taken to assess the advantages that will be achieved by increasing the number of stages in a multi-phase buck configuration. Furthermore, the optimal phase number should be evaluated over the entire duty cycle range. Moreover, Figure 4 shows the 3D plots of (23) as a function of duty cycle D and switching frequency f_{SW} - η (D, f_{SW}), %. Figure 4a shows the performance η at the following input data: I_0 = 200 A, N = 8, f_{SW} = 75 kHz ÷ 300 kHz, dead time td = 100 ns, and Figure 4b at N = 12. Here, the output voltage *Uout* is assumed to be fixed at 1.6 V, and the input voltage is varied, resulting in a duty cycle D changing from 0.1 to 0.9.

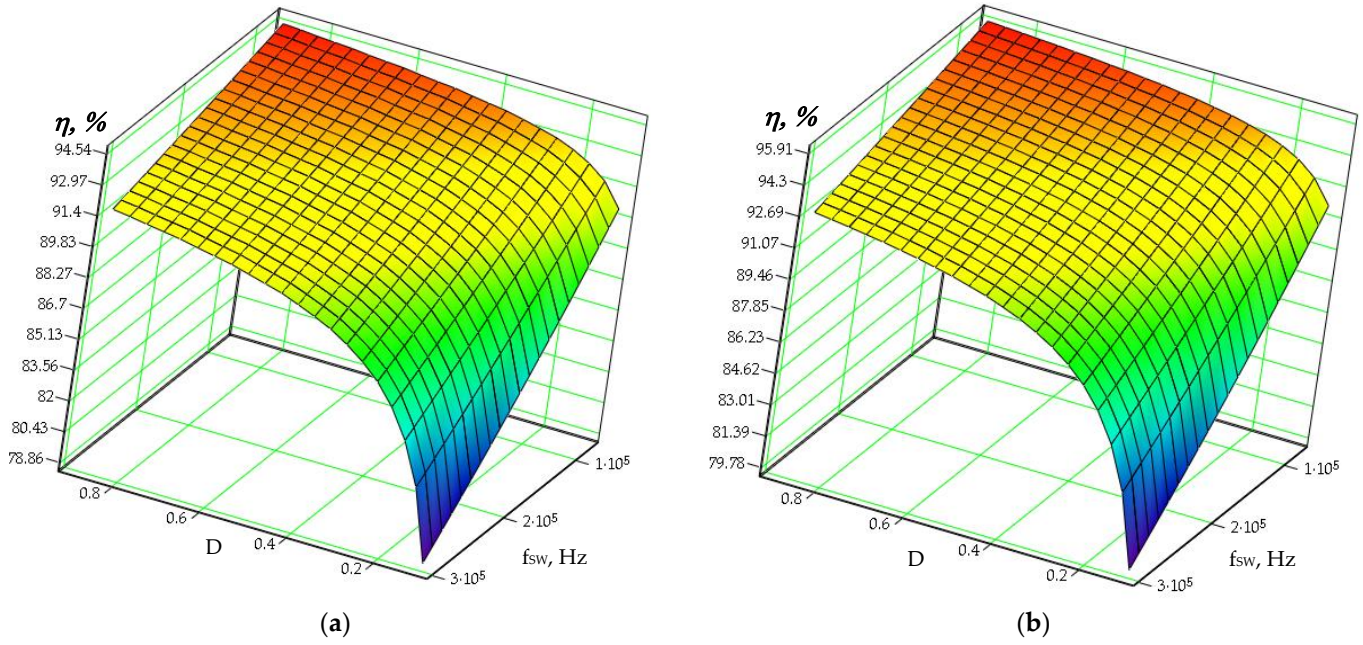

Figure 4. Multi-phase synchronous buck converter efficiency η (D, f_{SW}). (**a**) *Uout* = 1.6 V, I_0 = 200 A; N = 8; f_{SW} = 75 kHz ÷ 300 kHz; D = 0.1 ÷ 0.9; (**b**) *Uout* = 1.6 V, I_0 = 200 A; N = 12; f_{SW} = 75 kHz ÷ 300 kHz; D = 0.1 ÷ 0.9.

At N = 12, the efficiency of the circuit, over the whole range of the changes in duty cycle D, was higher by approximately 0.92 ÷ 1.37% compared to that at N = 8.

Based on the results presented in Figures 3 and 4, it is recommended to select the buck stages as outlined in Table 6, with a focus on optimizing circuit efficiency and minimizing ripple currents. Additionally, the cost-effectiveness of the schematic should be taken into account when choosing larger *N*-stage circuits.

Table 6. Optimal phase numbers considering circuit efficiency and minimizing ripple currents.

		$I_0 < 25$ A	25 A $< I_0 <$ 45 A	45 A $< I_0 <$ 90 A	90 A $< I_0 <$ 150 A	150 A $< I_0 <$ 200 A
Uin = 12 V/ f_{SW} = 200 kHz	$Uout$ = 1.6 V	N = 2	N = 4	N = 6, 8	N = 8	N = 8
	$Uout$ = 3.3 V	N = 2	N = 4	N = 4, 8	N = 8	N = 8, 12
	$Uout$ = 5 V	N = 2	N = 4	N = 6, 8	N = 8, 12	N = 12
Uin = 12 V/ f_{SW} = 300 kHz	$Uout$ = 1.6 V	N = 2	N = 4	N = 6, 8	N = 8	N = 8
	$Uout$ = 3.3 V	N = 2	N = 4	N = 4, 8	N = 8	N = 8, 12
	$Uout$ = 5 V	N = 2	N = 4	N = 6, 8	N = 8, 12	N = 12

4. Analytical and Simulation Study of Power Losses in an 8-Phase Synchronous Buck Converter

4.1. Analytical Study of Power Losses in an 8-Phase Synchronous Buck Converter

In this paragraph, power losses as a function of switching frequency f_{SW} and duty cycle D are investigated for a control example with the following data: $Uout$ = 1.6 V, I_0 = 200 A, f_{SW} = 75 kHz ÷ 300 kHz; dead time t_d = 100 ns. Based on the data shown in Table 6, the multi-phase synchronous buck converter with N = 8 is chosen. The used transistors are SiRA10BDP and SiRC10DP.

For the proper choice of the circuit elements, the estimation of the losses resulting from the changes in different parameters is of particular importance. All power losses plotted in Figure 5 consider the 8-phase synchronous buck converter (N = 8). Figure 5a shows the total power loss distribution $P_{out}(D, f_{SW})$ as a function of the duty cycle D and the switching frequency f_{SW}. Figure 5b illustrates the total HS MOSFETs power losses $P_{QHN}(D, f_{SW})$ and Figure 5c shows the total LS MOSFETs power losses $P_{QLN}(D, f_{SW})$. The inductance losses of the considered multi-phase synchronous buck converter versus the duty cycle D and the switching frequency f_{SW} are given in Figure 5d. The power losses in the output $P_{Cout}(D, f_{SW})$ and input capacitors $P_{Cin}(D, f_{SW})$ are illustrated in the next Figure 5e,f.

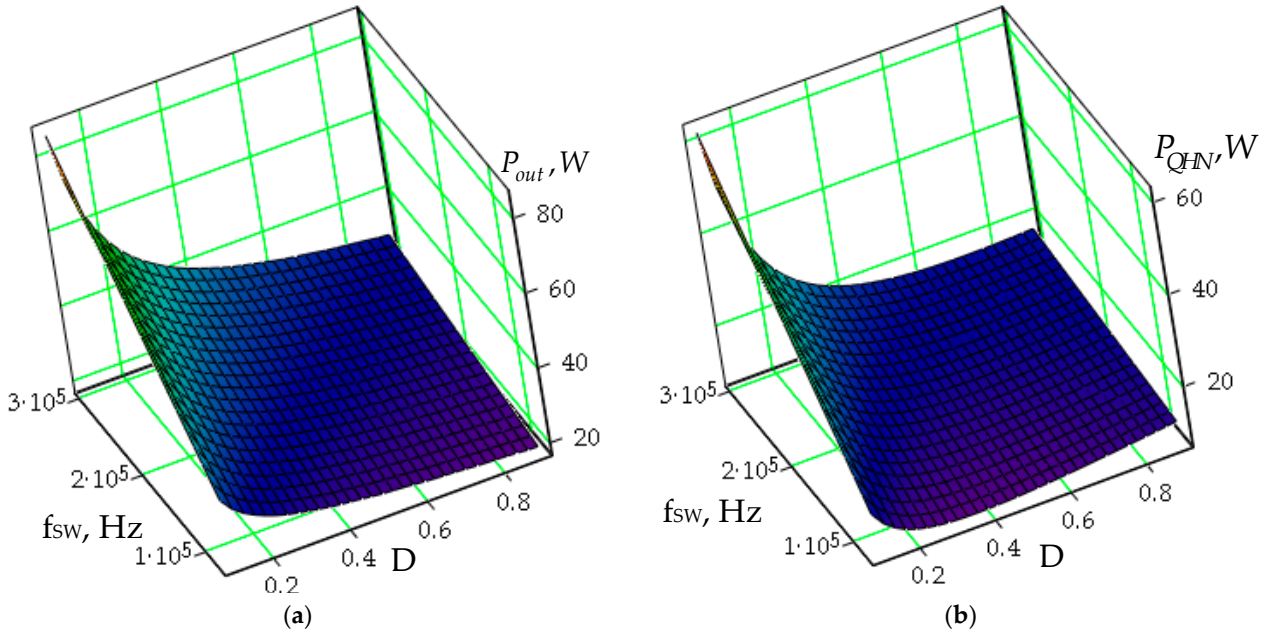

Figure 5. *Cont.*

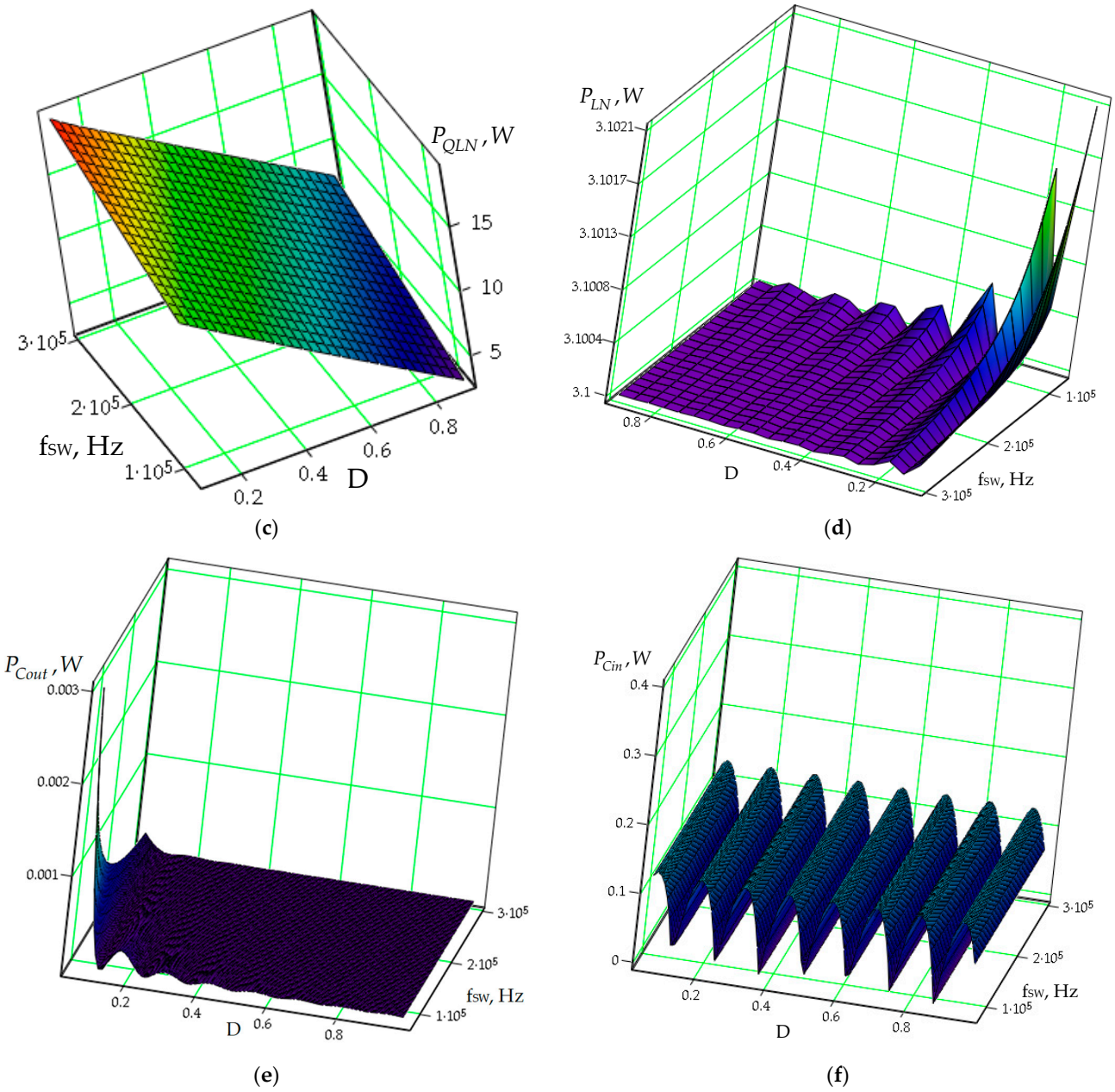

Figure 5. Multi-phase synchronous buck converter losses at $N = 8$: (**a**) Total power losses $P_{out}(D, f_{SW}), W$; (**b**) total HS MOSFETs power losses $P_{QHN}(D, f_{SW}), W$; (**c**) total LS MOSFETs power losses $P_{QLN}(D, f_{SW}), W$; (**d**) the inductances losses $P_{LN}(D, f_{SW}), W$; (**e**) the power losses in the output capacitor $P_{Cout}(D, f_{SW})$, W; (**f**) power losses in the input capacitor $P_{Cin}(D, f_{SW})$, W.

Power losses increase with increasing frequency, as at small duty cycles, the power losses are significant. In addition, power losses in the low-side transistors are considerable.

The following Figure 6a,b show the dependencies of total HS MOSFETs losses versus the total converter's power losses $P_{QHN}/P_{out}, \%$ and HS MOSFETs switching losses versus the HS MOSFETs total power losses $P_{QSW\_HN}/P_{QHN}, \%$ in the 8-phase synchronous buck converter, respectively. In Figure 6c, the dependencies of the total LS MOSFETs losses versus the total power losses $P_{QLN}/P_{out}, \%$ are plotted. The dependencies of the inductance losses of the considered 8-phase synchronous buck converter versus the total power losses $P_{LN}/P_{out}, \%$ are illustrated in Figure 6d.

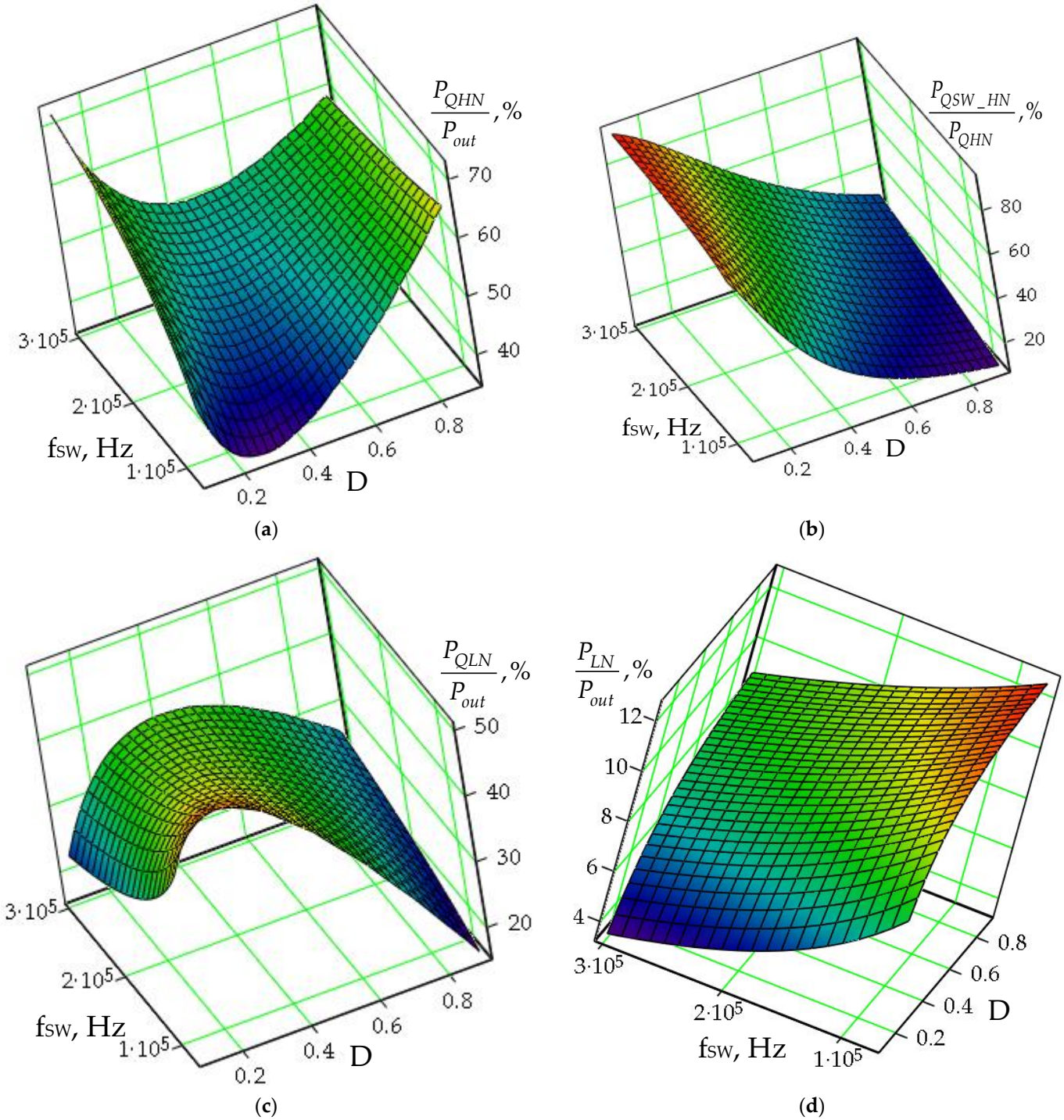

Figure 6. Multi-phase synchronous buck converter losses at *Uout* = 1.6 V, I_0 = 200 A, N = 8: (**a**) The total HS MOSFETs losses vs. to the total power losses P_{QHN}/P_{out}, %; (**b**) the HS MOSFETs switching losses vs. the total power losses in HS MOSFETs P_{QSW_HN}/P_{QHN}, %; (**c**) the total LS MOSFETs losses vs. the total power losses P_{QLN}/P_{out}, %; (**d**) the inductances losses vs. the total power losses—P_{LN}/P_{out}, %.

Based on these results, it is evident that in the range up to the duty cycle D ≈ 0.4, for the studied frequency range, the losses in the low-side transistors at frequencies up to f_{SW} ≈ 100 kHz are a significant part of the total losses in the converter (≈45%), whereas the losses in the high-side transistors are ≈35% of the total losses in the converter. Switching losses are the highest percentage of the total losses in the upper transistors (≈80%) at small values of duty cycle D regardless of the operation frequency range. With increasing the

frequency, the losses in the high-side transistors increase, and at a frequency of 300 kHz, the losses in the high-side transistors are ≈50% of the total losses in the circuit.

4.2. Simulation Study of Power Losses in 8-Phase Synchronous Buck Converter

To verify the considered design methodology, a simulation using *PSpice for TI* of a multi-phase synchronous buck converter has been performed with the following input data: *Uin* = 12 V, U_0 = 3.3 V, f_{SW} = 200 kHz, I_0 = 200 A, t_d = 100 ns. Based on the data presented in Table 6, a configuration circuit with N = 8 has been selected. The MOSFET CSD17581Q3A (*Q1*, *Q2*) built into the simulator libraries has been used to perform the simulations.

The comparison results between numerical calculations and those obtained from simulations are summarized in Table 7.

Table 7. A comparison of the design parameters obtained from the calculations and those from the simulations—f_{SW} = 200 kHz, I_0 = 200 A.

Quantity	Calc.	Simul.	δ, %
Output current I_0, A	200	196.987	1.5
Output voltage U_0, V	3.3	3.25	1.5
peak-to-peak inductor current ΔI_L	6.296	6.326	−0.48
HS MOSFET RMS current I_{QH_rms}, A	13.145	13.146	0
LS MOSFET RMS current I_{QL_rms}, A	21.343	20.922	1.97
Inductunce *L1* RMS current I_{L1_rms}, A	25.066	24.56	2
HS MOSFETs conduction losses P_{Qon_HN}, W	4.424	4.312	2.5
LS MOSFETs conduction losses P_{Qon_LN}, W	8.384	8.16	2.6
Inductances losses P_{LN}, W	3.12	3	3.8
HS MOSFETs total losses P_{QHN}, W	6.65	6.4	3.8
LS MOSFETs total losses P_{QLN}, W	15.44	14.84	3.9

By analyzing the results from Table 7, it can be concluded that the relative error δ between analytical and simulation results does not exceed 4%.

5. Conclusions

Increasing the need for rapid and accurate prediction of phase numbers in the design of multi-phase buck converters to minimize ripple currents and achieve high efficiency is of particular importance to power supply designers. Analytical and graphical (3D plots) analyses of output and input current ripples in the multi-phase converter, as well as the losses in the converter circuit, were conducted using control examples. Based on the analytical results, it was demonstrated that for the considered control examples, when the output current values I_0 are less than 20 A (I_0 < 20 A), the multi-phase synchronous buck converter with N = 2 exhibits the highest efficiency (90.8%). Meanwhile, for output current values in the range of 20 A < I_0 < 35 A, a configuration with N = 4 (η = 90.77%) achieves the highest efficiency. Other important results obtained show that for the output current range of 35 A < I_0 < 45 A, the highest efficiency is achieved with a configuration using N = 6 phases (η = 90.792%). At the same time, at an output current value of I_0 = 40 A, the efficiency of the N = 4 phase circuit is 0.21% lower than that of the N = 6 phase circuit. When the output current is I_0 = 100 A, the efficiency of the N = 12 phase configuration is 0.14% higher than that of the N = 8 phase configuration, whereas at I_0 = 200 A, the efficiency of the N = 12 phase circuit is 0.62% higher than that of the N = 8 phase circuit.

Furthermore, the article assesses power losses resulting from changes in various parameters such as duty cycle (D = 0.1 ÷ 0.9) and operating frequency (75 kHz ÷ 300 kHz). It is shown that power losses increase with an increase in frequency, as significant losses are observed at low-duty cycles. The simulation results of power losses in the multi-phase synchronous buck converter with N = 8 are also presented in the article. The relative error between analytical and simulation results does not exceed 4%. A discussion on the optimal phase numbers for common input and output voltages is included. The choice of the optimal number of phases should be approached comprehensively to evaluate the

advantages of increasing the number of phases in a multi-phase buck configuration. The proposed approach for a fast and accurate calculation of power losses and overall efficiency reduces preliminary computational procedures and optimizes solutions.

Therefore, the methodology discussed for design can find applications both in engineering practice and in the education of students in power electronics.

In further research, authors should focus their attention on calculating the induction core losses and the converter's practical implementation.

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