Review

Technical Reviews of Power Loss Optimization in High-Frequency PSiPs—In Relation to Power Switches and Power Inductors

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Abstract: Power losses of switches and inductors are consistent challenges that hinder the development of high-frequency power supply in package (PSiP). This paper investigates the roadmap for power loss optimizations of switches and inductors in high-frequency PSiPs. Firstly, a size and parallel quantity design method to reduce power loss in an integrated Si LDMOSFET is provided with comprehensive consideration of switching frequency and power levels. Secondly, quality factors of different air-core inductors are analyzed with consideration of geometric parameters and skin effect, which provides the winding structure optimization to reduce power losses. The power losses of the integrated Si LDMOSFET and air-core inductors are both reduced to less than 10% of the output power at 1~100 MHz switching frequency and 0.1~10 W power level. Finally, based on the above optimizations, power losses of switches and inductors are calculated with switching frequency and power level. Combining the calculated results, this paper predicts the efficiency boundaries of PSiPs. Upon efficiency normalization with consideration of input and output voltage levels, all the predictions are consistent with the published literature. The efficiency predication error is 1~15% at 1~100 MHz switching frequency and 0.1~10 W power level. The above power loss optimizations improve the efficiency, which provides potential roadmaps for achieving high-frequency PSiPs.

Keywords: power supply in package; power loss optimization; integrated Si LDMOSFET; air-core inductor; efficiency boundary

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1. Introduction

In CPU and MCU applications, there is a consistent pursuit of high-frequency point-of-load (PoL) power supplies [1–3]. The switching frequency has been increasing in the past few decades [4]. This miniaturizes switches and inductors that primarily dominate the system size and weight. As a result, the integration level has evolved into a 3D stacked power supply (3D-SPS, discrete switch and discrete inductor), power supply in package (PSiP, integrated switch and discrete inductor), and power supply on chip (PwrSoC, integrated switch and integrated inductor) [5–7]. These integration levels differentiate in switching frequency and power rate and applications, as shown in Table 1.

Table 1. Switching Frequencies and Power Levels of Different Integration Levels.

Integration Level	3D-SPS	PSiP	PwrSoC
Switching Frequency	<10 MHz	<100 MHz	>100 MHz
Power Level	<100 W	<10 W	<2 W
Application	Primary PoL power supply	Compact primary PoL power supply	Secondary PoL power supply (on chip)

The 3D-SPS adopts discrete switches and inductors, which allows for high power conversion (up to 100 W) [8–10]. It carries out a 3D stacking structure on the PCB, and usually places magnetic components above or below the entire PCB board. With relative high inductance, the 3D-SPS approach can operate at a switching frequency below 10 MHz. The reduced switching frequency benefits the overall efficiency, since the switching loss is proportional to the switching frequency.

The PSiP integrates all components in one package, which achieves single chip power conversion [7,11]. Typically, it integrates power switches, drivers and control modules on a single die, whereas discrete inductors with low profile are packaged into the chip. Owing to the reduced inductance, the PSiP approach usually operates at a frequency above 10 MHz that leads to high switching loss and reduced efficiency. Due to limited power devices and heat dissipation, the power range is restricted to under 10 W.

The PwrSoC integrates all components on a single die, which achieves the highest integration level [12–14]. The integrated on-chip power supply can be placed as near to the load as possible, which reduces the transmission loss in power lines [15]. However, with a low on-chip inductance, the switching frequency usually increases above 100 MHz to reduce ripples. As a result, power loss and heat dissipation are hard to optimize and that limits the power rate to below 2 W.

In comparison to 3D-SPS, the PSiP saves the interconnecting area of the control chip, which drives chip and power transistors in 3D-SPS. In comparison to PwrSoC, the PSiP generally adopts the standard CMOS process and does not require the CMOS process with power inductors, which is more mature and compatible with technology. Therefore, the PSiP power supply is more widely applied in communication, server automatic systems and so on.

For all integration levels, switching frequency and power levels are usually contradictory, and the major challenges toward high frequency are power losses of switches and inductors, as shown in Figure 1.

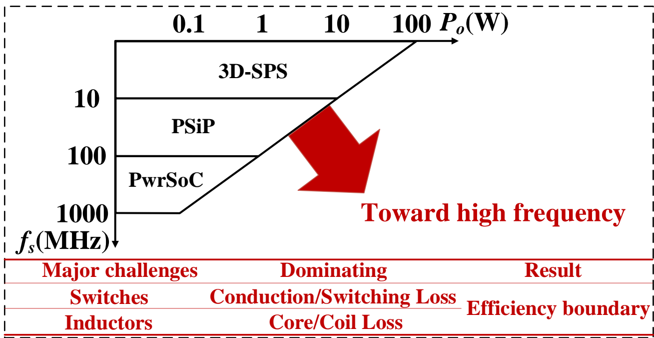

Figure 1. Roadmap for high-frequency PoL power supplies.

Among the major challenges, the power switch dominates conduction and switching losses. Conduction and switching losses are primarily determined by the on-resistance value (R_{on}) and total gate charge value (Q_G), respectively. Figure-of-merits (FOM = $R_{on} \times Q_G$) of the Si vertical trench, Si lateral trench and GaN lateral trench are shown in Figure 2 [16–18]. Due to the wider bandgap, higher electron mobility and electron velocity of GaN HEMT, its FOM is several times lower than that of Si MOSFET. These material characteristics result in lower power losses in GaN HEMT in high-frequency applications. However, GaN HEMTs are usually discretely packaged due to unique fabrication processes, which are preferable in 3D-SPS [19–21]. For low-power and high-integrated applications, the Si lateral diffused MOSFET (LDMOSFET) is usually applied in PSiP and PwrSoC because of compatible fabrication processes [22].

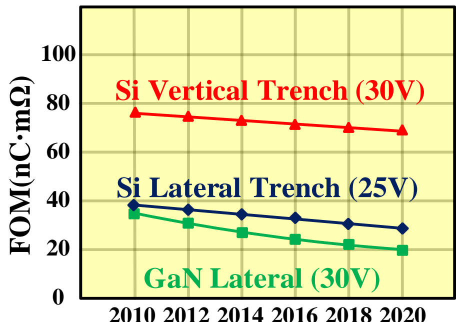

Figure 2. FOMs of GaN HEMT and Si MOSFET.

The power inductor dominates core and coil losses and primarily determines integration levels. Although the magnetic core helps increase the inductance, the core loss increases rapidly with frequency that harms the efficiency. For magnetic cores, their magnetic permeability, μ_i, of soft magnetic material decreases dramatically when the operating frequency reaches a critical value, which causes the dramatic decrement of the inductance value. In TDK Mn-Zn ferrites, MAGNETICS nanomaterial and alloy powders, their initial relative magnetic permeability, μ_i, is shown in Figure 3 [23–25]. Figure 3 shows that the permeability of magnetic materials decreases rapidly above 1 MHz. As the switching frequency increases, high-frequency inductors evolve from magnetic-core inductors to air-core inductors [26–28]. Without magnetic cores, air-core inductors do not suffer core loss and have good linearity to frequency. The inductance value decreases dramatically due to the removal of the magnetic core. In the literature and products, the typical inductance values of solenoid and planar spiral inductors are given in Table 2. All the investigated inductance values are less than 500 nH, which pushes the PoL power supply to operate at a frequency above 1 MHz.

Table 2. Typical Inductance Values of Solenoid and Planar Spiral Inductors.

Inductor Type	Literature	Operating Frequency	Inductance
Solenoid Inductor	0806SQ, 0807SQ, 0908SQ [29]	1~1000 MHz	5.5 nH~27.3 nH
	1111SQ [29]	1~500 MHz	27 nH~47 nH
	1515SQ, 2222SQ, 2929SQ [29]	1~100 MHz	47 nH~500 nH
Planar Spiral Inductor	[30]	150 MHz	1.5 nH
	[31]	10 MHz	2.7 nH
	[32]	100 MHz	5.8 nH
	[33]	10 MHz	220 nH
	[34]	550 MHz	1.54 nH
	[12]	450 MHz	0.85 nH

To address the above challenges, this paper analyzes integrated Si LDMOSFTs and air-core inductors in PSiPs. In terms of the integrated Si LDMOSFET, with consideration of parasitic resistors and capacitors, the size and parallel quantity optimization of integrated Si LDMOSFET are provided to reduce the switching and conduction losses. In terms of air-core inductors, with consideration of skin effect, quality factors of various air-core inductors are calculated for the winding structure optimization to reduce coil loss. Furthermore, combining the above optimizations, this paper predicts the efficiency boundaries of PSiP approaches based on power losses of switches and inductors.

This paper is organized as follows. Section 2 analyzes power losses of an integrated Si LDMOSFET to provide a size and parallel quantity optimization. Section 3 calculates the quality factors of solenoid inductors and planar spiral inductors to optimize wind-

ing structures. Section 4 predicts the efficiency boundaries of PSiP. Section 5 concludes this paper.

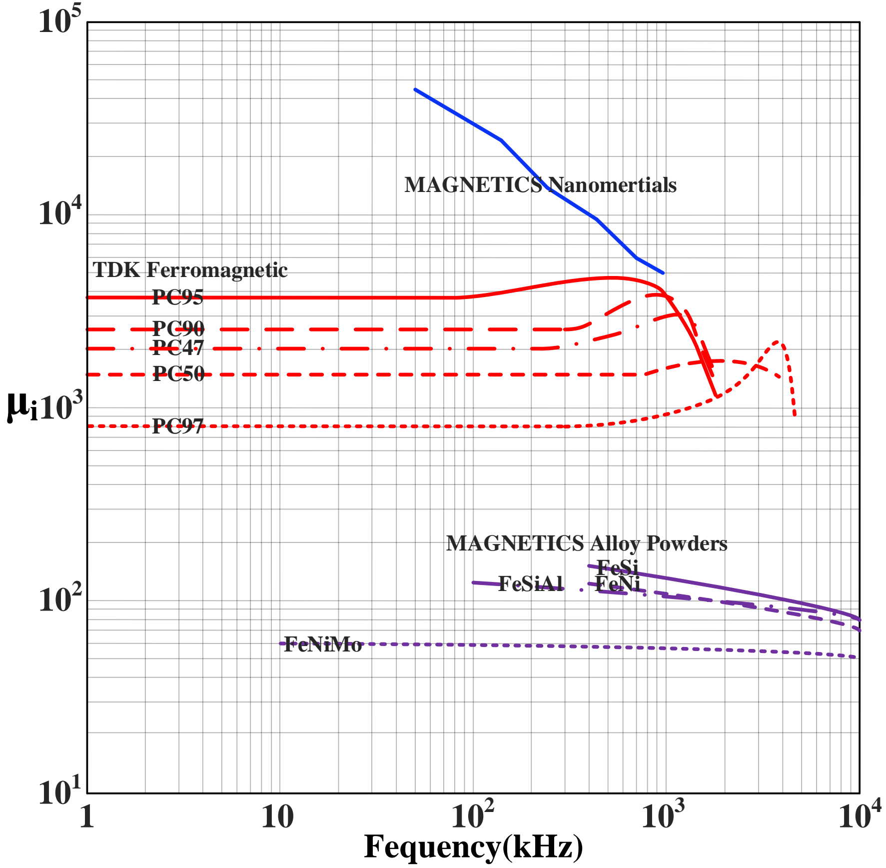

Figure 3. Initial relative magnetic permeabilities of TDK Mn-Zn ferrites, MAGNETICS nanomaterial and alloy powders.

2. Power Loss Analysis of Integrated Si LDMOSFET

In PSiPs, integrated Si MOSFETs have the most severe heat dissipation and the easiest thermal breakdown of all power devices. For PSiP, power loss caused by high frequency is a great challenge in terms of designing power switches. Power losses of integrated Si LDMOSFETs mainly include switching loss, driving loss, conduction loss and other power losses [35,36]. The equivalent model and switching process of an integrated Si LDMOSFET is shown in Figure 4. In Figure 4b,c, the gate voltage V_{GS} exits the miller platform due to the inductor in the output filter.

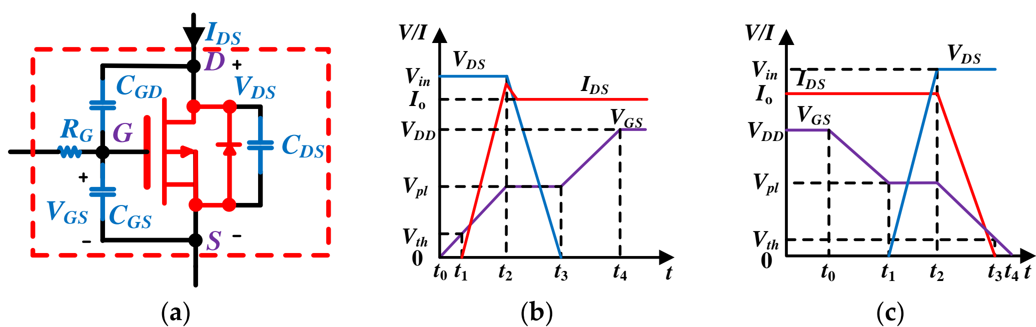

Figure 4. Equivalent model and switching process of an integrated Si LDMOSFET: (**a**) equivalent model (**b**) turn-on process (**c**) turn-off process.

Switching loss: At the period t_1~t_3 in turn-on and turn-off processes, the triangular overlapping area of drain-source current and voltage are switching losses. Therefore, according to the overlapping area, the switching loss is given by

$$\begin{array}{l} P_{on} = \frac{1}{2} f_s V_{in} I_o R_G \left[\frac{C_{ISS}(V_{PL}-V_{th})}{V_{DD}-\frac{V_{PL}+V_{th}}{2}} + \frac{C_{RSS}V_{in}}{V_{DD}-V_{PL}} \right] \\ P_{off} = \frac{1}{2} f_s V_{in} I_o R_G \left[\frac{C_{RSS}V_{in}}{V_{PL}} + \frac{2C_{ISS}(V_{PL}-V_{th})}{V_{PL}+V_{th}} \right] \end{array}. \quad (1)$$

Driving loss: At the period t_0~t_5 in turn-on and turn-off processes, gate voltage, V_{GS}, rises or falls via the charge, C_{GS}, or discharge, C_{GD}. The stored energies of C_{GS} and C_{GD} are dissipated by the driving resistor, R_G, which depends on the gate charge, Q_G. The driving loss is given by

$$P_G = f_s Q_G V_{DD}. \quad (2)$$

Conduction loss: In on-state, the Si LDMOSFET is equivalent to the on-resistor, R_{on}, dissipating the energy. Conduction loss is given by

$$P_{cond} = I_o{}^2 R_{on} \frac{V_{out}}{V_{in}}. \quad (3)$$

Other power losses: Other power losses mainly include output capacitance power loss and body diode power loss. The output capacitor stores the energy in off-state and releases the energy via the conducting channel in on-state. Based on the stored and released energies in a switching cycle, the output capacitance power loss is given by

$$P_{ds} = \frac{1}{2} f_s C_{OSS} V_{in}{}^2. \quad (4)$$

The body diode power loss includes forward conduction loss and reverse recovery loss. The forward conduction loss is caused by the forward body diode current during the dead time. It is given by

$$P_{d_f} = f_s V_F I_o t_d, \quad (5)$$

where V_F and t_d are the forward conduction voltage and forward conduction time of the body diode.

The reverse recovery loss is caused by the body diode reverse recovery after carrying the forward current. It is expressed as

$$P_{d_r} = f_s V_{DR} Q_{rr}, \quad (6)$$

where V_{DR} and Q_{rr} are the reverse recovery voltage and reverse recovery charge of the body diode.

Combining (1)–(6), the total power loss of M switches in parallel is given as

$$\begin{array}{l} P_{switch} = M(P_{on} + P_{off} + P_G + P_{ds} + P_{d_f} + P_{d_r}) + \frac{P_{cond}}{M} \\ = M f_s (X_1 I_o C_{ISS} + X_2 I_o C_{RSS} + X_3 C_{OSS} + X_4 I_o + X_5) + X_6 I_o{}^2 \frac{R_{on}}{M} \\ X_1 = V_{in} R_G \frac{2V_{DD}(V_{PL}-V_{th})}{(2V_{DD}-(V_{PL}+V_{th}))(V_{PL}+V_{th})} \\ X_2 = \frac{1}{2} V_{in} R_G \frac{V_{in}V_{DD}}{(V_{DD}-V_{PL})V_{PL}} \\ X_3 = \frac{1}{2} V_{in}{}^2, X_4 = V_F t_d, X_5 = Q_G V_{DD} + Q_{rr} V_{DR}, X_6 = \frac{V_{out}}{V_{in}} \end{array}, \quad (7)$$

where X_1, X_2, X_3, X_4, X_5 and X_6 represent coefficients in total power loss that do not depend on switching frequency and output current.

Based on the capacitance value per unit length and area, C_{ISS}, C_{OSS} and C_{RSS} of the integrated Si LDMOSFET are given by [37]

$$\begin{array}{l} C_{RSS} = C_{GD} = \frac{W_M L_M C_{ox}}{2} + W_M C_{ov} \\ C_{ISS} = C_{GD} + C_{GS} = W_M L_M C_{ox} + 2W_M C_{ov} \\ C_{OSS} = C_{GD} + C_{DS} = \frac{W_M L_M C_{ox}}{2} + W_M C_{ov} + \frac{W_M E_M C_j + (W_M + E_M) C_{jsw}}{2} \end{array}. \tag{8}$$

Based on I–V characteristic of the integrated Si LDMOSFET in the deep linear area, the on-resistance value is given by

$$R_{on} = \frac{1}{m_n C_{ox} \frac{W_M}{L_M} (V_{DD} - V_{th})}. \tag{9}$$

Based on (8) and (9), (7) can be derived as

$$\begin{array}{l} P_{switch} = M f_s (Y_1 I_o W_M + Y_2 W_M + X_4 I_o + Y_3) + Y_4 I_o{}^2 \frac{1}{M W_M} \\ Y_1 = X_1 (L_M C_{ox} + 2C_{ov}) + X_2 (L_M C_{ox} + 2C_{ov}) \\ Y_2 = X_3 \left(\frac{L_M C_{ox}}{2} + C_{ov} + \frac{E_M C_j + C_{jsw}}{2} \right) \\ Y_3 = X_5 + X_3 \frac{E_M C_{jsw}}{2}, Y_4 = X_6 \frac{L_M}{m_n C_{ox} (V_{DD} - V_{th})} \end{array}, \tag{10}$$

where coefficients Y_1, Y_2, Y_3 and Y_4 are obtained from X_1, X_2, X_3, X_5 and X_6 by excluding the channel width, W_M.

In (10), the power loss of the switch is determined by switching frequency, f_s, output current, I_o, switch size, W_M, and parallel quantity, M. As usual, f_s and I_o are determined by the power supply requirements. In order to reduce power loss, W_M and M are optimized as follows.

- M = 1: According to (10), taking V_{in} = 5 V and the 350 nm process as an example, the power loss is plotted with the integrated Si LDMOSFET size in Figure 5. It is obvious that there are different optimal sizes to minimize power loss at different switching frequencies and output currents [38]. This optimal size can be obtained by the simulation scan.

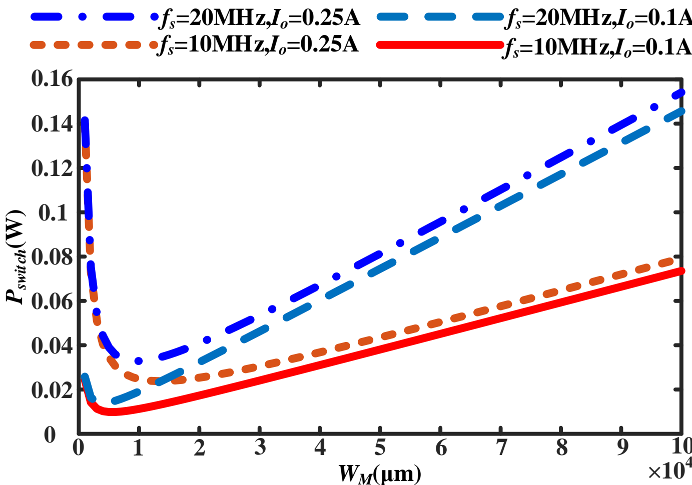

Figure 5. Power loss of the integrated Si LDMOSFET with size W_M when M = 1.

- $M \neq 1$: In fact, switch size is limited by the process. Therefore, the power switch is composed of multiple units in parallel. According to (10), the power loss is plotted with the output current in Figure 6. The size of a single unit is optimized at f_s = 10 MHz and I_o = 0.25 A, according to Figure 5. In Figure 6, comparing M = 4 to all load current

ranges, the parallel quantity of power switch changing with drain-source current is more beneficial to improving overall efficiency [39].

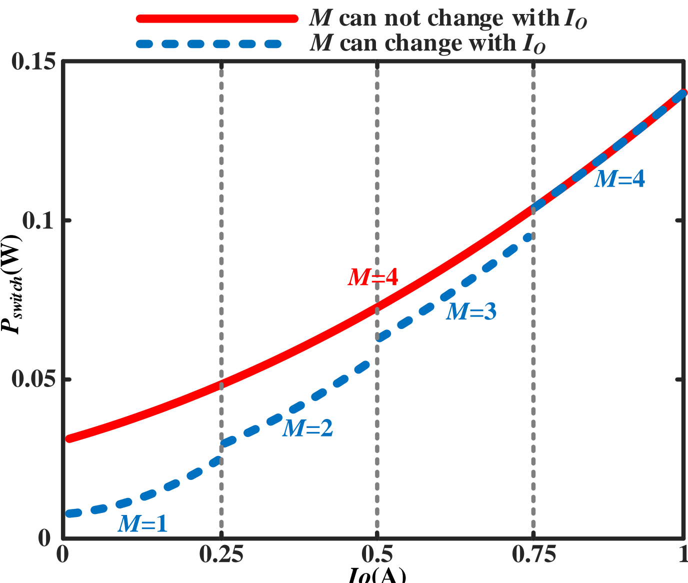

Figure 6. Power loss of the integrated Si LDMOSFET with drain-source current when $M \neq 1$.

3. Quality Factor Analysis of Air-Core Inductors

In PSiPs, the power loss of air-core inductors can be increased due to high-frequency effects. For megahertz PoL applications, power losses of air-core inductors are related to the inductance current, geometric parameters of coil-wire, coil material, skin effect, eddy effect, proximity effect, fringe effect, etc. Among many factors, the geometric parameters and skin effect are highly related to the switching frequency. To calculate the power loss of the air-core inductors, the inductance current is expanded into sinusoidal waves of various frequencies. Their frequencies and amplitudes are f_s, $2f_s$, $3f_s$, ... and I_{L1}, I_{L2}, I_{L3}, ... respectively. Upon consideration of the geometric parameters and skin effect, in [40], the power loss of air-core inductors can be estimated by

$$\begin{cases} P_{ind} = P_{ind,DC} + P_{ind,AC} \\ P_{ind,DC} = {I_{L0}}^2 R_{DC} = {I_{L0}}^2 \rho \frac{l}{A} \\ P_{ind,AC} = \frac{1}{2} \sum {I_{Ln}}^2 R_{AC,n} = \frac{1}{2} \sum {I_{Ln}}^2 \rho \frac{l}{\varphi \delta_n} \end{cases}. \quad (11)$$

In (11), the inductance power loss consists of the DC loss ($P_{ind,DC}$) and AC loss ($P_{ind,AC}$). Smaller R_{AC} at the same inductance value is more beneficial for efficiency, especially in reducing high-frequency power loss. In order to simplify the analysis, the quality factor, Q, is optimized to decrease the AC power loss, as given by

$$Q = \frac{2\pi f_s L}{R_{AC,n}}, \quad (12)$$

where higher Q means a lower AC resistance value at the same inductance value.

According to the profile, air-core inductors are classified into planar spiral inductors and solenoid inductors, as shown in Figure 7, which are discussed in the following sections.

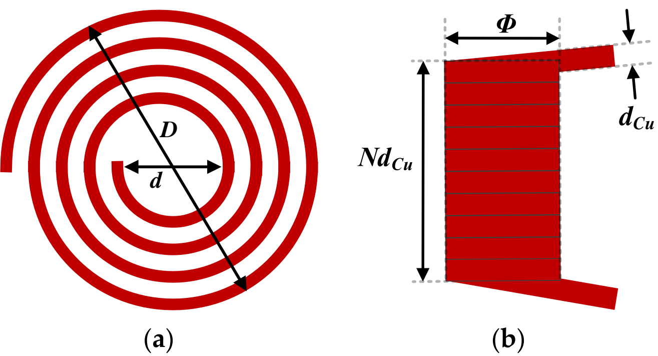

Figure 7. Structure schematics of air-core inductors: (**a**) planar spiral inductor (**b**) solenoid inductor.

3.1. Winding Structure Optimization of Planar Spiral Inductors

For a planar spiral inductor, the outer diameter, D, inner diameter, d, coil turn, N, coil-wire thickness and width determine its profile and inductance value. Inductance values of planar spiral inductors with different winding structures are uniformly expressed as follows [40]:

$$L = q_1 \mu_0 N^2 (D+d)\left[\ln\left(\frac{q_2}{T}\right) + q_3 T + q_4 T^2\right], T = \frac{D-d}{D+d}, \tag{13}$$

where D and d are the outer diameter and inner diameter, respectively, T is the ratio of difference and sum between outer and inner diameters, and N is the coil turn. The coefficients q_1, q_2, q_3 and q_4 of different winding structures are given in Table 3.

Table 3. Coefficients p, q_1, q_2, q_3 and q_4 in different winding structures of planar spiral inductors.

Winding Structure	Square	Hexagon	Octagon	Circle
p	2	1.732	1.657	1.571
q_1	0.3175	0.2725	0.2675	0.25
q_2	2.07	2.23	2.29	2.46
q_3	0.18	0	0	0
q_4	0.13	0.17	0.19	0.19

Considering skin effect and coil length, the nth harmonic AC resistance values of planar spiral inductors are given by

$$\begin{array}{l} R_{AC,n} = \rho \frac{l}{\varphi \delta_n} \\ \delta_n = \sqrt{\frac{\rho}{n\pi f_s \mu_0}}, l = p(D+d)N \end{array}, \tag{14}$$

where the coefficient, p, of different winding structures are as given in Table 3.

Combining (13) and (14), the quality factor of planar spiral inductors is derived as

$$Q_{planar} = 2\varphi\sqrt{\frac{\pi\mu_0 f_s \rho}{n}}\frac{q_1 N}{p}\left[\ln\left(\frac{q_2}{T}\right) + q_3 T + q_4 T^2\right]. \tag{15}$$

According to (15), the quality factor depends on the cross-section perimeter, φ, coil turn, N, and T. For φ and N, the quality factor increases monotonically with them. For T, the function-related T in Q is defined as

$$F(T) = \ln\left(\frac{q_2}{T}\right) + q_3 T + q_4 T^2. \tag{16}$$

Based on (16), the relationships between F and T are plotted in Figure 8 ($T < 1$). According to Figure 8, at the same D (area constraint), increasing d is beneficial for improving quality factor, Q.

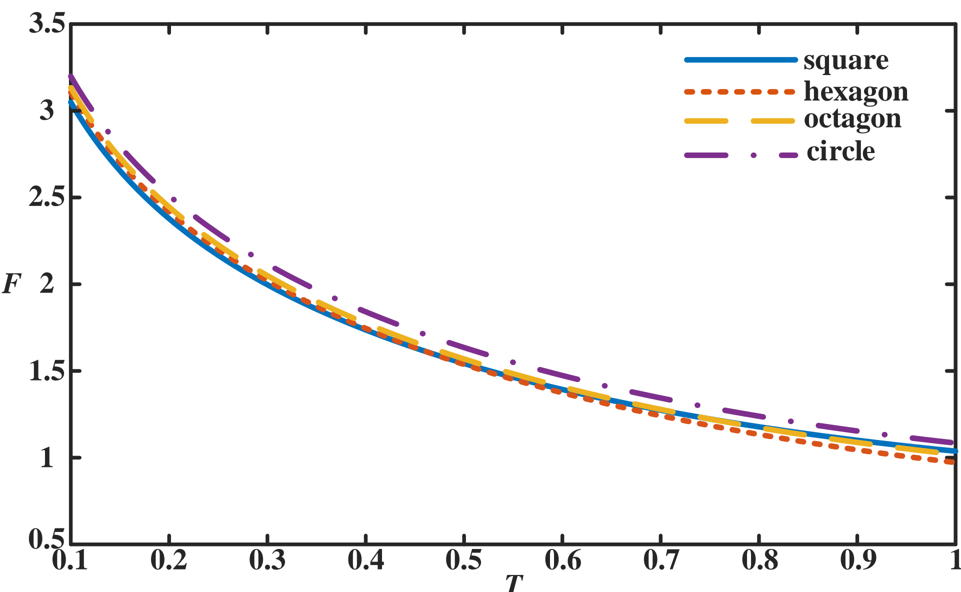

Figure 8. Relationships between F and T at different winding structures of planar spiral inductors.

In general, the outer diameter D is constrained by the inductance value. In order to improve the quality factor, d, N and φ should increase as much as possible. However, the above measures are contradictory in the winding structures of equal width. Therefore, in [41], wide outside winding and the narrow inside winding are applied to improve the quality factor, as shown in Figure 9. The quality factor of the proposed winding structure is calculated using the Greenhouse algorithm. Each turn of the winding structure is approximated as a polygon. The inductance value is the sum of self inductances and mutual inductances of all turns. The AC resistance value is the sum of AC resistance values for all turns. Therefore, the quality factor can be calculated based on the inductance and AC resistance values.

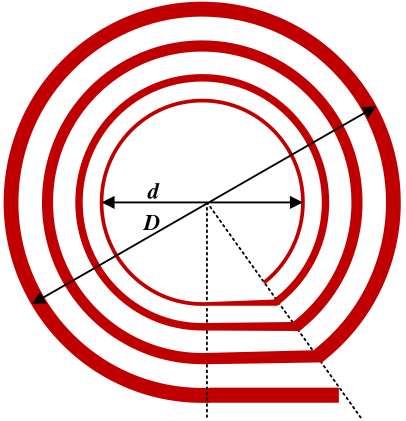

Figure 9. Wide outside winding and narrow inside winding structures of planar spiral inductors.

3.2. Winding Structure Optimization of Solenoid Inductors

For a tightly winding solenoid inductor, the winding diameter, ϕ, coil turn, N, and coil section diameter, d_{Cu}, determine its profile and inductance value. When the wind-

ing structure is cylinder, the inductance value of the solenoid inductor is given by [40] the following:

$$L = \frac{k\mu_0 \pi \phi^2 N}{4d_{Cu}}, \quad (17)$$

where Nagaoka's coefficient, k, depends on $\phi/(Nd_{Cu})$, as given in Table 4.

Table 4. Nagaoka's coefficients with $\phi/(Nd_{Cu})$.

$\phi/(Nd_{Cu})$	0.1	0.2	0.3	0.4	0.6	0.8	1
k	0.96	0.92	0.88	0.85	0.79	0.74	0.69
$\phi/(Nd_{Cu})$	1.5	2	3	4	5	10	20
k	0.6	0.52	0.43	0.37	0.32	0.2	0.12

The length of the solenoid inductor is given by

$$l = N\pi\phi. \quad (18)$$

Combining (14), (17) and (18), the quality factor of the solenoid inductor is derived as

$$Q_{solenoid} = \pi\sqrt{\frac{\pi\mu_0 f_s \rho}{n}} \frac{Nd_{Cu}}{2} k \frac{\phi}{Nd_{Cu}}. \quad (19)$$

According to (19), the quality factor depends on N, d_{Cu} and ϕ. For N and d_{Cu}, the quality factor increases monotonically with them. For ϕ, the function -related ϕ in Q is defined as

$$G\left(\frac{\phi}{Nd_{Cu}}\right) = k\frac{\phi}{Nd_{Cu}}. \quad (20)$$

Based on Table 4 and (20), the approximation relationship between G and $\phi/(Nd_{Cu})$ is plotted in Figure 10. According to Figure 10, at the same Nd_{Cu}, increasing ϕ is beneficial for improving quality factor, Q, which causes the large volume. Unlike in planar spiral inductors, there is no optimized structure to improve the quality factor.

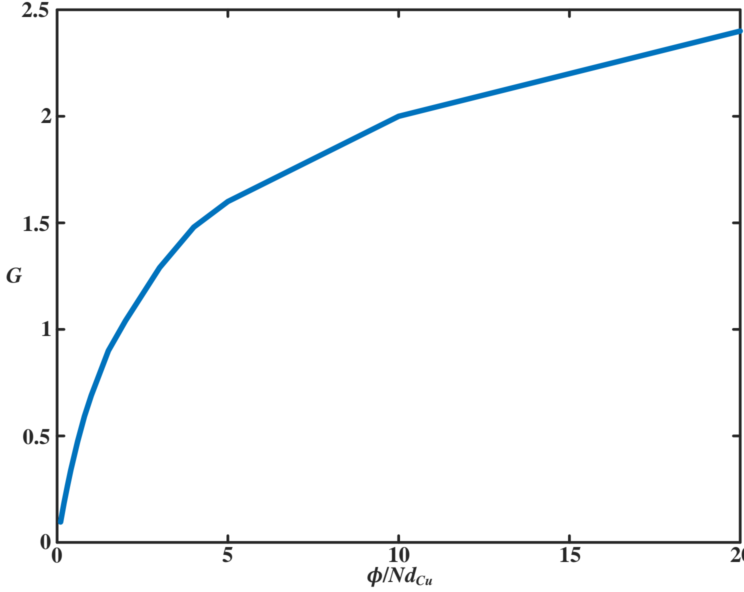

Figure 10. Approximation relationship between G and $\phi/(Nd_{Cu})$.

4. Efficiency Boundary Prediction of PSiP

Power losses of PSiPs mainly include power losses of switches and inductors. Only considering power losses of inductors and power switches, the PoL power supply efficiency is expressed as

$$\eta = \frac{P_o}{P_o + P_{ind} + P_{switch}} = \frac{1}{1 + \frac{P_{ind}}{P_o} + \frac{P_{switch}}{P_o}}, \tag{21}$$

where P_o, P_{ind} and P_{switch} are the output power, power losses of inductors and power switches, respectively.

In order to calculate the power losses of switches and inductors with the consideration of switching frequencies and power levels, V_{in} = 5 V, V_o = 1.8 V, f_s = 1~100 MHz, $\triangle i_L/I_{L0}$ = 0.4 and P_o = 0.1~10 W are used in calculations.

For the power loss of integrated Si LDMOSFETs, optimized sizes of integrated Si LDMOSFETs at 350 nm, 180 nm and 90 nm processes are calculated at different switching frequencies and output currents according to (7) and (10). The parameters of optimized integrated Si MOSFETs are given in Table 5. As the switching frequency increases, the R_{DS} of integrated Si MOSFET increases, and C_{ISS}, C_{RSS} and C_{OSS} decrease, which trades off power losses among switching loss, driving loss and conduction loss. Furthermore, based on the parameters of Si LDMOSFETs, the power losses of Si LDMOSFETs, P_{switch}, at 350 nm, 180 nm and 90 nm are shown in Figure 11a. Furthermore, the efficiency boundary, P_{switch}/P_o, is calculated as shown in Figure 11b.

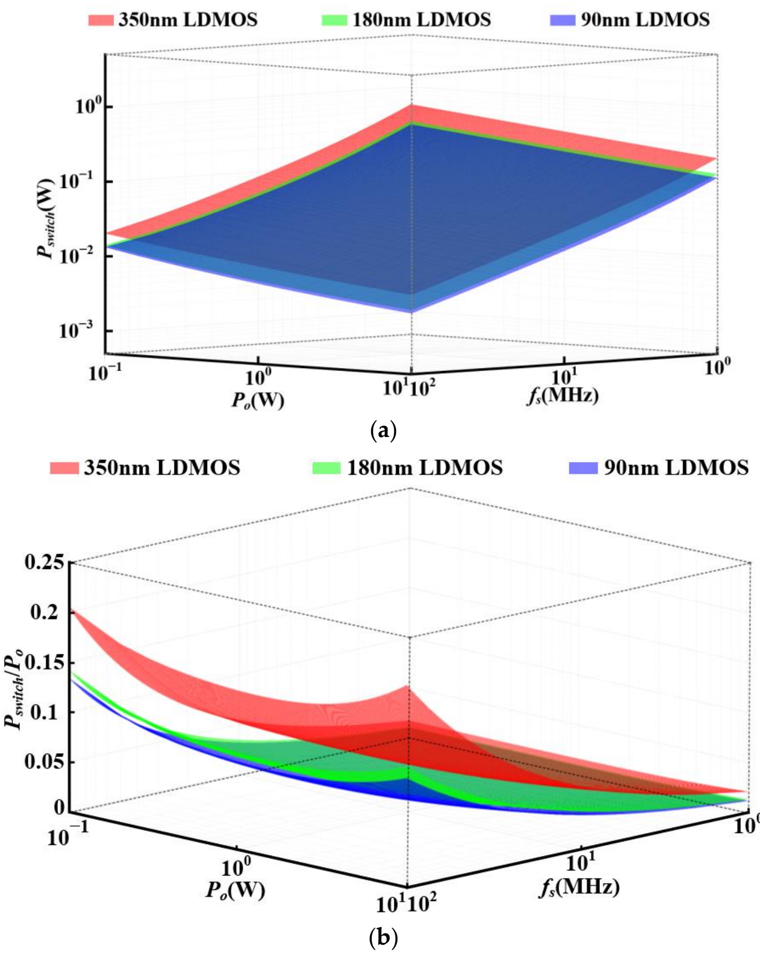

Figure 11. Power losses of switches, P_{switch} and P_{switch}/P_o, with switching frequency and power level of (**a**) P_{switch} (**b**) P_{switch}/P_o.

Table 5. Parameters of Integrated Si MOSFETS with Optimal Sizes at Different Frequencies.

Process	fs (MHz)	R_{on} (mΩ)	C_{ISS} (pF)	C_{RSS} (pF)	C_{OSS} (pF)
350 nm	1	35	295	147	355
	10	112	93	47	112
	100	354	29	15	35
180 nm	1	22	208	104	253
	10	69	66	33	80
	100	217	21	10	25
90 nm	1	18	176	88	179
	10	57	57	28	57
	100	179	17	9	18

In Figure 11a, the optimized power loss of the integrated Si LDMOSFET is proportional to ${f_s}^{1/2}$ instead of f_s, which shows the potential for high-frequency switches. As the switching frequency increases, the power loss of the integrated Si LDMOSFET increases at a rate of ${f_s}^{1/2}$. As the power level increases, the power loss of the integrated Si LDMOSFET increases at a rate of P_o. In addition, the power losses of the integrated LDMOSFEET under more advanced processes are reduced due to reductions of the parasitic capacitors and resistors.

For the power loss of air-core inductors, the required inductance value is calculated according to the switching frequency and ripple ratio of the inductance current. Then, with consideration of the optimized winding structures, the geometric parameters (D, d, ϕ) are estimated based on the inductance value according to (13) and (17). Furthermore, based on (14) and (18), the coil length is calculated according to inductance geometric shapes. Finally, based on (11), the power losses of air-core inductors, P_{ind}, with winding structure optimizations are shown in Figure 12a. Furthermore, the efficiency boundary, P_{ind}/P_o, is calculated as shown in Figure 12b. The following assumptions are introduced into the calculations according to common engineering values:

- For the tightly winding solenoid inductor, its wire width and coil turn are set as 1 mm and 10.
- For the planar spiral inductor, its thickness and coil turn are set as 100 μm and 10. Since it has a wide outside winding and narrow inside winding structure, its width is set as 1~2 mm.

In Figure 12a, as the switching frequency increases, the coil-wire length, l, and skin depth, δ, both decrease. Based on calculations, since the effect of coil-wire length reduction on power loss is greater than that of skin effect at 1~100 MHz, the power losses of air-core inductors decrease as the switching frequency increases. As the power level increases, the inductance current, I_L, and ripple, $\triangle i_L$, increase. The increase of $\triangle i_L$ results in reductions of inductance, L, and coil-wire length, l. Therefore, the power losses of air-core inductors are at the minimum value as the power level increases.

Combined with power loss calculations, P_{switch}/P_o and P_{ind}/P_o are shown in Figures 11b and 12b. It can be seen that the main power losses at low and high frequencies are from switches and inductors, respectively. Therefore, the directions of further reduction of power losses at low frequency and high frequency are different. At low frequency, the sizes of air-core inductors are slightly increased to reduce their DC and AC resistance values. At high frequency, advanced processes are applied to reduce the parasitic capacitance values of Si LDMOSFETs. According to the above analysis, for reducing power loss to improve switching frequency, PSiPs need to optimize the size of the integrated Si MOSFET in advanced processes and optimize the winding structure of air-core inductors. At a high enough switching frequency, air-core inductors are integrated in the chip, which represents the trend from PSiP to PwrSoC. Reducing power loss is also a heat dissipation requirement for the highly integrated PwrSoC package.

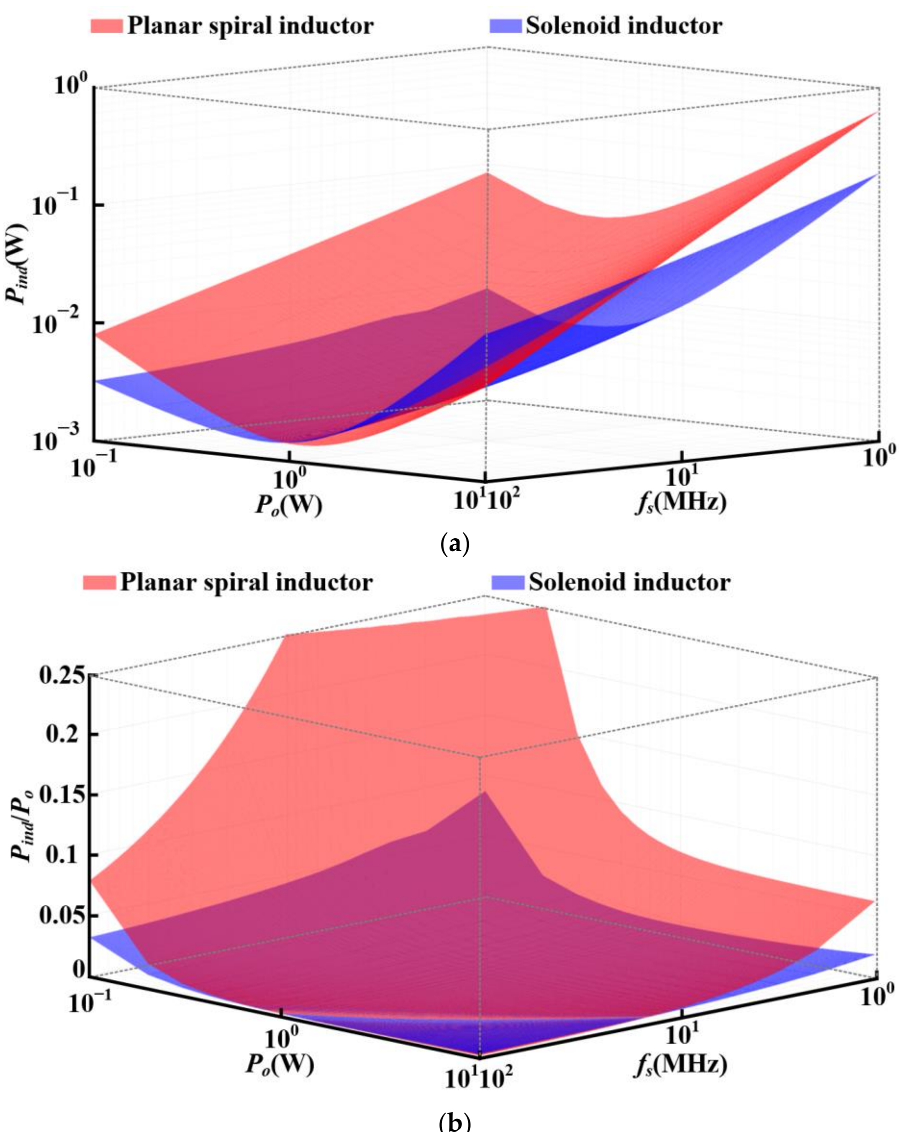

Figure 12. Power losses of inductors, P_{ind} and P_{ind}/P_o, with switching frequency and power level of (**a**) P_{ind} (**b**) P_{ind}/P_o.

According to Figures 11b and 12b, the efficiency boundaries of PSiPs are predicted and verified in Figure 13 [42–61]. In order to eliminate the effect of input and output voltages on efficiency, the efficiencies in the literature are normalized according to the following:

$$\eta_{st} = \frac{P_o}{P_o + (P_{ind} + P_{switch}) \cdot \frac{V_{out}}{V_{in}} \cdot \frac{5\text{V}}{1.8\text{V}}} = \frac{\eta}{\eta + (1-\eta) \cdot \frac{V_{out}}{V_{in}} \cdot \frac{5\text{V}}{1.8\text{V}}}, \quad (22)$$

where η_{st} and η are efficiencies with and without normalization.

In Figure 13, the efficiencies found in state-of-the-art research are lower than those of the predicted efficiency boundary, and most of them are close to the boundary, which verifies the prediction based on the power loss analysis. The predicted errors are mainly from power losses of the equivalent series resistor and controller. The above optimized measures reduce power losses and improve efficiency, which provides roadmaps for achieving high-frequency PSiPs.

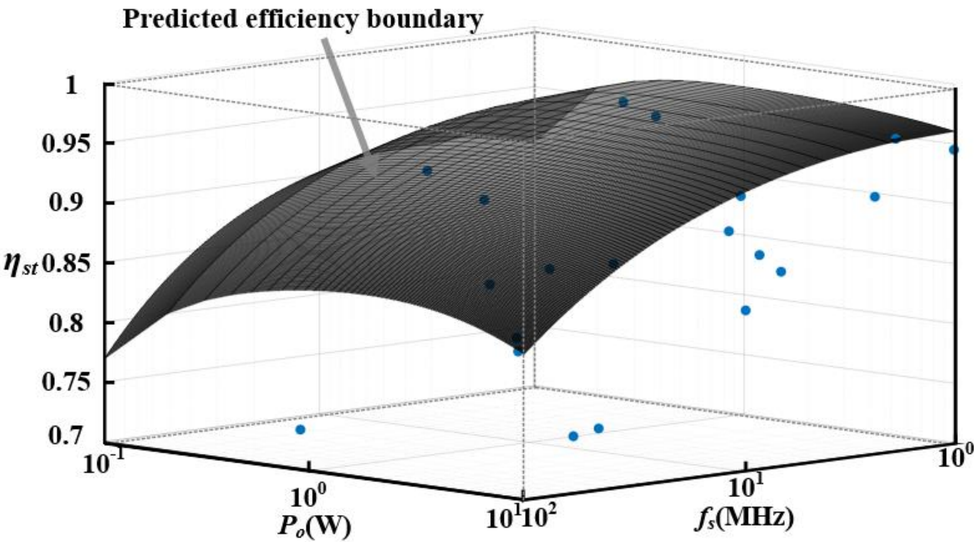

Figure 13. Prediction and verification of the efficiency boundary [42–61].

5. Conclusions

This paper provides power loss optimizations for PSiPs in relation to integrated Si LDMOSFETs and air-core inductors. For integrated Si LDMOSFETs, a size and parallel quantity optimization is provided based on power loss analyzation. For air-core inductors, quality factors are improved by winding structure optimization to reduce coil loss. The power losses of the integrated Si LDMOSFET and air-core inductor are both reduced to less than 10% of the output power at 1~100 MHz switching frequency and 0.1~10 W power level. Based on the analysis, this paper predicts the efficiency boundary of PSiPs. The efficiency prediction error is 1~15% at 1~100 MHz switching frequency and 0.1~10 W power level. The predicted results are consistent with the findings of state-of-the-art research. To improve the efficiency toward high-frequency PSiP, two technologies are proposed from the perspective of switches and inductors.

- For power switches, a parallel quantity of integrated Si LDMOSFET is designed based on power level. The size of each power switch is optimized based on switching frequency and power level.
- For power inductors, the planar spiral inductor provides a low profile for monolithic integration. An optimal winding structure with narrow inner and wider outer windings dramatically reduces power losses.

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Nomenclature

f_s	Switching frequency
V_{in}	Input voltage of PoL power supply
V_{out}	Output voltage of PoL power supply
I_{L0}, I_{Ln}	DC value and nth harmonic amplitude of inductance current
Δi_L	Ripple of inductance current
I_o	Load current of PoL power supply
C_{GD}	Capacitance between gate and drain of integrated Si LDMOSFT
C_{GS}	Capacitance between gate and source of integrated Si LDMOSFT
C_{DS}	Capacitance between drain and source of integrated Si LDMOSFT
C_{ISS}	Input capacitance of integrated Si LDMOSFET
C_{OSS}	Output capacitance of integrated Si LDMOSFET
C_{RSS}	Reverse transfer capacitance of integrated Si LDMOSFET
R_G	Gate resistance of integrated Si LDMOSFET
R_{on}	Drain-source on-resistance of integrated Si LDMOSFET
V_{DS}	Drain and source voltage of integrated Si LDMOSFT
V_{GS}	Gate and source voltage of integrated Si LDMOSFT
I_{DS}	Drain and source current of integrated Si LDMOSFT
V_{PL}	Miller voltage of integrated Si LDMOSFT
V_{th}	Gate threshold voltage of integrated Si LDMOSFT
V_{DD}	Power supply voltage of driver
m_n	Electron mobility
W_M	Channel width of integrated Si LDMOSFET
L_M	Channel length of integrated Si LDMOSFET
E_M	Drain/source width of integrated Si LDMOSFET
C_{ox}	Gate oxide capacitance per unit area of integrated Si LDMOSFET
C_{ov}	Gate-to-source/drain overlap capacitance per unit width of integrated Si LDMOSFET
C_j	Source/drain junction capacitance per unit area of integrated Si LDMOSFET
C_{jsw}	Source/drain sidewall junction capacitance per unit length of integrated Si LDMOSFET
L	Inductance value
l	Coil-wire length of inductor
A, φ	Cross-section area and perimeter of inductance coil-wire
μ_0	Space permeability
ρ	Resistivity of inductance coil-wire material
δ_n	Skin depth of nth harmonic inductance current
R_{DC}, $R_{AC,n}$	DC and nth harmonic AC equivalent resistances of inductor

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