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FPGA-Based Frequency Tracking Strategy with High-Accuracy for Wireless Power Transmission Systems

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Abstract: Aiming at the problem of the unavoidable phase-tracking error of the wireless power transfer (WPT) system caused by dead time, MOSFET drive and other factors, this paper proposes a frequency-tracking method with high accuracy based on a Field-Programmable Gate Array (FPGA) to track the current and voltage phase differences on the transmitting side. Compared with fixed-phase systems, the proposed method accurately controls the phase difference between voltage and current. It detects the phase difference in real time and adjusts the phase compensation angle dynamically to ensure that the system always operates under the optimal zero-voltage switching (ZVS) state, which reduces system loss. Experiments under operating conditions of varying transmission distances and load resistance values are carried out on a prototype. The experimental results show that the proposed method achieves a desired phase difference of 11.5° under the conditions of varying transmission distances and load resistance values, which meets the expectation of a phase difference between 10.5° and 13° to achieve ZVS. Within the range of over-coupling conditions, the output power and transmission efficiency of the WPT system are more significantly improved than those of the fixed-frequency system, which verifies the feasibility of the proposed method.

Keywords: wireless power transfer; frequency tracking; phase difference control; zero voltage switching

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1. Introduction

Wireless power transmission (WPT) technology is a power transmission mode that can transfer power to electric equipment without any tangible media contact. Due to its non-contact, safety, and flexibility advantages, WPT technology is often widely used in new energy electric vehicles, aerospace, smart homes, medical equipment, and other fields [1–6]. When the wireless power transmission system is under a resonating state, the transmission efficiency of electric energy is the highest. In practical work, the WPT system is a complex nonlinear system The stability of the system will be affected by multiple parameters, and a change in parameters will lead to the phenomenon of frequency detuning, which will lower the transmission efficiency of the system [7–9]. The literature [10–12] shows that frequency splitting will occur when the system works under over-coupling conditions, which will interfere with frequency-tracking technology and affect output power and transmission efficiency.

In order to avoid system detuning and improve transmission power and efficiency, there are mainly two methods: automatic tuning technology and frequency-tracking technology. Automatic tuning technology solves the problem of frequency detuning by automatically matching new compensation capacitors [13,14] with inductors [15,16]. This method regulates the operating frequency discontinuously and with low accuracy. Frequency-tracking technology tracks the resonating frequency by adjusting the switching frequency of the inverter circuit. This method has become a hot research model because of its fast response and high regulation accuracy.

In [17], an analogue phase-locked loop (PLL) was used to achieve frequency tracking. However, the analogue PLL circuit design is complex, the anti-noise performance is poor, and the phase lock range is narrow. Another study [18] proposed a frequency-tracking strategy for low-frequency WPT systems, which can improve transmission efficiency by varying the pulse width modulation frequency (PWM) and does not require communication between the transmitter and receiver. The authors of [19] proposed a natural frequency-tracking method by tracking the natural damping frequency of the resonating circuit, which can eliminate the detuning effect caused by static and transient changes in the system. However, this control is unstable, and there is always an error between the natural damping frequency and the resonating frequency. In [20], a frequency-tracking method using a PLL under coil offset conditions is presented, which has a phase difference between the load current at the receiver side and the inverter output voltage at the transmitter side for tracking and continuously reducing. Further, the study in [21] adopts a detuning control strategy of differential PLL to track the system's resonating frequency, reducing the WPT system's power fluctuation. The system works at a reasonable detuning rate by controlling the angle difference and realizes zero-voltage switching (ZVS).

Other studies [22,23] adopted a frequency-tracking control method based on the maximum received voltage, which monitors the voltage at the receiver and adjusts the transmitter source frequency based on the voltage's feedback information. However, this frequency-tracking method has poor accuracy and does not consider the system ZVS. In [24], a hybrid control method was proposed based on PLL frequency tracking control and dynamic compensation tuning. The system keeps frequency splitting from occurring by changing the capacitance. The operating frequency of the inverter circuit is the resonating frequency by precise tuning through frequency tracking. It is difficult to achieve continuous adjustment of capacitor parameters with this method, it has poor regulation accuracy and does not achieve ZVS, and the inverter output voltage spikes. The study in [25] achieved a resonating state that can follow frequency splitting by tracking the current at the receiver side. A fixed compensation of the phase difference achieves the ZVS. It is not considered that the phase difference will change, and fixed compensation cannot make the system always maintain a reasonable ZVS.

The above analysis shows that the existing methods have no closed-loop control of the phase difference. It is difficult to maintain the system under the optimal ZVS state at all times with the compensation of the fixed phase angle when there are large fluctuations in the phase difference. This paper proposes a frequency-tracking method based on FPGA to accurately track the phase difference and solve the above problems. The method achieves accurate control of the phase difference of the system by closed-loop control of the phase difference to make it into an optimal state, which enables the system to achieve an excellent ZVS characteristic and ensure the system reactive power loss remains at a low level. Section 2 presents equivalent modeling of the WPT system and analyzes the effects of frequency detuning, frequency splitting, and phase differences on the system. Section 3 proposes an FPGA-based frequency-tracking method to track phase differences and describes the composition and working principle of the method. Section 4 verifies the feasibility of the method through experiments. Section 5 concludes the paper,

2. WPT System Coupling Circuit Model

2.1. Coupled Circuit Model

This paper adopts a series-series (SS) compensation topology with a simple structure, a straightforward analysis, and a good power transmission effect at a short distance. Figure 1 shows the coupled circuit model. In the figure, L_1 and L_2 are the self-inductance of the transmitting and the receiving coils, C_1 and C_2 are the compensation capacitors of the transmitting and receiving terminals, R_1 and R_2 are the internal resistances of the two coils, M is the mutual inductance of the two coils, and R_L is the load resistance.

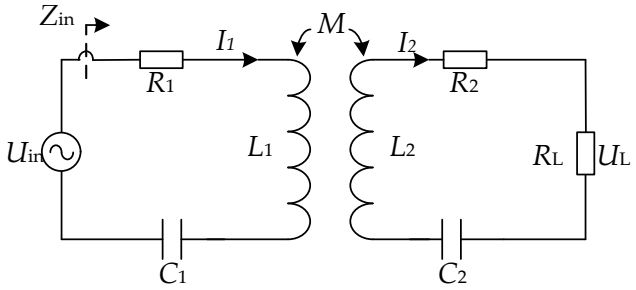


Figure 1. SS-type topology coupled circuit model.

The equivalent impedance in the transmitter loop, the equivalent impedance in the receiver loop, and the total input impedance of the system are as follows:

$$\begin{cases} Z_1 = R_1 + j\omega L_1 + \frac{1}{j\omega C_1} \\ Z_2 = R_2 + R_L + j\omega L_2 + \frac{1}{j\omega C_2} \\ Z_{\text{in}} = Z_1 + \frac{(\omega M)^2}{Z_2} \end{cases} \tag{1}$$

Writing the KVL equation based on the circuit model in Figure 1 yields:

$$\begin{cases} Z_1 I_1 - j\omega M I_2 = U_{\text{in}} \\ j\omega M I_1 - I_2 Z_2 = 0 \end{cases} \tag{2}$$

From the equation, the current in the two coil loops is:

$$\begin{cases} I_1 = \frac{Z_2 U_{\text{in}}}{Z_1 Z_2 + \omega^2 M^2} \\ I_2 = \frac{j\omega M U_{\text{in}}}{Z_1 Z_2 + \omega^2 M^2} \end{cases} \tag{3}$$

The output power P_{out} obtained from Equation (3) is:

$$P_{\text{out}} = |I_2|^2 R_{\text{L}} = \frac{(\omega M)^2 R_{\text{L}} U_{\text{in}}}{\left| Z_1 Z_2 + (\omega M)^2 \right|^2} \tag{4}$$

The transmission efficiency η is:

$$\eta = \frac{(\omega M)^2 R_{\text{L}}}{\left| Z_2 [Z_1 Z_2 + (\omega M)^2] \right|} \times 100\% \tag{5}$$

The resonating state frequency of the system under ideal conditions is:

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_1}} = \frac{1}{2\pi\sqrt{L_2 C_2}} \tag{6}$$

In this case, the total input equivalent impedance Z_{in} of the system is the minimum, the voltage and current phase angle φ of the transmitter is 0, and the power efficiency transmission is the maximum.

The phase difference φ calculated from the input impedance Z_{in} of the system is:

$$\varphi = \arctan\left[\frac{-\omega^2 M^2 X_2 + X_1 \left[(R_2 + R_{\text{L}})^2 + X_2^2 \right]}{\omega^2 M^2 (R_2 + R_{\text{L}}) + R_1 \left[(R_2 + R_{\text{L}})^2 + X_2^2 \right]} \right] \tag{7}$$

In the above equation, $X_1 = \omega L_1 - 1/\omega C_1$; $X_2 = \omega L_2 - 1/\omega C_2$.

2.2. System Frequency Splitting Analysis

The frequency of the wireless power transmission systems splits under different operating conditions. The critical value of frequency splitting is $\omega M = R_S = R_2 + R_L$ [10,12], and R_S is the sum of the internal resistance of the receiver coil and the load resistance. When $\omega M < R_S$, the system operates under under-coupling conditions, and frequency splitting does not occur. When $\omega M = R_S$, the system operates under critical coupling conditions. When $\omega M > R_S$, the frequency-splitting phenomenon will appear when the system operates under an over-coupling condition.

Figure 2 shows the relationship between the operating frequency of the system, the transmission efficiency, and the output power when the frequency splitting phenomenon occurs, as obtained from Equations (4) and (5). In the figure, splitting occurs at both the output power and transmission efficiency. The maximum output power obtains at the splitting point, and the maximum transmission efficiency obtains at the resonance point.

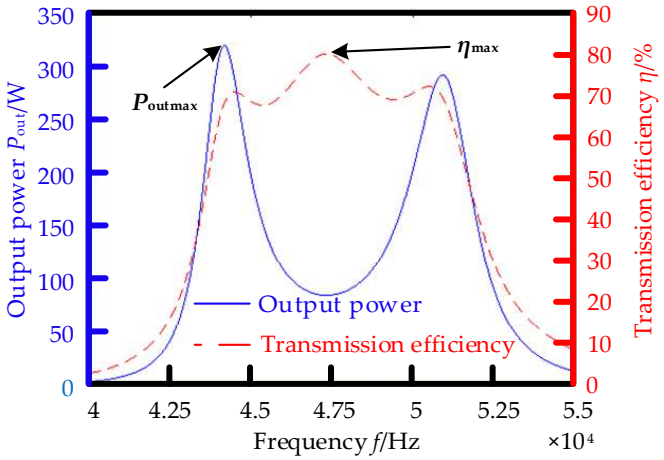


Figure 2. Relation curves of system frequency with transmission efficiency and output power when frequency splitting occurs.

The relationship between the phase difference φ and the operating frequency f is obtained from Equation (7), as shown in Figure 3. The coil distance is fixed. When the load R_L value is large, the system is under an under-coupled state, no frequency splitting occurs, and there is only a zero point at the resonating frequency. When the load R_L value is small, the system over-couples, and frequency splitting occurs. There are three zeros at the resonating frequency and two frequency splitting points. The resistance value is fixed. The frequency splits when the coil distance is close; the frequency does not split when the coil is far away. Since the PLL-based frequency-tracking technique tracks the zero point, the frequency splitting makes the frequency-tracking technique track the frequency of the splitting point rather than the resonating frequency.

The above analysis shows that the frequency splitting of the system has a significant impact on the output power and a negligible impact on the transmission efficiency. It also affects the input phase angle of the transmitter, which further affects the nature of the system and makes the frequency tracking follow the frequency that is not the resonating frequency.

2.3. System Frequency Detuning State Analysis

In the actual design of the experimental platform, due to the design error of the coil inductance and resonant capacitance values and the influence of environmental changes, the component parameter values change. It is challenging to keep the system transmitter and receiver circuits under resonance. Regardless of operating at any fixed frequency, the system does not resonate all the time, which leads to system frequency detuning.

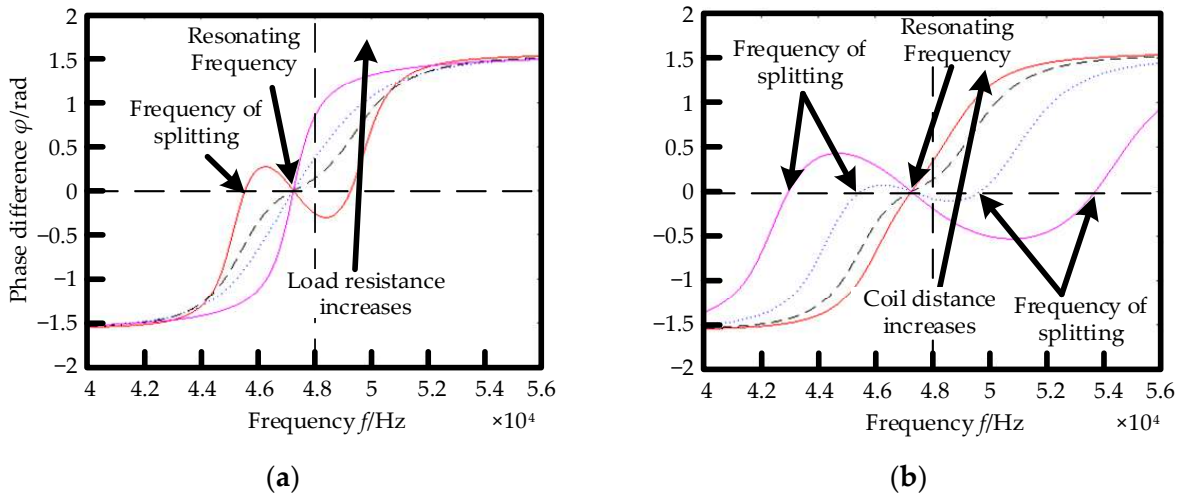


Figure 3. The relationship between the phase difference and operating frequency: (**a**) distance fixed, resistance increases; (**b**) resistance fixed, distance increases.

In order to further analyze the effect of frequency detuning on output power, transmission efficiency, and phase difference, the circuit model parameters of Figure 1 are brought into Equations (4), (5), and (7) for analysis. The coupling coils are $L_1 = L_2 = 275$ μH, the compensation capacitors are $C_1 = C_2 = 40$ nF, and the resonating frequency is 48 kHz. Considering the error of design parameters and the influence of the environment, it is assumed that the coil inductance of the transceiver shifts to 279 μH and 280 μH, and the compensation capacitance shifts to 41 nF and 40.5 nF. On this basis, the effects of different operating frequencies are investigated.

Figure 4 shows the operating frequency versus transmission efficiency and output power for a system without the splitting phenomenon. The maximum output power of the system is 46.9 kHz, which deviates from the designed resonant frequency. The maximum efficiency is 47.1 kHz, which is close to the maximum output power. The power and efficiency at the fixed frequency of 48 kHz decline significantly.

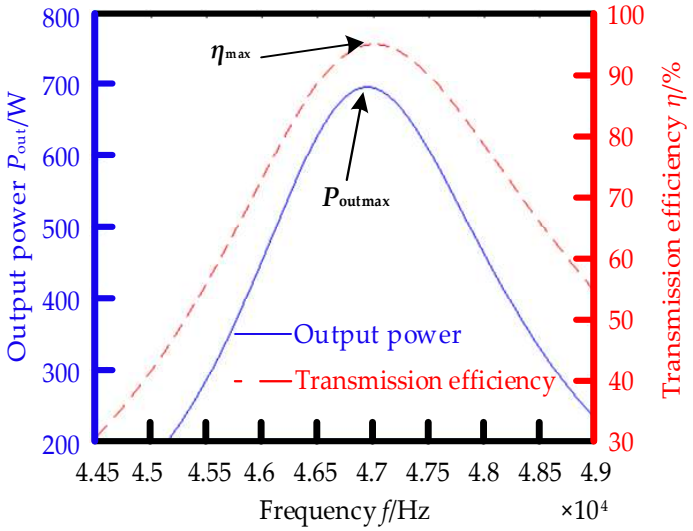


Figure 4. Relation curve of system frequency with transmission efficiency and output power when there is no frequency splitting.

In Figure 3, the change in load and coil distance causes a change in the phase difference when the system frequency is detuned. As the load changes from small to large and from near to far, the phase difference changes from less than 0° to more than 0°, and the system

changes from capacitive to inductive. When the coil is too close, or the load is too small, the phase difference is smaller, and the system becomes more capacitive. When the coil is too far away, or the load is too large, the phase difference increases, and the system becomes more inductive.

The frequency detuning phenomenon will reduce the output power and transmission efficiency of the system and make it possible for the system to work under a capacitive state, increasing the loss and insecurity of the system.

2.4. Effect of Phase Difference on the System

Figure 5 shows the transmitter side's current and voltage waveforms under the system's capacitive state. In the figure, when the system operates in a capacitive state, the inverter output voltage will produce large spikes and have reversed polarity, increasing the possibility of damaging the switching tubes. In order to avoid the above phenomenon, the system works at ZVS by using frequency-tracking technology.

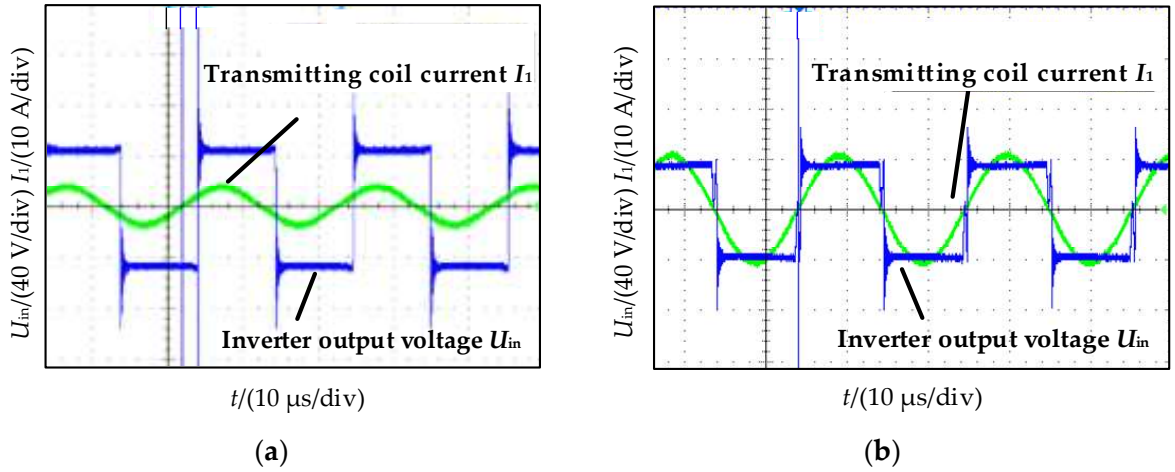


Figure 5. Voltage and current waveforms when the system is capacitive: (**a**) R_L = 5 Ω, coil distance of 25 cm; (**b**) R_L = 15 Ω, coil distance of 15 cm.

The frequency-tracking method usually tracks the transmitter's current to achieve the same frequency and phase voltage of the inverter output. In practice, the signal delays are due to the acquisition circuit, the over-zero comparison circuit, the dead zone, and the inverter diver module. As a result, the generated voltage will lag behind the current, so the phase angle of the collected current signal needs to be compensated for. Furthermore, different coils, coil distances, and load variations will have some effect on the phase angle, so using a fixed phase angle compensation is not reliable.

In order to solve the impact of the phase lag on the frequency tracking and the system in the above problems, this paper proposes a frequency-tracking method based on FPGA to track the phase difference accurately. This method fixes the phase difference between voltage and current through feedback control of the phase difference. The system always works under the optimal ZVS state, increasing the system's output power and transmission frequency.

3. Frequency-Tracking Control System

3.1. Frequency-Tracking System Design

Figure 6 shows a block diagram of the frequency-tracking control proposed in this paper. It mainly consists of a voltage acquisition circuit, a current acquisition circuit, over-zero comparisons, a digital phase locked loop, a frequency measurement module, a dead zone, and an inverter drive module.

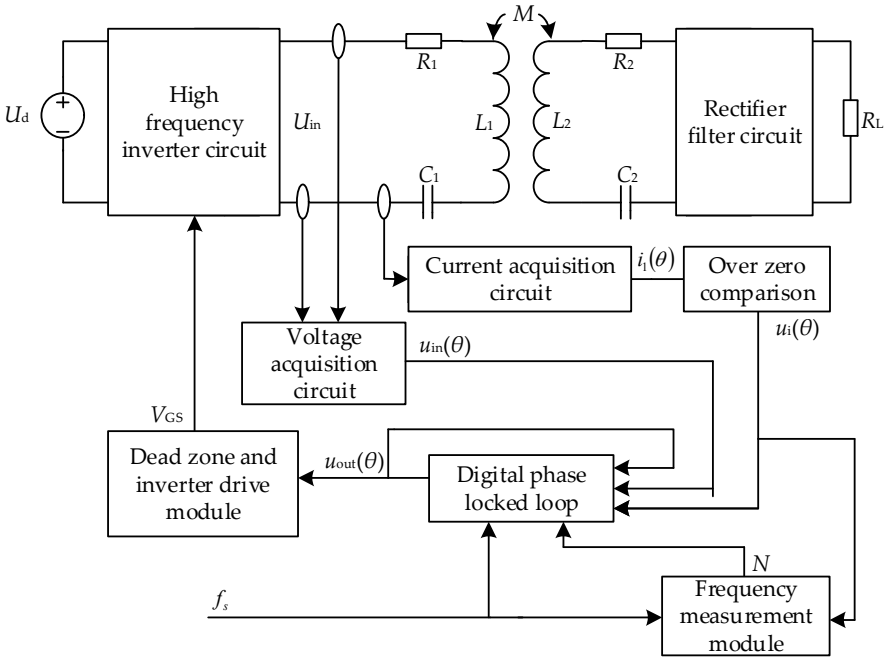


Figure 6. Block diagram of the frequency-tracking system control.

In Figure 6, the current acquisition circuit collects the current $i_1(\theta)$ in the emitter loop. The voltage acquisition circuit acquires the system's input voltage $u_{in}(\theta)$. The over-zero comparison circuit converts the collected current $i_1(\theta)$ into a square wave signal $u_i(\theta)$ of the same frequency and phase. The phase-locked loop module tracks the real-time input signal $u_i(\theta)$ frequency and regulates the output signal $u_{out}(\theta)$ frequency and phase angle. It should be ensured that the system is always under a resonating state and has a fixed input phase angle transmitting side. The frequency measurement module obtains the relationship value N between the frequency of the $u_i(\theta)$ signal and the system clock frequency f_s in real-time. The dead time and inverter drive module convert the received $u_{out}(\theta)$ signal into a drive signal V_{GS} with dead time. The V_{GS} signal drives the high-frequency inverter circuit to output the voltage signal $u_{in}(\theta)$.

Figure 7 is a control strategy block diagram of the digital PLL module in Figure 6. It consists of a digital phase discriminator, digital loop filter, increase or decrease pulse counter, dynamic frequency divider module, frequency measurement module, dynamic phase control module, and phase compensation module.

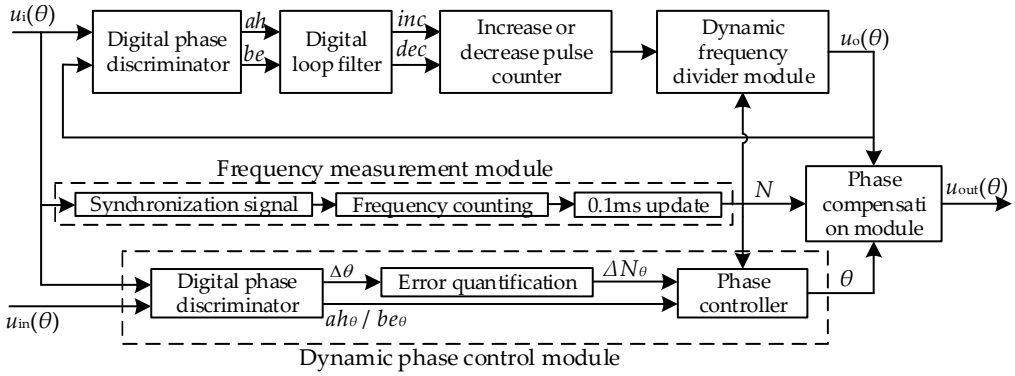


Figure 7. Block diagram of frequency-tracking control strategy based on transmitter current and voltage–current phase difference.

The digital phase discriminator performs a phase comparison between the input signal $u_i(\theta)$ and the signal $u_o(\theta)$ fed back from the dynamic divider module. The phase lead signal

ah is high when the signal $u_o(\theta)$ is ahead of the signal $u_i(\theta)$, and the phase lag signal *be* is high when it lags behind.

The function of the digital loop filter is to filter out the interference of noise and burr during the transmission of digital signals. It consists of two parts: an add and a subtract counter. The *ah* signal is high, and the add counter begins to count. When the count is equal to the set value, the emptying counter and the carry signal *inc* is output. The *be* signal is high, and the subtract counter begins to count. When the count value is 0, the count value is reassigned, and the borrow signal *dec* is output.

When the *inc* or *dec* signal is not received, the increase or decrease pulse counter will divide the system clock by two. When the *inc* signal is received, the pulse of the output signal increases. When the *dec* signal is received, the pulse of the output signal decreases. This ensures that the phase difference between the output signal and the signal $u_i(\theta)$ is zero and completes the phase-locking process.

The dynamic frequency divider module divides the frequency of the received signal, and the output signal $u_o(\theta)$ feeds back to the digital phase discriminator. The signal $u_o(\theta)$ frequency is determined by the received frequency division factor N.

The frequency measurement module consists of a synchronization signal, frequency counting, and 0.1 ms update. Synchronous signal processing eliminates the glitch generated by the input signal in the hopping process and solves the content and risk problems caused by delay and combination logic. Frequency counting is counting the collected current signal $u_i(\theta)$ and obtaining the relationship between the current frequency and the system clock. The 0.1 ms update records the count N that appears most frequently within 0.1 ms and outputs it to other modules.

The dynamic phase control module consists of a digital phase discriminator, error quantization, and a phase controller. The digital phase discriminator compares the phase of difference between the voltage and the current at the transmitting side and outputs the phase difference and the phase lead signal ah_θ or phase lag signal be_θ. The error quantization is to determine different count values ΔN_θ according to the phase difference. The phase controller selects the output angle θ by comparing the set values. Compare the count value of phase difference ΔN_θ with the internal set value $E_{min} = 10.5^\circ \times N/360^\circ$, $E_{max} = 13^\circ \times N/360^\circ$. Generate *model* = 10 when $\Delta N_\theta > E_{max}$ and the leads signal ah_θ is high. Generate *model* =01 when $E_{min} < \Delta N_\theta < E_{max}$ and the lead signal ah_θ is high. Generate *model* = 00 when $\Delta N_\theta < E_{min}$ or when the phase lag signal be_θ is high. The phase control module determines the size of the output compensation angle θ according to the value of the internally generated *model*. Output $\theta = \theta + 1$ when *model* = 00. Output $\theta = \theta$ when *model* = 01. Output $\theta = \theta - 1$ when *model* = 10.

The phase compensation module consists of two counters. Counter one is used to delay the output signal $u_o(\theta)$ of the dynamic voltage divider module. Counter one starts counting when it detects that $u_o(\theta)$ is low, and the count value is $N - \theta \times N/180$. The phase compensation module output $u_{out}(\theta)$ goes high, and counter two starts counting when the count value is complete. Counter two ensures that the frequency of the module output is the same as the input frequency. The output $u_{out}(\theta)$ goes low when the counter counts to N. This way, phase compensation of the received $u_o(\theta)$ signal is achieved. Let the output signal $u_{out}(\theta)$ overtake the signal $u_o(\theta)$ by θ degrees to further control the phase difference of the current and voltage at the transmitter.

3.2. Simulation Analysis

The control chip of this system adopts FPGA, whose main advantage is that it is stable and has very low latency. It can quickly respond to a change in phase difference and precisely realize control of the phase difference. First, the analysis and design of each module of the frequency-tracking control method is based on Section 3.1. Then, the corresponding code is written in the Verilog language. Finally, the RTL top-level view of the frequency-tracking control system of this paper is compiled in Quartus-II and shown in Figure 8.

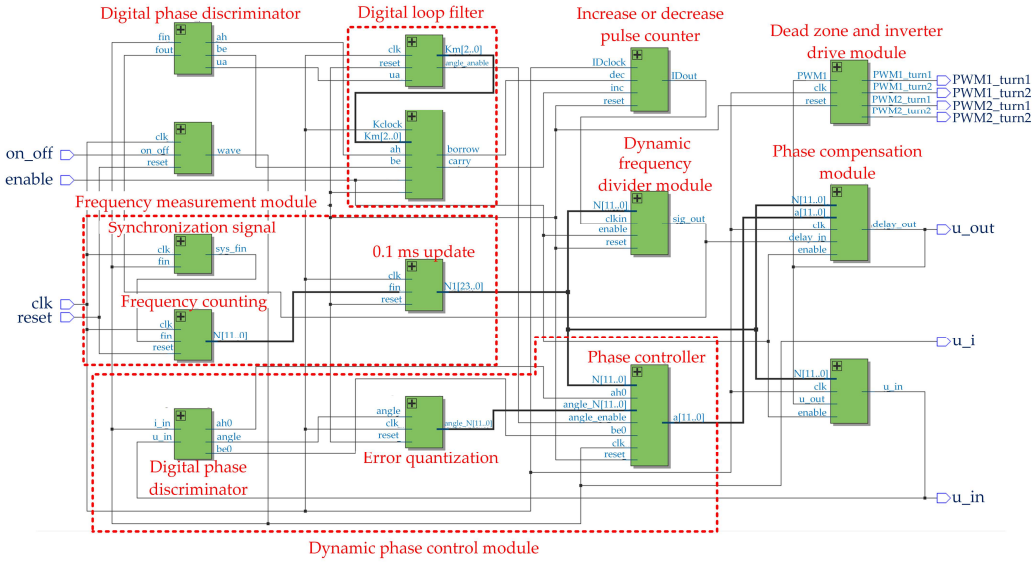


Figure 8. RTL top-level view of the frequency-tracking control system.

The digital phase-locked loop is simulated in ModelSim software. When the system clock is at 50 MHz, and the input signal frequency of the digital phase-locked loop is 48 kHz, the simulation waveform of the digital phase-locked loop is shown in Figure 9. The simulation shows that when the input signal frequency is 48 kHz, the output signal can follow the input signal after 13 cycles, and the phase locking is achieved.

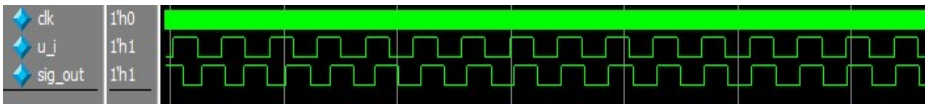


Figure 9. Function simulation diagram of digital phase-locked loop.

Figure 10 shows the waveform of the input signal frequency of the digital phase-locked loop. In the figure, after the input signal frequency jumps from 48 kHz to 30 kHz, the output signal of the digital phase-locked loop will follow the input signal again in the seventh input cycle to achieve phase locking. The simulation results show that the all-digital phase-locked loop designed in this paper meets the expected goals and has the advantages of a fast phase-locking speed and high precision.

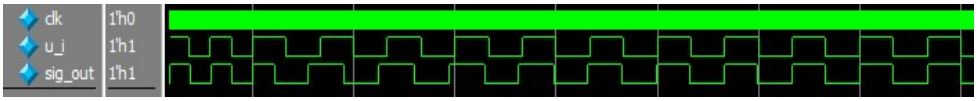


Figure 10. Input signal frequency hopping.

Figure 11 is the simulation waveform of the frequency-tracking control experiment, where u_in is the voltage waveform in the WPT system, u_i is the current waveform, and u_out is the waveform output by the frequency-tracking control circuit. The phase difference of the voltage and the current in the first two cycles has been locked, the voltage is ahead of the current, and the system is inductive. In the third cycle, the phase difference jump causes the impedance angle to decrease to close to 0°. After 12 cycles, the system impedance angle will be locked again to the previous degree. The simulation results show that the impedance angle of the frequency-tracking control method proposed in this paper is fixed, and the system is always under the ZVS state.

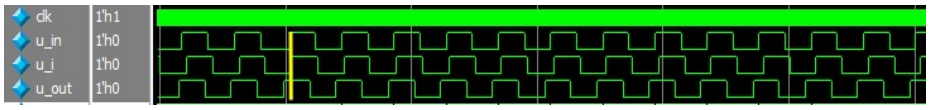


Figure 11. Simulation waveform of frequency-tracking control experiment.

4. Experimental Verification

4.1. Experimental Platform

In order to verify the feasibility of the above frequency-tracking control method, Figure 12 is used as an experimental platform for WPT system design. The experimental platform mainly consists of a high-frequency power supply, a transceiver coil, an oscilloscope, current probes, a rectifier circuit, and an electronic load. Built into the high-frequency power supply are current and voltage acquisition circuits. The FPGA chip controls the output voltage frequency of the power supply; the operating frequency is 48 kHz at a fixed frequency. Table 1 shows the circuit parameters of the platform.

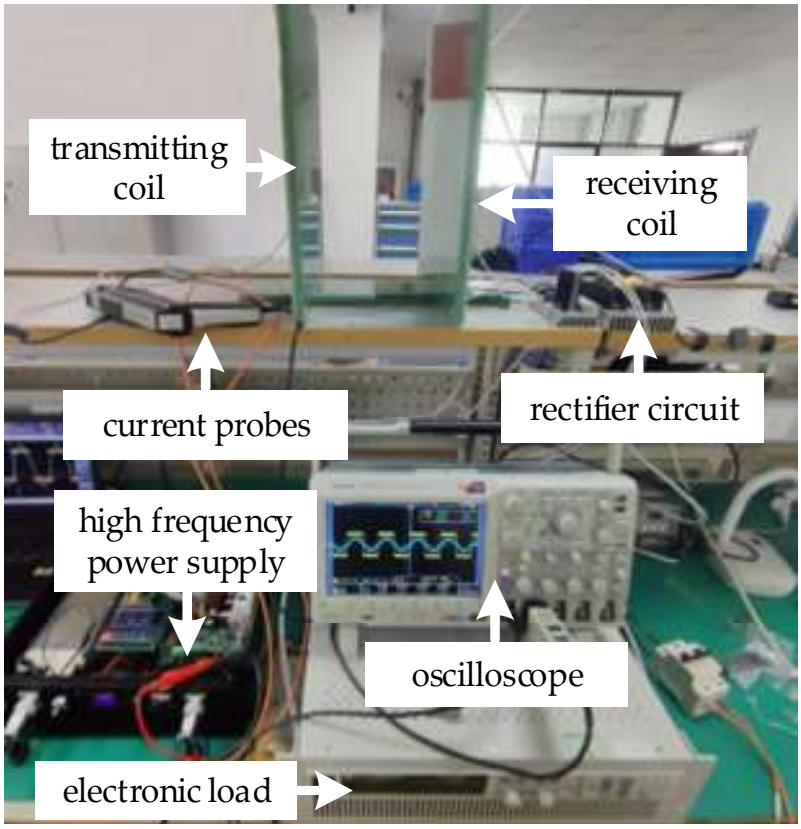


Figure 12. WPT system experimental platform.

Table 1. Main parameters of WPT system.

Parameters	Symbol	Value
transmitting coil self-inductance	L_1	275 μH
receiving coil self-inductance	L_2	275 μH
transmitter compensation capacitance	C_1	40 nF
receiver compensation capacitance	C_2	40 nF
internal resistance of transmitting coil	R_1	0.18 Ω
internal resistance of receiving coil	R_2	0.16 Ω
inherent resonating frequency	f_0	48 kHz

4.2. Fixed-Frequency Mode Experiment

In fixed-frequency mode, a fixed coil spacing of 24 cm is used. A phase diagram of the voltage and current at the emitter when the load R_L is 5 Ω and 15 Ω, respectively, is shown in Figure 13. At R_L = 5 Ω, the voltage lags behind the current by 12.12°, and the system is capacitive at this time. At R_L = 15 Ω, the voltage leads the current by 19.04°, and the system is inductive at this time.

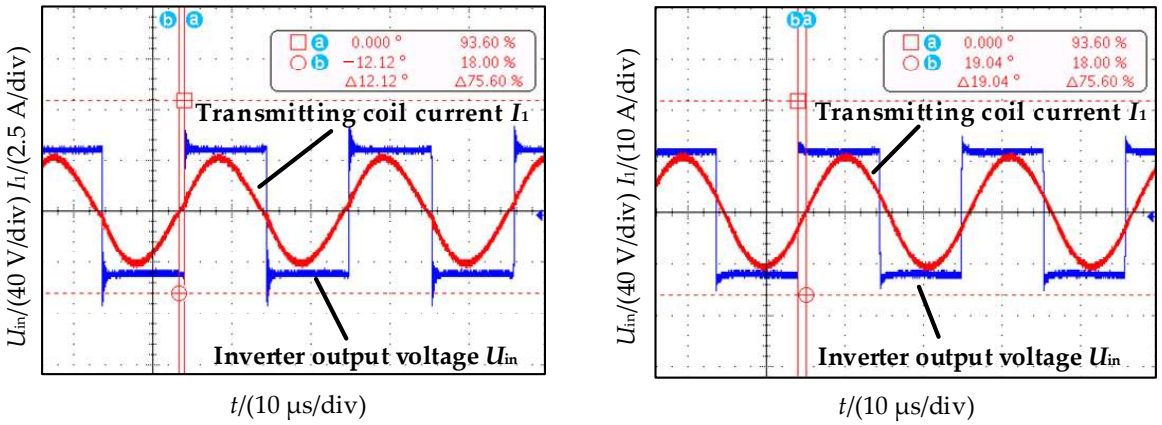


Figure 13. The coil distance is 24 cm, the voltage and current phase diagram of the transmitter: (**a**) R_L = 5 Ω; (**b**) R_L = 15 Ω.

Figure 14 shows the phase diagram of the voltage and current at the emitter when the load R_L = 7 Ω. When the coil distance is 18 cm, the voltage lags behind the current by 10.38°, and the system is weakly capacitive. When the coil distance is 28 cm, the voltage leads the current by 15.65°, and the system is inductive.

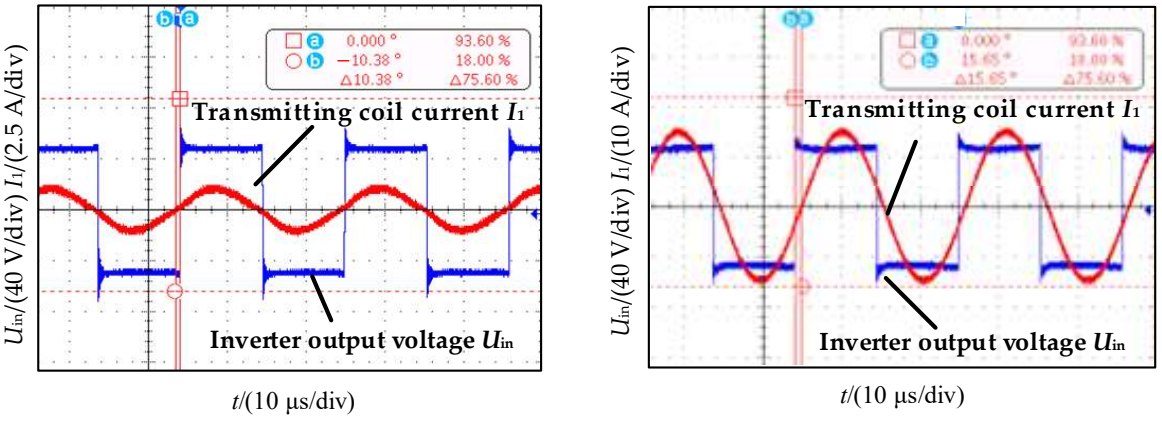


Figure 14. R_L = 7 Ω, voltage and current phase diagram of transmitter: (**a**) coil distance of 18 cm; (**b**) coil distance of 28 cm.

From the amount of frequency detuning and the analysis of the waveforms in Figures 13 and 14 above, the actual resonant frequency of the system inferred should be less than 48 kHz.

4.3. Frequency-Tracking Experiment

Keeping the experimental conditions consistent with Section 4.2, the frequency-tracking method based on the FPGA tracking input phase difference proposed in this paper is used for the experiments. Figure 15 shows the experimental waveforms.

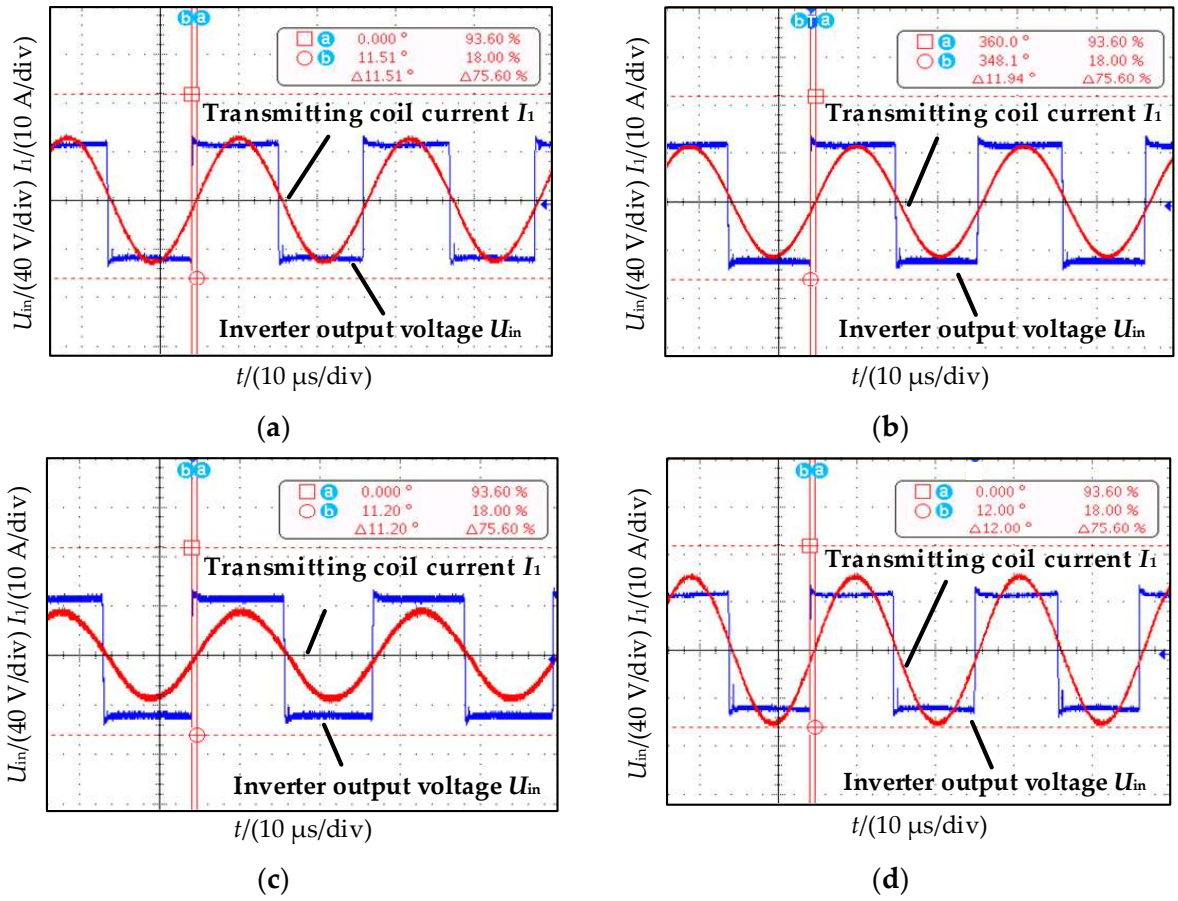


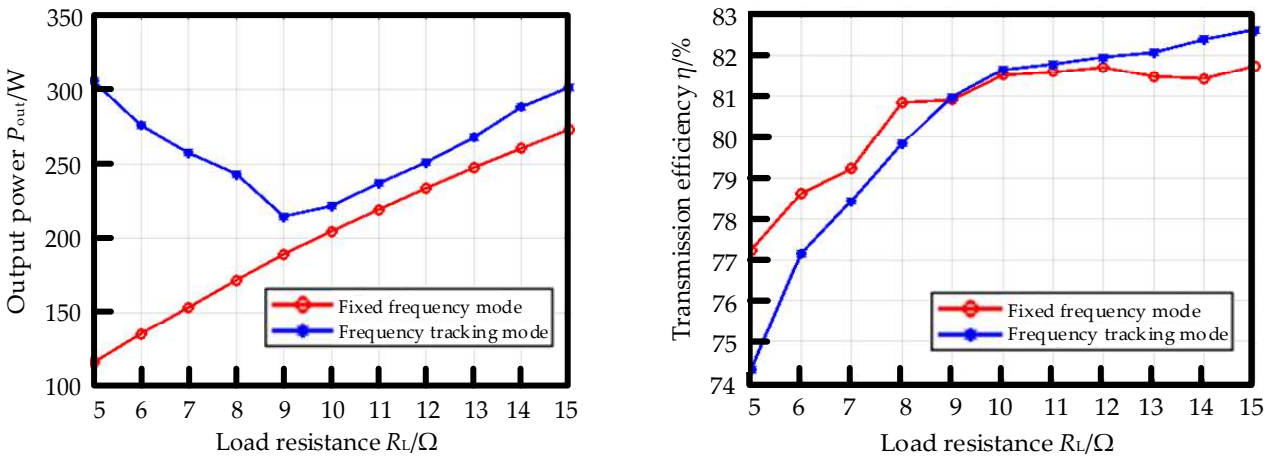
Figure 15. Voltage and current phase diagram based on frequency-tracking method: (**a**) R_L = 5 Ω, coil distance of 24 cm; (**b**) R_L = 15 Ω, coil distance of 24 cm; (**c**) R_L = 7 Ω, coil distance of 18 cm; (**d**) R_L = 7 Ω, coil distance of 28 cm.

In order to prevent the switch tube from being damaged due to the bridge arm conduction, the drive signal should have a certain dead time. Considering the characteristics of the selected MOSFET, the dead time design is 600 ns, and the corresponding angle is $\varphi \geq 360^\circ \times f \times t_d = 10.37^\circ$, where f is the drive signal frequency, and t_d is the dead time selected by the system. In order to ensure that the system can work to maintain ZVS while preventing the inverter output voltage from generating large spikes and polarity reversal phenomena that can lead to damage to the switching tubes, the voltage and current phase difference should be greater than the dead time and leave a certain margin. This paper selects the phase difference between 10.5° and 13°.

Figure 15a shows that the voltage leads the current by 11.51° after phase locking when R_L = 5 Ω. The system changes from capacitive to inductive at a fixed frequency. With output power from a fixed frequency of 116.34 W to 305.55 W, the power has a relatively apparent increase. Figure 15b shows that the voltage leads the current by 11.94° after phase locking when R_L = 15 Ω. The output power is increased from 273.13 W at a fixed frequency to 301.52 W. Figure 15c shows that the voltage leads the current by 11.20° after phase locking. The output power is increased from 53.6 W at a fixed frequency to 229.13 W. Figure 15d shows that the voltage leads the current by 12° after phase locking. The output power is increased from 311.33 W to 328.24 W at a fixed frequency. The phase difference of the emitter current and voltage after phase locking all meet within the set range.

The transmitting and receiving coils are placed parallelly and symmetrically on the same axis, keeping the distance between the two coils at 24 cm. The resistance value of the load at the receiver side is changed, and the transmission efficiency and output power of

fixed frequency and frequency-tracking modes are compared. Figure 16 shows a graph of the comparison results.

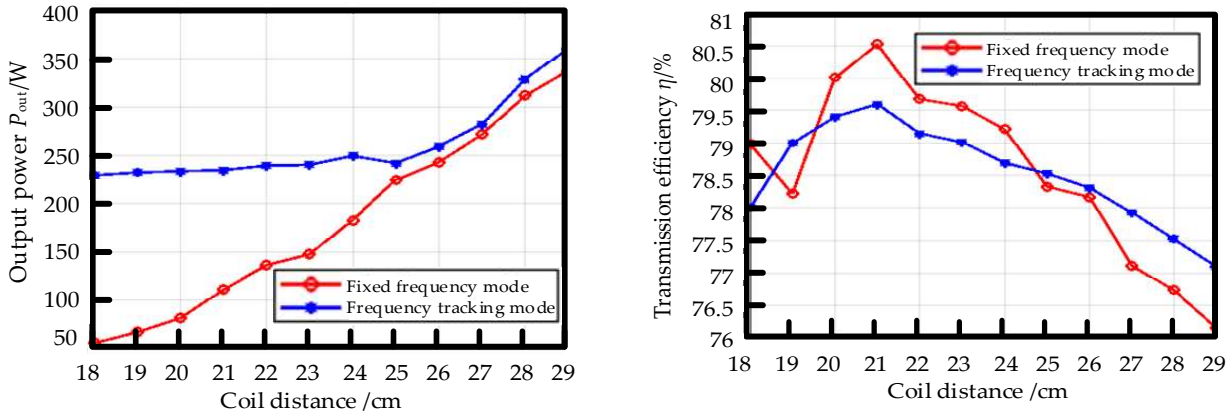


(**a**) (**b**)

Figure 16. Different load and transmission characteristics diagram: (**a**) output power versus load resistance diagram; (**b**) transmission efficiency versus load resistance diagram.

It can be observed from Figure 16 that as the load resistance gradually increases, the output power and transmission efficiency of the WPT system in the fixed frequency mode gradually increase. The frequency-splitting phenomenon occurs when the load is less than 9 Ω. The output power in frequency-tracking mode is much larger than that in fixed-frequency mode, and the transmission efficiency is lower than that of the fixed-frequency mode. After the load is greater than 9 Ω, the system frequency does not split. The output power is still higher than in the fixed-frequency mode, and the transmission efficiency is also higher than in the fixed-frequency mode.

With a fixed load of 7 Ω at the receiver side of the system, the distance between the transmit and receive coils varies. Figure 17 shows the comparison results of transmission efficiency and output power for the two operating modes.



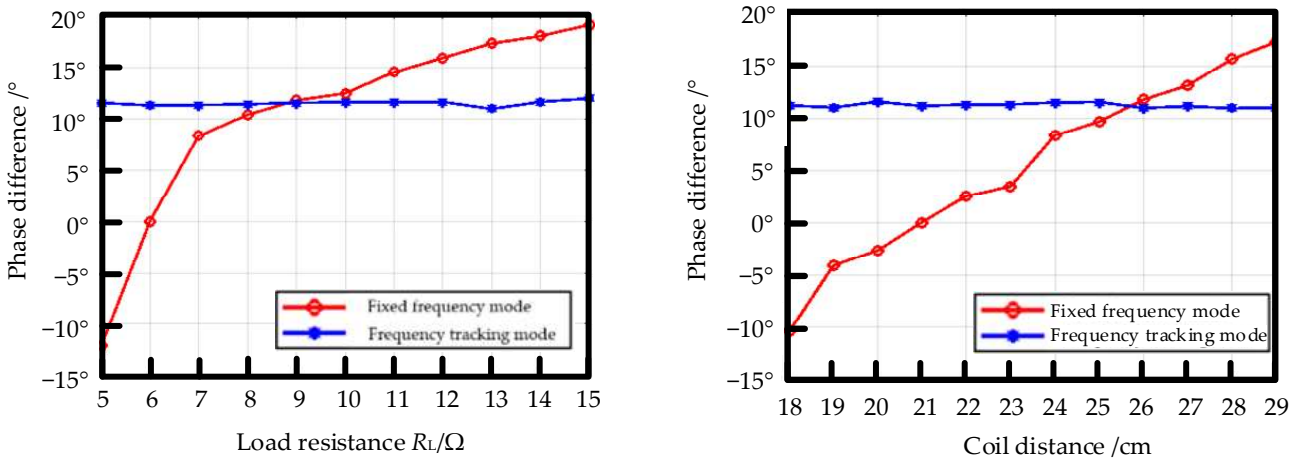
(**a**) (**b**)

Figure 17. Different coil distance versus output power and transmission efficiency diagram: (**a**) output power versus coil distance diagram; (**b**) transmission efficiency versus coil distance diagram.

In Figure 17, the output power of the WPT system in the fixed-frequency mode gradually increases as the coil distance gradually becomes farther away, and the transmission efficiency first increases and then decreases. The output power of the frequency-tracking mode is significantly higher than that of the fixed-frequency mode at any distance, which

is especially obvious within 25 cm, indicating that frequency splitting occurs in this range. After 25 cm, the transmission efficiency of the frequency-tracking mode is higher than that of the fixed-frequency mode.

Under the above conditions of varying the distance and loads, Figure 18 shows the relationship between the voltage and current phase difference at the transmitter side for comparing the frequency-tracking mode and the fixed-frequency mode. The figure shows that as the distance and the load resistance increase, the phase difference in the fixed frequency mode gradually changes from less than 0° to more than 0°, and the system changes from capacitive to inductive. When operating in frequency-tracking mode, whether the system is frequency split or not, the phase difference between the current and voltage at the transmitter side is fixed at about 11.5°. At this time, the system is weakly inductive, and ZVS is maintained to prevent excessive voltage spikes and polarity reversals that may damage the components. This also avoids the excessive equivalent impedance of the system caused by its large phase difference, which significantly increases the system loss. The output power in the frequency-tracking mode is always higher than that in the fixed-frequency mode.



(**a**) (**b**)

Figure 18. Voltage and current phase difference and coil distance, load resistance relationship diagram: (**a**) voltage and current phase difference versus load diagram; (**b**) voltage and current phase difference versus coil distance diagram.

5. Conclusions

In order to solve the problem of a current and voltage phase lag caused by various factors in the WPT system, this paper proposes a frequency-tracking method based on a FPGA to accurately track the current and voltage phase differences on the transmitting side. A frequency-tracking system and a control block diagram are built. A scale-down prototype is fabricated, and the experimental results show that the phase difference of the system remains at 11.5° under different transmission distances and load resistances. This satisfies the expected phase difference between 10.5°~13° and ensures that the system should always work under the ZVS state. In the range of over-coupling conditions, the output power and transmission efficiency are significantly improved compared with the fixed-frequency system.

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