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Thermal Interaction and Cooling of Electronic Device with Chiplet 2.5D Integration

Jianyu Feng [1,2], Minghao Zhou [3], Chuan Chen [1,*], Qidong Wang [1,*] and Liqiang Cao [1]

[1] Institute of Microelectronics of the Chinese Academy of Sciences, Beijing 100029, China; fengjianyu@ime.ac.cn (J.F.); caoliqiang@ime.ac.cn (L.C.)
[2] School of Integrated Circuits, University of Chinese Academy of Sciences, Beijing 100049, China
[3] School of Electronic Science and Engineering, Nanjing University, Nanjing 210093, China; zm_sunsky@126.com
* Correspondence: chenchuan@ime.ac.cn (C.C.); wangqidong@ime.ac.cn (Q.W.)

Abstract: With the development of artificial intelligence (AI) and high-performance computing (HPC), the microelectronic industry is challenged with increased device integration density. Chiplet architecture can break through a variety of limitations on the system-on-chip (SoC) to create a high-computility system. However, chiplet heterogeneous integration suffers from high heat flux and serious thermal interaction problems. The factors affecting thermal interaction are not clear. In this paper, a collective parameter model and a distribution parameter model are developed to clarify the optimization method to mitigate thermal interaction. The trends predicted by the parameter model are consistent with the finite element method (FEM) simulation results. Furthermore, to cool the chiplets, a thermal test vehicle is designed and fabricated, and the cooling performance of the test vehicle with different flow rates, different TIMs (Thermal Interfacial Materials) (DOW5888 vs. liquid metal), and different heat modes is experimentally investigated. Compared with DOW5888, the utilization of liquid metal TIM can mitigate thermal interaction by 56% and 76% at flow rates of 0.2 L/min and 0.8 L/min, respectively. Consequently, at a temperature rise of 60 °C and a flow rate of 0.8 L/min, using liquid metal TIM can achieve heat fluxes of 330 W/cm^2 and 520 W/cm^2 for two chiplets, respectively.

Keywords: thermal interaction; chiplet 2.5D integration; near-chip cooling; TIM; liquid metal

Citation: Feng, J.; Zhou, M.; Chen, C.; Wang, Q.; Cao, L. Thermal Interaction and Cooling of Electronic Device with Chiplet 2.5D Integration. *Appl. Sci.* **2024**, *14*, 8114. https://doi.org/10.3390/app14188114

Academic Editors: Patrice Estellé, Lioua Kolsi and Walid Hassen

Received: 30 July 2024
Revised: 29 August 2024
Accepted: 30 August 2024
Published: 10 September 2024

1. Introduction

Moore's Law has driven the electronics industry for over 55 years. However, in recent years, semiconductor processes are nearing their physical constraints. The cost of the monolithic system-on-chip (SoC) is rising as integrated circuit process technology continues to evolve and design complexity increases [1,2]. Chiplet heterogeneous integration offers a cost-effective alternative to SoC design, with many benefits such as intellectual property (IP) reuse, quick time-to-market, and less risk and cost [3,4]. The chiplet architecture involves dividing a larger monolithic SoC into smaller chiplets and integrating them into a system [5].

Currently, 2.5D and 3D integration are mainly utilized to package chiplets, and several innovative packaging technologies have been developed. TSMC's Chip-on-Wafer-on-Substrate (CoWoS) is a typical 2.5D package which integrates multiple chips via an interposer [6]. Other 2.5D packages include Intel's Embedded Multi-die Interconnect Bridge (EMIB) technology [7]. In 3D integration, two or more dies are directly stacked vertically by micro-bumps or hybrid bonding technology, such as Intel's Foveros and TSMC's System on Integrated Chip (SoIC) technology [8,9]. Compared with the 3D integrated chip, the 2.5D integrated chip has lower heat accumulation and multiple chips are stacked side by side on the interposer mounted on the substrate [10].

To improve the computing performance of the heterogeneous integration system, the performance of a single chiplet is improved by laying out more processing units and then integrating multiple chiplets together, which will generate more heat during operation. For example, Intel's newly released GPU chip Ponte Vecchio in 2022 integrates 47 chiplets belonging to five process nodes via EMIB and Foveros packaging technology, with a thermal design power (TDP) of up to 600 W [11], and Intel's SoC-based system Xeon W-3365 chip released in 2022 with a TDP of only 270 W [12]. AMD's Instinct MI300X GPU, released in 2023, has a TDP of up to 750 W and includes 12 chiplets [13]. Based on the performance evolution needs, the TDP of GPUs integrated by chiplets will continually increase in the next five years. The increased TDP strongly influences the functionality and stability of chips and integrated systems, making thermal management critical. Therefore, it is of great significance to develop suitable and efficient cooling technology for high-power chiplets. Common HPC cooling technologies include the following three schemes: jet cooling, spray cooling, and microfluidic cooling. In contrast to other technologies, microchannel cooling stands out for its structural simplicity and cost-effectiveness, while near-chip microfluidic cooling is superior in terms of structural complexity and cost and is suitable for chiplet 2.5D integration [14].

Transistor feature size reduction no longer meets the demands of AI and HPC, and more chiplets must be integrated in a package; the pitch of the chiplets will decrease, and high-density integration will cause considerable thermal interaction between multiple chiplets. For the integration with two or more chiplets, a single value of thermal resistance cannot explain the interactions between chiplets; thermal resistance matrixes are needed. Unfortunately, existing thermal resistance matrixes are not suitable for chiplet heterogeneous integration and only apply to multiple heat sources on a single chip [15]. For multiple heat sources in a monolithic chip, the superposition strategy is a useful tool for predicting temperatures of multiple heat sources and has been applied in the thermal management process. According to the superposition strategy, the temperature distribution caused by multiple chips can be linearly superimposed from temperature profiles with each chip functioning individually [16,17]. Wang et al. experimentally verified the accuracy of the superposition strategy by fabricating multiple hotspots on one chip [18]. Ye et al. also experimentally verified the concept of the thermal superposition effect based on the relationship between the cooling efficiency of two hotspots and their relative positions [19]. Proper thermal modeling and analysis are crucial for the successful design of chiplet 2.5D integration; the current research mainly focuses on thermal interaction within a monolithic chip, and there is no relevant research on thermal interaction in chiplet 2.5D integration. The influence of thermal interaction on chiplet 2.5D integration is still unclear. It is necessary to study the mechanism and influencing parameters of thermal interaction in chiplet integration and the methods to mitigate it.

In this work, a collective parameter model and a distribution parameter model are proposed to analyze the thermal interaction in chiplet 2.5D integration in Section 2. The mechanism of thermal interaction and the influence parameters are elucidated. In Section 3, through finite element simulation, the effects of different parameters on thermal interaction are analyzed and the trend predicted by the parameter model is also verified. In Section 4, the performance of a near-chip cooling scheme with two different TIMs (silicone grease vs. liquid metal) is experimentally investigated.

2. Thermal Interaction Model of Chiplet 2.5D Integration

2.1. Chiplet 2.5D Integration

Figure 1 illustrates the typical schematic of chiplet 2.5D integration, whereby two chiplets are mounted to an interposer via microbumps, and the interposer is bonded to the substrate using C4 bumps. The underfill is filled in between the chiplets and the interposer, as well as between the interposer and the substrate. A Cu heat sink as lid is attached to the top surface of the chiplets and the substrate via TIM and adhesive. This type of cooling scheme is called near-chip cooling. In contrast to remote cooling, near-chip cooling

eliminates the spreader and a layer of TIM, resulting in a shorter heat transfer path. In contrast to embedded cooling, near-chip cooling has one more layer of TIM, yet it simplifies the fabrication process.

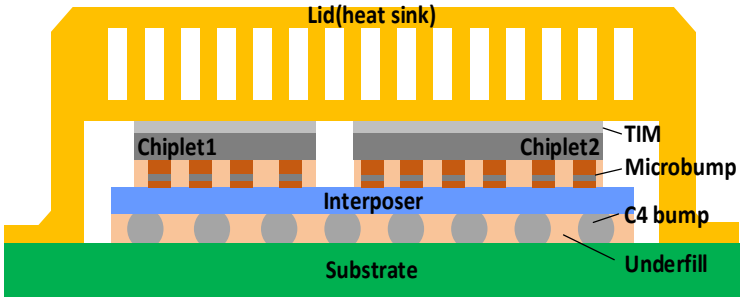


Figure 1. Schematic of near-chip cooling for chiplet 2.5D integration.

2.2. Collective Parameter Model

To study the thermal interaction between two chiplets, the collective parameter model is established. The nodal method is used to solve the heat conduction equation under steady state conditions, and the thermal resistance between nodes represents the total thermal resistance between the two faces corresponding to the nodes. Depicted in Figure 2 is the collective parameter model. The total thermal resistance of C4 bump layer and the substrate (R_{second}) is neglected in this model. When chiplet1 is heated and chiplet2 is not heated, we define chiplet1 as the active chip and chiplet2 as the passive chip. The heat transfer direction of the active chip is depicted in Figure 2. The thermal resistances of the heat sink, TIM, chiplet, microbump layer, and interposer are denoted as R_{hs}, R_T, R_D, R_b, R_{inter}, respectively. The sum of the thermal resistances of the microbump layer and interposer is represented as R_{c_t}. In addition, R_{J1} represents the thermal resistance between chiplet1 and the ambient temperature, and R_{J2} represents the thermal resistance between chiplet2 and the ambient temperature.

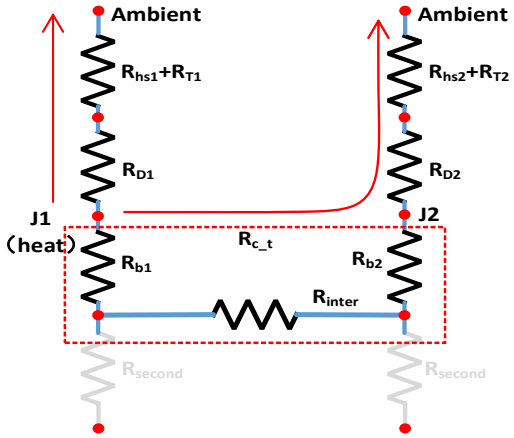


Figure 2. Collective parameter model.

The temperature rise of the passive chip is calculated as Equation (1):

$$\Delta T_{J2} = Q_2 \times (R_{D2} + R_{T2} + R_{hs2}) \tag{1}$$

where

$$Q_2 = Q \times \frac{1}{1 + \frac{R_{c\_t} + R_{D2} + R_{T2} + R_{hs2}}{R_{D1} + R_{T1} + R_{hs1}}} \tag{2}$$

thus

$$\Delta T_{J2} = Q \times \frac{R_{D2} + R_{T2} + R_{hs2}}{1 + \frac{R_{c\_t} + R_{D2} + R_{T2} + R_{hs2}}{R_{D1} + R_{T1} + R_{hs1}}} \tag{3}$$

According to Equation (3), decreasing R_{c_t} will increase the temperature rise of the passive chip. Consequently, by increasing the thermal conductivity of the microbump layer, decreasing the thickness of the microbump and the spacing between the chiplets, and increasing the thickness and thermal conductivity of the interposer, R_{c_t} will decrease and the temperature rise of the passive chip will increase.

As R_{J1} increases, R_{J2} also increases due to the same TIM and heat sink in chiplet 2.5D integration. We can define the increased thermal resistance as:

$$R'_{J1} = \alpha R_{J1}\ R'_{J2} = \alpha R_{J2}\ \alpha > 1 \tag{4}$$

where

$$\Delta T'_{J2} = Q_1 \times \frac{\alpha R_{J2}}{1 + \frac{R_{c\_t} + \alpha R_{J2}}{\alpha R_{J1}}} \tag{5}$$

where

$$\frac{\alpha R_{J2}}{1 + \frac{R_{c\_t} + \alpha R_{J2}}{\alpha R_{J1}}} > \frac{R_{J2}}{1 + \frac{R_{c\_t} + R_{J2}}{R_{J1}}} \tag{6}$$

and thus

$$\Delta T'_{J2} > \Delta T_{J2} \tag{7}$$

According to Equations (5) and (7), as R_{J1} increases, the temperature rise of the passive chip increases. Thus, by decreasing the thermal conductivity of the TIM and the heat sink and increasing the thickness of the chiplet, the temperature rise of the passive chip increases.

2.3. Distributed Parameter Model

The optimization method to mitigate thermal interaction can be clarified by the collective parameter model. However, due to the large size of the chiplet, there will be a large difference in temperature distribution within one chiplet, and the collective parameter model cannot reflect the effect of parameters on the difference of temperature rise at various points in the passive chip. Based on the collective parameter model, the distributed parameter model is proposed, and two points on one chiplet are selected as temperature nodes to establish a more detailed thermal resistance network, as depicted in Figure 3.

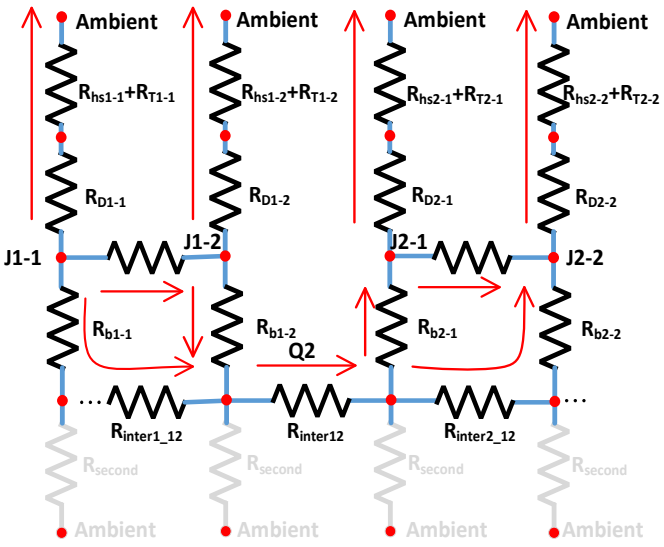


Figure 3. Two-node distribution parameter model.

Based on the distribution parameter model depicted in Figure 3, the temperature rise at node $J_{1\text{-}1}$ will be the maximum in chiplet1, while the temperature rise at node $J_{1\text{-}2}$ will be the minimum. The maximum temperature rise resulting from thermal interaction will occur in node $J_{2\text{-}1}$ (in chiplet2), and $J_{2\text{-}2}$ has the minimum temperature. The temperature rise difference between two nodes in the passive chip is calculated with Equation (8):

$$\begin{cases} \frac{T_{J2\text{-}1}}{R_{JA}} + \frac{T_{J2\text{-}1}-T_{J2\text{-}2}}{R_{inter\_J}} + \frac{T_{J2\text{-}1}-T_0}{R_{b2\text{-}1}} = 0 \\ \frac{T_{J2\text{-}2}}{R_{JA}} + \frac{T_{J2\text{-}2}-T_{J2\text{-}1}}{R_{inter\_J}} + \frac{T_{J2\text{-}2}-T_0}{R_{b2\text{-}2}+R_{inter2\_12}} = 0 \\ \frac{T_0-T_{J2\text{-}1}}{R_{b2\text{-}1}} + \frac{T_0-T_{J2\text{-}2}}{R_{b2\text{-}2}+R_{inter2\_12}} = Q_2 \end{cases} \tag{8}$$

Both nodes are presumed to have the same thermal resistance to the ambient temperature as they are at the same chiplet, with the same TIM and heat sink.

$$\begin{aligned} R_{J2} &= R_{D2\text{-}1} + R_{\text{hs}2\text{-}1} + R_{T2\text{-}1} \\ &= R_{D2\text{-}2} + R_{\text{hs}2\text{-}2} + R_{T2\text{-}2} \end{aligned} \tag{9}$$

The node temperature rise difference can be computed through Equation (8) as follows:

$$T_{J2\text{-}1} - T_{J2\text{-}2} = Q_2 \frac{R_{inter2\_12}}{\frac{2R_{b\&i}}{R_{inter\_J}} + \frac{R_{b\&i}}{R_{JA}} + 2} \tag{10}$$

where

$$R_{b\&i} = R_{b2\text{-}1} + R_{b2\text{-}2} + R_{inter2\_12} \tag{11}$$

According to Equation (2), when the spacing between the active and passive chips decreases, Q_2 will increase, and the other thermal resistances in Equation (10) remain unchanged, and the temperature difference between the two nodes in the passive chip increases. When the thermal conductivity of the TIM decreases, R_{J1} increases, Q_2 will increase, and R_{J1} in Equation (10) increases, while the other thermal resistances remain unchanged, and the temperature difference between the two nodes increases.

When the thermal conductivity of the interposer decreases, R_{inter2_12} increases, and according to Equation (2), Q_2 will decrease. Equation (10) can be transformed as follows:

$$T_{J2\text{-}1} - T_{J2\text{-}2} = Q_2 \frac{1}{\frac{2}{R_{inter\_J}} + \frac{1}{R_{JA}} + A} \tag{12}$$

where

$$A = \frac{2\left(\frac{R_{b2\text{-}1}+R_{b2\text{-}2}}{R_{inter\_J}}\right) + \frac{R_{b2\text{-}1}+R_{b2\text{-}2}}{R_{JA}} + 2}{R_{inter2\_12}} \tag{13}$$

According to Equation (13), an increase in R_{inter2_12} leads to a decrease in A. The temperature difference at the nodes does not always monotonically increase or decrease with the change in interposer thermal conductivity when Q_2 decreases.

3. Simulation Verification

To verify the accuracy of the above parameter model analysis, a simplified chiplet 2.5D integration model is established by the FEM simulation. The steady state thermal module in Ansys used for the simulation, as shown in Figure 4, is the 3D thermal model of the simulation, and the number of FEM simulation grids is 1,026,200. The thermal conductivities of each layer in the simplified model are depicted in Table 1. In this FEM simulation, it is assumed that the thermal conductivity is independent of temperature, and the thermal conductivity is set to a constant value. The bottom convection coefficient of the substrate is specified as 2 W/m^{2}K, whereas the convection coefficient of the heat sink surface is specified as 50,000 W/m^{2}K [20,21]. The ambient temperature is taken as 22 °C. The heat source is located between the chiplet and microbump layer, where the

chiplet is a flip chip. The metal and underfill composite structure of the microbump and C4 bump layer are considered to have an equivalent thermal conductivity of 5 W/mK. The two chiplets are of various sizes; chiplet1 has a dimension of 4 mm × 4 mm, while chiplet2 has a dimension of 5 mm × 5 mm. The dimensions of the heat sink and substrate are both 25 mm × 25 mm, while the interposer has a dimension of 20 mm × 10 mm. Additionally, the thickness of the chiplet is 0.5 mm, the heat sink is 1 mm, the substrate is 0.5 mm, the TIM is 0.1 mm, the microbump layer is 0.06 mm, and the interposer is 0.2 mm.

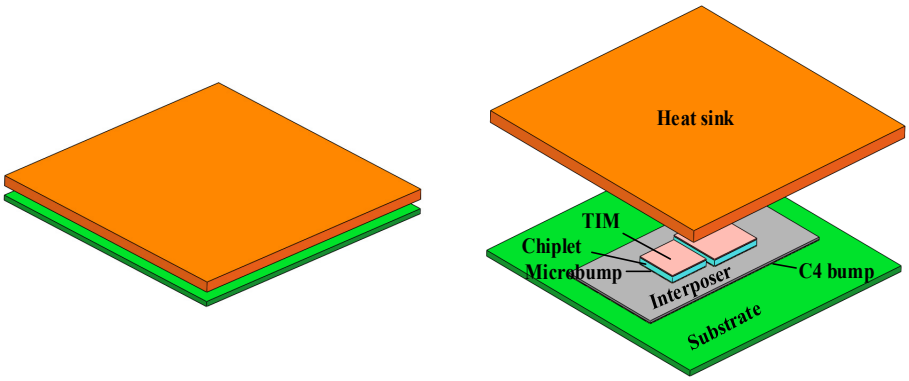


Figure 4. (**a**) Chiplet 2.5D integration simulation model. (**b**) Exploded view.

Table 1. Thermal conductivity in the model.

Materials	Thermal Conductivity (W/mK)
Interposer	148
Bump	5
Chiplet	148
Heat sink	390
TIM	5.2
Substrate	2

3.1. The Effect of Spacing

The effect of chiplet spacing on thermal interaction between chiplets is examined. Chiplet1, with a heat flux of 200 W/cm^2, is the active chip, while chiplet2, with no heat flux, is the passive chip. Figure 5 shows the temperature distribution with a spacing of 0.1 mm; the maximum and minimum temperatures of the active and passive chips are recorded to study the effect of different parameters. The temperature rise is the temperature obtained from the simulation minus the ambient temperature. The active chip has a maximum temperature rise of 52.1 °C and a minimum temperature rise of 45.1 °C. The passive chip has a maximum temperature rise of 14.7 °C and a minimum temperature rise of 4.5 °C. Figure 6 illustrates the temperature rise of both active and passive chips when the chiplet spacing is changed while keeping the other parameters constant. As the spacing decreases, the temperature rise of the passive chip increases, and the temperature rise of the passive chip near the edge of the active chip is always higher than that of the other edge position, and the difference in temperature rise between the two increases. Additionally, the difference within the active chip increases.

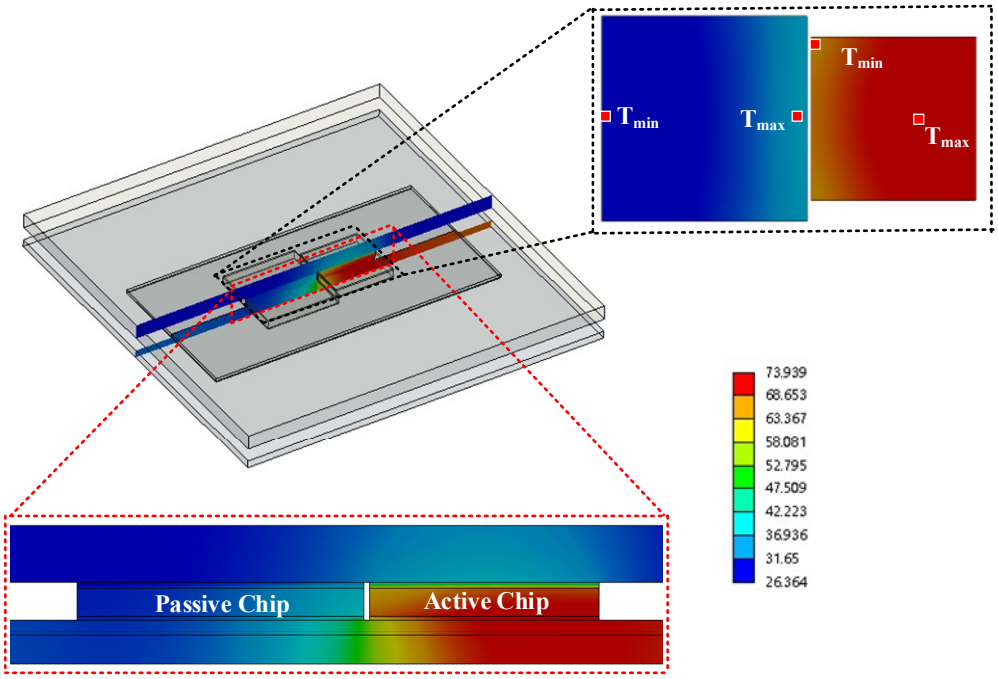


Figure 5. Temperature distribution of the model with 0.1 mm chiplet spacing.

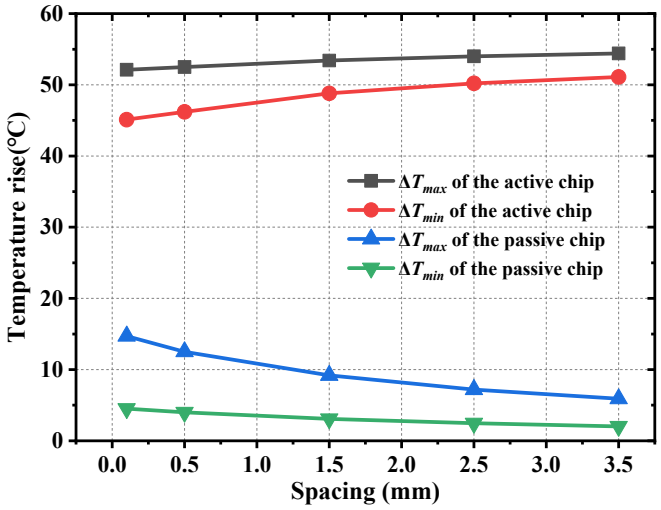


Figure 6. Relationship between chiplet temperature rise and different chiplet spacing.

3.2. The Effect of TIM

The fixed spacing between chiplets is 0.1 mm, with varying thermal conductivity of the TIM being 5.2 W/mK, 40 W/mK, 70 W/mK, 105 W/mK, and 140 W/mK, while keeping other parameters constant. Figure 7 illustrates the temperature rise of the active and passive chips while using various TIMs. The selection of TIM has a significant effect on the temperature rise of the active chip. As the thermal conductivity decreases, the temperature rise of both the active chip and the passive chip increases, with the greater difference in the passive chip.

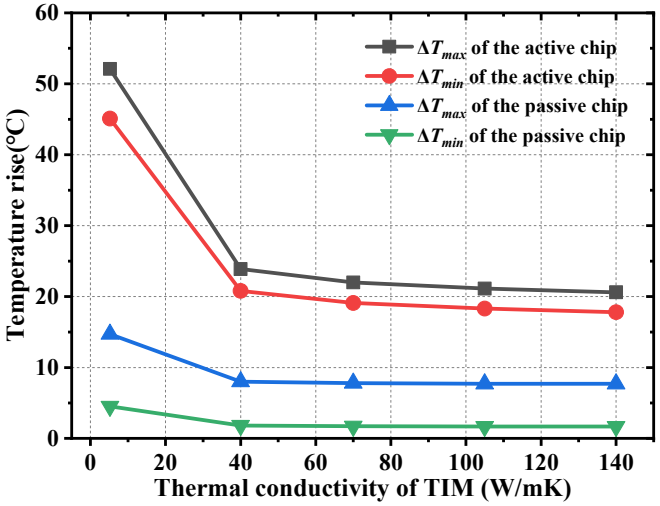


Figure 7. Relationship between chiplet temperature rise and different TIMs.

3.3. The Effect of the Interposer

The fixed spacing between the two chiplets is 0.1 mm, with the varying thermal conductivity of the interposer being 5 W/mK, 40 W/mK, 70 W/mK, 110 W/mK, and 148 W/mK, while keeping other parameters constant. Figure 8 shows the relationship between chiplet temperature rise and different interposers. As the thermal conductivity of the interposer decreases, the temperature rise of the passive chip decreases, while the temperature rise of the active chip increases. The temperature difference within the passive chip does not always increase or decrease. This is consistent with the trend predicted by the distribution parameter model.

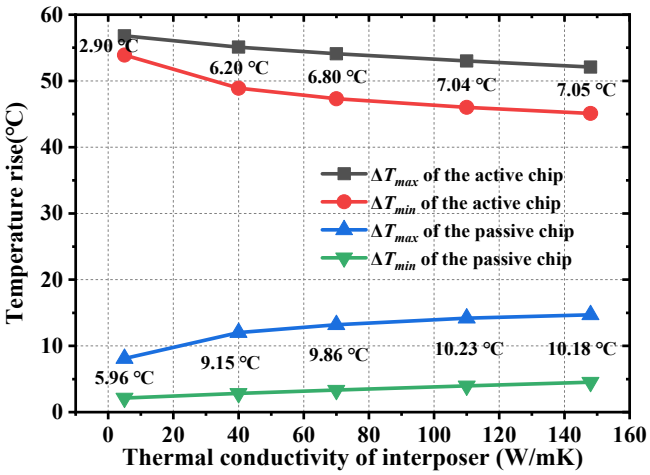


Figure 8. Relationship between chiplet temperature rise and different interposers.

3.4. The Effect of Chiplet Thickness

Fixing the spacing between chiplets as 0.1 mm and varying the chiplet thickness to be 0.1 mm, 0.2 mm, 0.3 mm, 0.4 mm, and 0.5 mm, the other parameters are kept constant. Figure 9 illustrates the temperature rise of the active chip and the passive chip with different chiplet thicknesses. The study reveals that the chiplet thickness has minimal effect on the temperature rise of the active chip and passive chip. As the chiplet thickness increases, the temperature rise of the active chip also increases, while the temperature rise of the passive chip decreases.

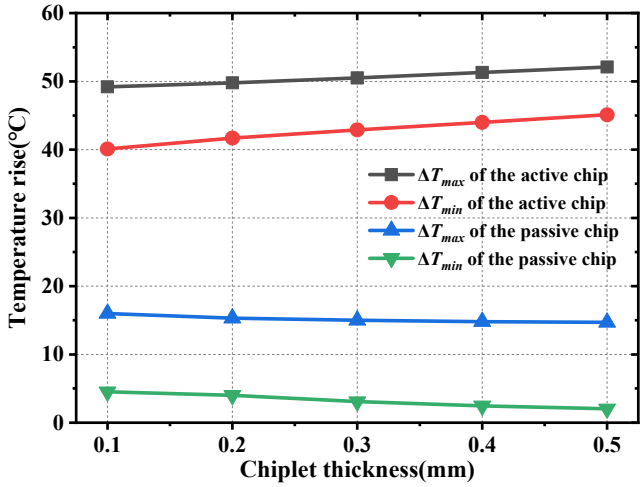


Figure 9. Relationship between chiplet temperature rise and different chiplet thicknesses.

3.5. The Effect of Convective Heat Transfer Coefficient

Fixing the spacing between chiplets as 0.1 mm and varying the convective heat transfer coefficient to be 2 kW/m^{2}K, 5 kW/m^{2}K, 10 kW/m^{2}K, 20 kW/m^{2}K, and 50 kW/m^{2}K, the other parameters are kept constant. Figure 10 illustrates the temperature rise of the active and passive chips with different convective heat transfer coefficients. It is found that the convective heat transfer coefficient has a significant effect on chiplets. As the convective heat transfer coefficient decreases, both the temperatures of the active chip and the passive chip increase. A greater convective heat transfer coefficient is necessary to mitigate the thermal interaction between chiplets.

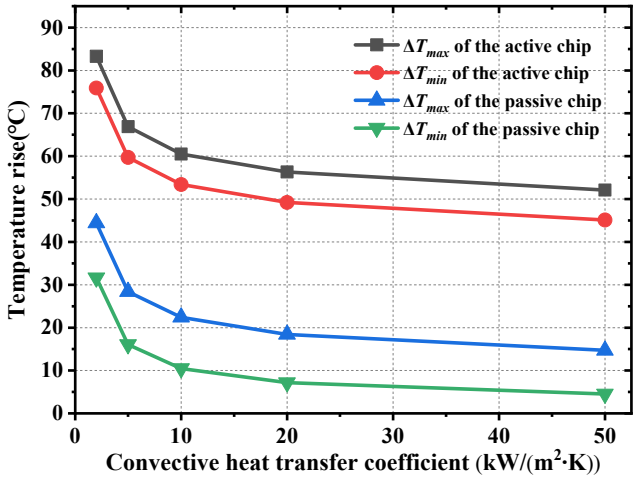


Figure 10. Relationship between chiplet temperature rise and different convective heat transfer coefficients.

The above simulation results demonstrate that the temperature rise of the passive chip increases as the spacing decreases. Utilizing high thermal conductivity TIM can effectively decrease the temperature rise of both active and passive chips and mitigate the thermal interaction between chiplets. Increasing the thermal conductivity of the interposer decreases the temperature of the active chip, increases the temperature of the passive chip, and exacerbates the thermal interaction. High convective heat transfer coefficients can effectively decrease the active and passive chip temperature, as well as mitigate the thermal interaction. To mitigate the thermal interaction, chiplet 2.5D integration necessitates the use of high thermal conductivity TIMs and liquid cooling. The results obtained from the simu-

lation are consistent with the trends predicted by the collective and distributed parameter model. The parameter models can provide a reference for chiplet 2.5D integration.

4. Near-Chip Cooling

4.1. Test Vehicle

Based on the simulation results, a thermal test vehicle for 2.5D integration is designed and fabricated, and a thermal test chip (TTC) is utilized instead of a chiplet in the test vehicle. Depicted in Figure 11a is the schematic of the TTC, where the orange Pt serpentine wire is utilized as heater, with one end connected to the positive terminal and the other end connected to the negative terminal. Temperature measurement of the TTC is determined by measuring the linear relationship between Pt metal resistance and temperature. Pt resistance temperature detectors are manufactured using metal lift-off technology. First, platinum is deposited onto the chip by thin-film deposition. Subsequently, a serpentine pattern is created using photoresist, and then photolithographically exposed, developed, and etched. Finally, the photoresist is removed to complete the fabrication process. The resistance of metals is measured by the four-wire method. The two TTCs are at different dimensions, one with a dimension of 5 mm × 5 mm and the other with a dimension of 4 mm × 4 mm. To mitigate the thermal interaction between the chiplets, based on the FEM simulation findings, 2 mm is selected as the chiplet spacing in this experiment. As depicted in Figure 11b, the TTCs are bonded to the interposer via microbumps, while the substrate is bonded to the PCB via C4 bumps to enable voltage loading and resistance measurement. The heat sink is made of copper, as depicted in Figure 11c, the microchannel in the heat sink has a width of 0.5 mm and a depth of 1 mm, and the dimensions of the microchannel region are 22 mm × 10.8 mm. To prevent the oxidation and corrosion of the copper, a nickel layer is electroplated on the surface of the heat sink. The heat sink, as the metal lid, is contacted with the TTC via the TIM and fixed on the pressboard, as depicted in Figure 11d.

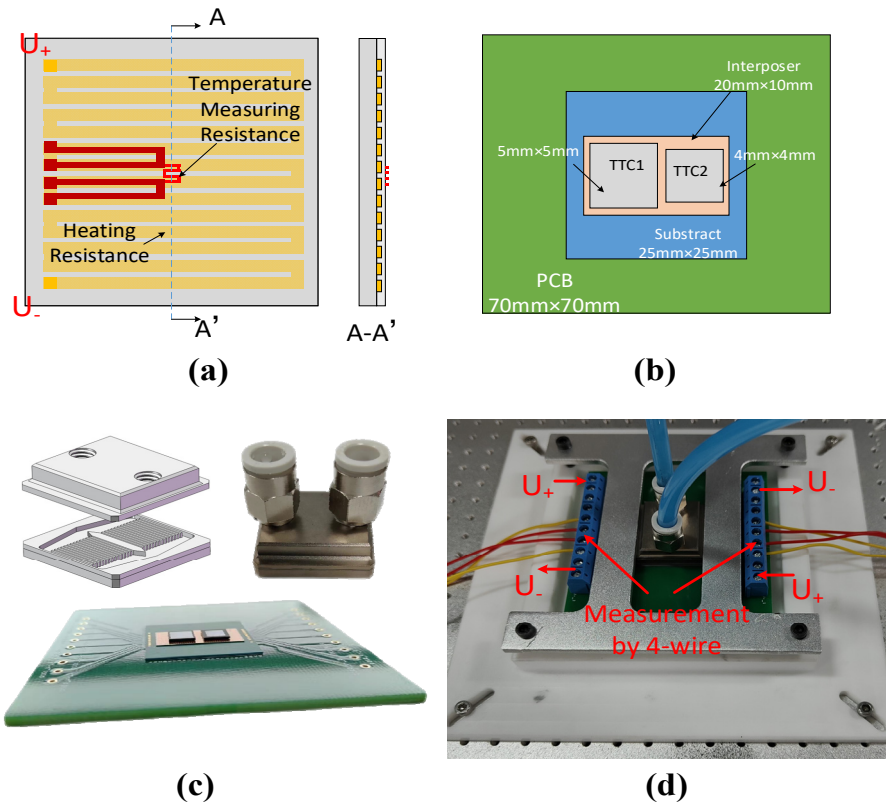


Figure 11. (**a**) TTC. (**b**) The schematic of chiplet 2.5D integration. (**c**) Heat sink and chiplet 2.5D integration. (**d**) Near-chip cooling test vehicle.

The entire test closed-loop system comprises several key components: a water tank for storing deionized water as the coolant; valves for controlling the flow of the coolant; a flow meter (OMEGA FLR1004) for measuring coolant flow rate; a data acquisition unit (RIGOL M300) for collecting the Pt resistance values within the chip and the temperature of the coolant at the inlet and outlet of the cooling structure; a DC power supply (Faith FTP020-80-60) for providing heating power to the chip; K-type thermocouples (5TC-TT-K-40-36) positioned at the inlet and outlet of the cooling structure to measure water temperature; and a plunger pump (PB-6L5M) for supplying coolant.

To accurately characterize the temperature of the chiplet, the temperature–resistance curves of the temperature-measuring resistors in Figure 11a need to be corrected. The 2.5D integrated structure in Figure 11c is placed in a thermostat (temperature measurement accuracy 1.1 K) and the resistance values of chiplet1 and chiplet2 are measured at various temperatures to obtain the temperature–resistance curves, as depicted in Figure 12. The curves are fitted using a linear equation and the relationship between temperature and thermal resistance is expressed as:

$$T_1 = 0.2975R_1 - 349.8 \quad (14)$$

$$T_2 = 0.2530R_2 - 260.6 \quad (15)$$

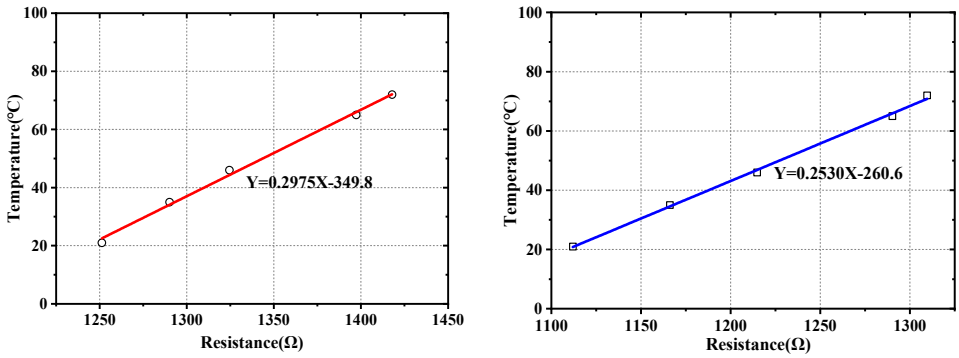


Figure 12. Resistance–temperature curves for Pt temperature measuring resistors. (**a**) Chiplet1. (**b**) Chiplet2.

4.2. Experiments and Results

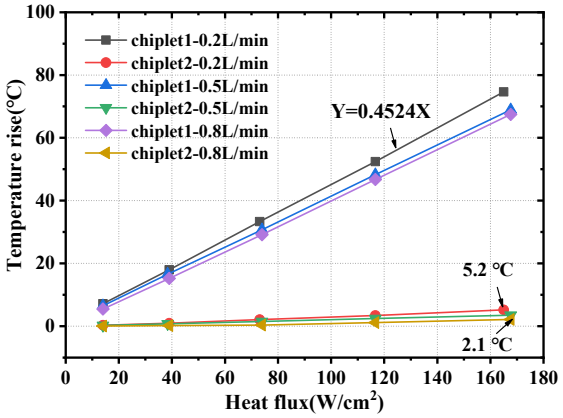
In this study, the coolant is deionized water, and two different heat modes are examined: (1) chiplet1 is heated and chiplet2 is not heated; (2) both chiplet1 and chiplet2 are heated. The heat flux of the TTC is controlled by the input voltage, which ranges from 9 V to 33 V in increments of 6 V. The heat modes and voltages are shown in Table 2. In the experiment, the volume flow rate of the coolant is changed to 0.2 L/min, 0.5 L/min, and 0.8 L/min. Since the heating resistance value of the Pt serpentine wire drifted with temperature during the experiment, there is a slight difference in the input power of the same input voltage for the same input voltage under different heat modes and flow rates, and the heat flow of the two TTCs is determined by the output current and voltage of the power supply, and the heat flux is obtained.

By varying the TIM (silicone grease vs. liquid metal with thermal conductivities of 5.2 W/mK and 72 W/mK, respectively), the resistance values of chiplet1 and chiplet2 in different heat modes are examined in Table 2, and the temperature values are determined by Equations (14) and (15). The relationship between chiplet temperature rise and various heat fluxes in heat mode 1 when the TIM is silicone grease (DOW5888) is shown in Figure 13a. When the flow rates are 0.2 L/min and 0.8 L/min, at an input voltage of 33 V, the temperature rises of chiplet1 are 74.6 °C and 67.4 °C, respectively, while the temperature rises of chiplet2 are 5.2 °C and 2.1 °C. The relationship between chiplet temperature rise and various heat fluxes in heat mode 1 when the TIM is liquid metal is shown in Figure 13a.

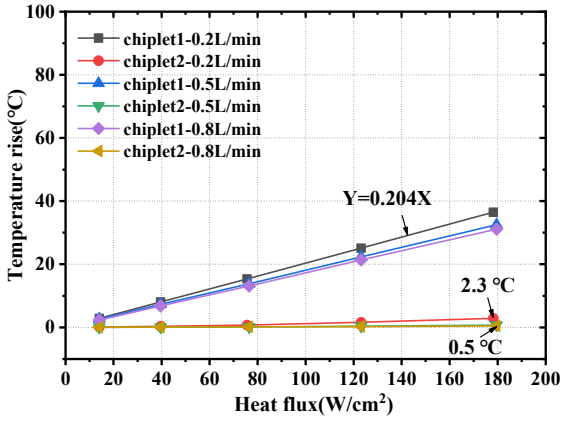
When the flow rates are 0.2 L/min and 0.8 L/min, at an input voltage of 33 V, the temperature rises of chiplet1 are 36.5 °C and 31.1 °C, respectively, while the temperature rises of chiplet2 are 2.3 °C and 0.5 °C. Compared with DOW5888, the liquid metal TIM mitigates thermal interaction by 56% and 76% at the flow rates of 0.2 L/min and 0.8 L/min. Lower thermal interaction is obtained when liquid metal is used as the TIM, which is consistent with the trend predicted by the collective parameter model. Furthermore, the thermal resistance decreases by 24.8 Kmm^2/W at a flow rate of 0.2 L/min. The variation in the TIM significantly increases the cooling capacity of chiplet 2.5D integration and mitigates thermal interaction, especially for higher-heat-flux chiplets in the future.

Table 2. Chiplet loading voltage in two different heat modes.

Mode	Test Number	Chiplet1	Chiplet2
Mode 1	1	9 V	0 V
	2	15 V	0 V
	3	21 V	0 V
	4	27 V	0 V
	5	33 V	0 V
Mode 2	1	9 V	9 V
	2	15 V	15 V
	3	21 V	21 V
	4	27 V	27 V
	5	33 V	33 V

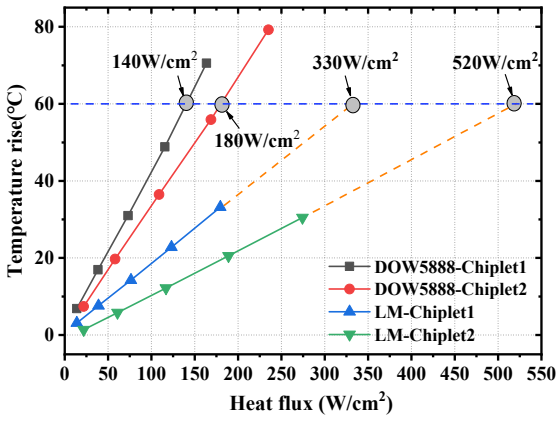


(**a**)



(**b**)

Figure 13. *Cont.*



(**c**)

Figure 13. Temperature rise of chiplets in different heat modes. (**a**) When TIM is DOW5888, heat mode 1. (**b**) When TIM is liquid metal, heat mode 1. (**c**) Heat mode 2.

Figure 13c demonstrates the relationship between the temperature rise of the two chiplets and different heat fluxes in heat mode 2 with a flow rate of 0.8 L/min. According to Figure 13c, when the highest allowable temperature rise in the chiplet is 60 °C and two chiplets are heated at the same time, using DOW5888 as the TIM, the maximum heat fluxes of chiplet1 and chiplet2 are 140 W/cm^2 and 180 W/cm^2, respectively. When liquid metal is used as the TIM, the maximum allowable heat fluxes of chiplet1 and chiplet2 are 330 W/cm^2 and 520 W/cm^2, respectively; the liquid metal can greatly increase the allowable heat flux of the chiplets.

5. Conclusions

The focus of this paper is to investigate the factors influencing the thermal interaction between chiplets and evaluate the cooling performance of 2.5D integration with different TIMs. Through FEM simulation, the effects of different parameters on chiplet thermal interaction are verified, and the simulation results are consistent with the trends predicted by the collective parameter model and distributed parameter model proposed. Furthermore, a near-chip cooling vehicle for chiplet 2.5D integration based on simulation results utilizing different TIMs is employed and experimentally investigated. Compared with DOW5888, the utilization of liquid metal can mitigate thermal interaction by 56% and 76% at the flow rates of 0.2 L/min and 0.8 L/min, and the experimental results agree with the trends shown in the collective parameter model. At a flow rate of 0.8 L/min, when the temperature rise reaches 60 °C, the cooling scheme utilizing the liquid metal TIM can achieve heat fluxes of 330 W/cm^2 and 520 W/cm^2 for chiplet1 and chiplet2, respectively. For high-heat-flux chiplets in the future, near-chip cooling with a high thermal conductivity TIM is a reasonable solution.

Author Contributions: Conceptualization, J.F. and C.C.; methodology, J.F.; software, J.F.; formal analysis, M.Z.; investigation, J.F.; data curation, J.F. and C.C.; writing—original draft preparation, J.F.; writing—review and editing, J.F., C.C. and Q.W.; supervision, L.C.; funding acquisition, C.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the National Natural Science Foundation of China (Grant No. 62104249), the Youth Innovation Promotion Association and the Chinese Academy of Sciences under grant 2023126.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: No new data were created or analyzed in this study.

Acknowledgments: This work acknowledges the software support provided by National Center for Advanced Packaging Co., Ltd.

Conflicts of Interest: The authors declare no conflicts of interest.

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