



Article

DC-DC Buck Converters with Quasi-Online Estimation of Filter Capacitor Equivalent Parameters

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Abstract: The article focuses on devising solutions for monitoring the condition of the filter capacitors of DC-DC converters. The article introduces two novel DC-DC buck converter designs that monitor the equivalent series resistance (ESR) and the capacitance of capacitors using a parameter observer (PO) and simple variable electrical networks (VEN). For the first scheme, the PO processes in real time the voltage at the capacitor terminals during a discharge-charge cycle. For the second scheme, the filtering is performed with two or more capacitors in parallel, and the PO processes the voltage at the terminals of each capacitor during two discharge processes without interrupting the filtering operation of the converter. The paper presents the principles and theoretical support on which the two schemes of DC-DC buck converters are based, design details regarding PO and VEN, as well as experiments performed with each of the schemes. In the experimental schemes, the PO is implemented with a microcontroller, and the parameters of some aluminum electrolytic filter capacitors are calculated in a real-time manner of about 40 ms. The calculation accuracy of the equivalent capacity is very good. Regarding the calculation accuracy of the ESR, it is shown that it depends on the fulfillment of certain ratios between the VEN resistances, on the one hand, as well as between them and the ESR, on the other hand.

Keywords: DC-DC buck converter; condition monitoring of filter capacitor; parameter observer; quasi-online estimation; real-time processing; VEN



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1. Introduction

DC-DC converters are electronic subassemblies used in a huge amount of equipment in numerous fields of activity. The online knowledge of the behavior of the circuits or components and the knowledge of their state-of-health serve in operation as a prerequisite both for the adjustment and adaptation of the control of the converters and for predictive maintenance [1,2]. In the design and operation of DC-DC converters, it is important to model them, completely or partially, i.e., only some of the main components, mostly the output filter capacitor [3]. It can be found both at buck [4] and boost converter [5]. The filter capacitor behavior is described by models with schemes of varying complexity, depending on the details of the physical phenomena with impact on the system functioning [6–9]. The most used model is the R-C series one [10–12].

The R-C series simplified model is suitable for capacitor functions in a low-band frequency [3]. Regarding the monitoring of a capacitor, the equivalent series resistance (ESR) and the equivalent capacitance are frequently used as diagnostic parameters [13]. Always, in applications, the ESR and capacitance vary over a frequency range determined by the spectrum of the current corresponding to the operating regime [13]. In this context, the “equivalent” attribute underlines, in addition to the “effective” attribute used, for example, in [14], the fact that the estimated values of the two parameters characterize the behavior of the capacitor across an entire operating regime [15].

Condition monitoring of capacitors basically includes two phases: the estimation of the equivalent parameters, followed by the use of the estimated values to assess the capacitor condition [2,16,17]. The classifications of estimation techniques and evaluation methods are also addressed in papers [3,18]. In [19], attention is paid to the classification of condition monitoring techniques for aluminum electrolytic capacitors (AEC) in offline, online, and quasi-online techniques.

In control systems engineering and system analysis, mathematical models called observers are frequently used to estimate individual or hybrid variables (combinations of states and input signals) from real systems, called master systems. The inputs of an observer are the measurable inputs and outputs of the master system [20]. Observers are essentially subsystems tracking one or more measurable outputs of the master system.

Numerous studies on DC-DC converters and their components imply observers for estimation, performance control, and fault detection [1,21–26]. In [21], specific observers are used in a buck converter for the fault diagnosis, inductance, and capacitance estimations. In reference [22], the observer serves to control a switching-mode DC-DC converter. The study [25] proposes distinct observers for the ESR and for the capacitance C of the output capacitor of a boost converter. In [1], a state observer is proposed to counterbalance the errors with an ideal model of a boost converter. The paper [23] introduces a piecewise linear observer designed for fault-sensitive detection filters for power electronics systems and exemplified for a dual-redundant buck converter. The study in [24] focuses on the design, analysis, and experimental integration of an enhanced robust adaptive parameter identifier for DC-DC converter applications, based on a closed-loop linear switched state observer. This identifier is designed considering for the capacitor a simple C -model. An observer for estimating the load resistance of a DC-DC buck converter is presented in [26].

In [15] is proposed a new type of observer, distinct from those typically employed in control systems, in particular from those used in DC-DC converters, designed to estimate the time constant of a first-order system. The PO was implemented by the authors to estimate the capacitor parameters of a buck converter based on discharging the capacitor in two stages: over the load resistance in the first stage and over the load resistance connected in parallel with additional resistance in the second stage [27]. The PO uses as input only the measured output of the master system, namely, the voltage at the terminals of the filter capacitor.

This article aims to introduce novel DC-DC buck converter schemes provided with the capability to estimate the equivalent parameters of one or more filter capacitors using a parameter observer (PO).

The main contribution of this paper consists of:

- (i) The proposal of two new schemes of DC-DC buck converters from the category of those estimating the parameters of the R-C series capacitor impedance model using the principle of non-periodic large-signal charging/discharging profiles [17]. From the point of view of the contribution of the monitored capacitor to the filtering operation during the estimation of the parameters, the schemes are working in a quasi-online mode of operation.
- (ii) The implementation of a new monitoring principle for the equivalent parameters with PO based on a capacitor discharge/charge process. Compared to the converter in [26], where the PO monitors a two-stage discharge process, in the new scheme the time to disconnect the capacitor and the load from the converter is reduced. Also, compared to the technique described in [19], current injection into the capacitor is avoided.
- (iii) The implementation of the monitoring principle with PO by performing the filtering with two capacitors connected in parallel instead of a single capacitor.
- (iv) The experimental validation of the proposed principles on converters with electrolytic filter capacitors.

The following sections of the paper comprise: the theoretical and analytical support of the POs used in DC-DC buck converters (Section 2), the principles of designing the novel schemes (Section 3.1), and the depiction of the converters' schematics along with their experimental validation methods (Sections 3.2 and 3.3), discussing the theoretical and experimental results (Section 4), and finally summarizing the conclusions. The article ends

with an Appendix A, important in terms of outlining the conditions that must be met to reduce the estimation errors of the filter capacitors' equivalent parameters.

2. Materials and Methods

2.1. Analytical Support of the Estimation Methods Used in the Schemes Proposed in This Article

The schemes proposed in this article use the estimation method in [15] that estimates the parameter $T(t)$ of the observed (master) system (1) from its free response with PO (2). The observation is made starting from the initial moment t_0 when y has the value y_0 .

$$T(t) \cdot \dot{y}(t) + y(t) = 0, \quad y(t_0) = y_0. \tag{1}$$

$$PO : \begin{cases} z(t) = \ln(y(t)), \\ \frac{dz(t)}{dt} = \hat{c}(t), \quad \hat{z}(0) = \hat{z}_0, \\ \varepsilon(t) = z(t) - \hat{z}(t), \\ \hat{c}(t) = K_p \varepsilon(t) + K_i \int_0^t \varepsilon(\tilde{t}) d\tilde{t} + \hat{c}_0, \\ \hat{T}(t) = -\frac{1}{\hat{c}(t)}. \end{cases} \tag{2}$$

PO (2) is a stable second-order tracking system of the variable $z(t) = \ln(y(t))$. It has the state variables \hat{z} and \hat{c} . The variable \hat{c} provides through the opposite of its inverse the estimated \hat{T} of T . The variable ε represents the tracking error, \hat{z}_0 and \hat{c}_0 are the initial values of the state variables, and $K_p = 2 \cdot \omega_0$ and $K_i = \omega_0^2$ are adjustable parameters of the PI block of the PO. They are adjusted so that the tracking process stabilizes as quickly as possible. For this purpose, ω_0 is chosen so that $\tau \cdot \omega_0 \geq 10$, τ being the length of the time interval after which it is desired to install the tracking regime.

The above principle is applied in Section 3 to the filter capacitors of two buck converters. For the first converter, the principle is used for a capacitor charge/discharge process, while for the second converter, the principle is only applied for processes of discharge, as in [15].

For the first scheme, the principle is applied to estimate the time constants T_1 and T_2 of a process with a variable structure of the form (3):

$$T(t)\dot{v}(t) + v(t) = u(t), \quad \text{with } \begin{cases} T(t) = T_1, u(t) = 0, t \in [t_0, t_1], v(t_0) = v_0 \\ T(t) = T_2, u(t) = K, t \in [t_1, t_2] \end{cases}. \tag{3}$$

The signals $u(t)$ and $v(t)$ are the input and output of the system (3). The modification of the structure occurs at the moment t_1 , simultaneously with the step variation, of amplitude $K > 0$, of the input signal. The initial state of the system is v_0 . Through a simple calculation, it results that the output signal has the expression (4), to which corresponds the curve in V from Figure 1. On the descending portion, the signal has the time constant T_1 , and on the ascending portion, the time constant T_2 .

$$v(t) = \begin{cases} v_0 \cdot e^{-\frac{t-t_0}{T_1}}, & t \in [t_0, t_1] \\ v_0 \cdot e^{-\frac{t_1-t_0}{T_1}} + \left(K - v_0 \cdot e^{-\frac{t_1-t_0}{T_1}} \right) \cdot \left(1 - e^{-\frac{t-t_1}{T_2}} \right), & t \in [t_1, t_2] \end{cases} \tag{4}$$

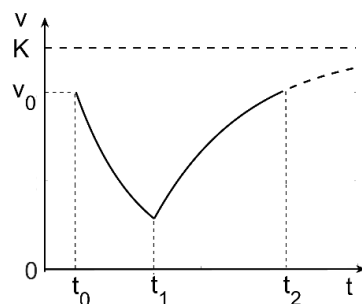


Figure 1. V curve of Equation (4).

To adapt the PO to an input signal of the form (4), we use the fact that this signal can be considered as the output of the exogenous system with variable structure (5).

$$\begin{cases} T(t) \cdot \dot{y}(t) + y(t) = 0, & y(t_0) = v_0, & T(t) = \begin{cases} T_1, & t \in [t_0, t_1) \\ T_2, & t \in [t_1, t_2] \end{cases} \\ v(t) = \begin{cases} y(t), & t \in [t_0, t_1) \\ K - y(t), & t \in [t_1, t_2] \end{cases} \end{cases} \quad (5)$$

If the signal $v(t)$ of system (3) is measurable, then interpreting it also as the output of system (5) allows $T(t)$ to be estimated using a PO. The statement is based on two observations: (i) if the signal $v(t)$ is measurable, then the signal $y(t)$ can be determined from it according to Equation (6) obtained from the system output Equation (5); (ii) given the signal $y(t)$ the parameter $T(t)$ can be estimated using a PO based on the state equation in (5).

$$y(t) = \begin{cases} v(t), & t \in [t_0, t_1) \\ K - v(t), & t \in [t_1, t_2] \end{cases} \quad (6)$$

The block diagram in Figure 2 is obtained by concatenating observations (i) and (ii). Block S contains the observed system (OS) with model (3) and the operations in (6) necessary to obtain $y(t)$. The K and 0 blocks generate the constant values written inside. SW is a switch initially in position 2. At time t_1 it switches to position 1.

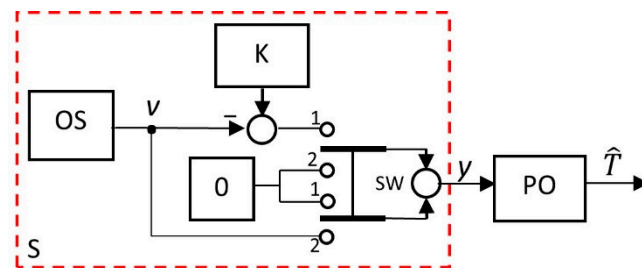


Figure 2. The connection of PO to the observed system OS in order to estimate the parameter $T(t)$. For $t \in [t_0, t_1)$ the switch SW is in position 2, and for $t \in [t_1, t_2]$ in position 1.

Figure 3 exemplifies the behavior of the system in Figure 2 when $v(t)$ has Equation (7). The signal $v(t)$ is represented in Figure 3a and the system response in Figure 3b. The results were obtained by simulation in the Matlab/Simulink environment.

$$v(t) = \begin{cases} 2.5 \cdot e^{-\frac{t}{0.002}}, & t \in [0, 0.008) \\ 2.5 \cdot e^{-4} + \left(\underbrace{3}_K - 2.5 \cdot e^{-4} \right) \cdot \left(1 - e^{-\frac{t-0.008}{0.001}} \right), & t \in [0.008, 0.014] \end{cases} \quad (7)$$

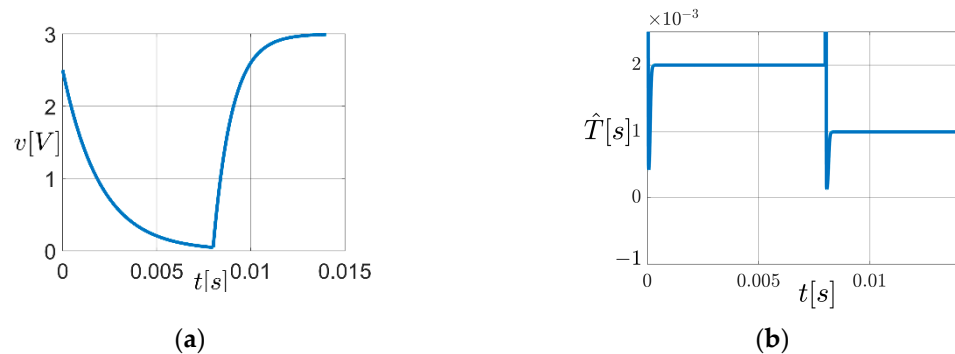


Figure 3. The behavior of the system in Figure 2 when $v(t)$ has the Equation (7): (a) input signal; (b) the estimated time constant $\hat{T}(t)$.

From the perspective of Equation (4) and Figure 2, signal (7) is characterized by the parameters $T_1 = 2 \cdot 10^{-3}$ s, $T_2 = 10^{-3}$ s, $K = 3$, $t_0 = 0$ s, $t_1 = 8 \cdot 10^{-3}$ s, and PO (2) by the parameters $\hat{z}_0 = 0$, $\hat{c}_0 = 0$, $\tau = 0.001$ s, $\omega_0 = 50/\tau$, $K_p = 100,000$ s $^{-1}$, $K_i = 2.5 \cdot 10^9$ s $^{-2}$. As expected, PO returns the values $\hat{T}_1 = 2 \cdot 10^{-3}$ s and $\hat{T}_2 = 10^{-3}$ s with a short delay due to the transients, unavoidable regimes that occur at the start of the estimation and at the change of the monotony of signal $v(t)$.

Omitting the OS block, the structure in Figure 2 can be integrated into a new PO as in Figure 4a. This new structure, intended to operate both on the falling edge of the $v(t)$ signal and on the rising edge, we call it a parameter observer on two edges (PO2). In the practical case, the processing of the signal $v(t)$ is carried out in discrete time, so the connection of PO2 to the OS is carried out as in Figure 4b, PO2 operating according to Equation (8). The used notations have the following meanings: h is the sampling time with which $v(t)$ is acquired and operates PO2, IA—Input Adapter, I—Integrator (modified model of OS), C—Comparator (provides tracking error ϵ), PI—Tracking Controller type PI, OA—Output Adapter.

$$PO2 : \begin{cases} (IA) : y[k] = \begin{cases} v[k], & t \in [t_c, t_d) \\ K - v[k], & t \in [t_d, t_f] \end{cases}, z[k] = \ln(y[k]), \\ (I) : \hat{z}[k] = \hat{z}[k-1] + h \cdot \hat{c}[k], \hat{z}[0] = \hat{z}_0, \\ (C) : \epsilon[k] = z[k] - \hat{z}[k], \\ (PI) : \hat{c}[k] = K_p(\epsilon[k] - \epsilon[k-1]) + hK_i\epsilon[k-1] + \hat{c}[k-1], \hat{c}[0] = \hat{c}_0, \\ (OA) : \hat{T}[k] = -\frac{1}{\hat{c}[k]}. \end{cases} \quad (8)$$

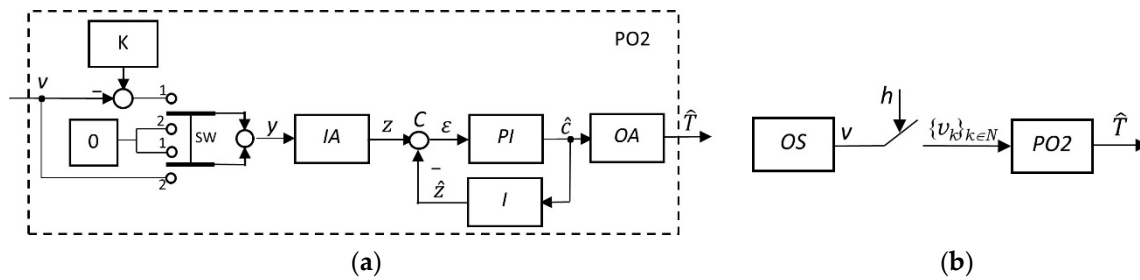


Figure 4. Parameter observer on two edges: (a) the structure of PO2; (b) the block diagram of the connection OS-PO2 for discrete time processing.

2.2. Parameter K of PO2

The parameter K in Equation (8) represents the limit value of the asymptotic increasing exponential variation of the observed signal $v(t)$ of Equation (4), i.e., of the signal that the designer supposes to apply to the PO2 input.

In practical applications, the correct use of PO2 requires an accurate estimation of the value of K related to the applied signal $v(t)$. As a motivation of this statement, Figure 5 is considered. The exponential in the figure has the equation $K \cdot e^{-t/T}$ with $K = K_0$. The parameter T being constant, its value is equal to the length of the subtangent corresponding to the current point A on the exponential curve, i.e., to the segment B_0C_0 measured on the asymptote $v(t) = K_0$. When A changes its position, successively passing through the positions A' and A'' , the length of the subtangent does not change. If we wrongly consider for the same exponential that the asymptote is in another position, i.e., that the parameter K has a value different from K_0 , the property is no longer preserved. Thus, if we consider $K = K_1 > K_0$ the length of the subtangent, B_1C_1 is greater than the subtangent B_0C_0 ; moreover, as A passes through the positions A', A'', \dots , it increases tending to infinity. If we consider that $K = K_2 < K_0$, the length of the subtangent B_2C_2 is smaller than the subtangent B_0C_0 . When the exponential reaches the value K_2 the length of the subtangent takes the value 0, and then disappears.

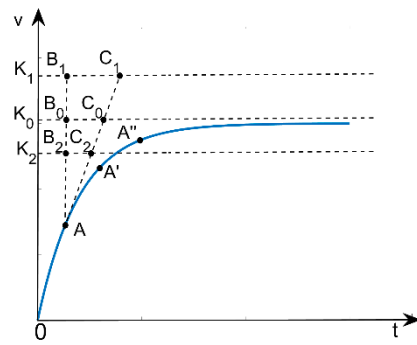


Figure 5. The influence of the K parameter of PO2 on T value.

Analytically, the above discussion translates into the analysis of Equation (9), where $v_{K_0}(t)$ is the signal interpreted by PO2 when K is tuned correctly, i.e., $K = K_0$, and $v_K(t)$ is the signal interpreted by PO2 when K is not tuned correctly, i.e., $K \neq K_0$.

$$v_K(t) = v_{K_0}(t) + (K - K_0) \left(1 - e^{-\frac{t}{T}}\right), \quad t \geq 0. \tag{9}$$

The effect of the additional term in (9) is illustrated in Figure 6. In Figure 6a are displayed more characteristics of the type such as that in Figure 3b, of parameter K , generated by PO2 when the signals of Equation (7) were applied to its input with $K \in \{2.9, 2.95, 2.98, 2.99, 3, 3.01, 3.02, 3.05, 3.1\}$. The group includes the $K = 3$ case. With $\hat{T}_{1,K}(t)$ we denote the segments of $\hat{T}(t)$ on the time interval on which $v(t)$ decreases and with $\hat{T}_{2,K}(t)$ the segments corresponding to the time interval on which $v(t)$ increases. The latter are detailed in Figure 6b. All estimates $\hat{T}_{1,K}(t)$ overlap and stabilize at the value $\hat{T}_1 = 2 \cdot 10^{-3}$ s. This is explained by the fact that in processing the decreasing variations of $v(t)$ PO2 does not use the value of K . Among the curves $\hat{T}_{2,K}(t)$, only the curve $\hat{T}_{2,3}(t)$ stabilizes at the correct value $\hat{T}_2 = 10^{-3}$ s. All other curves fail to stabilize. After the damping of the transients that appears starting from the moment $t = 0.8 \cdot 10^{-3}$ s they have either a monotonically increasing or a monotonically decreasing shape, as K takes values lower or higher than the value 3.

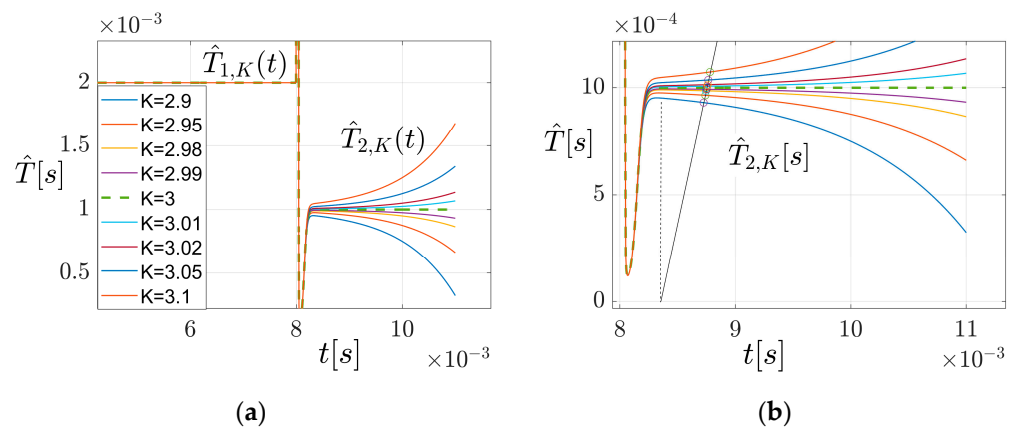


Figure 6. A group of characteristics $\hat{T}(t)$ of parameter K for the case when the system observed in Figure 4b generates the signal (7); $K \in \{2.9, 2.95, 2.98, 2.99, 3, 3.01, 3.02, 3.05, 3.1\}$: (a) Highlighting the segments $\hat{T}_{1,K}(t)$ și $\hat{T}_{2,K}(t)$; (b) Obtaining \hat{T}_2 estimates from segments $\hat{T}_{2,K}(t)$.

The practical conclusion from the above presentation is:

To apply PO2 to a physical system, it is necessary to tune the value of the parameter K in Equation (8) as precisely as possible to match the value that the same-named parameter assumes in the observed signal (4) generated by the physical system. We call this condition “PO2—tuning condition of K ”.

The PO2—tuning condition of K is more experimental. Tuning can be completed in several ways. The simplest way is to consider K equal to $v(t)$ final value after stabilization. K can also be determined according to the above discussion of Figure 6.

Once K is tuned, the values of T_1 and T_2 in (4) can be estimated with PO2 using the method presented in [27]. According to it, the estimates \hat{T}_i , $i = 1, 2$ of the time constants T_i , $i = 1, 2$ are found as solutions of the equation in (10):

$$\hat{T}_i = \{t > t'_i | \hat{T}_{i,K}(t) = \alpha \cdot (t - t'_i)\}, i = 1, 2, \tag{10}$$

where

$$\alpha = 2.5. \tag{11}$$

The procedure is illustrated in Figure 6b with reference to determination of \hat{T}_2 using the curve segments $\hat{T}_{2,K}(t)$. The values of \hat{T}_2 are given by the ordinates of the intersection points of these segments with the semi-straight line of slope α originating from the coordinate point $(t'_2, 0)$. The results are presented in Table 1. It also contains the percentage errors $\Delta\hat{T}_{2\%}$ in relation to the value of T_2 in (7).

Table 1. Estimated T_2 values according to the K parameter of PO2 for the cases in Figure 6.

K	\hat{T}_2 [s]	$\Delta\hat{T}_{2\%}$
2.9	0.000930	6.970
2.95	0.000965	3.540
2.98	0.000988	1.420
2.99	0.000993	0.713
3.00	0.001000	0.000
3.01	0.001007	−0.720
3.02	0.001014	−1.440
3.05	0.001036	−3.630
3.10	0.001074	−7.360

The obtained results confirm the findings related to Figure 5.

2.3. Calculation of the Equivalent Parameters of a Capacitor

Discharging a capacitor, modeled by an R-C series connection, across a resistor or charging it from a constant voltage source through a resistor are processes described by first-order systems (1) and (5), respectively. The time constants T_1 and T_2 correspond to the product of the equivalent capacitance C_e of the capacitor and the total resistance of the circuit according to Equation (12).

$$T_1 = C_e \cdot (R_{se} + R_{ext1}), T_2 = C_e \cdot (R_{se} + R_{ext2}). \tag{12}$$

R_{se} represents the equivalent ESR, and R_{ext1} and R_{ext2} the resistances in the discharge/charge circuit external to the capacitor.

PO or PO2 provides the estimates \hat{T}_1 and \hat{T}_2 of the time constants and calculates the estimates \hat{C}_e and \hat{R}_{se} of the equivalent parameters as the solutions of system (13):

$$\begin{cases} \hat{C}_e \cdot (\hat{R}_{se} + R_{ext1}) = \hat{T}_1 \\ \hat{C}_e \cdot (\hat{R}_{se} + R_{ext2}) = \hat{T}_2 \end{cases} \tag{13}$$

The calculation formulas of \hat{C}_e and \hat{R}_{se} resulting from system (13) show different sensitivities in relation to the errors affecting the values of \hat{T}_1 , \hat{T}_2 , R_{ext1} and R_{ext2} . The statement is substantiated by the analysis undertaken in Appendix A. While the value of \hat{C}_e is a little sensitive in relation to these errors, the value of \hat{R}_{se} presents a high sensitivity. From this perspective, ensuring the PO2—tuning condition of K becomes a mandatory requirement for the implementation of PO2, as it affects the value of \hat{T}_2 .

3. Two Schemes of DC-DC Buck Converter with Estimation of Equivalent Parameters of Filter Capacitor Using PO

The two buck converter configurations proposed in the principle schemes in Figure 7a,d are obtained by adding a variable electrical network (VEN) [28] and a microcontroller to a switching regulator circuit based on the LM2596 integrated circuit [29]. They allow the implementation of the measurement process, the mentioned observers, and the management of the VENs. In the first scheme, an auxiliary source of stabilized DC voltage is included as well. The schemes are shown in Sections 3.2 and 3.3. The part represented in black corresponds to the basic scheme in [29], and the part represented in red includes the performed adaptations. The POs are implemented in the microcontroller in the discrete-time system version (8).

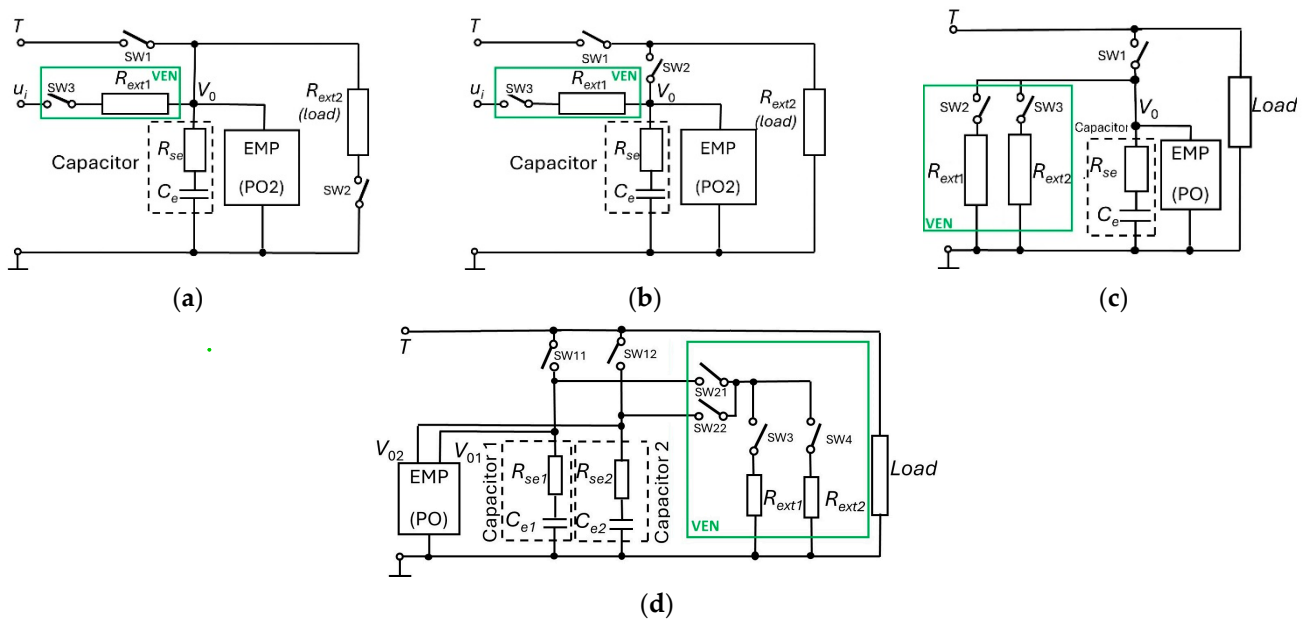


Figure 7. Principle schemes used for the realization of DC-DC buck converters with the estimation of the equivalent parameters of the filter capacitors: (a,b) Schemes with the monitoring of the discharging and charging of the capacitor using PO2 (c,d) Schemes with monitoring of two distinct discharges using PO.

3.1. Principle Schemes

From the point of view of the continuous supply of the converter load, the proposed schemes are of two categories: schemes with short-term disconnection of the load from the converter and schemes without disconnection of the load from the converter. The schemes in Figure 7a,b belong to the first category, and those in Figure 7c,d to the second category. The load and the filter capacitor are connected to the converter via terminal T. In all schemes, the filter capacitor is modeled by the serial equivalent circuit $R_{se}-C_e$. POs are implemented in the measurement and processing (EMP) device. They calculate the estimates \hat{C}_e and \hat{R}_{se} by processing the voltage at the capacitor terminals denoted, as appropriate, by V_0, V_{01}, V_{02} . The values of R_{ext1}, R_{ext2}, R_1 and R_2 are chosen considering the requirements mentioned at the end of Appendix A. Schemes in the second category have the advantage of not including the converter load in the capacitor discharge sequences, thereby not being constrained by the requirements of Appendix A.

In the schemes of the first category, the parameters of the capacitor are obtained during a discharge/charge process using PO2 of Equation (8). The charging of the capacitor is carried out at the voltage u_i from a stabilized voltage source and not from the converter. When switches sw1 and sw2 are in the ON position and sw3 is in the OFF position, the circuits are in normal operation mode (DC-DC mode). Switching sw1 from the OFF position to the ON position results in transients at the load level.

Figure 8 illustrates the $V_0(t)$ signal in an estimation cycle associated with a discharge/charge process corresponding to the schemes in Figure 7a,b. During the I interval, the schemes operate in DC-DC mode. In intervals III and V, PO2 estimates the equivalent time constants. In intervals II and IV, of duration t_n , PO2 acquires the voltage $V_0(t)$ but does not calculate \hat{T}_{1e} and \hat{T}_{2e} . The VI interval corresponds to a transient regime of DC-DC mode restoration. Table 2 shows the sequence of switch states and regimes for an estimation cycle of the scheme in Figure 7a.

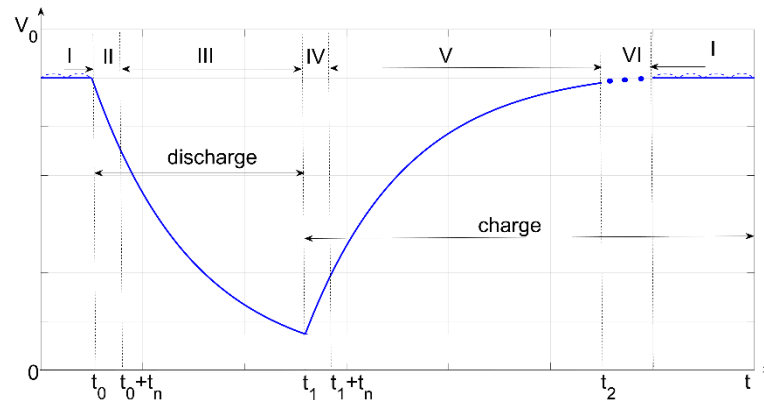


Figure 8. The time sequence for filtering capacitor parameter estimation by a discharge/charge process.

Table 2. Regimes of schematic from Figure 7a in the estimation process.

Regime	Regime/Zones in Figure 8	sw1	sw2	sw3
R1	DC-DC mode on/I	1↑*	1	0
R2	DC-DC mode off, discharging the capacitor through R_{ext2} /II, III	0	1↑	1
R3	Stopping the capacitor's discharging	0	0	0↓
R4	Charging the capacitor from u_i through R_{ext1} /IV, V	0	0	1↑
R5	Stopping capacitor charging	0↓	0	0
R6	Further capacitor's charging through T/VI	1	0↓	0
R7	DC-DC mode on/I	1	1	0

* The meaning of the notations: 0—open, 1—closed, ↑/↓—the switch opens/closes to switch the scheme to the new operating mode.

In second-category schemes, capacitor parameters are obtained using the discrete-time variant of PO (2) during two separate discharges of the capacitor through resistors R_{ext1} and R_{ext2} , which have different values. Between discharges, the monitored capacitor is recharged via the T terminal from the converter when the T-sw1 switch is closed and the LM2596 is ON. Reconnections of the capacitor to the converter result in this case also with transient regimes at the load level. In Figure 7d, the filtering is performed using a capacitance created by connecting two capacitors in parallel. Each capacitor is monitored separately. During monitoring of one capacitor, the other capacitor provides filtering by remaining connected to the converter. This option is advantageous for at least two reasons: (i) the scheme ensures filtering throughout the estimation; (ii) the transients caused by the disconnection and reconnection of the capacitors to the converter are mitigated. The principle can be generalized for batteries of filter capacitors or schemes where “dividing” the filter capacity in at least two capacities can offer technical benefits. Table 3 shows for the scheme in Figure 7d the sequence of regimes that occur when estimating the parameters of capacitor 1 (regimes R1–R9) and of capacitor 2 (regimes R1'–R9'). The manner in which time is handled during discharges is detailed below within Section 3.3. in the explanations regarding the proposed converter as an application to the diagram in Figure 7d.

Table 3. Scheme regimes from Figure 7d in the estimation process.

Regime	sw11	sw12	sw21	sw22	sw3	sw4	Regime	sw11	sw12	sw21	sw22	sw3	sw4
R1	1↑*	1	0	0	0	0	R1'	1	1↑*	0	0	0	0
R2	0	1	0↓	0	0↓	0	R2'	1	0	0	0↓	0	0↓
R3	0	1	1	0	1↑	0	R3'	1	0	0	1	0	1↑
R4	0↓	1	1	0	0	0	R4'	1	0↓	0	1	0	0
R5	1↑*	1	1	0	0	0	R5'	1	1↑*	0	1	0	0
R6	0	1	1	0	0	0↓	R6'	1	0	0	1	0↓	0
R7	0	1	1↑	0	0	1↑	R7'	1	0	0	1↑	1↑	0
R8	0↓	1	0	0	0	0	R8'	1	0↓	0	0	0	0
R9	1	1	0	0	0	0	R9'	1	1	0	0	0	0

* The meaning of the notations: 0—open, 1—closed, ↑/↓—the switch opens/closes to switch the scheme to the new operating mode.

3.2. Scheme Based on the Implementation of the Principle from Figure 7a

The proposed scheme is the one in Figure 9. The converter supplies the resistive load R_L and C_2 is the filtering capacitor. It is a 220 $\mu\text{F}/50\text{ V}$ electrolytic capacitor. Its frequency characteristics, measured using a BK Precision RLC-bridge, are illustrated in Figure 10a,b. The transistors T-sw1, T-sw2, and T-sw3 are used to realize the switches sw1, sw2, and sw3 in Figure 7a. The LDO is a voltage regulator that provides the voltage $u_i = 3.291\text{ V}$ for charging C_2 through the resistor R_{ch} . A microcontroller with computing power based on the Cortex[®]-M7 architecture was used for measuring and processing. The signal $V_0(t)$ was acquired with the sampling time $h = 20\ \mu\text{s}$. The microcontroller sends signals towards the LM2596 circuit and switches using the digital ports P1, P2, P3, and P4 and measures the voltage V_0 at capacitor and load terminals using the analog port AIN. To estimate the capacitor's equivalent parameters, the microcontroller executes the successive operation of the regimes R1–R7 in Table 2. In stages III and V (Figure 8), PO2 implemented in the microcontroller calculates \hat{T}_1 , \hat{T}_2 , \hat{C}_e and \hat{R}_{se} . To achieve a more accurate diagnosis of the capacitor's condition, a sensor S_0 is thermally coupled with the capacitor and interfaced with the microcontroller. The measured result is sent together with the estimated values of the capacitor parameters using a serial SOUT interface towards external assessment of C_2 .

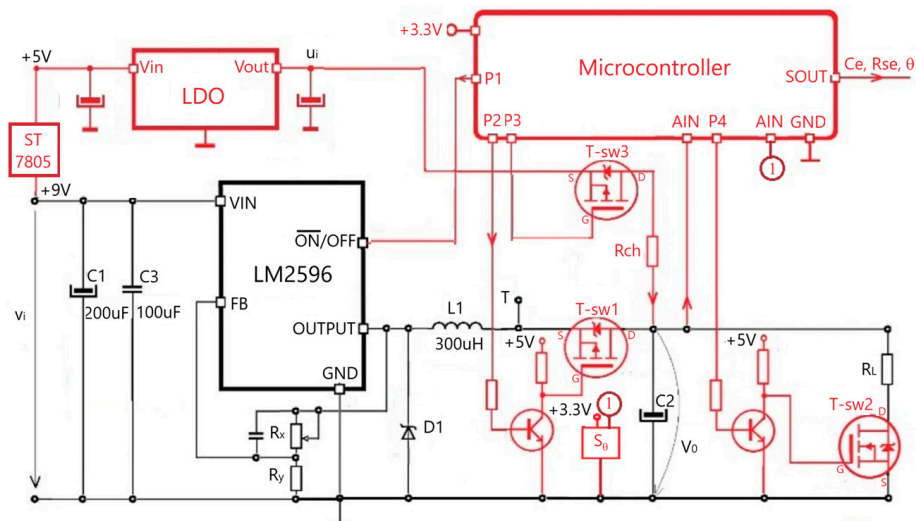


Figure 9. Buck converter scheme made based on the principle scheme in Figure 7a.

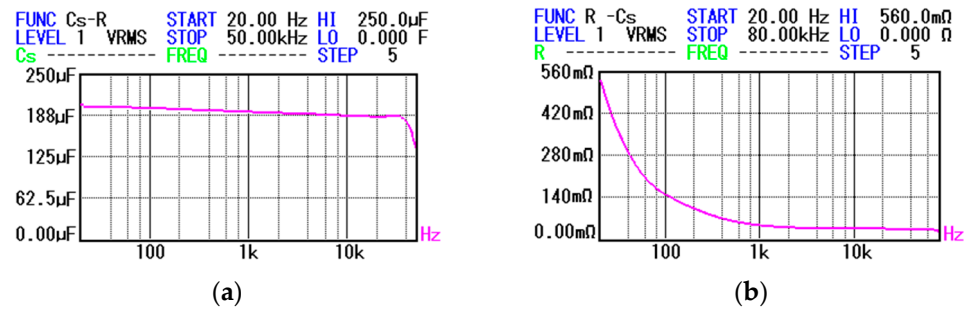


Figure 10. Frequency characteristics of the filter capacitor C2 of the converter in Figure 9: (a) $C(f)$ characteristic; (b) Characteristic $R_s(f)$.

Below are some practical results that validate the structure in Figure 9. Experimentally, by commuting and maintaining the Figure 9 scheme in the R4 regime from Table 2, a value of $K = u_i = 3.291$ V was obtained. To determine the values of \hat{C}_e and \hat{R}_{se} six sets of 25 discharge/charge experiments of C2 were performed. In each set, the experiments were repeated with a frequency of 3.33 Hz. Each discharge/charge process took 40 ms. In Figure 11a is illustrated how the voltage V_0 varies in an experiment, and in Figure 11b the corresponding characteristics $\hat{T}_{1,3.291}(t)$ and $\hat{T}_{2,3.291}(t)$ are represented. The values resulting from the experiment are $\hat{T}_1 = 0.0183244$ s and $\hat{T}_2 = 0.000690196$ s. From the perspective of Figure 1, for Figure 11a: $t_0 = 0.00919$ s, $t_1 = 0.03855$ s, $t_2 = 0.3935$ s. The calculation of the characteristics $\hat{T}_{1,3.291}(t)$ and $\hat{T}_{2,3.291}(t)$ is turned off when the condition in Equations (10) and (11) is met, resulting in the moments 0.1655 s and 0.3935 s. The time t_0 is an arbitrary time according to the series of experiments mentioned below. The time t_1 , when the capacitor commutes from discharging to charging corresponds to the moment when V_0 reaches the value of 0.6 V, so that for the calculation of \hat{T}_2 remains available a voltage interval of approx. 2 V. Time t_2 corresponds to the moment when \hat{T}_2 is obtained. It is observed that the value of V_0 from the moment when OP2 provides \hat{T}_1 is approx. 2 V. If t_1 had been associated with this moment, then for the calculation of \hat{T}_2 there would have been a rather small tension interval available, of approx. 1V.

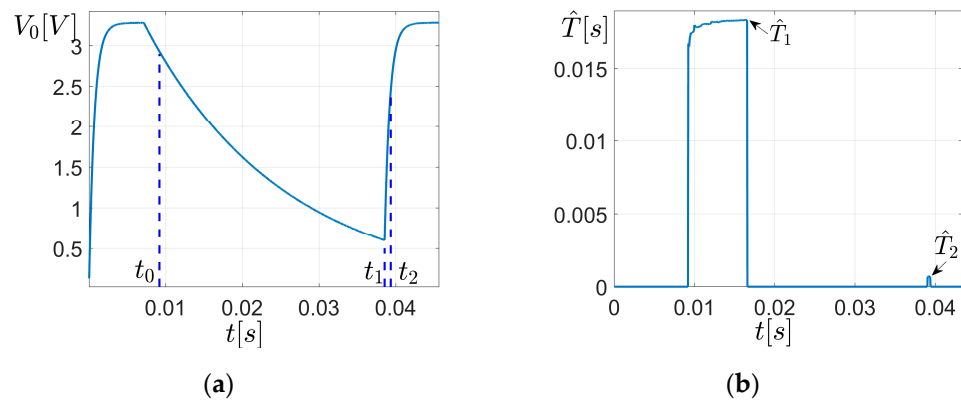


Figure 11. C2 capacitor charging/discharging signal in Figure 9 and the result of its processing with PO2: (a) The signal $V_0(t)$ on capacitor terminal; (b) $\hat{T}_{1,K}(t)$ and $\hat{T}_{2,K}(t)$, $K = 3.291$ V characteristics generated by PO2.

Across the 150 experiments, the parameters fell within the ranges in Table 4, corresponding to the average values indicated by (14).

Table 4. Ranges for the parameters of C2 in Figure 9 determined by PO2 for $K = 3.291$ V and their standard deviations.

\hat{T}_1 [ms] $\sigma_{\hat{T}_1}$ [%]	\hat{T}_2 [ms] $\sigma_{\hat{T}_2}$ [%]	\hat{C}_e [μF] $\sigma_{\hat{C}_e}$ [%]	\hat{R}_{se} [Ω] $\sigma_{\hat{R}_{se}}$ [%]
[18.4718 ÷ 18.4822] [0.13774 ÷ 0.19571]	[0.71102 ÷ 0.71285] [0.27062 ÷ 0.46067]	[202.088 ÷ 202.213] [0.14702 ÷ 0.20012]	[0.20516 ÷ 0.21592] [4.90394 ÷ 8.2696]

According to the frequency characteristics in Figure 10a,b, the equivalent values \hat{C}_e and \hat{R}_{se} from (14) correspond to frequencies of approx. 55.6 Hz and 59.5 Hz, respectively.

$$\hat{T}_1 = 18.474 \text{ ms}, \hat{T}_2 = 0.71193 \text{ ms}, \hat{C}_e = 202.15 \text{ μF}, \hat{R}_{se} = 0.21054 \text{ Ω}. \quad (14)$$

To investigate the impact of K 's assignment errors on the values of \hat{C}_e and \hat{R}_{se} obtained with PO2, six series of 25 capacitor discharge/charge experiments were performed for six different K values within the range [3.2836, 3.3036]. The parameter ω_0 of PO2 was set to the values of 7000 s^{-1} for the discharge phase, and $11,000 \text{ s}^{-1}$ for the charge phase. The experiments confirmed the aspects revealed by Figure 5 and Appendix A: \hat{T}_2 is increased due to the increase of K , \hat{C}_e variations are reduced, \hat{R}_{se} is pronouncedly increased, and the dispersion intervals of the parameters are reduced.

3.3. Scheme Based on the Implementation of the Principle from Figure 7d

The proposed scheme has the configuration of Figure 12. The converter supplies a load that is not purely resistive. The circuit was made for $R_1 = 0$ and $R_2 = 0$. In Figure 7d, the switches sw_{ij} were implemented with T-sw_{ij} transistors. Each of the capacitors C21 and C22 of the filter capacitor bank independently discharges across the resistors of the VEN, initially across the resistance R_{ext1} , then across the resistance $R_{ext2} \neq R_{ext1}$. Any discharge of a capacitor is immediately followed by a recharge of it from the converter, triggered when the PO completes the determination of the discharge time constant. Equivalent parameters \hat{C}_{e_i} and \hat{R}_{se_i} of the two capacitors C2i, $i = 1, 2$ are calculated as solutions of the systems of Equation (15). The load impedance does not appear in the equations.

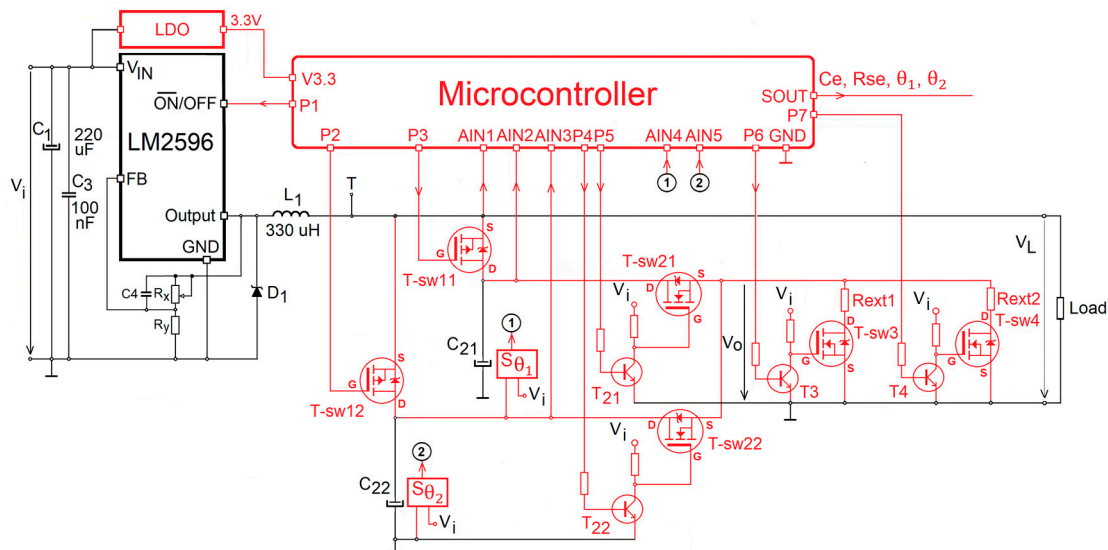


Figure 12. Buck converter scheme made based on the principle scheme in Figure 7d.

$$\begin{cases} \hat{C}_{e_i} \cdot (\hat{R}_{se_i} + R_{ext1}) = \hat{T}_{1_i} \\ \hat{C}_{e_i} \cdot (\hat{R}_{se_i} + R_{ext2}) = \hat{T}_{2_i} \end{cases}, \quad i = 1, 2. \quad (15)$$

Unlike the scheme in Figure 9, the scheme in Figure 12 contains two temperature sensors $S_{\theta 1}$ and $S_{\theta 2}$ that measure the operational temperature of each capacitor.

The proposed scheme has three key advantages: (i) The load is permanently connected to the buck converter; (ii) The time constants \hat{T}_{1_i} and \hat{T}_{2_i} , $i = 1, 2$ are determined on the beginning portions of the discharge waves $V_0(t)$, i.e., on the portions least affected by acquisition errors, with a favorable signal/noise ratio; (iii) The duration of an estimation process is of the order of the time constant.

A more complete picture of the behavior of the scheme in Figure 12 is given by the validation experiments presented below. The two stages differ in the nature of the converter load. In both stages, the parameter ω_0 of the PO was set to the value $10,000 \text{ s}^{-1}$.

Stage 1: Background: The converter feeds a resistive load $R_L = 20 \text{ } \Omega$ at a voltage $V_1 = 3.307 \text{ V}$. Filtering is performed with the pair of electrolytic capacitors C21—470 $\mu\text{F}/25 \text{ V}$, C22—220 $\mu\text{F}/25 \text{ V}$ having the frequency characteristics in Figure 13. The external resistances of VEN have the values $R_{ext1} = 3.321 \text{ } \Omega$ and $R_{ext2} = 89.16 \text{ } \Omega$. For processing, the same microcontroller as in Figure 9 was used, the signal $V_0(t)$ being acquired with an equivalent sampling time $h = 20 \text{ } \mu\text{s}$.

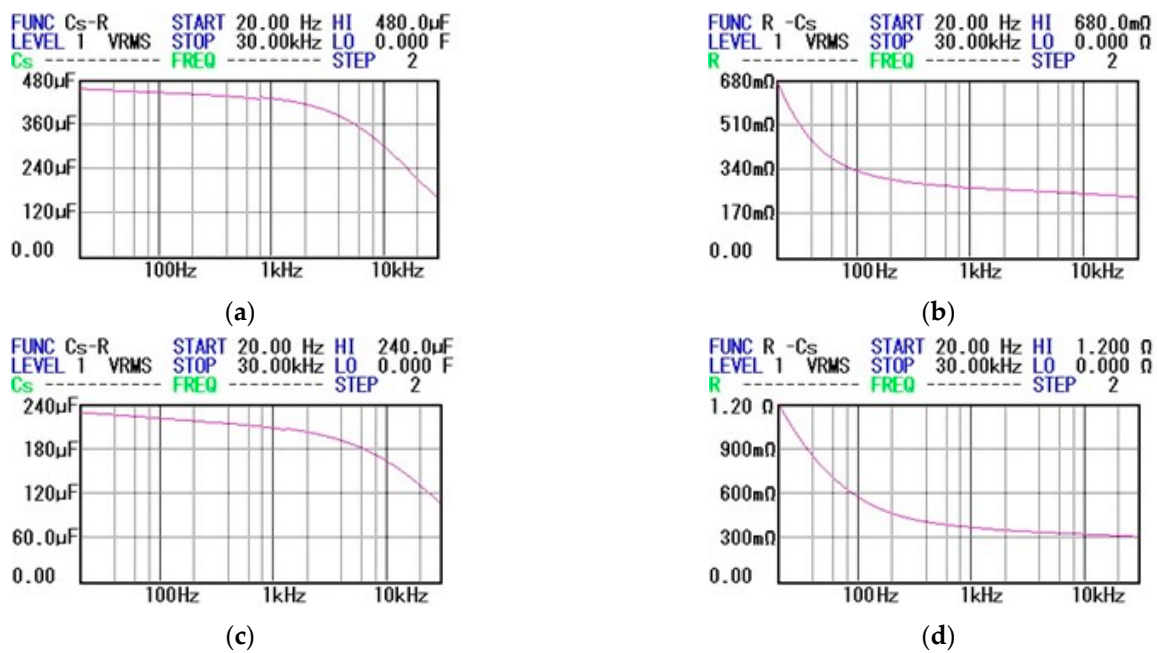


Figure 13. Frequency characteristics of the filter capacitors in Figure 12: (a,b) $C(f)$ and $R_s(f)$ characteristics of the electrolytic capacitor C21 (470 $\mu\text{F}/25 \text{ V}$); (c,d) $C(f)$ and $R_s(f)$ characteristics of electrolytic capacitor C22 (220 $\mu\text{F}/25 \text{ V}$).

Figure 14 shows an estimation process. Portions ①, ②, ③ and ④ in Figure 14a represent the characteristics, $\hat{T}_{1_1}(t)$, $\hat{T}_{2_1}(t)$, $\hat{T}_{1_2}(t)$ and $\hat{T}_{2_2}(t)$ provided by PO by processing the voltage $V_0(t)$ during the progress of the four partial discharges in Figure 14b. The values of $\hat{T}_{1_1}, \dots, \hat{T}_{2_2}$ from Equation (15) are given by the amplitudes of $\hat{T}_{1_1}(t), \dots, \hat{T}_{2_2}(t)$ from the final moments of the portions when the conditions of Equations (10) and (11) are checked. However, the moments of fulfillment of these conditions define the durations of the portions ①, ②, ③ and ④ not being necessary to monitor the time or voltage level V_0 . The time intervals between portions (① and ②, ..., ③ and ④) correspond to the charging of the capacitors and the transient regimes in the PO. Within these intervals, PO monitors the voltage $V_0(t)$ but does not calculate $\hat{T}_{1_i}(t)$ and $\hat{T}_{2_2}(t)$. The effect of connecting/disconnecting capacitors C21 and C22 on the voltage V_L measured from the load terminals of the microcontroller is shown in Figure 14c. The average voltage at the load terminals, \overline{V}_L , has different values depending slightly on the active filtering capacitor: $\overline{V}_L = 3.2895 \text{ V}$ in portions ① and ② where filtering is performed with C22, $\overline{V}_L = 3.2907 \text{ V}$

in portions ③ and ④ where filtering is performed with C21 and $\overline{V}_L = 3.2974$ V in normal operation when filtering is completed with both capacitors.

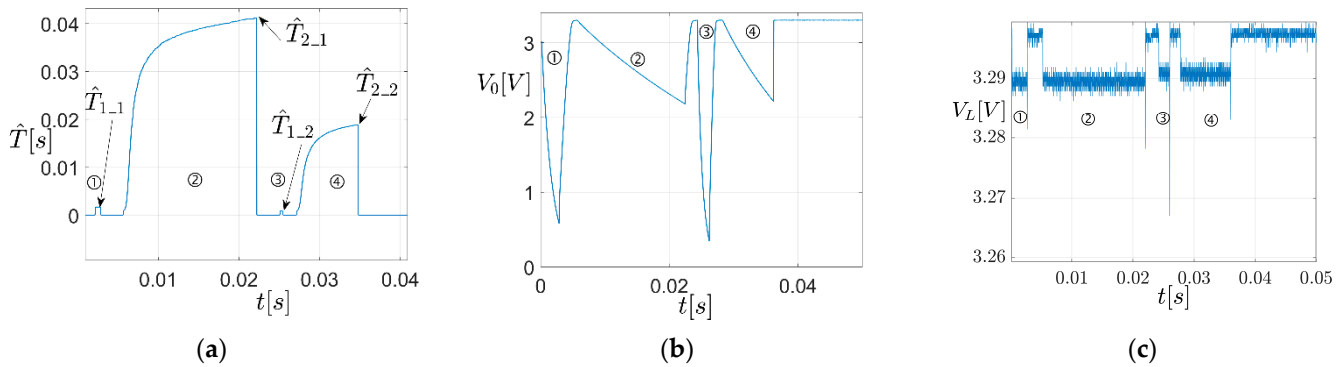


Figure 14. Experiment performed with the converter from Figure 12 in stage 1: (a) Characteristics $\hat{T}_{1,1}(t)$, $\hat{T}_{2,1}(t)$, $\hat{T}_{1,2}(t)$ și $\hat{T}_{2,2}(t)$; (b) Voltage variation $V_0(t)$ from the terminals of capacitors C21 and C22; (c) Voltage variation $V_L(t)$ at the load terminals.

In Table 5, the results obtained for six sets of 25 experiments are systematized. The average values of the parameters on the set of 150 experiments have the values in (16). Each set of experiments was repeated again with a period 0.3 s (3.33 Hz). Also, the duration of an experiment did not exceed 40 ms.

Table 5. Parameters estimated with PO for the buck converter in Figure 12 (average values, average squared deviations in absolute values, and in percentages compared to the average value) for the case C21—470 μ F/25 V, C22—220 μ F/25 V.

Capacitor	Parameter (P)	\overline{P}	σ_P	$\sigma_P[\%]$
C21	$\hat{T}_{1,1}[\text{ms}]$	1.68772	0.00051816	0.030702
	$\hat{T}_{2,1}[\text{ms}]$	41.20848	0.03851804	0.066143
	$\hat{C}_{e,1}[\mu\text{F}]$	460.4057	0.452717	0.09833
	$\hat{R}_{se,1}[\Omega]$	0.345	0.004538	1.315316
C22	$\hat{T}_{1,2}[\text{ms}]$	0.8836596	0.000506425	0.05731
	$\hat{T}_{2,2}[\text{ms}]$	18.98359	0.005894927	0.031053
	$\hat{C}_{e,2}[\mu\text{F}]$	210.8587	0.067257	0.0319
	$\hat{R}_{se,2}[\Omega]$	0.869533	0.00267	0.307099

$$\hat{C}_{e,1} = 460.4057 \mu\text{F}, \hat{R}_{se,1} = 0.345 \Omega, \hat{C}_{e,2} = 210.8587 \mu\text{F}, \hat{R}_{se,2} = 0.86953 \Omega. \quad (16)$$

The values $\hat{C}_{e,1}$ and $\hat{R}_{se,1}$ roughly correspond to the frequency range 65 Hz ÷ 80 Hz from the frequency characteristics in Figure 13a,b. The different values of the frequencies are due to the non-sinusoidal nature of the experimental regime and from the measurement errors mentioned in Appendix A.

Stage 2: Context: The converter feeds a resistive-inductive load. In series with the load resistance $R_L = 20 \Omega$ were connected separately, in series, then in parallel, two coils with $R' = 1.775 \Omega/L' = 0.463$ mH and $R'' = 1.8 \Omega/L'' = 0.426$ mH. For each of the 4 cases, six series of 25 experiments were performed. On the set of 600 experiments, the average values were obtained: $\overline{\hat{C}_{e,1}} = 465.8374 \mu\text{F}$, $\overline{\hat{R}_{se,1}} = 0.3123 \Omega$ for C21 and $\overline{\hat{C}_{e,2}} = 211.34 \mu\text{F}$, $\overline{\hat{R}_{se,2}} = 0.87595 \Omega$ for C22. The equivalent capacitance values are practically within $\pm 1\%$ of those in Table 5, while the ESR values are within much higher limits.

4. Discussion

1. The paper proposes two new DC-DC buck converter schemes shown in Figures 9 and 12. They are intended for real-time simultaneous estimation of the equivalent capacitance and the ESR of the converter filter capacitor. In both schemes, a PO coded on a microcontroller is used for estimation purposes. The schemes differ from the original converter scheme [29] by adding a microcontroller, some VENs composed of discharge or charge resistors with the related switches and temperature sensors, and in the first case also a stabilized voltage source. The VEN resistances are adopted taking into account the recommendations in Appendix A. Failure to comply with these recommendations results in high values of the dispersion of R_{se} , therefore, ESR calculation. Both schemes work in a quasi-online mode. This means that while estimating, the connection between the monitored capacitor and the converter load is interrupted for a few milliseconds. From the point of view of the continuity of the connection between the load and the converter during estimation, the first scheme operates in a quasi-online mode, while the second operates in an online mode.

2. The first scheme (Section 3.2) provides the equivalent parameters of the capacitor based on the estimation with a PO2 of the values of the equivalent time constants related to the discharge/charge process of the capacitor. The VEN only serves to charge the capacitor. Its discharge is carried out through the load resistance of the converter. Estimating the time constant of the charging process with a PO2 (Section 2.1) is a novel approach that requires prior experimental calibration of the K parameter, according to the capacitor charging conditions (Section 2.2). During parameter estimation, the scheme is in quasi-online mode of operation, characterized by the short-term disconnection (approx. 0.040 s) of the capacitor and the load from the converter. This means that the proposed scheme can trigger the estimation of the capacitor parameters only when the load is disconnected from the converter. Depending on the power load tolerance, this can be performed intermittently, more or less often, or when the converter is off.

Compared to the conditions in Appendix A, in the experiments presented in the paper, we worked with $\rho_R = 27.54$ and $\rho_2 = 0.06358$. As such, the condition $\rho_R \gg 1$ was met, while the condition for ρ_2 to be as close as possible to 1 could not be met for reasons of limiting the current through the circuit. This fact influenced the dispersion of the calculated \hat{R}_{se} values, the average value being 6.58677%. Consequently, the experiments with the scheme in Figure 9 show that PO2 can determine with a very good approximation the value of the equivalent capacity through a single discharge/charge process. Since the value of ρ_2 is small, the determination of the ESR value, however, requires performing a series of successive experiments and averaging the obtained values.

3. The second DC-DC buck converter configuration (Section 3.3) uses a pair of capacitors for filtering, connected in parallel, and a VEN consisting of two resistors. The estimation of the parameters of each capacitor is completed alternatively by processing the discharge voltage of each capacitor across each of the resistances of the VEN. The novelty of the proposed scheme lies in the sequential investigation of the two capacitors. The estimation of the equivalent parameters is completed for one capacitor at a time, while the load, together with the second capacitor, remains connected to the converter output. As a result, the scheme operates in a quasi-online measurement regime during which neither the filtering operation nor the load supply from the converter is interrupted. In this process, the filtering capacity changes in steps.

From the perspective of the conditions in Appendix A, the scheme used in the experiments was characterized by $\rho_R = 26.92$ and $\rho_{2_1} = 0.10419$ for the 470 μF capacitor C21 and $\rho_{2_2} = 0.2626$ for the 220 μF capacitor C22. In this case also, the scheme lends itself to determining with a good approximation the value of the equivalent capacities. For a purely resistive load of the converter, the impact of the higher values of ρ_{2_1} and ρ_{2_2} , in relation to the diagram in Figure 9 is visible: the dispersion of \hat{R}_{se_1} values are 1.31531%, and that of \hat{R}_{se_2} only 0.307099%. As a result, the values of the equivalent parameters of the filter capacitors, obtained in the mentioned experimental conditions, confirm the validity of the proposed scheme.

Theoretically, the proposed converter scheme can be applied regardless of the type of load: resistive or resistive-inductive. Experimentally, it was found that in the presence of the resistive-inductive load, the dispersion ranges of the values of \hat{R}_{se_1} and \hat{R}_{se_2} increased by approx. 5 times. The experiments carried out in this context failed to identify a cause that could explain this effect.

Finally, it should be noted that the method underlying the scheme in Figure 12 can also be used when the output filter of the converter is a battery of at least two capacitors connected in parallel.

4. Both schemes estimate equivalent parameters C_e , R_{se} and measure operating temperatures θ or θ_1 and θ_2 of the filter capacitors and send them out. The operating temperature is necessary to take into account its influence on the estimated values of the equivalent parameters [2]. Since the estimating process of the capacitor parameters with POs takes less than one second, the temperature of the investigated capacitor can be considered constant during the estimation.

5. The proposed DC-DC buck converter schemes are designed by completing the basic scheme of the converter (represented in black in Figures 9 and 12) with new components, including a microcontroller (represented in red in the two figures). This means additional costs for the converter. However, they offer the benefit of enabling predictive maintenance for the converter, leading to reduced operational costs in applications where increased reliability is required.

6. Each of the DC-DC buck converter schemes proposed in this paper is suitable for integration into a specialized integrated circuit. For example, in Figure 12, the integration can be based on the segmentation in Figure 15. The components within the boxed part of Figure 15 have been selected both for their technological integration feasibility and because they do not require parameterization in the application design process. Outside the integrable part are connected components that cannot be integrated (Load and coil L_1) and components whose parameters depend on the application (capacitors C_{21} , C_{22} , external resistors R_{ext1} , R_{ext2} and temperature sensors $S_{\theta1}$ and $S_{\theta2}$).

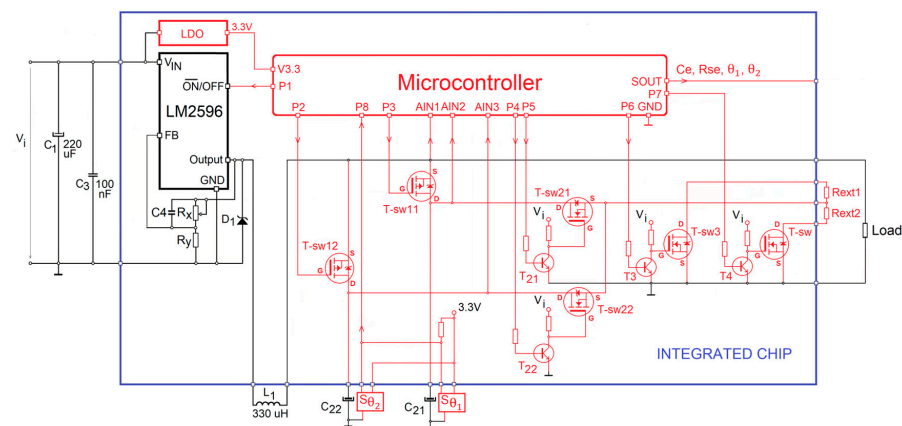


Figure 15. Integrated circuit diagram associated with the DC-DC buck converter in Figure 12. The integrated chip includes 6 switches ($T\text{-sw}_{ij}$, $i, j = \{1, 2\}$; $T\text{-sw}_i$, $i = \{3, 4\}$), the LM2596 circuit, the LDO circuit, and the microcontroller. The unembedded components are the filtering capacitors C_{21} , C_{22} , the VEN resistors R_{ext1} , R_{ext2} , the temperature sensors, the inductance L_1 , and the input capacitors C_1 , C_2 .

5. Conclusions

The article proposes two novel DC-DC buck converter schemes designed to monitor the ESR and equivalent capacitance of filter capacitors. For this purpose, parameter observers are used to calculate the equivalent parameter values of the capacitors quasi-online.

In the first scheme, the capacitor parameters are calculated by real-time processing of the voltage at the capacitor terminals during a discharge/charge process. By using the charging sequence, the duration of the estimation operation is reduced.

The second scheme achieves the output filtering by using two or more capacitors connected in parallel. In this way, the monitoring of the filter capacitors receives the advantage of the continuous supply of the load from the converter. The advantage of this connection type is that at least one filter capacitor remains connected and assures a non-interrupted supply of energy to the load. The equivalent parameters of each component capacitor are estimated in real time using two monitored discharges.

The experiments performed with both schemes, using electrolytic filter capacitors, shows that: (i) the estimation processes take approx. 40 ms; (ii) the equivalent capacity value is estimated with a precision of less than 0.25%; (iii) the estimation of the ESR value is performed with a precision dependent on both ESR and VEN resistor values.

The implementation of both schemes is associated with the acceptance of some compromises, such as limitations in the design of VENs imposed by the correlated values of the load resistance, as well as transient regimes of small amplitude occurring during the monitoring of the filter capacitor.

The estimation principles used in the two schemes are not limited to the proposed DC-DC buck converters. They are applicable in similar situations that need capacitor monitoring. Several future research opportunities open in this context, primarily by the application of the principles described in the proposed schemes for power converters and by the implementation of one of the two monitoring principles.

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Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

EMP	Electronic Measurement and Processing Device
ESR	Equivalent Serial Resistance
PO	Parameter Observer
PO2	Parameter observer on two edges
VEN	Variable Electrical Network

Appendix A

Computing formulas \hat{R}_{se} and \hat{C}_e obtained from system (13) have the expression (A1)

$$\hat{R}_{se} = \frac{\hat{T}_2 \cdot R_{ext1} - \hat{T}_1 \cdot R_{ext2}}{\hat{T}_1 - \hat{T}_2}, \quad \hat{C}_e = \frac{\hat{T}_1 - \hat{T}_2}{R_{ext1} - R_{ext2}}. \quad (A1)$$

They are valid in the following working assumptions:

- 1 The values of R_{se} , C_e , R_{ext1} and R_{ext2} are constant during the measurement of \hat{T}_1 and \hat{T}_2 from the signal $V_0(t)$ and have the same value for both transients.
- 2 The values of R_{ext1} and R_{ext2} are measured beforehand at a temperature equal to that during the measurement of \hat{T}_1 and \hat{T}_2 .

Let x be the measured value of a variable in (A1) or a calculated value for \hat{R}_{se} or \hat{C}_e , \check{x} the true value of x and ε_x the measurement or calculation error of x defined by formula (A2):

$$\varepsilon_x = \frac{x - \check{x}}{\check{x}}, \quad x \in \{R_{ext1}, R_{ext2}, \hat{T}_{1e}, \hat{T}_{2e}\}. \quad (A2)$$

By applying this formula to \hat{R}_{se} și \hat{C}_e in (A1), the Formulas (A3) and (A4) for error calculation $\varepsilon_{\hat{R}_{se}}$ and $\varepsilon_{\hat{C}_e}$ are derived. They used the notations (A5):

$$\varepsilon_{\hat{R}_{se}} = \frac{\rho_R(1 + \varepsilon_{\hat{T}_2})(1 + \varepsilon_{R_{ext1}}) - \rho_\tau(1 + \varepsilon_{\hat{T}_1})(1 + \varepsilon_{R_{ext2}})}{\rho_2[\rho_\tau(1 + \varepsilon_{\hat{T}_1}) - (1 + \varepsilon_{\hat{T}_2})]} - 1, \tag{A3}$$

$$\varepsilon_{\hat{C}_e} = (1 + \rho_1) \frac{1 + \varepsilon_{\hat{T}_1} - \frac{1 + \varepsilon_{\hat{T}_2e}}{\rho_\tau}}{1 + \varepsilon_{R_{ext1}} - \frac{1 + \varepsilon_{R_{ext2}}}{\rho_R}} - 1, \tag{A4}$$

$$\rho_R = \frac{\widetilde{R_{ext1}}}{\widetilde{R_{ext2}}}, \rho_{T_e} = \frac{\widetilde{T_1}}{\widetilde{T_2}}, \rho_1 = \frac{\widetilde{R_{se}}}{\widetilde{R_{ext1}}}, \rho_2 = \frac{\widetilde{R_{se}}}{\widetilde{R_{ext2}}}. \tag{A5}$$

To obtain a picture of the problem, we consider the experimental data in columns 2 and 3 of Table A1, taken from [28], Table VI. They refer to five electrolytic capacitors and were obtained using a VEN who provided $R_{ext1} \cong 980.7692 \Omega$ and $R_{ext2} \cong 0.08999984 \Omega$. In columns 4 and 5, the values obtained with formulas (A1) are inserted.

Table A1. Equivalent time constants experimentally determined in [28] for five electrolytic capacitors and equivalent capacitor parameters calculated with Formulas (A1).

Capacitor	\hat{T}_1 [s]	\hat{T}_2 [ms]	\hat{R}_{se} [mΩ]	\hat{C}_e [μF]
C1	7.941	0.86881	17.30	8096.56
C2	7.862	0.85763	16.90	8016.01
C3	7.946	0.89847	20.90	8101.63
C4	6.209	0.67340	16.37	6330.63
C5	4.774	0.56306	25.67	4867.48

To roughly establish the error ranges in which the calculated values for \hat{R}_{se} and \hat{C}_e fall, we assume that the measurement errors of \hat{T}_{1e} , \hat{T}_{2e} , R_{ext1} and R_{ext2} are located in the ranges $\varepsilon_{\hat{T}_1} \in [-0.01, 0.01]$, $\varepsilon_{\hat{T}_2} \in [-0.02, 0.02]$, $\varepsilon_{R_{ext1}} \in [-0.01, 0.01]$ and $\varepsilon_{R_{ext2}} \in [-0.02, 0.02]$, that \widetilde{T}_1 and \widetilde{T}_2 take exactly the values from Table A1, and $\widetilde{R_{ext1}}$ and $\widetilde{R_{ext2}}$ have the values of R_{ext1} and R_{ext2} specified above. Consequently, using Equation (A5) yields the results in Table A2.

Table A2. Error ranges for calculated values of capacitors in Table A1.

Capacitor	$\frac{\rho_R}{\rho_{T_e}}$	$\frac{\rho_1}{\rho_2}$	$[\varepsilon_{\hat{R}_{se_min}}, \varepsilon_{\hat{R}_{se_max}}]$	$[\varepsilon_{\hat{C}_e_min}, \varepsilon_{\hat{C}_e_max}]$
C1	10897.45 9140.88	$1.76 \cdot 10^{-5}$ 0.192	$[-0.344708, 0.351977]$	$[-0.019908, 0.020208]$
C2	10897.45 9167.123	$1.73 \cdot 10^{-5}$ 0.188	$[-0.355805, 0.363399]$	$[-0.019908, 0.020208]$
C3	10897.45 8843.924	$2.13 \cdot 10^{-5}$ 0.232	$[-0.295129, 0.301498]$	$[-0.019908, 0.020208]$
C4	10897.45 9140.88	$1.67 \cdot 10^{-5}$ 0.182	$[-0.367653, 0.375486]$	$[-0.019908, 1.020208]$
C5	10897.45 8478.67	$2.61 \cdot 10^{-5}$ 0.285	$[-0.248404, 0.253828]$	$[-0.01990, 1.020208]$

Two observations emerge from these results for the case when $\rho_1 \ll 1$ and $(3 \div 4)\rho_2 \approx 1$:

3. The estimation errors of C_e with Formula (A1) are within $\pm 2\%$.
4. R_{se} estimation errors with Formula (A1) vary practically between limits of $\pm 25\%$ to $\pm 37\%$.

The wide error limits from the last observation are due to the relatively small values of the ρ_2 ratio. This finding is corroborated by (A3) which highlights a hyperbolic variation of $\varepsilon_{\hat{R}_{se}}$ with respect to ρ_2 . The lower the ρ_2 , the higher the $\varepsilon_{\hat{R}_{se}}$. In the range $\rho_2 \in [0.2, 1]$ inverse $1/\rho_2$ decreases from the value 5 to the value 1.

The objective pursued in the estimation methods of the equivalent parameters of a capacitor modeled by a serial connection R – C is to achieve the approximations $\hat{R}_{se} \cong \widetilde{R}_{se}$ and $\hat{C}_e \cong \widetilde{C}_e$, i.e., $\varepsilon_{\hat{R}_{se}} \cong 0$ and $\varepsilon_{\hat{C}_e} \cong 0$. Assuming that the measurement errors can be minimized from a technical point of view, the means of achieving the objective consists in the appropriate manipulation of the values of the ratios $\rho_R \cong \rho_{T_e}$ and ρ_1 or ρ_2 , practically of the values of the resistances R_{ext1} and R_{ext2} .

To obtain $\varepsilon_{\hat{R}_{se}}$ as close as possible to 0 the value of R_{ext2} must be adopted as low as possible, so that ρ_2 is as high as possible. Ensuring high values of ρ_2 is in principle a critical problem from the electrical point of view because discharging the capacitor over a resistance of value $2 \times R_{se}$, from an initial voltage $V_0(0)$ suitable for measurement, is equivalent to short-circuiting it. Moreover, the value of T_2 becoming very small, the time available for measuring T_2 becomes very short, which could also become a critical problem for the online implementation of the measurement method in order to monitor the capacitor parameters. Also, a small value of T_2 is likely to cause an increase in the absolute value of the measurement error $|\varepsilon_{\hat{T}_2}|$. Hence, R_{ext2} should be chosen so that the initial current $V_0(0)/(R_{ext2} + R_{se})$ is, on the one hand, as high as possible, and on the other hand, it does not endanger the capacitor and the resistor. To obtain a $\varepsilon_{\hat{C}_e}$ as close as possible to 0 the ratio ρ_R must have a value as high as possible. Once R_{ext2} is adopted, there are no problems adopting the value of R_{ext1} .

In conclusion, for designing the monitoring circuit, in order to provide the best estimates for both Formula (A1), it is necessary to assure:

5. $\rho_R \gg 1$, i.e., $R_{ext1} \gg R_{ext2}$;
6. ρ_2 , i.e., $\widetilde{R}_{se}/\widetilde{R}_{ext2}$, as close as possible to 1.

If these requirements are not met, the \hat{R}_{se} formula leads to erroneous estimates, strongly influenced by the errors in the measurements of \hat{T}_{1e} , \hat{T}_{2e} , R_{ext1} and R_{ext2} , even when they are only a few percent. In this case, the formula of \hat{C}_e will also produce errors outside the range of $\pm 2\%$.

For DC-DC buck converters in this paper, the following values were used:

- Converter in Figure 9: $R_{ext1} = R_L = 91.19 \Omega$, $R_{ext2} = 3.311 \Omega$, $\hat{R}_{se} = 0.21054 \Omega$, $\rho_R = 27.54$ and $\rho_2 = 0.06358$;
- Converter in Figure 12: $R_{ext1} = 3.311 \Omega$, $R_{ext2} = 89.16 \Omega$, $\hat{R}_{se_1} = 0.345 \Omega$, $\hat{R}_{se_2} = 0.86953 \Omega$, $\rho_R = 26.92$, $\rho_{2_1} = 0.10419$ for C21 and $\rho_{2_2} = 0.2626$ for C22.

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