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A Fully Integrated High Linearity CMOS Dual-Band Power Amplifier for WLAN Applications in 55-Nm CMOS

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Abstract: This paper presents a dual-band fully integrated high linearity CMOS power amplifier (PA). The PA employs a reconfigurable transformer in the input matching network to achieve low reflection coefficient across both bands, demonstrating significant flexibility in the design of dual-band power amplifiers with high output powers. Additionally, a detailed design methodology for the dual-band matching network is introduced. By utilizing this methodology, the PA has been designed using 55 nm CMOS technology. For continuous-wave operation, the PA achieves a saturated power (P_{sat}) of 28.03 dBm and 27.5–28.2 dBm, with power-added efficiency (PAE) of 33.2% and 24.6–31.1%, in the 2.4 GHz and 5 GHz WLAN bands, respectively. Concurrently, the PA power cells, which employ multi-gate transistor (MGTR) technology, achieve an intermodulation distortion (IMD3) of below 30 dBc at an output power of 15 dBm in both the 2.4 GHz and 5 GHz WLAN bands. The proposed PA outperforms other dual-band or multi-band PAs in terms of output power and exhibits great potential for WLAN applications.

Keywords: CMOS power amplifier; dual band; transformer; wireless local area network (WLAN)

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1. Introduction

In recent years, wireless local area network (WLAN) technology has experienced rapid development and application across billions of mobile devices such as computers, smartphones, and tablets. To meet the requirements of high data throughput applications such as video conferences and 4K video streaming, WLAN standards have continuously increased signal bandwidth and adopted more advanced techniques. The current 802.11ax standard utilizes OFDMA technology and a 1024 QAM modulation scheme to boost data throughput, achieving a data rate of 9.6 Gbps. The development of new WLAN standards is drawing much effort in academia and industry. Additionally, system-on-chip (SoC) implementation with CMOS technology for WLAN applications has been the focus of attention in recent years [1–6].

IEEE 802.11ax devices need to operate in two frequency bands and also require compatibility with previous WLAN standards. Integrating multiple channel transceivers operating in different bands on a single chip is a common approach [7–11]. However, this approach results in a large chip area, which means the cost will be high. A preferable alternative is using a single transceiver supporting reconfigurable 2.4/5 GHz operation.

As the core block of the transmitter, power amplifiers should also support either dual-band or broadband operation, with a bandwidth that covers at least both the 2.4 GHz to 5 GHz bands. Currently, the design of broadband power amplifiers primarily relies on high-order matching networks [12–16]. However, for broadband amplifiers that comply with IEEE 802.11ax standards, the required operating bandwidth is extensive (at least from 2.4 GHz to 5.9 GHz), which necessitates a substantial matching network area. Furthermore, because high-order matching networks require multiple inductors or transformers

for matching, they inherently increase matching network losses and significantly reduce the power amplifiers' efficiency. Consequently, dual-band or multi-band power amplifiers employing switching capacitors or varactors [17–20] are more effectively suited for reconfigurable transmitters. However, the output power of current dual- or multi-band power amplifiers are not sufficiently high for certain WLAN applications (typically below 26 dBm). To address this issue, this paper aims to design a fully integrated dual-band power amplifier with improved output power. Additionally, existing dual- and multi-band power amplifier design methodologies struggle to meet high power output requirements. This paper proposes a new design methodology focused on optimizing the insertion loss of the matching network to achieve dual-band matching. This proposed methodology is highly universal and easily replicable. Based on the proposed design methodology, this paper develops a low-loss matching network, enabling the power amplifier to achieve sufficiently high output power. On the other hand, while some optimization methods for improving power amplifier linearity have been proposed [21–23], existing dual- or multi-band power amplifiers lack specific explanations and optimizations for linearity. This paper analyzes the causes of nonlinearity in power amplifiers and employs multi-gate transistor (MGTR) [24] technology to enhance linearity, enabling the power amplifier to achieve high linear output power.

The paper is organized as follows: Section 2 first introduces the topology of reconfigurable dual-band output matching network and then proposes a design methodology for the dual-band matching network based on passive insertion loss at both 2.4 GHz and 5 GHz. Finally, a reconfigurable transformer is thoroughly studied and subsequently employed in the proposed dual-band input matching network to achieve a low reflection coefficient across both bands. Section 3 describes the detailed circuit implementations. Section 4 presents the simulation results of the proposed CMOS PA. Section 5 discusses the research direction of CMOS PAs for WLAN applications, and Section 6 concludes this article.

2. Design of Dual-Band Matching Networks

2.1. Design of Dual Band Output Matching Networks

The design of the dual-band output matching network is crucial to achieving high output power across dual frequency bands. To achieve this goal, the dual-band output matching network should transform the 50 ohm impedance to the optimum load impedance of the power amplifier at both frequency bands. Additionally, the dual-band output matching network is required to maintain minimal loss at both frequency bands. This paper employs the reflection coefficient and insertion loss of the dual-band output matching network as guidance.

The optimal load impedance of the PA is given by a load resistance in parallel with an equivalent negative capacitance [17] and determined through load-pull simulations, as

$$Z_{opt}(\omega) = R_{opt} // \left(\frac{-1}{j\omega C_{out}} \right) \quad (1)$$

In this design, the simplified output matching schematic is shown in Figure 1. The reconfigurable output matching network comprises a fixed transformer and switching capacitors C_{sws}, which can adjust the load impedance seen in the matching network to achieve the optimum impedance in the two bands of interest. Ideally, the reflection coefficient $\Gamma_{ins} = 0$ and $IL_{output} = 0$. However, due to the Bode-Fano limit [25] and transformer parasitic resistance, the ideal matching network is unachievable. Thus, in practice, we set $|\Gamma_{ins}| \leq -20$ dB and $|IL_{output}| \leq 1.5$ dB as the target.

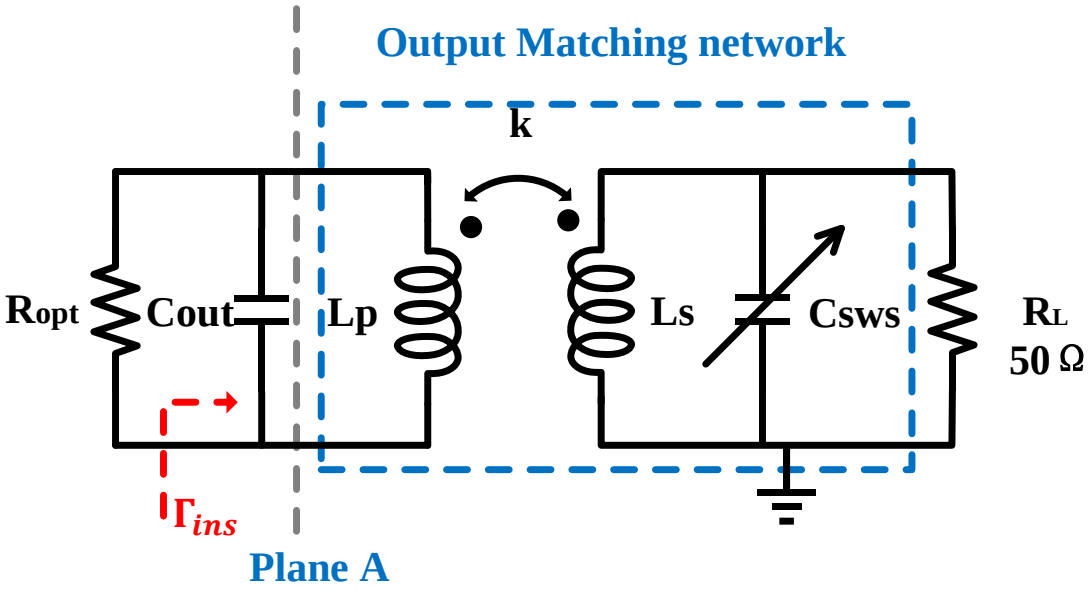

Figure 1. Simplified schematic of output matching circuit.

The *Z*-parameter matrix for the transformer is as follows [26]:

$$Z = \begin{bmatrix} R_p + j\omega L_p & -j\omega M \\ j\omega M & -(R_s + j\omega L_s) \end{bmatrix} \tag{2}$$

where

$$M = k\sqrt{L_p L_s} \tag{3}$$

and k represents the coupling factor between primary and secondary coils.

Therefore, the equivalent load impedance for the power amplifier (PA) can be derived as Equation (4).

$$Z_{load} = \left\{ R_p + \frac{(\omega M)^2 (R_s + R_{eq})}{(R_s + R_{eq})^2 + (\omega L_s + X_{eq})^2} \right\} + j\left\{ \omega L_p - \frac{(\omega M)^2 (\omega L_s + X_{eq})}{(R_s + R_{eq})^2 + (\omega L_s + X_{eq})^2} \right\} \tag{4}$$

where

$$\mathrm{R}_{eq} = \frac{R_L}{1 + (\omega R_L C_{sws})^2} \tag{5}$$

$$\mathrm{X}_{eq} = \frac{-\omega {R_L}^2 C_{sws}}{1 + (\omega R_L C_{sws})^2} \tag{6}$$

So $|\Gamma_{ins}|$ and IL can be derived as

$$|\Gamma_{ins}| = 20log\left|\frac{Z_{ins} - R_{opt}}{Z_{ins} + R_{opt}}\right| \tag{7}$$

$$IL_{output} = 20log\left|\frac{j\omega M}{(\mathrm{R_s} + R_{eq}) + j(\omega \mathrm{L_s} + X_{eq})} \cdot \frac{C_{out} - Z_{ins}}{(Z_{ins} + R_{opt})C_{out}} \cdot \sqrt{\frac{R_{opt}}{R_L}}\right| \tag{8}$$

where

$$Z_{ins} = C_{out} // Z_{load} \tag{9}$$

It can be seen that there are three main parameters (L_p, L_s and C_{sws}) to be determined. Considering the matching target, we calculate the minimum value of the $|\Gamma_{ins}|$ and IL by sweeping values of the main parameters to find the optimum value range of L_p and L_s,

where the value of C_{sws} is chosen to minimize the reflection coefficient and insertion loss. During this process, the quality factors of transformer windings are both assumed to be 12 at 2.45 G and 14 at 5.5 G, while the coupling factor of transformer windings is assumed to be 0.75, which are reasonable values for practical transformers in CMOS process. In addition, the value range of C_{sws} is limited to 0–3 pF, and the value of C_{sws} above 3 pF is regarded as unacceptable and is abandoned because of the low quality factor and large off-state capacitance (C_{off}). So far, the values of the components in the proposed dual-band output matching network have been preliminarily determined.

2.2. Implementation of Dual-Band Output Matching Network

Now, we can take the next step to implement the dual-band output matching network according to the proposed methodology. The simulated power and PAE contours for 2.4 and 5.5 GHz are shown in Figure 2. In general, the pursuit is not singularly focused on either efficiency or output power; instead, a tradeoff between output power and PAE is normally made. In this design, the optimal load impedances are determined as 15.05 + j15.08 at 2.45 G and 9.87 + j15.86 and 5.5 G, respectively. The corresponding R_{opt} and C_{out} are 30.17 Ω and 2.16 pF at 2.4 GHz and are 35.36 Ω and 1.32 pF at 5.5 GHz.

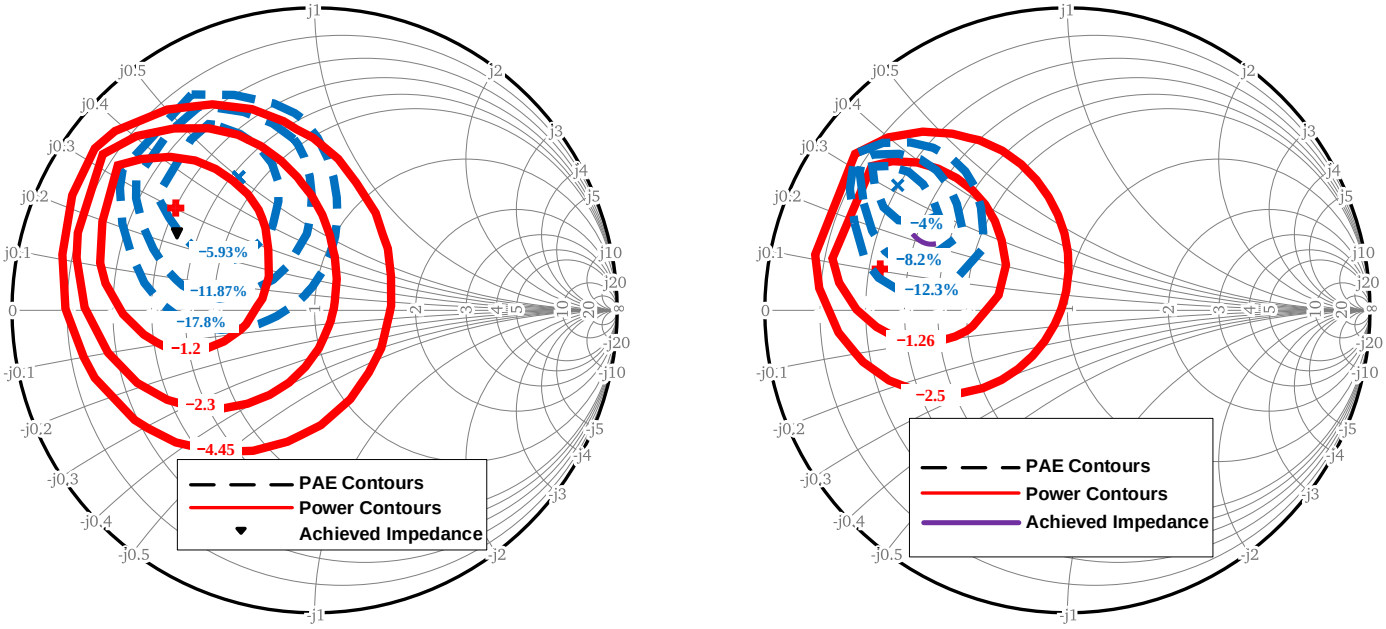

Figure 2. Simulated power contours and PAE contours in 2.4 and 5 GHz bands. (**a**) 2.4 GHz. (**b**) 5.5 GHz.

Therefore, the calculated values of the $|\Gamma_{ins}|$ and IL are plotted in Figures 3 and 4. Thus, we now have the optimum values of L_p, L_s, and C_{sws}.

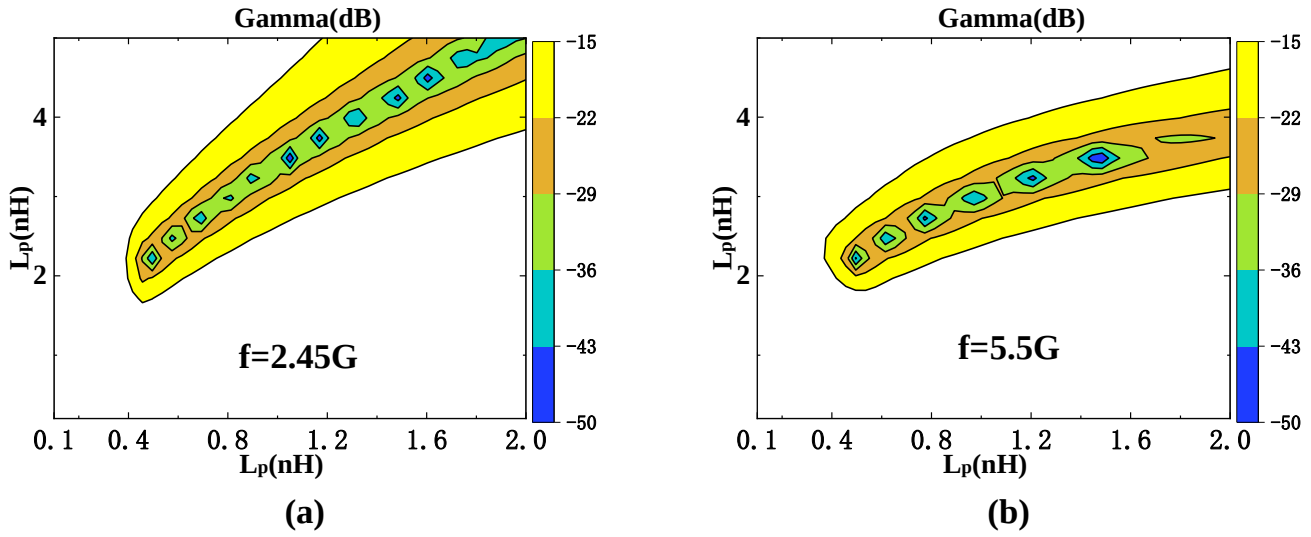

Figure 3. Reflection coefficient contours of output matching network. (**a**) 2.45 G. (**b**) 5.5 G.

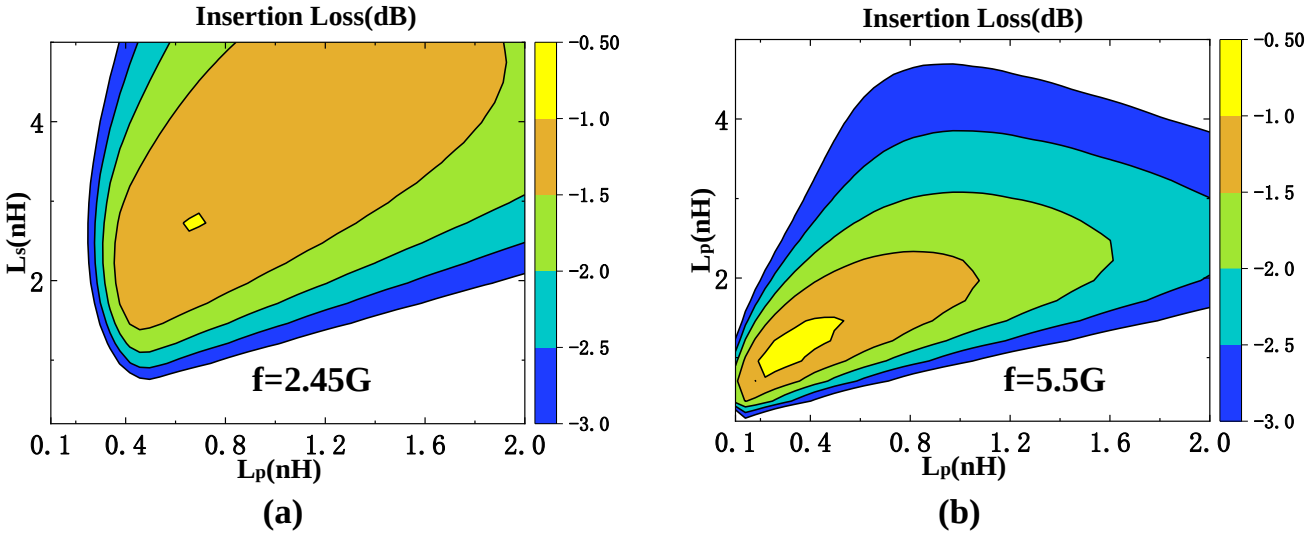

Figure 4. Insertion loss contours of output matching network. (**a**) 2.4 G. (**b**) 5.5 G.

We then take the next step to implement the output matching network with optimum values. In this design, the used CMOS process only has one thick metal layer. Consequently, all inductor coils are designed using the thickest metal layer with an octagonal shape to enhance the Q value of the inductors. To further improve the quality factor of the transformer, this design integrates a patterned ground shielding (PGS), constructed from poly layers, into the on-chip transformer to mitigate substrate losses. Simultaneously, a low doping substrate beneath the transformer is used to increase resistivity, thereby reducing the substrate magnetic losses. Therefore, the total layout of the transformer is depicted in Figure 5, and the parameters obtained from electromagnetic (EM) simulation for L_p, L_s, and k are as shown in Table 1.

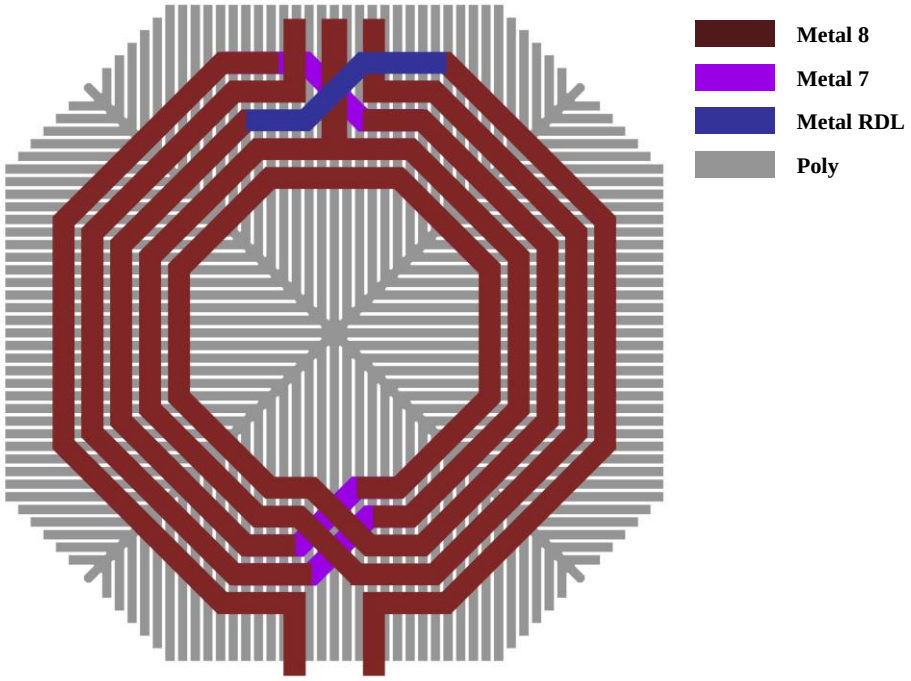

Figure 5. Layout of output transformer.

Table 1. Parameter of output transformer.

	Inductance	Quality Factor (Q)	Coupling Coefficient (k)
L_p	1.49 nH	16.33	0.75
L_s	2.83 nH	19.39	

The schematic of the switching capacitor is shown in Figure 14. Two stacked thick-gate transistors are used, considering reliability when the switch is closed [16,27]. The quality factor of the switching capacitor is mainly determined by the on-resistance of the switching transistors, while the on-resistance is determined by the size of the transistor. To increase the quality factor of the switching capacitor, larger transistor sizes are preferred. However, larger transistor sizes result in a larger parasitic capacitance in the off state, which is a capacitance that must be considered in the matching network. Therefore, the size of the switch needs to be carefully balanced, taking into account both on-state resistance and off-state capacitance.

The on-resistance and off-state parasitic capacitance have been simulated for different transistor sizes, as shown in Figure 6. In this design, the C_{sws} is 1.37 pF, and the switching transistor size is 900 µm/280 nm. Furthermore, by using parallel switching capacitors, the parasitic resistance of the overall switching capacitors can be further reduced when the switches are closed.

Finally, the achieved output load impedance and the insertion loss of the output matching network in this design are shown in Figures 1 and 7. The insertion loss is higher than the target at the 5.5 GHz band due to the requirement of operating bandwidth at 2.4 G bands. The value of the transformer windings (L_p, L_s) cannot be too small, causing larger insertion loss in 5.5 GHz band, and the degradation of the insertion loss is acceptable in practice. The simulation results demonstrate that the implemented output matching network exhibits superior matching performance across both the 2.4 GHz and 5 GHz frequency bands, fully validating the effectiveness of the dual-band matching network design methodology presented in this work.

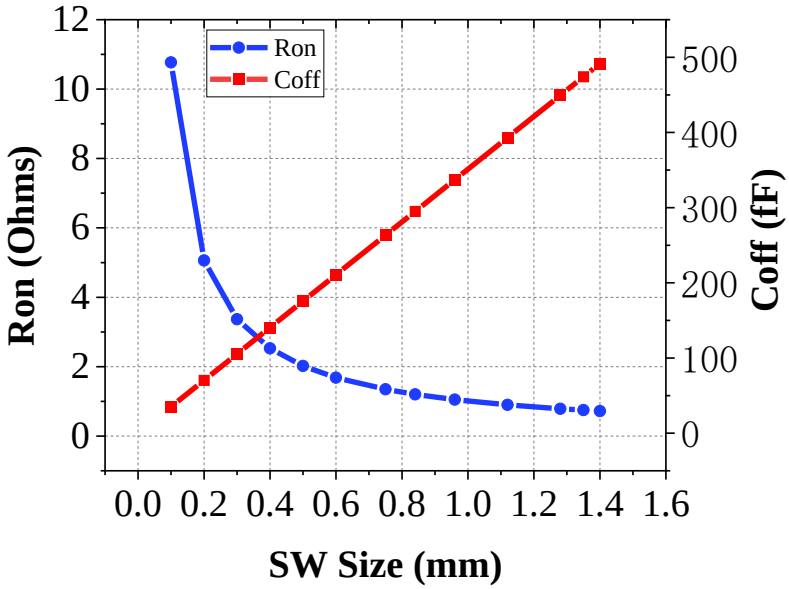

Figure 6. On-resistance and Coff of switch transistor versus size.

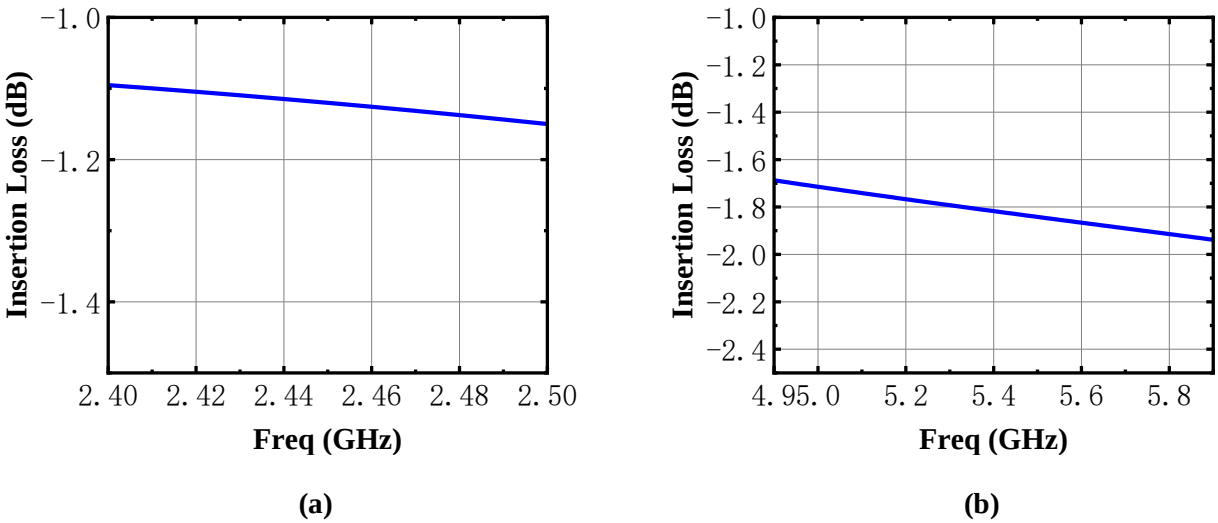

Figure 7. Achieved insertion loss of the output matching network. (**a**) 2.4 GHz. (**b**) 5 GHz.

2.3. Implementation of Dual-Band Input Matching Network

Different from the output matching, input matching is more sensitive to inductor and capacitor values. Small variations can have a significant impact on the reflection coefficient, making it challenging to achieve good matching within dual bands at high output power conditions. To address this issue, this article proposes a novel reconfigurable input matching circuit. The schematic is shown in Figure 8, and the input matching circuit consists of the switching capacitors and reconfigurable transformers. Applying a reconfigurable transformer significantly enhances dual-band input matching under high output power conditions. At the high-frequency band (5 GHz), the inductance values of the reconfigurable transformer decrease, ensuring effective input matching. Conversely, at the low-frequency band (2.4 GHz), the inductance values increase, facilitating optimal input matching at the lower band.

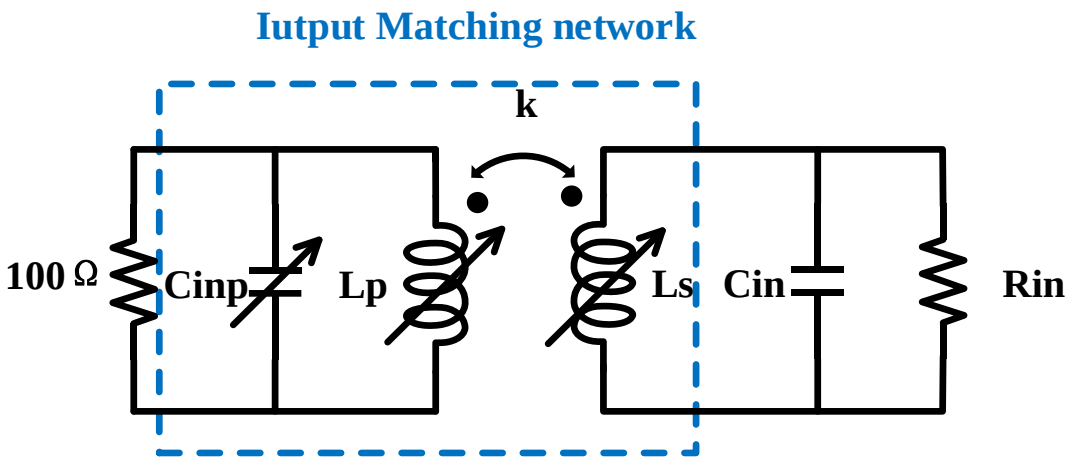

Figure 8. Reconfigurable input matching circuit.

The simplified schematic of the reconfigurable transformers is shown in Figure 9:

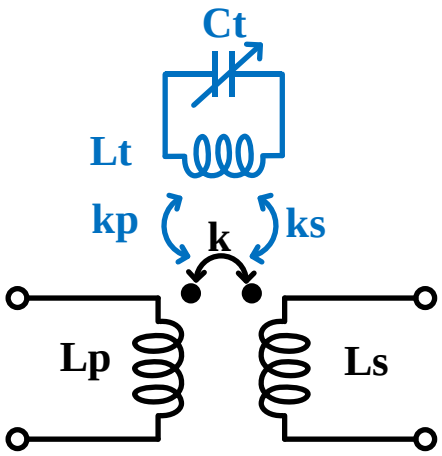

Figure 9. Simplified schematic of the reconfigurable transformer.

The reconfigurable transformer is composed of the main transformer windings (L_p, L_s), tuning inductor L_t, and tuning capacitor C_t. The tuning inductor L_t is magnetically coupled to the main transformer with coupling coefficients k_p and k_s, which is also connected directly with the tuning capacitor C_t. The reconfigurable transformer is based on a tunable inductor, which is shown in Figure 10. The R_t is the parasitic resistance of the entire tuning branch, which includes the parasitic resistances of both the resonant inductor L_t and the switching capacitor C_t. When the main inductor L_1 inputs a signal, the induced current I_t through L_t and C_t will generate an induced magnetic field. Thus, the total magnetic flux of the main inductor is influenced by the induced magnetic field, and so the equivalent inductance of the main inductor will be changed and can be derived as Equation (8).

$$L_{eq} = L_1 + \frac{L_1 L_t C_t k_t^2 \omega^2 \left(1 - L_t C_t \omega^2\right)}{\left(L_t C_t \omega^2 - 1\right)^2 + R_t^2 C_t^2 \omega^2} \tag{10}$$

$$R_{eq} = R_1 + \frac{C_t^2 L_1 L_t R_t k_t^2 \omega^4}{\left(L_t C_t \omega^2 - 1\right)^2 + R_t^2 C_t^2 \omega^2} \tag{11}$$

$$Q_{eq} = \frac{\left(1 - C_t^2 L_t^2 \left(k_t^2 - 1\right)\omega^4 + C_t\left(R_t^2 C_t + L_t\left(k_t^2 - 2\right)\right)\omega^2\right)\omega L_1}{C_t^2 L_t \left(L_1 R_t k_t^2 + R_1 L_t\right)\omega^4 + C_t R_1 \left(R_t^2 C_t - 2L_t\right)\omega^2 + R_1} \tag{12}$$

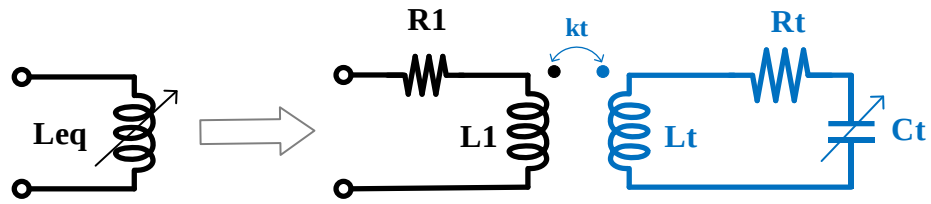

Figure 10. Simplified schematic of the tunable inductor.

Meanwhile, due to magnetic coupling, the quality factor of the main inductor is also manipulated and is derived as Equation (10). Figure 11a illustrates the variations in main inductance value and Q factor when the tuning capacitor C_t changes. Figure 7b shows the impact of R_t on the main quality factor. It can be seen that the values of the main inductor (L_1) and quality factor (Q) are significantly influenced by the tuning capacitor, while quality factor has low relativity to R_t, indicating that the tuning capacitor should be within an appropriate range to prevent a severe reduction in Q. On the other hand, changing the tuning capacitor within the appropriate range allows for changes in inductance with minimal impact on the Q factor. The reconfigurable transformer in this work is formed by one tunable inductor L_t. Thus, the values of the main reconfigurable transformer windings are influenced by L_t, C_t with coupling factor k_p, k_s.

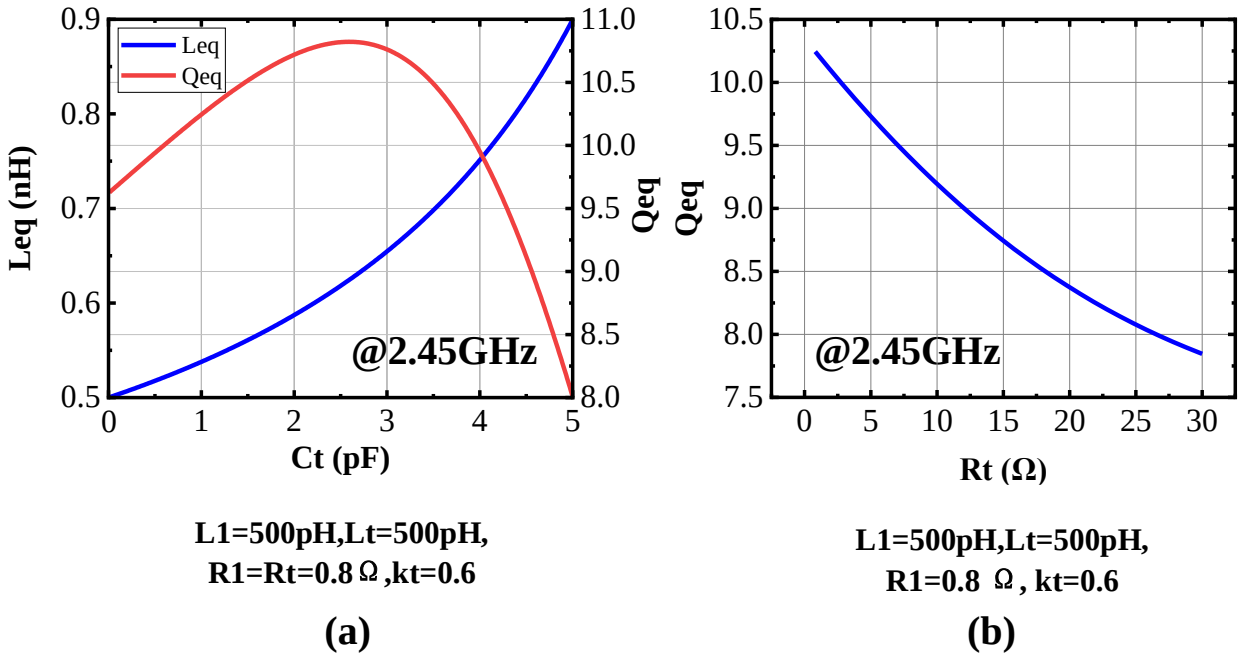

Figure 11. (**a**) Equivalent inductance and quality factor versus C_t. (**b**) Equivalent quality factor versus R_t.

By applying the proposed dual-band matching network design methodology, the required transformer parameters of the input matching network can be determined. Moreover, the incorporation of the reconfigurable transformer in this work substantially expands the inductance range of the practical transformer, thereby enabling more effective dual-band input matching. We then take the next step to implement the input matching network with optimum values. The layout of the reconfigurable transformer is shown in Figure 12, with a turn ratio of 2:2 for the main transformer and the tuning coil located on the outermost layer. All inductor coils employ the same metal layer to enhance the quality factor of the transformer. To avoid a significant impact on the Q values of L_p and L_s, the maximum value of C_t should not exceed 3 pF. The value of C_t in this design is 2.8 pF.

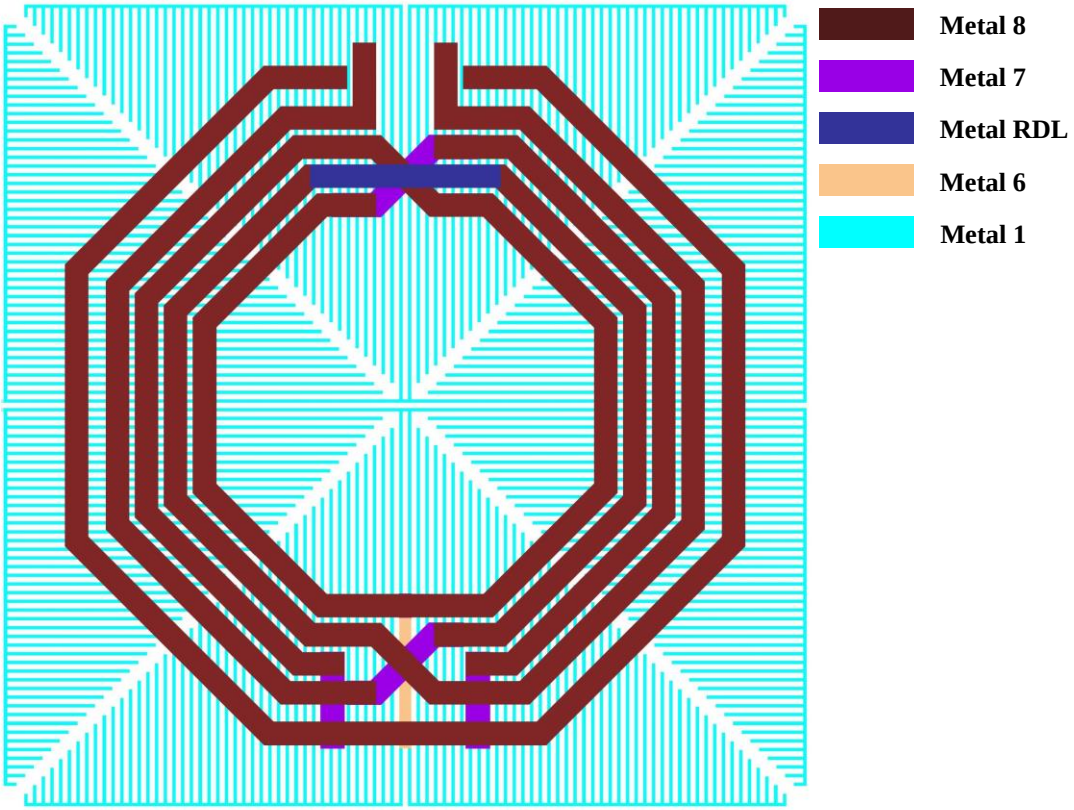

Figure 12. The layout of the reconfigurable transformer.

When the switching capacitor C_t changes, the values of the reconfigurable transformer are changed and are shown in the table below.

It can be seen that the proposed reconfigurable transformer in this paper achieves a change of approximately 100 pH in inductance with an acceptable decrease in Q. This feature is advantageous for achieving dual-band input matching. The final schematic of the dual-band input matching network is shown in Figure 8. The transistor sizes of the switch C_{inp} and C_t are 450 µm/280 n and 540 µm/280 n, respectively. The off capacitances of the switches are 307 fF and 513 fF. The parameter of the reconfigurable transformer is shown in Table 2.

Table 2. Parameters of reconfigurable transformer.

SW-Off		**SW-On**	
L_p	1.03 nH	L_p	1.15 nH
Q_p	8.39	Q_p	7.55
L_s	877.15 pH	L_s	936.65 pH
Q_s	9.56	Q_s	9.21
k	0.76	k	0.77

In comparison to a fixed transformer, the reconfigurable transformer proposed in this article demonstrates excellent impedance matching, as shown in Figure 13. It is evident that under the same matching capacitor conditions, the lowest point of S_{11} for the fixed transformer deviates significantly from the expected frequency bands. To match within the desired frequency bands, the capacitance value needs to be increased to 3.7 pF under fixed transformers, which is unacceptable for the circuit. On the one hand, this decreases the Q value of the switch capacitor, leading to a reduction in gain. On the other hand, it increases off-state parasitic capacitance, resulting in poor S_{11} performance in the 5 G frequency band.

It can be seen that with the implementation of the proposed reconfigurable transformer, favorable matching results are achieved in dual bands.

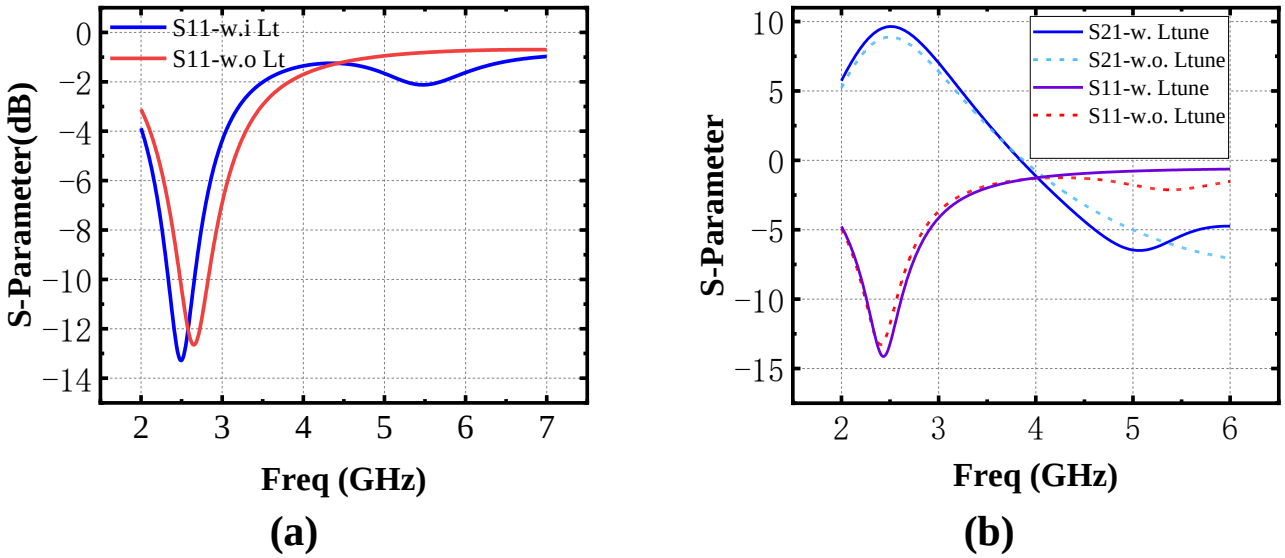

Figure 13. S-parameter comparison with fixed transformer. (**a**) Same C_{inp}. (**b**) Larger C_{inp} in fixed transformer.

3. Circuit Implementation

The complete schematic of the proposed power amplifier in this article is shown in Figure 14. It consists of three parts: the matching networks, the PA power cell, and the integrated bias circuits. The power cell employs a differential structure to suppress even-order harmonics and reduce linearity degradation caused by the ground bonding wires.

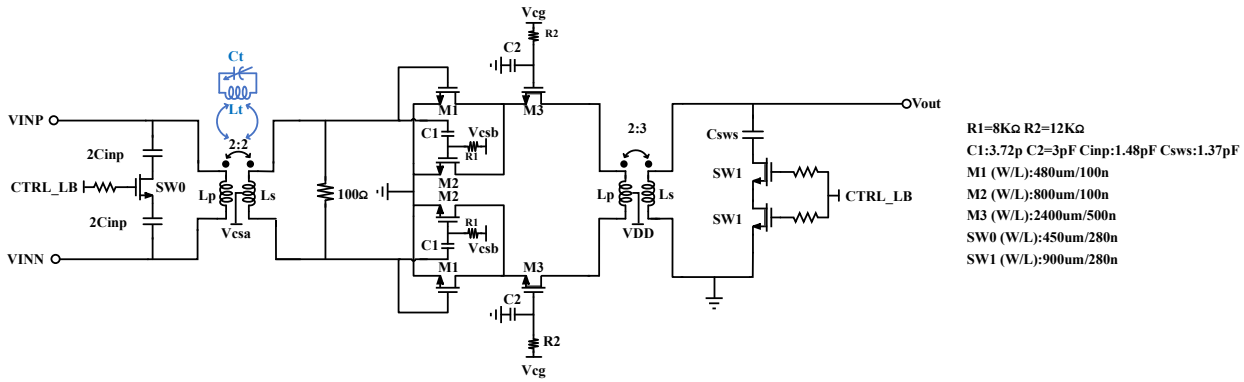

Figure 14. The complete schematic of the proposed power amplifier.

3.1. Cascode PA Power Cell

IEEE 802.11ax employs 1024 QAM modulation to boost data rate, which imposes stringent linearity requirements on power amplifiers. As a result, power amplifiers for WLAN applications are usually biased to Class AB to take a balance between linearity and efficiency. CMOS PAs usually use cascode devices to provide high output power and enhance reliability. In this design, PA needs to deliver an average power of 17 dBm for a 802.11ax signal. Considering at least 10 dB PAPR (peak-to-average ratio) of the signal, the transistor sizes of the common source and common gate devices are set to 2.56 mm/100 nm and 4.8 mm/500 nm, respectively, so the PA can ideally deliver a maximum output power of 29 dBm under a 3.3 V supply.

To reduce the distortion of the PA, we analyze the cause of the distortions. The most significant source of nonlinearity in power amplifiers arises from the drain current. In general, the drain current of transistors can be expressed by the power series and represented as

$$i_d = g_m V_{gs} + g_d V_{ds} + g_{m2} V_{gs}^2 + g_{d2} V_{ds}^2 + g_{md} V_{gs} V_{ds} + g_{m3} V_{gs}^3 + \cdots \tag{13}$$

The g terms represent the transconductance, drain conductance, and cross terms. In modern communication systems, nonlinear distortion is usually studied using a two-tone signal test. For simplicity, higher order nonlinearities are ignored. In addition, assuming that the optimum load impedance is a pure real value at the fundamental frequency due to the resonance of the imaginary part, the nonlinear lower and upper IM3sof the output voltage can be derived and simplified as

$$\begin{aligned} V_{ds}(2\omega_2 - \omega_1) \approx R_L(\omega_L) \Big[&\tfrac{3}{4} g_{m3} A^3 + \tfrac{1}{2} Z_L(\omega_2 - \omega_1) g_{m2} g_{md} A^3 \\ &+ \tfrac{1}{4} Z_L(2\omega_c) g_{m2} g_{md} A^3 \Big] \end{aligned} \tag{14}$$

$$\begin{aligned} V_{ds}(2\omega_1 - \omega_2) \approx R_L(\omega_L) \Big[&\tfrac{3}{4} g_{m3} A^3 + \tfrac{1}{2} Z_L(\omega_1 - \omega_2) g_{m2} g_{md} A^3 \\ &+ \tfrac{1}{4} Z_L(2\omega_c) g_{m2} g_{md} A^3 \Big] \end{aligned} \tag{15}$$

where

$$\omega_c = \frac{(\omega_1 + \omega_2)}{2} \approx \omega_1 \approx \omega_2 = \omega_L \tag{16}$$

where ω_1 and ω_2 are lower and upper two-tone input frequencies, respectively, and Z_L is the frequency-dependent load impedance. It can be seen that the IMD3 of the circuit is highly dependent on the third-order transconductance (g_{m3}) of the transistor. The third-order transconductance of the transistor exhibits a strong dependence on its bias voltage, as demonstrated in Figure 15. Notably, we can observe that there is a sweet spot for the third-order transconductance, where the IMD3 distortion can be minimized.

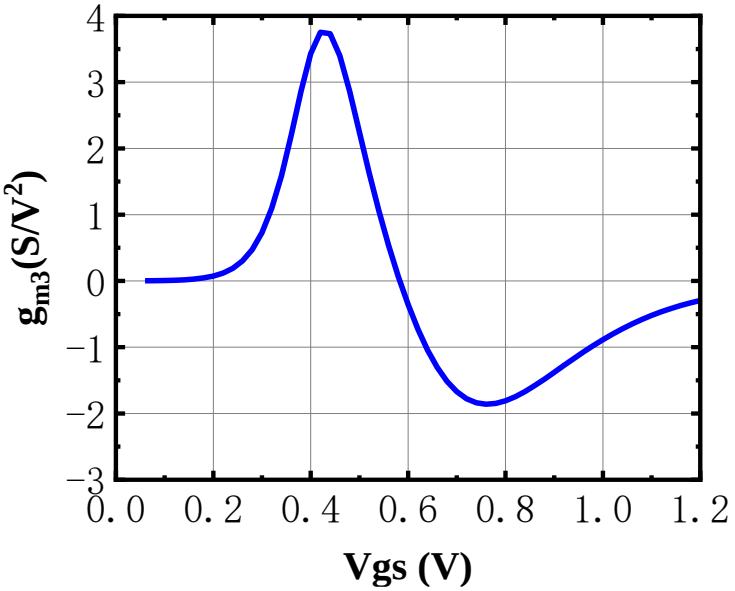

Figure 15. g_{m3} vs. gate voltage.

To expand the sweet spot range of the third-order transconductance across the expected power range, this work divides the power cell into two sections, each with different bias voltages. By compensating for the nonlinear components produced by each power cell operating under different bias conditions, the overall power amplifier achieves a low

IMD3 distortion. Figure 16 compares the IMD3 performance of the circuit with and without using MGTR. It can be seen that after adopting MGTR technology, the circuit's IMD3 distortion can be effectively suppressed by choosing an appropriate combination of different bias voltages.

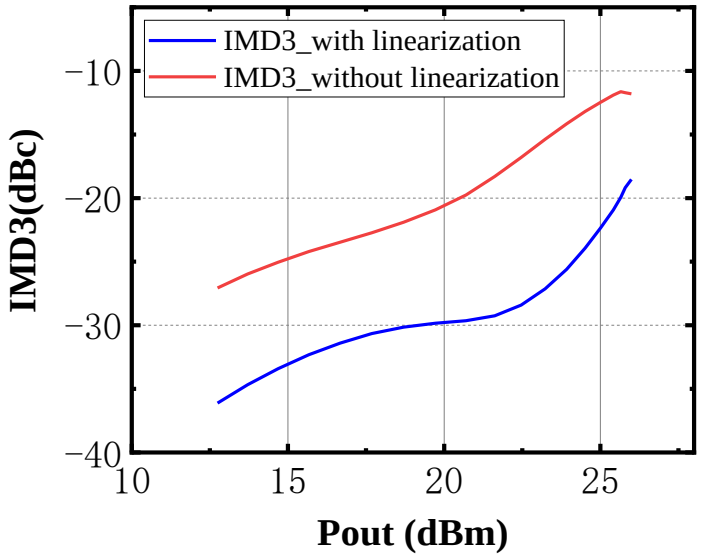

Figure 16. Comparison of IMD3 with and without MGTR.

3.2. The Integrated Bias Circuit

The linearity of the power amplifier is closely related to its bias voltage. CMOS integrated bias circuits can be employed to optimize the power amplifier's linearity, which is one of the advantages of CMOS technology. Additionally, the implementation of an integrated bias circuit eliminates the necessity for ESD protection circuits due to external bias voltages, thereby improving system integration and simplifying the design.

In this work, the bias voltages of the power amplifier are adjustable and are shown in Figure 17. The common-source transistor voltage can be adjusted within the range of approximately 400 mV to 680 mV, while the common-gate transistor voltage can be tuned between approximately 1.9 V and 2.9 V. By adjusting the bias voltages, it is ensured that under all PVT conditions, the voltage across each power transistor remains within its maximum tolerable limit, thereby ensuring the reliability of the power amplifier and long-term operational stability of the design. Additionally, at different bias voltages, the output impedance of the common gate bias circuit undergoes significant changes. To prevent the impact of output impedance variations on the PA's linearity, this paper adds a voltage buffer following the adjustable resistor in the common-gate bias circuit (Figure 17b) to stabilize circuit output impedance.

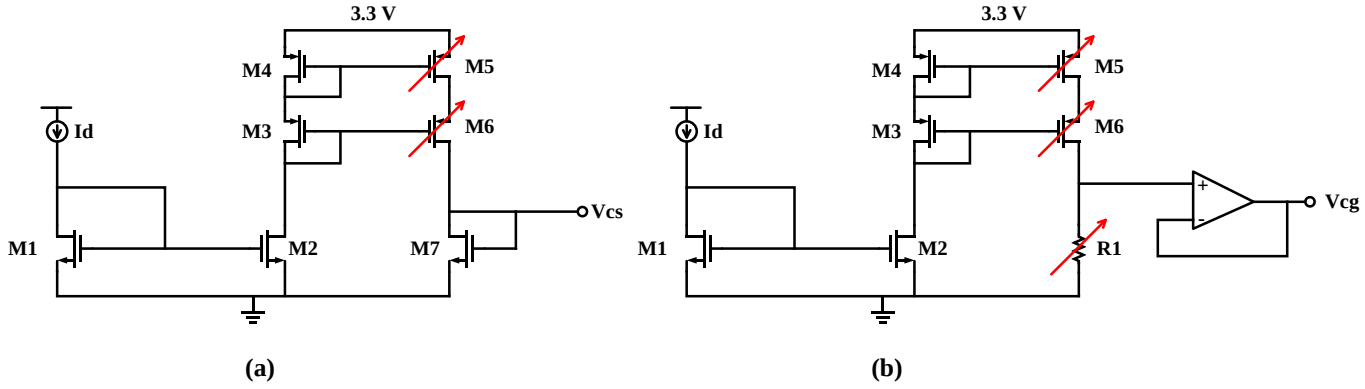

Figure 17. Schematic of integrated circuits. (**a**) Common source. (**b**) Common gate.

4. Simulation Results

The fully integrated power amplifier in this design is manufactured using the SMIC 55 nm process, with a 3.3 V supply voltage. Occupying an area of 0.57 mm^2, as shown in Figure 18a, multiple ground pads are strategically placed to reduce the inductance of the bonding wires. The chip occupies an area of 1.45 mm^2, as shown in Figure 18. In addition to the power amplifier, the chip also includes the SPI module, a bandgap, and other test modules. The simulation software used in this design is Cadence IC 617.

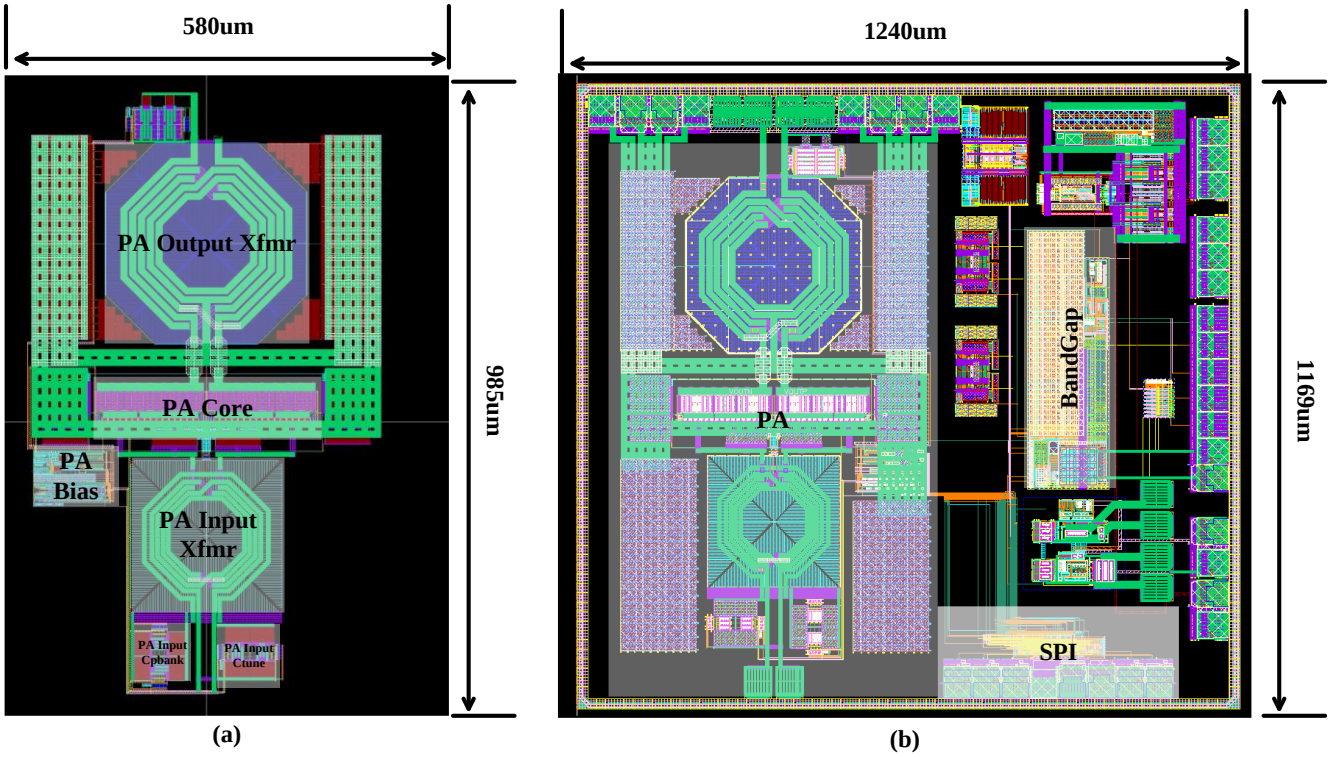

Figure 18. (**a**) Layout of proposed PA. (**b**) Layout of test chip.

The simulated S-parameter results, shown in Figure 19, indicate that the small-signal gain of the PA is approximately 9.46 dB/9.98 dB-11.48 dB at both 2.4 GHz and 5 GHz. Within the 5 GHz frequency range, the gain remains relatively flat across the entire bandwidth.

To characterize the linearity and efficiency of the PA, continuous wave simulations were employed. The simulation results displayed in Figures 20 and 21 illustrate the single-tone linearity of the PA. The saturation power, power gain, and power-added efficiency (PAE) are presented in the operating frequency range. It is seen that at 2.4 GHz and 5 GHz, the saturation power is 28.03 dBm/27.5–28.2 dBm, PAE is 33.25/24.5–31.1%, and the power gain is 9.37/11.5–10.03 dB. Additionally, the saturation power of the PA remains above 27.5 dBm.

The results for two-tone linearity are depicted in Figure 22. In the 2.4 GHz and 5 GHz frequency bands, the IMD3 is within −30 dBc when the output power is 15 dBm, meeting the requirements of WLAN standards.

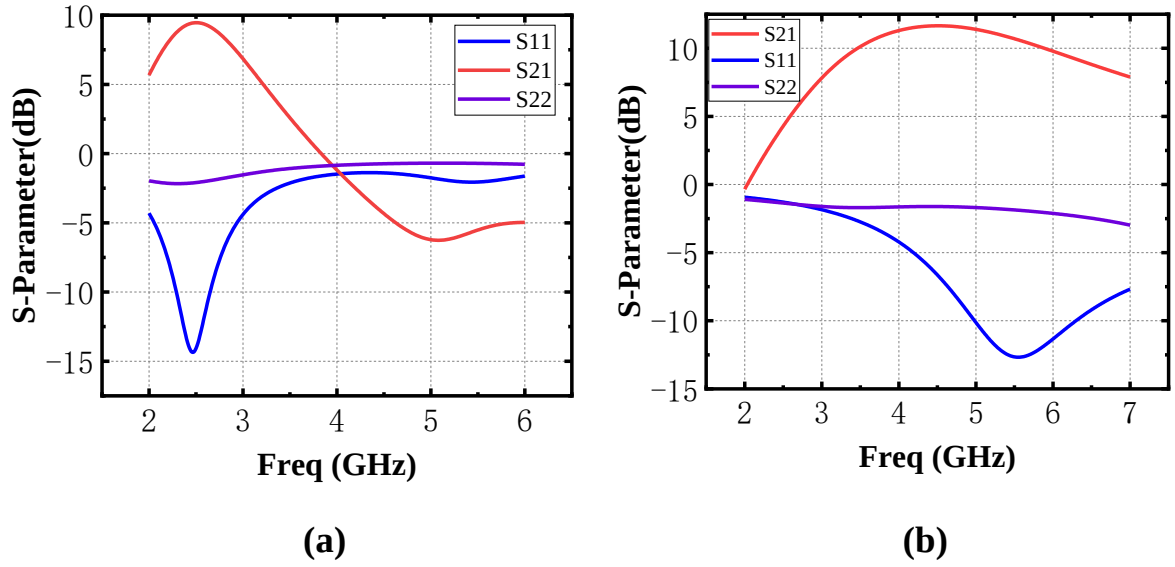

Figure 19. Simulated S-parameters. (**a**) 2.4 G band. (**b**) 5 G band.

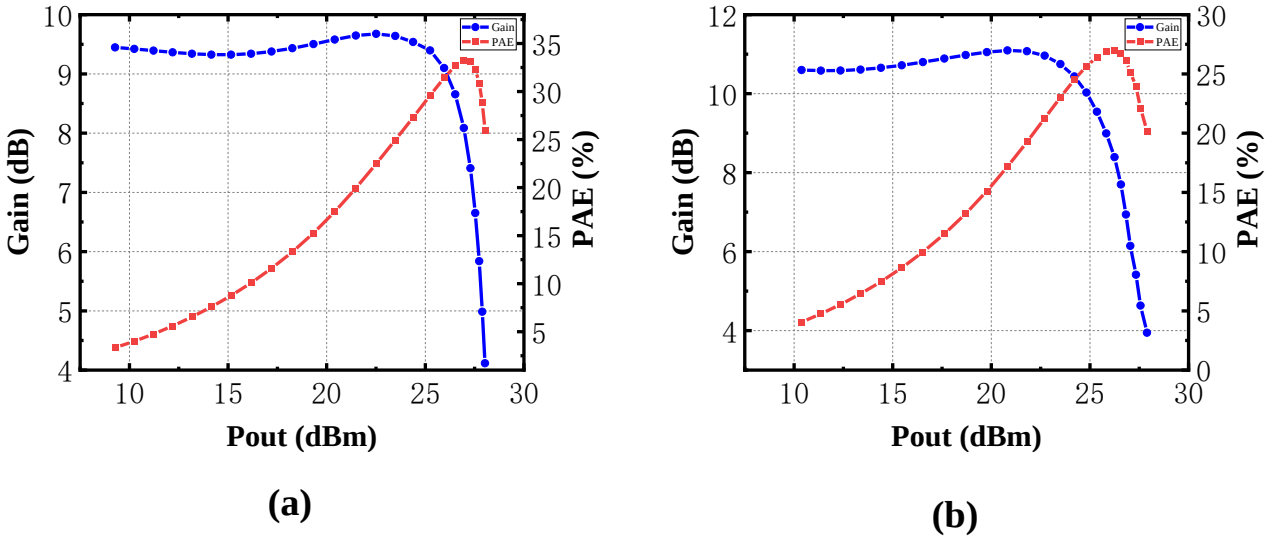

Figure 20. Simulated power gain and PAE versus output power. At (**a**) 2.4 and (**b**) 5.5 GHz modes.

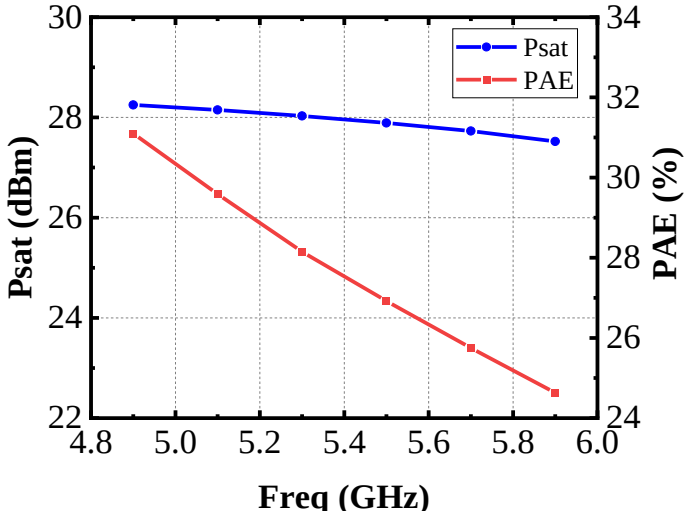

Figure 21. Simulated P_{sat} and PAE at different frequencies.

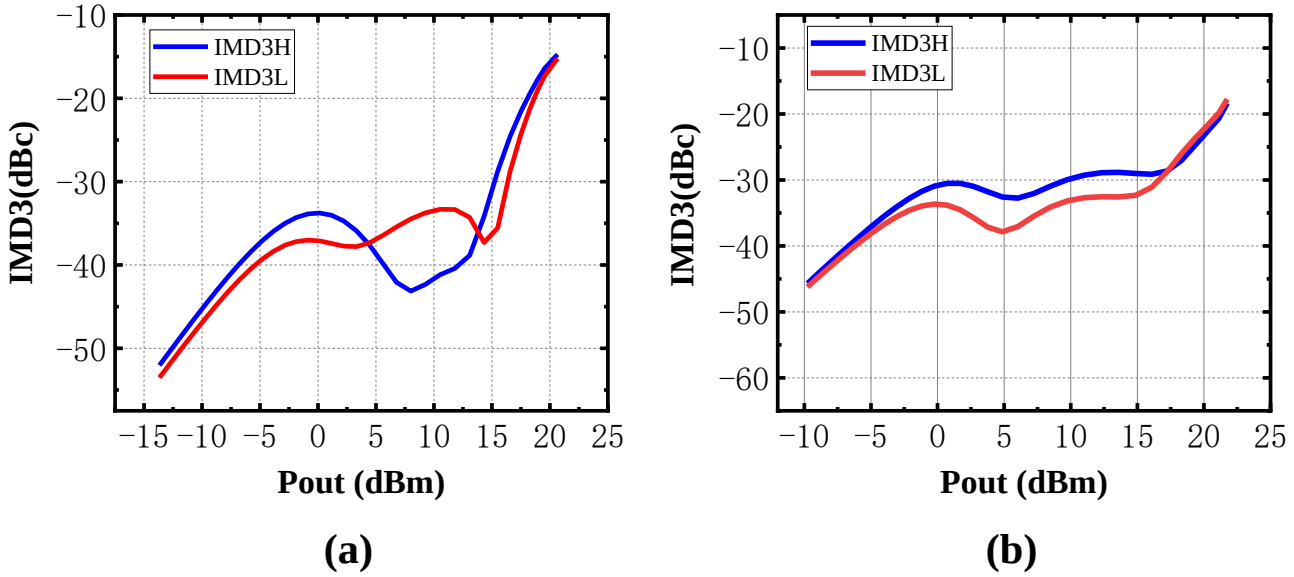

Figure 22. Simulated IMD3 versus output. At (**a**) 2.4 and (**b**) 5.5 GHz modes.

Finally, a comparison between the proposed dual-band PA in this study and other PAs is presented in Table 3.

Table 3. Comparison with other dual-band PAs.

	This Work ***	[17] **	[28] **	[29] **	[30] **	[31] **
Freq (GHz)	**2.4/4.9–5.9**	2.4/5–6	2.4/4.9–5.9	2.5/3/3.5	1.8/2.6	2.4/5
Bandwidth (−3 dB)	**2.06–3.04/3.15–6.6**	2.1–2.8/4–6 *	2.2–3.2/3.8–6.5 *	2.2–2.8/2.8–3.6/3.1–4.1 *	N. A	2–5 *
Gain (dB)	**9.45/11.48–10.03**	14/18–16	9.2/11.3–11.9	~15	10–11 *	12.3/8.4
P_{sat} (dBm)	**28.03/27.5–28.2**	25.4/24.4–24.8	23/21.9–22.4	22.5/21.5	26.2/23.1	21.5/21.4
PAE (%)	**33.25/24.6–31.1**	25/20.8–27.3	27/24.2–28.2	16.5/15(DE)	32.2/31.8	38.4/31
VDD (V)	**3.3**	2.5	2.5	1.2	3.3	3.6
Chip Area (mm^2)	**0.57**	1.14	0.72	2.97	1.4	0.5
Technology	**55 nm**	40 nm	40 nm	65 nm	0.35 µm	0.18 µm

* Graphically estimated; ** measurement results; *** post-layout simulation results.

5. Discussion

From the performance summary in Table 3, it is evident that the output power of current dual-band or multi-band power amplifiers is generally insufficient (below 26 dBm). Furthermore, when the distance between high and low frequency bands is significant, both the output power and efficiency in the higher frequency bands tend to decrease. However, the saturated output power of the proposed dual-band power amplifier, achieved using the design methodology proposed in this paper based on the insertion loss optimization of matching networks, is significantly higher than that of current power amplifiers of the same type. Moreover, its efficiency does not show notable degradation, which validates the correctness of the proposed design methodology. This paper addresses the issue of insufficient output power commonly found in current dual-band and multi-band power amplifiers.

In terms of topologies of PAs, both this paper and references [17,28–30] employ a linear power amplifier topology biased in Class A or Class AB. In contrast, reference [31] uses a switching power amplifier biased in Class E, which offers a significant efficiency advantage over linear power amplifiers. In terms of occupied area, references [17,29]

require a larger area due to the multi-path linear power combining, which, however, offers a significant gain advantage over other power amplifiers. The remaining amplifiers utilize a single-stage amplification structure, resulting in a smaller occupied area but consequently lower gain. In summary, the proposed dual-band power amplifier has a compact footprint and demonstrates a distinct advantage in output power. Additionally, it achieves a favorable trade-off between gain and efficiency, making it well-suited for dual-band IEEE 802.11ax applications.

To continuously boost data throughput, WLAN standards are progressively increasing bandwidth, optimizing spectral efficiency, and adopting more complicated modulation schemes, which pose more stringent linearity and efficiency requirements on power amplifiers. The future research focus for power amplifiers in WLAN applications may aim at improving linearity and efficiency at power back-off levels while meeting high linearity requirements in broadband or multi-band switching conditions

6. Conclusions

This paper presents a dual-band fully integrated high linearity CMOS power amplifier (PA). To deliver high output power, a design methodology for a dual-band matching network is proposed. Based on the proposed methodology, reconfigurable dual-band matching networks are implemented. Furthermore, the proposed input dual-band matching network employs a reconfigurable transformer to achieve a low reflection coefficient across both bands, and the principle of the reconfigurable transformer is thoroughly studied. The simulation results validate the PA's dual-band operation. For continuous-wave operation, the PA achieves saturated powers (P_{sat}) of 28.03 dBm and 27.5–28.2 dBm, with power added efficiencies (PAE) of 33.2% and 24.6–31.1%, in the2.4 GHz and 5 GHz WLAN bands, respectively. Compared with other dual-band or multi-band PAs, the PA demonstrates a superior performance in output power. According to the simulation results, the proposed PA shows great potential for WLAN applications.

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Conflicts of Interest: Bin Wu was employed by Zhejiang CASEMIC Electronics Technology Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial re-lationships that could be construed as a potential conflict of interest.

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