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An S–K Band 6-Bit Digital Step Attenuator with Ultra Low Insertion Loss and RMS Amplitude Error in 0.25 μm GaAs p-HEMT Technology

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Featured Application: The DSA proposed in this paper is well suited for wideband phasedarray systems.

Abstract: This paper presents an ultra-wideband, low insertion loss, and high accuracy 6-bit digital step attenuator (DSA). To improve the accuracy of amplitude and phase shift of the attenuator, two innovative compensation structures are proposed in this paper: a series inductive compensation structure (SICS) designed to compensate for high frequency attenuation values and a small bit compensation structure (SBCS) intended for large attenuation bits. Additionally, we propose insertion loss reduction techniques (ILRTs) to reduce insertion loss. The fabricated 6-bit DSA core area is only 0.51 mm^2, and it exhibits an attenuation range of 31.5 dB in 0.5 dB steps. Measurements reveal that the root-mean-square (RMS) attenuation and phase errors for the 64 attenuation states are within 0.18 dB and 7°, respectively. The insertion loss is better than 2.54 dB; the return loss is better than −17 dB; and the input 1 dB compression point (IP1 dB) is 29 dBm at IF 12 GHz. To the best of our knowledge, this chip presents the highest attenuation accuracy, the lowest insertion loss, the best IP1dB, and a good matching performance in the range of 2–22 GHz using the 0.25 μm GaAs p-HEMT process.

Keywords: digital step attenuator; GaAs; insertion loss reduction technique; series inductive compensation structure; small bit compensation structure

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1. Introduction

Attenuators serve as a crucial component in RF communication, radar, and measurement systems. Their primary function is to provide amplitude control, including linearity adjustment and damage protection [1,2]. The phased array system, with its high precision beam pointing, fast beam synthesis, and scanning capability, is widely used in modern RF-integrated systems such as radar remote sensing and low orbit broadband satellite communications. In phased-array systems, attenuators are required for high accurate amplitude control to obtain lower side lobe levels, better null points, and higher beam sharpness. Digital step attenuators (DSAs) show superior switching speed, reduced power consumption, enhanced linearity, minimal current variation, precise amplitude control, and diminished amplitude/phase change characteristics when compared to variable gain amplifiers. Furthermore, digital attenuators demonstrate higher attenuation accuracy, an improved voltage standing wave ratio, and a broader attenuation dynamic range when compared to continuous variable attenuators [3–6].

In passive DSAs, three primary topologies have been investigated in the literature: distributed, switched path, and switched T-/π-type attenuators [7–13], where, TL is a λ/4 microstrip line, Ms is a series transistor, Mp is a parallel transistor, Rs is a series branch resistor, Rp is a parallel branch resistor, and Vc and $\overline{Vc}$ are a pair of complementary voltages for controlling the on and off of the transistor.

Switched path attenuators use single-pole-double-throw (SPDT) switches to steer the signal path between a thru line and a resistive network, as shown in Figure 1a. This topology provides low phase variation over attenuation states, but it shows high insertion losses at reference states due to the cumulative losses of all SPDT switches for a multi-bit design, and it occupies a large chip area [7,8].

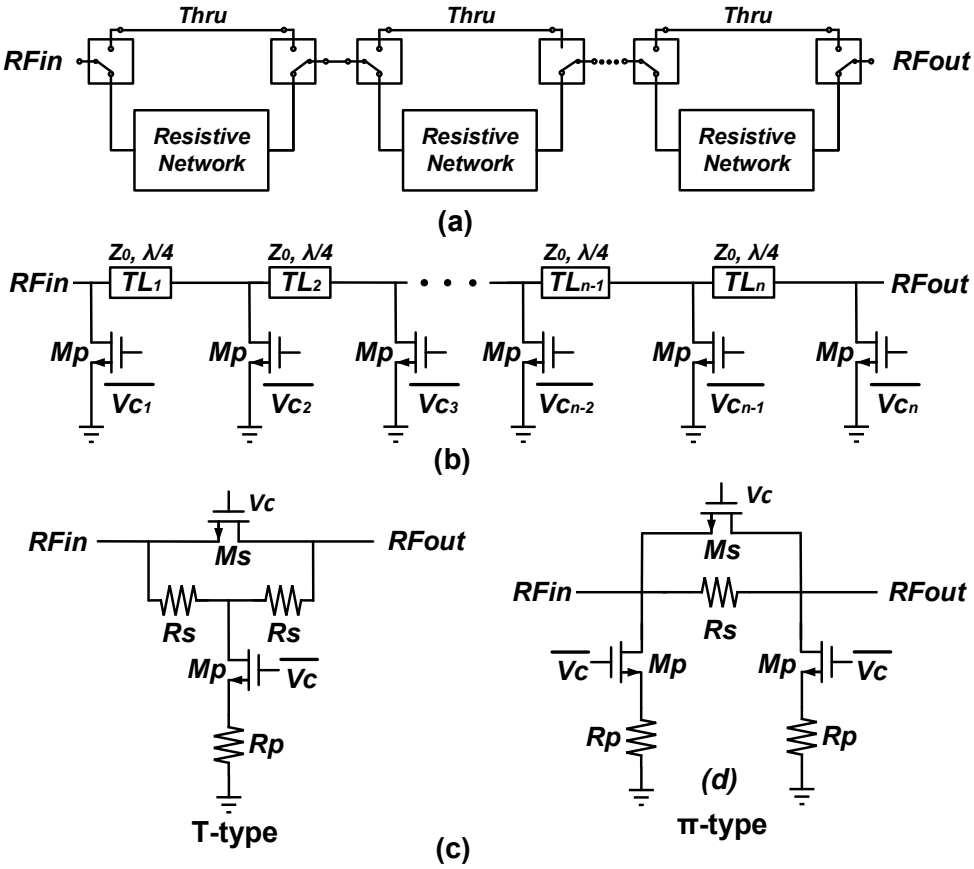


Figure 1. Topologies of DSAs. (**a**) Switched path attenuator. (**b**) Distributed attenuator. (**c**) Switched T/π attenuators.

Distributed attenuators do not have series switches in the signal path and therefore have the advantage of low insertion loss, as shown in Figure 1b. However, they show lower maximum attenuation values and larger chip sizes [9,10].

Switched T-/π-type attenuators show low IL, high maximum attenuation, and compact size, as shown in Figure 1c. However, they still show relatively large attenuation variation and phase variation at higher frequencies, which can limit fine amplitude control in broadband applications [11–13].

The primary source of errors in the amplitude and phase of switched T-/π attenuators is attributed to the parasitic capacitance (Coff) of switching transistors [14]. In order to minimize the Coff-induced errors and improve the accuracy of the attenuator amplitude and phase, several compensation structures have been proposed recently. References [15,16] introduced a parallel capacitive compensation structure that transforms the attenuator into a two-pole, two-zero system, significantly reducing phase error. However, the insertion loss of this structure rapidly deteriorates with frequency increase. At 6 GHz, the insertion loss

reaches 2.3 dB and 4 dB, respectively. Consequently, this structure is unsuitable for ultra-wideband attenuators. Adding a tail capacitor in the shunt branch was reported in [17], but this series capacitor limits the bandwidth, counteracting the benefits of the switched-type topology. The inductive compensation structure shows a lower insertion loss compared to the capacitive compensation structure. A parallel inductive compensation structure was introduced by reference [18]. However, the inductor is parallel to the resistance network, resulting in a smaller attenuation value. To address this issue, additional series resistance needs to be incorporated, thereby increasing circuit complexity. Furthermore, as frequency increases, the impact of the phase lag in the parallel inductive compensation structure gradually diminishes. Therefore, this structure is only suitable for low-frequency applications. Consequently, the challenge arises with increasing bandwidth to maintain high linearity, low insertion loss, compact area, and minimal amplitude and phase error concurrently.

In this paper, we propose two innovative compensation structures: a series inductive compensation structure (SICS) designed to compensate for high frequency attenuation values and a small bit compensation structure (SBCS) for large attenuation bits. Additionally, this study adopts a simplified T-type structure and low-pass compensation structure, which not only reduces the insertion loss but also greatly improves the matching performance. Building upon the aforementioned innovations, the proposed 6-bit DSA shows ultra-low insertion loss, excellent attenuation accuracy, high power capacity, and commendable matching performance.

This paper is structured as follows:

In Section 2, we give an in-depth analysis of the conventional switch T-/π structure, deriving optimal resistance values for each attenuation topology to avoid undesired impedance mismatch.

In Section 3, we explain the limitations of conventional digital attenuator design.

In Section 4, we propose a series inductive compensation structure and a small bit compensation structure to effectively extend the operating bandwidth of the attenuator and reduce the additional phase shift.

In Section 5, we propose two methods to reduce the insertion loss, which reduce the insertion loss by 50%.

In Section 6, we cascade the six attenuation bits to maximize performance over the entire bandwidth (from 2 GHz to 22 GHz).

In Section 7, we present the measurement results of the chip and compare with other recently published broadband digital attenuators. The measurement results show that the DSA proposed in this paper can achieve ultra-wideband operation from 2 GHz to 22 GHz with high amplitude tuning accuracy (i.e., <0.18 dB RMS amplitude error) and low phase error (i.e., <7° RMS phase error). Therefore, the proposed DSA can meet the requirements of multi-band phased array systems.

2. Design Method of Conventional Switched Type Attenuators

Conventional attenuators of the switched type typically show three prevalent topologies: T-type [19–25], simplified T-type [4–6,26,27], and π-type [24–31] structures. Each topology is capable of functioning in two distinct states: reference state and attenuation state. The disparity in loss between these two states constitutes the relative attenuation. Given that these three topologies display varying attenuation characteristics, their selection necessitates careful consideration to design specific attenuation bits. Although the resistances of the three topologies can be found in [6,32], calculations ignoring transistor losses are inaccurate for switching attenuators. In this section, we derive the optimal attenuation resistance values considering transistor losses.

2.1. Conventional T-Type Attenuator

Figure 2 shows the conventional T-type attenuation structure and its equivalent circuits.

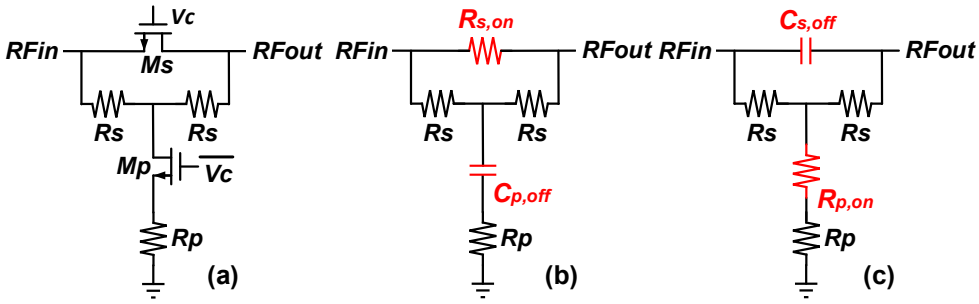


Figure 2. (**a**) Schematic diagram of the conventional T-type attenuation structure and its equivalent circuits. (**b**) Reference state. (**c**) Attenuation state.

In the reference state, transistor *Ms* is on, and transistor *Mp* is off. The insertion loss is determined by the on-resistance of transistor *Ms* and the series resistance *Rs*. Consequently, the corresponding transmission S-parameter can be expressed as follows:

$$S_{21,REF-T} = 1 - \frac{R_s R_{s,on}}{(2R_s + R_{s,on})Z_0 + R_s R_{s,on}} \tag{1}$$

where *Rs,on* represents the on-resistance of the transistor *Ms*, and *Z*0 is the characteristic impedance.

In the attenuation state, transistor *Ms* is off, and transistor *Mp* is on; the insertion loss is determined by the T-type attenuation network and the on-resistance of transistor *Mp*. Consequently, the corresponding transmission S-parameter can be expressed as follows:

$$S_{21,ATT-T} = \frac{2Z_0(R_p + R_{p,on})}{2(Z_0 + R_s)(R_p + R_{p,on}) + 2Z_0R_s + {Z_0}^2 + {R_s}^2} \tag{2}$$

where *Rp,on* represents the on-resistance of the transistor *Mp*.

The relative attenuation $\Delta S21$ can be expressed as follows:

$$\Delta S_{21} = \frac{S_{21,REF-T}}{S_{21,ATT-T}} \tag{3}$$

Furthermore, it is imperative that the *S*11 of both the reference state and attenuation state be as minimal as possible to ensure impedance matching. Notably, the transistor *Ms*, typically larger in size, is designed to minimize insertion loss. Consequently, this results in a superior impedance matching of the reference state. The *S*11 of attenuation state can be expressed as follows:

$$S_{11,ATT-T} = \frac{2R_s(R_p + R_{p,on}) + {R_s}^2 - {Z_0}^2}{2Z_0(R_p + R_{p,on}) + 2Z_0R_s + 2R_s(R_p + R_{p,on}) + {R_s}^2 + {Z_0}^2} \tag{4}$$

When the value of $S_{11,ATT\text{-}T} = 0$, it allows for the computation of the following:

$$R_s = \frac{Z_0(1 - S_{21,ATT-T})}{(1 + S_{21,ATT-T})} \tag{5}$$

$$R_p = \frac{2Z_0S_{21,ATT-T}}{(1 - S^2_{21,ATT-T})} - R_{p,on} \tag{6}$$

Based on (1), (3), (5), and (6), we can calculate *Rs* and *Rp* under the optimal impedance matching condition.

2.2. Simplified T—Type Attenuator

When the value of attenuation is small, the resistance of the series resistor *Rs* in the T-type structure is also small. Taking the 0.5 dB attenuation bit as an example, we find that the resistance of the series resistor *Rs* in the T-type structure is only 1.34 Ω, which means that the microstrip line can be used to replace the series resistor *Rs*.

Figure 3 shows the simplified T-type structure and its equivalent circuits. In this configuration, *Cp,off* represents the equivalent capacitance of the parallel transistor in its off state, while *Rp,on* denotes the on resistance during the parallel transistor's on state. The simplified T-type design eliminates both the series resistor *Rs* and the series transistor *Ms* found in conventional T-type structure. This allows for targeted attenuation by solely adjusting *Rp* and *Mp* [26,27]. Notably, this architecture boasts reduced insertion loss and a compact layout area.

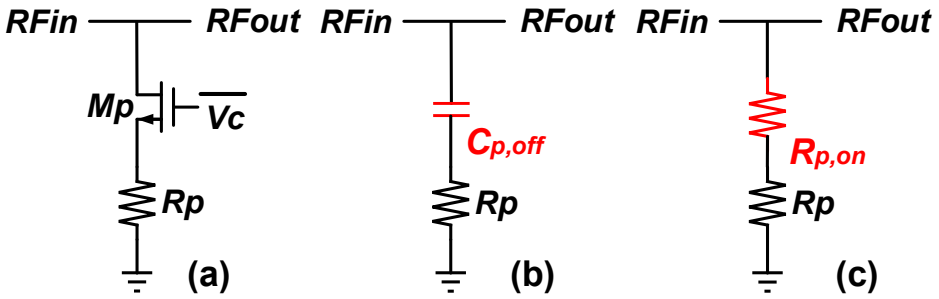


Figure 3. (**a**) Schematic diagram of the simplified T-type attenuation structure and its equivalent circuits. (**b**) Reference state. (**c**) Attenuation state.

In the reference state, the transistor *Mp* is turned off, and the signal to ground shows a high resistance state; at this time, the insertion loss tends to be close to zero. Conversely, in the attenuation state, the transistor *Mp* is on, and the signal leaks to the ground to achieve the attenuation. The resistance value of Rp can still be obtained by (6).

2.3. Conventional π-Type Attenuator

As can be seen from (4), as attenuation increases, *Rp* diminishes, and the return loss of the T-type structure deteriorates. Notably, when the attenuation reaches 8 dB, there is a marked deterioration in the return loss, indicating that the T-type structure is not suitable for large attenuation bits. In contrast, the π-type structure shows greater suitability for large attenuation bits. Figure 4 shows the conventional π-type structure and its equivalent circuits.

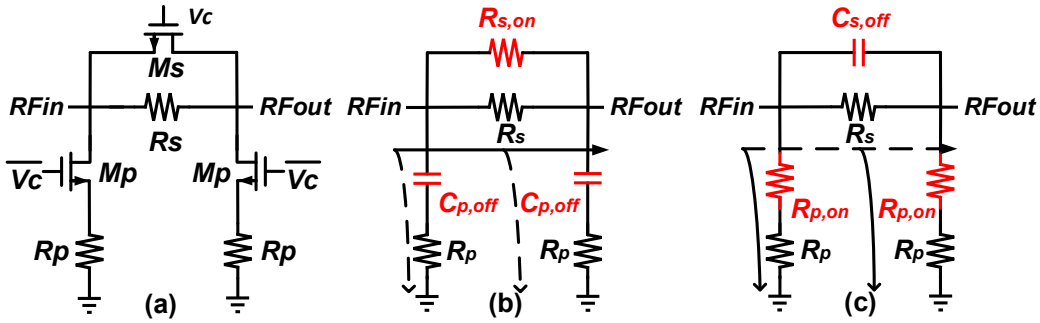


Figure 4. (**a**) Schematic diagram of the π-type attenuation structure and its equivalent circuits. (**b**) Reference state. (**c**) Attenuation state.

In the reference state, transistor *Ms* is on, and transistor *Mp* is off. The insertion loss is determined by the on-resistance of transistor *Ms* and the series resistance *Rs*. Consequently, the corresponding transmission *S*-parameter can be expressed as follows:

$$S_{21,REF-\pi} = 1 - \frac{R_s R_{s,on}}{2(R_s + R_{s,on})Z_0 + R_s R_{s,on}} \tag{7}$$

In the attenuation state, transistor *Ms* is off, and transistor *Mp* is on; the insertion loss is determined by the T-type attenuation network and the on-resistance of transistor *Mp*. Consequently, the corresponding transmission *S*-parameter can be expressed as follows:

$$S_{21,ATT-\pi} = \frac{2Z_0(R_p + R_{p,on})^2}{(2Z_0 + R_s)(R_p + R_{p,on})^2 + (2R_p + 2R_{p,on} + R_s){Z_0}^2} \tag{8}$$

The relative attenuation $\Delta S21$ can be expressed as follows:

$$\Delta S_{21} = \frac{S_{21,REF-\pi}}{S_{21,ATT-\pi}} \tag{9}$$

The *S*11 of attenuation state can be expressed as follows:

$$S_{11,ATT-\pi} = \frac{R_s(R_p + R_{p,on})^2 - {Z_0}^2(2R_p + 2R_{p,on} + R_s)}{(R_s + 2Z_0)(R_p + R_{p,on})^2 + 2Z_0(R_s + Z_0)(R_p + R_{p,on}) + R_s{Z_0}^2} \tag{10}$$

Similarly, when the value of $S11,ATT\text{-}\pi = 0$, it allows for the computation of the following.

The relative attenuation $\Delta S21$ can be expressed as follows:

$$R_s = \frac{Z_0(1 - S_{21,ATT-\pi}^2)}{2S_{21,ATT-\pi}} \tag{11}$$

$$R_p = \frac{Z_0(1 + S_{21,ATT-\pi})}{(1 - S_{21,ATT-\pi})} - R_{p,on} \tag{12}$$

Based on (7), (8), (11), and (12), we can calculate *Rs* and *Rp* under the optimal impedance matching condition.

3. Limitations of Conventional Structures

In general, attenuation bits with large attenuation values contribute large amplitude and phase variations and limit the bandwidth. In this section, the limitations of the conventional structure are analyzed using a conventional π-type attenuator as an example.

Figure 4 shows the equivalent circuit of the conventional π-type attenuator. Considering the parasitic capacitance of the transistor, the equivalent circuit of the reference state can be considered as a low-pass filter with phase lag, and the parasitic capacitance *Cp,off* of the shunt transistor will cause the leakage of the high-frequency signal to ground. Conversely, the equivalent circuit of the attenuation state can be considered as a high-pass filter with phase advance, and the high-frequency signal can be directly output through the parasitic capacitance *Cs,off* of the series transistor. Consequently, the presence of *Cs,off* and *Cp,off* leads to a relative attenuation value that is less than the ideal one, accompanied by an additional phase shift exceeding 0°.

The transmission matrix for a conventional π-type structure in the reference state is given by the following (13):

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} 1 + \frac{\omega^2 {C_{p,off}}^2 R_p R_{s,on} R_S}{R_s + R_{s,on}} + \frac{j\omega C_{p,off} R_{s,on} R_s}{R_s + R_{s,on}} & \frac{R_s R_{s,on}}{R_s + R_{s,on}} \\ 2\omega^2 {C_{p,off}}^2 (R_p - \frac{R_s R_{s,on}}{R_s + R_{s,on}}) + j2\omega C_{p,off} & 1 + \frac{\omega^2 {C_{p,off}}^2 R_p R_{s,on} R_s}{R_s + R_{s,on}} + \frac{j\omega C_{p,off} R_{s,on} R_s}{R_s + R_{s,on}} \end{pmatrix} \tag{13}$$

The corresponding transmission S-parameter is given by the following (14):

$$S_{21} = \left(\frac{2}{A + \frac{B}{Z_0} + Z_0 C + D}\right) = \frac{1}{1 + \frac{R_{s,on}R_s}{R_{s,on}+R_s}(\omega^2 C_{p,off}{}^2 R_P + j\omega C_{p,off} + \frac{1}{2Z_0}) + \omega Z_0 C_{p,off}(\omega C_{p,off} R_P - \frac{\omega C_{p,off} R_{s,on} R_s}{R_{s,on}+R_s} + j)} \quad (14)$$

where *Cp,off* is the parasitic capacitance in the off state of the parallel transistor.

The transmission phase in the reference state can be expressed as follows:

$$\varphi_R \approx -\tan^{-1} \frac{2\omega Z_0^2 C_{p,off}(R_{s,on} + R_s)^2 (R_{s,on}R_s + R_{s,on}Z_0^2 + R_s Z_0^2)}{R_{s,on}R_s} \quad (15)$$

Similarly, the transmission phase in the attenuation state can be expressed as follows:

$$\varphi_A \approx -\tan^{-1} \frac{\omega C_{s,off}(Z_0^2 + R_{p,on}R_p)}{2R_{p,on}Z_0^2 + 2R_p Z_0^2} \quad (16)$$

where $\omega^2 C_{s,off}{}^2 R_s{}^2$ and $\omega^2 C_{p,off}{}^2 R_p{}^2$ are omitted to simplify the calculations.

In order for the transmission phase difference to be zero, the following equation must be satisfied:

$$\Delta\varphi = \varphi_A - \varphi_R = 0 \quad (17)$$

The transmission phase φ_R is less than or equal to 0, while φ_A is greater than or equal to 0°. Therefore, to achieve zero transmission phase difference, the following relationship should be satisfied:

$$\varphi_A = \varphi_R = 0 \quad (18)$$

However, the parasitic capacitance of the transistor cannot be zero, so the phase of the attenuation state of the conventional π-type topology is always ahead of the phase of the reference state. Additionally, as the frequency increases, the reactance of the capacitor decreases, which can exacerbate the amplitude and phase errors between the two states.

4. Design of the Proposed Structures

In this section, we propose two innovative compensation structures: a series inductive compensation structure (SICS) designed to compensate for high frequency attenuation values and a small bit compensation structure (SBCS) for large attenuation bits. The proposed compensation structures effectively broaden the bandwidth of the attenuator and reduce the high-frequency additional phase shift. Furthermore, the compensation structures are equally applicable to T-type attenuators.

4.1. Series Inductive Compensation Structure (SICS)

Figure 5 shows the modified π-type attenuator with a series inductive compensation structure and its equivalent circuits for the reference and attenuation states.

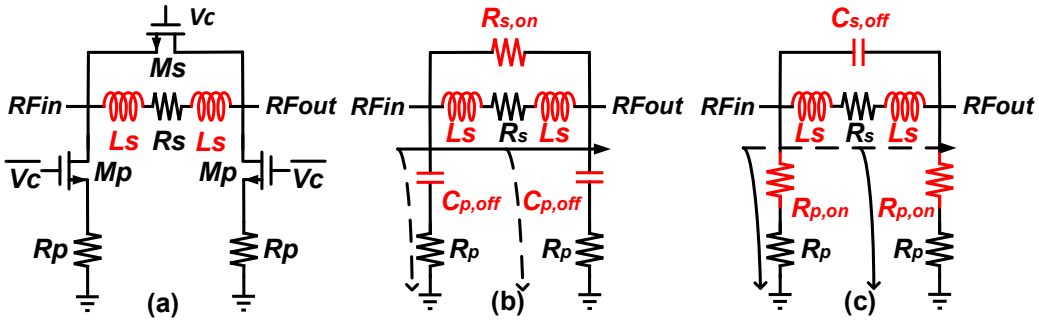


Figure 5. (**a**) Schematic diagram of the modified π−type attenuator and its equivalent circuits. (**b**) Reference state. (**c**) Attenuation state.

For the amplitude, when the resistance *Rs* is connected in series with two inductors *Ls*, the resultant total impedance becomes $Rs + 2j\omega Ls$. Notably, the total impedance value escalates in correlation with the frequency, thereby compensating for the attenuation values at high frequencies.

For the phase, the transmission phases φ_R and φ_A in the reference and attenuation states of SICS can be written as (1) and (2), respectively.

$$\varphi_R = -\tan^{-1}\left(\frac{2((R_{s,on}{}^2 + 4\omega^2 L_s C_{p,off} Z_0 (Z_0 + R_{s,on}))L_s + (Z_0 R_{s,on}{}^2 + R_s R_{s,on}(R_{s,on} + 4Z_0) + R_s{}^2(Z_0 + R_{s,on}))Z_0 C_{p,off})\omega}{(2Z_0 + R_s)R_{s,on}{}^2 + 4R_{s,on}R_s{}^2 + 2(R_s{}^2 + 2R_s R_{s,on})Z_0 - 2\omega^2 L_s(2C_{p,off}R_{s,on}{}^2 Z_0 - 2L_s R_{s,on} - 4L_s Z_0)}\right) \quad (19)$$

$$\varphi_A = \tan^{-1}\left(\frac{(C_{s,off}R_s{}^2 + 12\omega^2 L_s{}^2 C_{s,off} - 2L_s)(R_p + Z_0)\omega}{(R_s R_p + Z_0 R_s + 4Z_0 R_p)(1 - 4\omega^2 L_s C_{s,off})}\right) \quad (20)$$

The inductor required to realize (17) is derived as follows:

$$L_S \cong \frac{1 - \sqrt{1 - 16\omega^2 R_s{}^2 C_{s,off}{}^2}}{2\omega^2 C_{s,off}} \quad (21)$$

Figure 6 shows the simulated relative attenuation and additional phase shift versus frequency for different *Ls* values of the 8 dB modified π-type attenuator. As the value of compensation inductance *Ls* increases, both the relative attenuation value and additional phase shift progressively approach ideal values. Selecting the appropriate *Ls*, the attenuation bandwidth can be broadened, and the additional phase shift can be optimized. This paper uses microstrip lines instead of series inductors to achieve compensation functions.

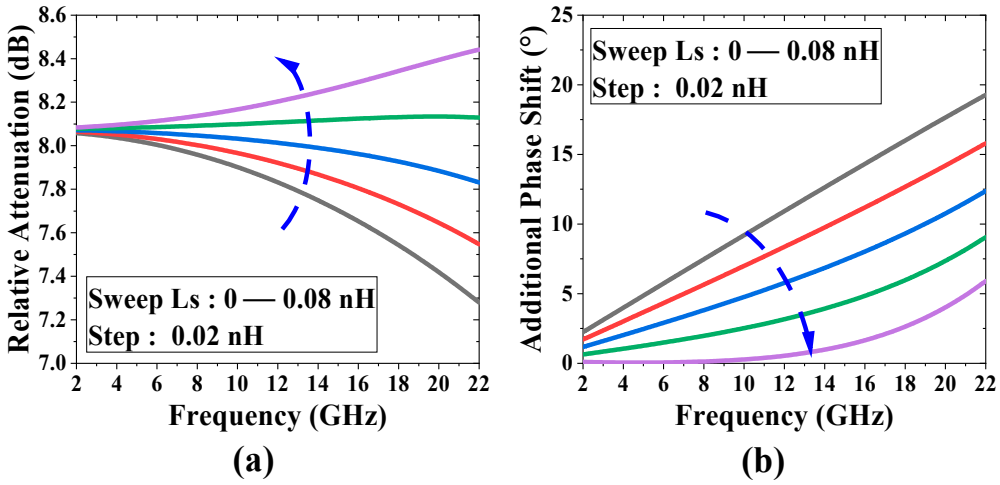


Figure 6. Simulated (**a**) relative attenuation and (**b**) additional phase shift using SICS for different *Ls* values.

It is worth noting that *Ls* has little effect on the low-frequency performance, which is critical for designing ultra-wideband attenuators.

4.2. Small Bit Compensation Structure (SBCS)

The conventional method to achieve a 16 dB attenuator is to cascade two 8 dB conventional π-type attenuators. However, there are many parasitic parameters in the π-type structure, and the parasitic effect will cause errors in the high frequency attenuation and additional phase shift. Cascading two π-type attenuators will accumulate these errors and deteriorate matching performance. The matching performance of the conventional T-type structure deteriorates with the increase of attenuation, which will lead to the deterioration of the performance of the whole 6-bit DSA.

Figure 3a shows the simplified T-type structure, which has the dual capability of compensating attenuation and minimizing insertion loss. Notably, the attenuation values of both the T-type and π-type structures diminish with increasing frequency. In contrast, the attenuation value of the simplified T-type structure escalates with frequency, enabling a small bit compensation through its utilization. Specifically, a modified π-type and T-type attenuator is employed to achieve most of the attenuation firstly, and a simplified T-type attenuator is then inserted between them to compensate for the high-frequency attenuation and further improve the matching performance, as shown in Figure 7.

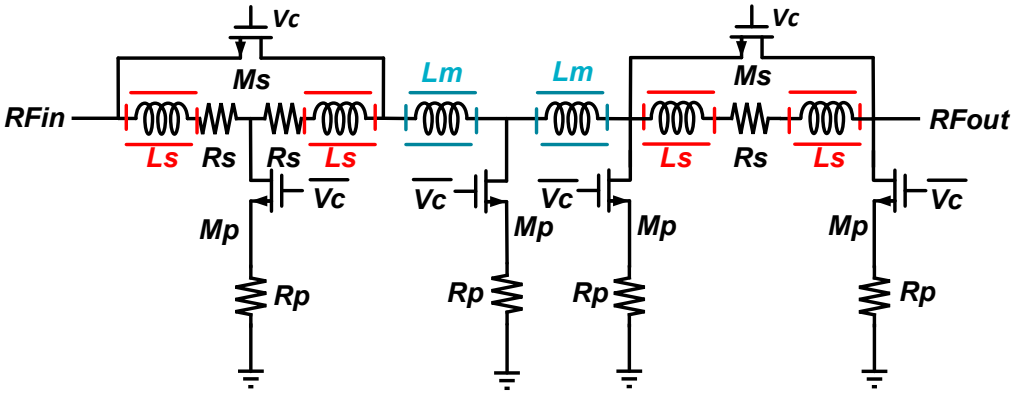


Figure 7. Schematic of 16 dB attenuator with small bit compensation structure.

Figure 8 shows the comparison of simulation results for these two structures, where, the dashed line represents the simulation results of the conventional structure, and the solid line represents the simulation results of the small bit compensation structure proposed in this paper. The simulation results show that the implementation of SBCS enhances the high-frequency attenuation value of a 16 dB attenuator by 1.2 dB, significantly broadening the operating bandwidth of the attenuator. Furthermore, it substantially improves the return loss.

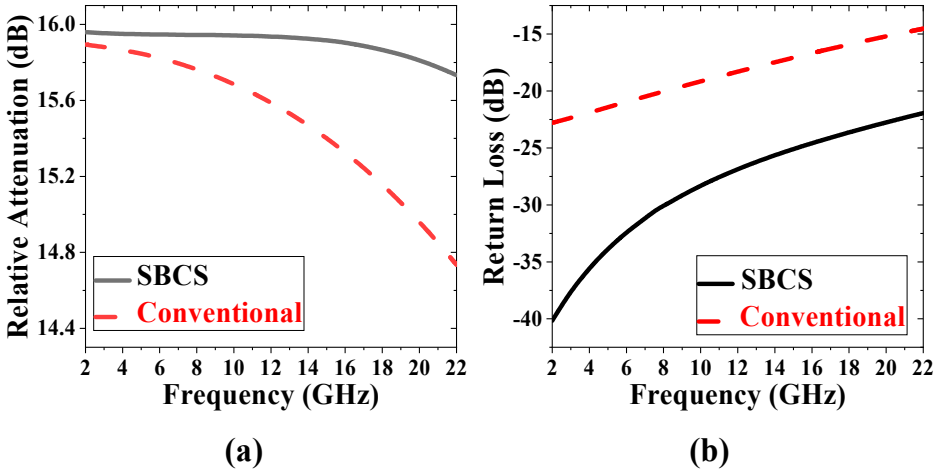


Figure 8. Simulation results of conventional structure and SBCS. (**a**) Relative attenuation and (**b**) return loss.

The SBCS offers an effective design strategy for the creation of attenuators with large attenuation value.

5. Insertion Loss Reduction Techniques (ILRTs)

The primary sources of DSA insertion loss are twofold: the transistor on-resistance and reflection between multiple attenuation bits. Consequently, this paper proposes ILRTs to minimize circuit insertion loss and enhance matching performance.

5.1. Simplified T-Structure

The insertion loss of a conventional T-type attenuator is related to the on-resistance of the series transistors. While the on-resistance of series switches is unavoidable in a switching T-type topology, in some cases, the series transistors can be removed without loss of functionality.

Figures 2a and 3a show the T-type and simplified T-type structure, respectively. The simplified T-type structure removes the series transistor Ms and series resistors *Rs*, which greatly reduces the insertion loss.

Figure 9 shows the insertion loss of the simplified T-type and the T-type attenuators, where, the dashed line shows the simulation results for the conventional T-structure and the solid line shows

the simulation results for the simplified T-structure. The result shows that the insertion loss of the simplified T-type structure is reduced by 1.15 dB. In this paper, both 0.5 dB and 1 dB attenuation bits use the simplified T-type structure, which reduces the insertion loss of the 6-bit DSA by 2.3 dB.

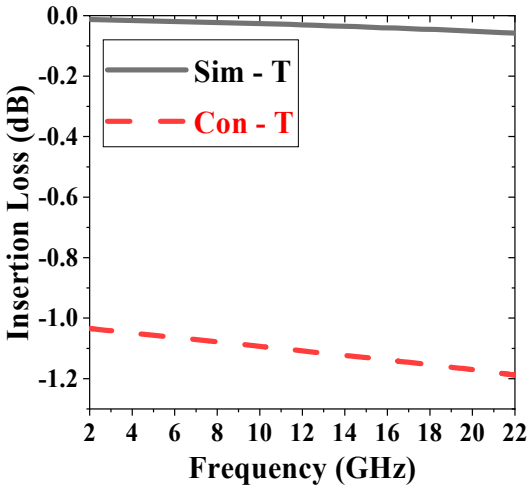


Figure 9. Comparison of insertion loss between T-type and simplified T-type attenuators.

5.2. Low-Pass Inductive Compensation Structure

When cascading attenuation bits, the parasitic capacitance of transistors causes mismatch, which results in reflected signal power and causes unnecessary loss. Since the transistor parasitic capacitance forms a high-pass structure, we aim to construct a low-pass filter to compensate for its tendency to change; thus, we connect inductors in series at the input and output of the π-type structure to realize the low-pass filtering function, and the π-type topology of the structure employing low-pass inductive compensation is shown in Figure 10a.

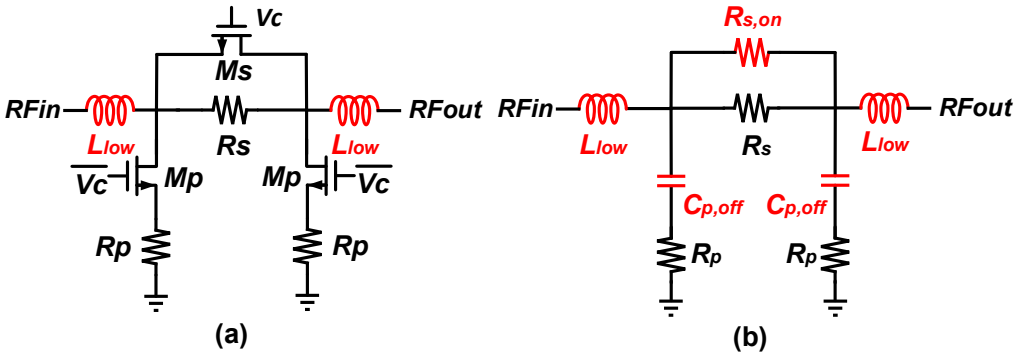


Figure 10. (**a**) π-structure with low-pass inductive compensation and its equivalent circuit. (**b**) Reference state.

Figure 10b shows the equivalent circuit of Figure 10a in its reference state. *Llow*, *Cp,off*, *Rs,on* and *Rs* form a low-pass filter.

Figure 11 shows the insertion loss before and after using low-pass inductive compensation structure to the conventional 8 dB π-type attenuator. Low-pass inductive compensation structure reduces the insertion loss from −1.36 dB to −0.92 dB, effectively compensating for the circuit's capacitive losses. This paper uses microstrip lines instead of inductors to achieve compensation functions.

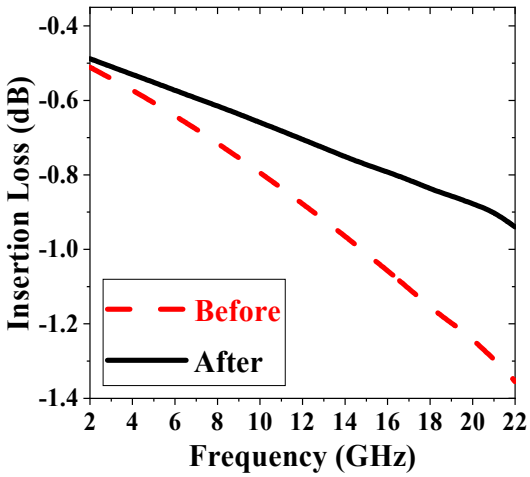
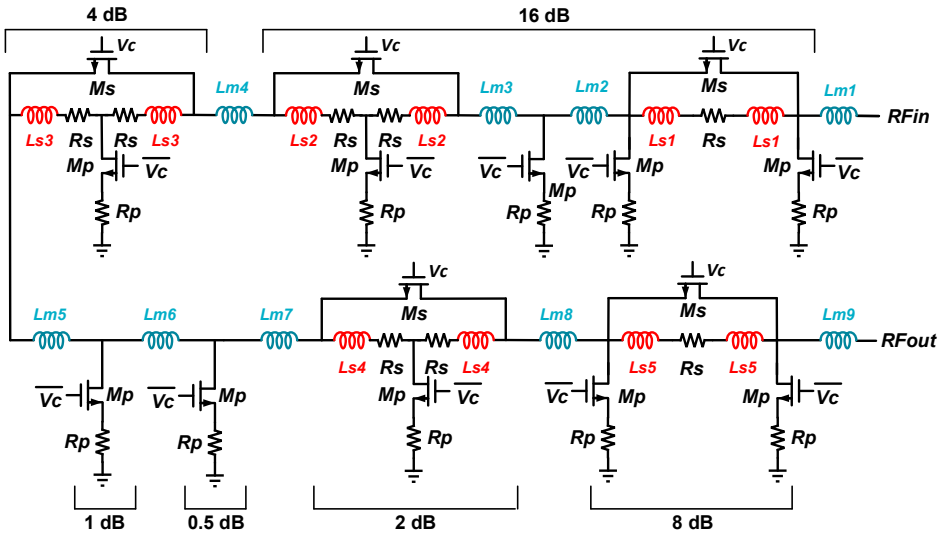


Figure 11. Comparison of insertion loss between the π-type attenuator before and after using low-pass inductive compensation structure.

6. Implementation of The Six-Bit DSA

Figure 12 shows the complete schematic of the 6-bit DSA, which has an attenuation range of up to 31.5 dB in 0.5 dB steps. The 0.5 dB and 1 dB attenuation bits use a simplified T-type structure to minimize insertion loss; the 2 dB and 4 dB attenuation bits use a modified T-type structure based on SICS; the 8 dB attenuation bit uses a modified π-type structure based on SICS; and the 16 dB attenuation bits use an innovative multi-type structure based on SBCS to minimize amplitude errors and phase fluctuations. Since the parasitic capacitance associated with the transistors and the interconnection structures presents a negative imaginary impedance, this shifts S_{11} and S_{22} down along the 50 Ω circle on the Smith chart. Inserting series inductors *Lm* between bits improves the matching characteristics, thereby maximizing operational bandwidth. In this paper, transmission lines are used instead of inductors. In addition, the transistors in each attenuation bit are optimized to achieve a balance between insertion loss and phase error.



Lm1 = 0.159 nH Lm8 = 0.081 nH
Lm2 = 0.059 nH Lm9 = 0.163 nH
Lm3 = 0.039 nH Ls1 = 0.056 nH
Lm4 = 0.073 nH Ls2 = 0.036 nH
Lm5 = 0.030 nH Ls3 = 0.038 nH
Lm6 = 0.051 nH Ls4 = 0.036 nH
Lm7 = 0.026 nH Ls5 = 0.052 nH

Att. (dB)	Rs (Ω)	Rp (Ω)	Ms (μm)	Mp (μm)
0.5 (sim-T)	/	499	/	30
1 (sim-T)	/	219	/	30
2 (mod-T)	7.21	188	350	50
4 (mod-T)	9.84	67	420	50
8 (mod-π)	57	100	350	60
16 (sim-T)	/	462	/	50
16 (mod-T)	15	62	195	50
16 (mod-π)	55	103	560	90

Figure 12. Schematic of the 6-bit DSA.

7. Measurement Results

Figure 13 shows the chip micrograph of the proposed 6-bit DSA implemented by a 0.25 μm GaAs process, with a core area of 0.51 mm^2. The chip integrates a positive voltage controller and realizes compatibility with conventional CMOS TTL control voltage.

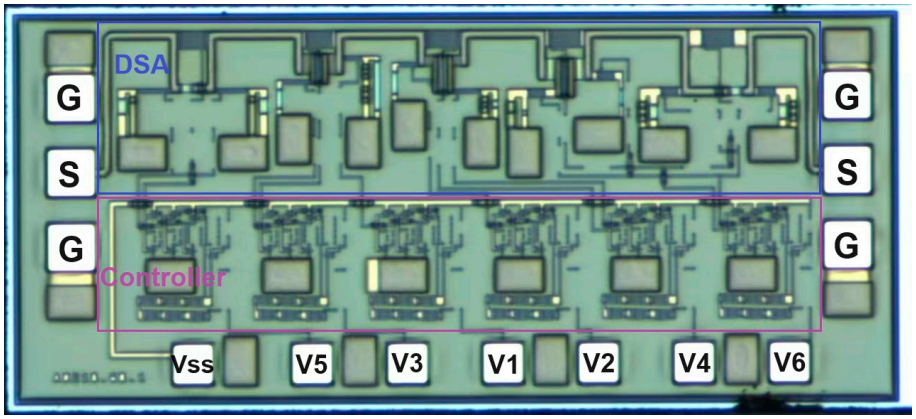


Figure 13. Micrograph of the proposed 6-bit DSA.

To evaluate the performance of the DSA, the root mean square (RMS) amplitude/phase error is defined as follows:

$$RMS\_Amplitude\_Error = \sqrt{\frac{1}{2^n - 1}\sum_{i=1}^{i=2^n-1}\left(RA_{i\_measured} - RA_{i\_ideal}\right)^2} \quad (22)$$

$$RMS\_Phase\_Error = \sqrt{\frac{1}{2^n - 1}\sum_{i=1}^{i=2^n-1}\left(\phi_{i\_measured} - \phi_{ref}\right)^2} \quad (23)$$

where *RAi_measured* and *RAi_iedal* are the relative attenuation values measured at state i and the ideal relative attenuation value of state *i*, respectively. Similarly, *φi_measured* and *φref* are the additional phase shift measured at state *i* and the reference state, respectively.

The electrical properties of the chip were measured on-chip using a Cascade probe station, an ACP-GSGI50 microwave probe, an Agilent 5227B vector network analyzer, a digital multi-channel power supply, and a DC bias power supply. The DC bias voltage applied to the chip, along with the truth table for the digitally controlled power supply, is detailed in Table 1, where 0 represents 0 V, and 1 represents 5 V. This configuration enables the chip to attain 64 states by changing the control voltages.

Table 1. Bias Voltage and Truth Table.

Bias Voltage/V	Digitally Controlled Voltage						Status
	Vc1	Vc2	Vc3	Vc4	Vc5	Vc6	
−5	0	0	0	0	0	0	0 dB
−5	0	0	0	0	0	1	0.5 dB
−5	0	0	0	0	1	0	1 dB
−5	0	0	0	1	0	0	2 dB
−5	0	0	1	0	0	0	4 dB
−5	0	1	0	0	0	0	8 dB
−5	1	0	0	0	0	0	16 dB
−5	1	1	1	1	1	1	31.5 dB

Figure 14 shows the results for this chip. Figure 14a shows the measured relative attenuation of all 64 states, with no overlap. Figure 14b shows the measured insertion loss of −2.54 dB. This remarkably low insertion loss can be primarily ascribed to ILRTs. Figure 14c shows the measured RMS amplitude and phase errors, which are within 0.18 dB and 7°, respectively, exhibiting the lowest amplitude error with small phase error between in 2 to 22 GHz in the GaAs process. As expected, the phase error increases when the frequency is increased. However, the additional phase shift is greatly reduced due to the use of series inductive compensation structures. Figure 14d,e show the measured return loss, and the return loss of all 64 states is better than −17 dB, indicating excellent matching performance. Figure 14f shows the measured power capacity at the reference state with the input 1 dB compression point (IP1 dB) of 29 dBm at IF 12 GHz, indicating that the DSA has a

sufficiently high-power performance to notbe a limiting factor in the linearity of the phased array system.

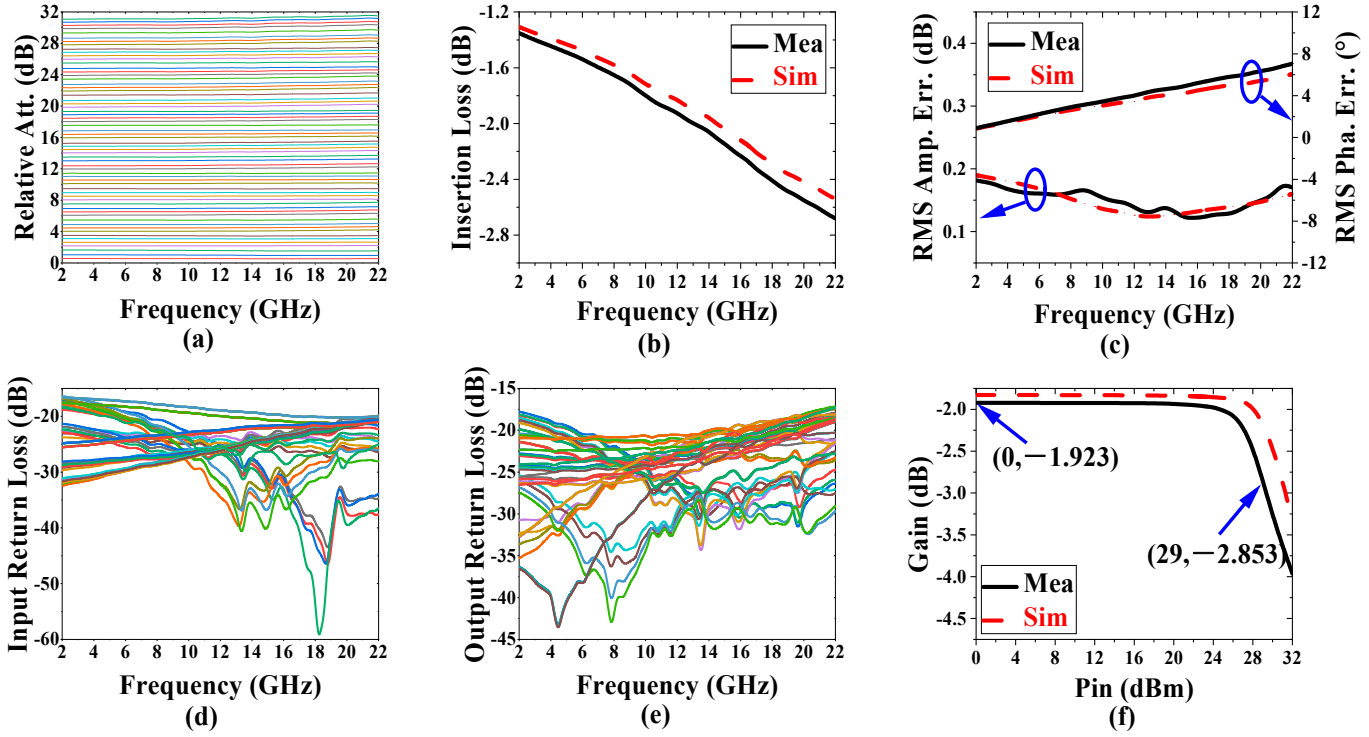


Figure 14. (**a**) Measured relative attenuation. (**b**) Simulated and measured RMS amplitude and phase errors. (**c**) Simulated and measured insertion loss. (**d**) Measured input return loss. (**e**) Measured output return loss. (**f**) Simulated and measured IP1 dB at 12 GHz.

Table 2 presents the comparison of the designed DSA with the published attenuators with state-of-the-art performance. The results show that the proposed DSA shows the best performance in terms of insertion loss, RMS amplitude error, return loss, linearity, and FOM.

Table 2. Comparison of The Prior-Art Attenuators.

Reference	[33]	[34]	[35]	[6]	This Work
Technology	GaAs	GaAs	GaAs	CMOS	GaAs
BW (GHz)	6–18	5–18	DC–23	DC–20	2–22
Range (dB)	31.75	31.5	31.5	31.5	31.5
IL (dB)	9	6.2	6.2	7.4	2.6
RMS Amp error (dB)	0.6	1.1	0.35	0.37	0.18
RMS Phase error (°)	5	2	5	4	7
RL (dB)	12	8	10	12	17
IP1dB (dBm)	N/A	24	N/A	10	29
Area (mm^2)	5.4	3.75	0.47	0.98*/0.14	0.51
FOM #	169	240	668	690	3269

* with pads and non-active space. # $\text{FOM} = \frac{\text{BW} \times \text{Range} \times \text{RL}}{\text{IL} \times \text{RMS AmpErr} \times \text{RMS PhaseErr}}$.

8. Conclusions

In this paper, insertion loss reduction techniques reduce the insertion loss of 6-bit DSA by 50%; series inductive compensation and small bit compensation structures are innovatively proposed to greatly broaden the bandwidth of the attenuator and effectively improve the return loss. To the best of our knowledge, the fabricated DSA shows the lowest insertion loss, optimal impedance matching, the highest attenuation accuracy and linearity, and the best FOM using the 0.25 μm GaAs process and is suitable for wideband phased array systems.

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