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Analysis and Compensation of Dead-Time Effect of a ZVT PWM Inverter Considering the Rise- and Fall-Times

Hailin Zhang, Baoquan Kou *, Lu Zhang and He Zhang

Department of Electrical Engineering, Harbin Institute of Technology, Harbin 150080, China; zhanghailin0310@sina.com (Ha.Z.); zhanglu24@hit.edu.cn (L.Z.); antonyamanda@163.com (He.Z.)
* Correspondence: koubq@hit.edu.cn; Tel.: +86-451-8640-3771

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Abstract: The dead-time effect, as an intrinsic problem of the converters based on the half-bridge unit, leads to distortions in the converter output. Although several dead-time effect compensation or elimination methods have been proposed, they cannot fully remove the dead-time effect of blanking delay error, because the output current polarity is difficult detect accurately. This paper utilizes the zero-voltage-switching (ZVT) technique to eliminate the blanking delay error, which is the main drawback of the hard-switching inverter, although the technique initially aims to improve the efficiency. A typical ZVT inverter—the auxiliary resonant snubber inverter (ARSI) is analyzed. The blanking delay error is completely eliminated in the ARSI. Another error source caused by the finite rise- and fall-times of the voltage is analyzed, which was not considered in the hard-switching inverter. A compensation method based on the voltage error estimation is proposed to compensate the rise- and fall-error. A prototype was developed to verify the effectiveness of the proposed control. Both the simulation and experimental results demonstrate that the qualities of the output current and voltage in the ARSI are better than that in the hard-switching inverter due to the elimination of the blanking delay error. The total harmonic distortion (THD) of the output is further reduced by using the proposed compensation method in the ARSI.

Keywords: dead-time effect; zero-voltage-switching (ZVT); auxiliary resonant snubber inverter (ARSI)

1. Introduction

The half-bridge, as a basic unit, employs two stacked semiconductor switches connected across the DC voltage to realize energy transfer. In AC-DC or DC-AC applications, most of the converters consist of the half-bridge, such as the full-bridge converter and three-phase converter. The two switches in a half-bridge are complementarily conducted. Due to turn-on and turn-off delays and finite rise-time and fall-time during the commutation, a dead-time is inserted between the turn-on and the turn-off of the switches to avoid short circuiting. This results in a current-dependent switching node voltage during the dead-time, which increases the output distortion.

To date, extensive studies have focused on the problem of dead-time effect. Most of the compensation and elimination methods can be divided into three categories: the pulse-based compensation [1,2], the voltage feedforward compensation [3,4] and the dead-time elimination [5–7]. For the pulse-based compensation method, the dead-time effect is modeled as a pulse shift error. A dead-time width pulse is added or reduced based on the shift error to compensate the dead-time effect [1,2]. For the voltage feedforward compensation, the dead-time effect is modeled as an average voltage error, which is regarded as a disturbance to the output voltage. The voltage error is added to

the reference voltage directly to compensate the dead-time effect [3,4]. For the dead-time elimination method, the driving signal is only put on one switch, whereas the driving signal of the other switch is removed. The body diode conducts the current. Therefore, the dead-time is not required in this method [5–7]. Theoretically, these three methods can fully compensate or eliminate the dead-time effect. In practice, however, the results depend on the detection precision of the output current polarity. Due to the output current ripple and zero current clamping, the output current polarity is difficult to detect accurately. Moreover, beyond the three methods, some other methods employing proper current control are proposed to solve the problem of dead-time effect [8–11]. However, these techniques are still not capable of completely removing the dead-time effect.

In the half-bridge circuits, the voltage and current transitions can be turn-off controlled or turn-on controlled, which is influenced by the output current polarity. The turn-off controlled type refers to the case that the commutation is triggered by the turn-off of the switches. Thus, the body diodes of the next turn-on switches are conducted during the dead-time, whereas the turn-on controlled type refers to the case that the commutation is triggered by the turn-on of the switches. Different commutation type leads to different voltage error caused by the dead-time. This kind of dead-time effect is blanking delay error, which is the main error in the half-bridge-based topology [12]. Essentially, the commutation type, which is related to the output current polarity, makes the dead-time effect difficult to remove completely.

Zero-voltage-switching (ZVT) soft-switching technique can be used to eliminate the blanking delay error, although the technique aims to reduce the switching loss and improve the efficiency. The transitions are all turn-off controlled in the ZVT soft-switching converters with the conduction of the anti-parallel diode during the dead-time, which is irrelevant to the output current. Therefore, the dead-time effect of blanking delay error can be completely removed by using the ZVT soft-switching technique. Until now, several topologies of the ZVT pulse-width-modulation (PWM) inverters have been proposed. The auxiliary resonant commutated pole inverter (ARCPI) has been proposed with two auxiliary switches per phase [13,14]. The ARCPI can meet the demand for high efficiency, as well as low voltage and current stresses. However, the major drawback is the existence of the split capacitors, which causes capacitor charge unbalance. The auxiliary resonant snubber inverter (ARSI) has been proposed to eliminate the split capacitors, but the three-phase topology cannot utilize the conventional space-vector-pulse-width modulation (SVPWM) [15,16]. Thus, they are more suitable for permanent magnet brushless DC motors than all types of motors. The single-phase topology is very attractive with only two auxiliary switches well fit to the conventional PWM. Meanwhile, the ZVT inverter using coupled magnetics has been proposed to eliminate the split capacitors [17–19]. However, these topologies need coupled inductors and a large number of auxiliary switches, which unfortunately increase the cost and difficulty of the circuit realization. The ZVT PWM converter has been synthesized and summarized in [20,21].

Without adding the external resonant capacitors, the ZVT inverters can completely remove the dead-time effect. However, the external resonant capacitors are always required to reduce the voltage changing rate of the switches, so that the turn-off loss and electromagnetic interference (EMI) can be reduced. This will lead to output voltage distortion, which is caused by the finite commutation time. This kind of dead-time effect is quite different from that in the hard-switching inverters. Thus, this paper analyzes the dead-time effect of a typical example of ZVT PWM soft-switching inverters—ARSI. Then, a compensation method is proposed to remove the dead-time effect. Finally, the simulation and experiment are undertaken to verify the effectiveness of the proposed method.

2. Dead-Time Effect of the Auxiliary Resonant Snubber Inverter (ARSI)

2.1. Principle

Figure 1 depicts the single-phase ARSI topology analyzed in this paper, which consists of a standard H-bridge inverter, resonant capacitors and an auxiliary circuit. With a proper operation of

the auxiliary switches, S_{r1} and S_{r2}, the zero-voltage-switching (ZVS) condition of the main switches, S_1-S_4, can be created. Meanwhile, the auxiliary switches can realize zero-current switching (ZCS).

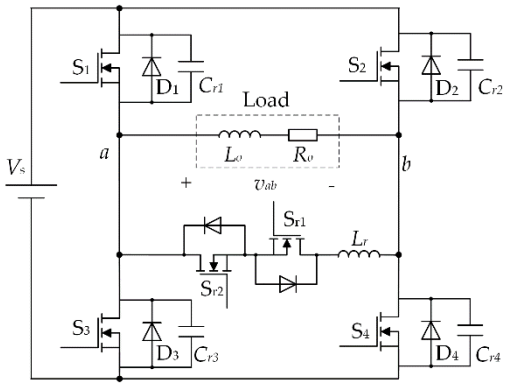


Figure 1. Circuit of auxiliary resonant snubber inverter.

In order to realize soft-switching for the entire load range and maintain a low auxiliary current, the ARSI operates in two modes of heavy load mode (HLM) and light load mode (LLM), as determined by the load condition [22]. In the heavy load condition, the auxiliary circuit is only operated once in each switching period, thus achieving auxiliary ZVS (AZVS) of a set of switches. The other set of switches can achieve natural ZVS (NZVS) without the operation of auxiliary circuit. In the light load condition, the auxiliary circuit is operated twice in each switching period. Therefore, all the switches achieve AZVS.

The operating principle of the ARSI is introduced in [22]. The detailed dead-time effect of LLM and HLM will be analyzed in the case of positive load current as follows. When the load current is negative, the operation is similar.

To analyze the circuit, we assume that

(1) All components and devices are ideal;
(2) The gate signals of the MOSFETs are ideal square-wave;
(3) The output inductor L_o is high enough to be a constant current source.

2.1.1. Heavy Load Condition

In the heavy load condition, "AZVS + NZVS," namely achieving AZVS of a set of switches and NZVS of the other set of switches, is realized. One switching cycle of the operating waveforms are shown in Figure 2, where v_{ds} is the drain-source voltage of a MOSFET, i_d is the drain current of a MOSFET, v_g is the actual gate signal with dead-time, $v_{g,id}$ is the ideal gate signal, i_{Lr} is the resonant inductor current, v_{ab} is the actual pole voltage across the load with dead-time, $v_{ab,id}$ is the ideal pole voltage across the load and v_{err} is the voltage error between v_{ab} and $v_{ab,id}$.

During the dead-time t_{H1}–t_{H3}, the resonant capacitors first resonate with the load inductor. Owing to the positive load current, C_{r2} and C_{r3} are discharged and C_{r1} and C_{r4} are charged. After C_{r2} and C_{r3} are discharged to zero-voltage at t_{H2}, the body diodes D_2 and D_3 conduct the current and then the voltage is clamped to zero. Thus, S_2 and S_3 can be turned on at the ZVS condition. Regarding the dead-time t_{H1}–t_{H3}, it consists of the resonant stage and diode clamping stage. The dead-time causes the pole voltage error. As for the ARSI, the voltage error only occurs in the resonant stage, which is caused by the finite rise- and fall-times of the voltage.

During the resonant stage t_{H1}–t_{H2}, the actual pole voltage can be obtained as follows:

$$v_{ab}(t) = V_s - \frac{i_o}{C_r}(t - t_{H1}) \quad (1)$$

Conversely, the ideal pole voltage should be as follows:

$$v_{ab,id}(t) = -V_s \tag{2}$$

Thus, the voltage error can be given as follows:

$$v_{err}(t) = v_{ab}(t) - v_{ab,id}(t) = 2V_s - \frac{i_o}{C_r}(t - t_{H1}) \tag{3}$$

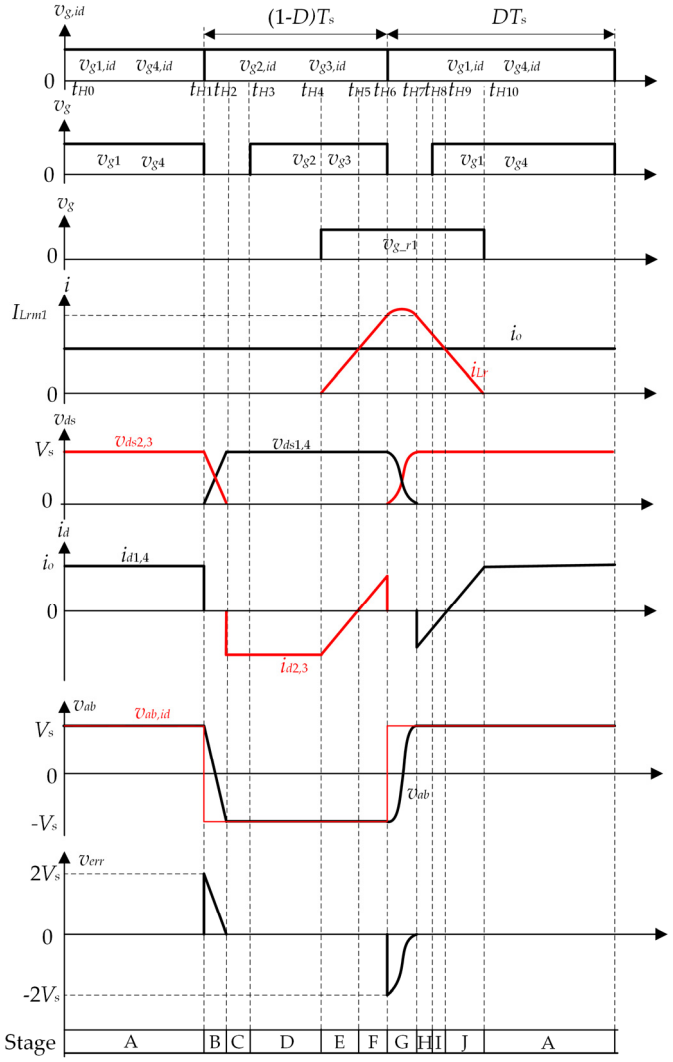


Figure 2. Key waveforms of the the auxiliary resonant snubber inverter (ARSI) in the heavy load condition.

For Equation (1) $v_{ab}(t) = -V_s$, the resonant time can be obtained:

$$\Delta t_{H12} = t_{H2} - t_{H1} = \frac{2C_r V_s}{i_o} \tag{4}$$

Regarding the next commutation, S_{r1} is turned on at t_{H4} to charge the resonant inductor, so that the switch current reverses at t_{H5}. Therefore, after S_2 and S_3 are turned off at t_{H6}, the resonant capacitors can resonate with the resonant inductor, which discharges C_{r1} and C_{r4} to zero-voltage at t_{H7}. Subsequently, the body diodes D_1 and D_4 conduct the current. Thus, S_1 and S_4 can be zero-voltage

turned on at t_{H8}. Regarding the dead-time t_{H6}–t_{H8}, it also consists of the resonant stage and diode clamping stage. Only the resonant stage t_{H6}–t_{H7} brings about the dead-time effect, which is caused by the finite rise- and fall-times. Some equations can be given as follows during the resonant stage.

$$v_{ds1}(t) + v_{ds3}(t) = V_s \tag{5}$$

$$i_{cr1}(t) = C_r \frac{dv_{ds1}(t)}{dt} \tag{6}$$

$$i_{cr3}(t) = C_r \frac{dv_{ds3}(t)}{dt} \tag{7}$$

$$i_{cr1}(t) + i_{Lr}(t) = i_o + i_{cr3}(t) \tag{8}$$

$$v_{ds1}(t) - v_{ds3}(t) = L_r \frac{di_{Lr}(t)}{dt} \tag{9}$$

The initial resonant condition is given as follows:

$$v_{ds1}(t_{H6}) = v_{ds4}(t_{H6}) = V_s \tag{10}$$

$$v_{ds2}(t_{H6}) = v_{ds3}(t_{H6}) = 0 \tag{11}$$

$$i_{Lr}(t_{H6}) = I_{Lrm} \tag{12}$$

According to Equations (5)–(12), the inductor current and drain-source voltages of the main MOSFETs can be obtained as follows:

$$i_{Lr}(t) = (I_{Lrm} - i_o)\cos\omega_A(t - t_{H6}) + \frac{V_s}{Z_A}\sin\omega_A(t - t_{H6}) + i_o \tag{13}$$

$$v_{ds1}(t) = v_{ds4}(t) = \frac{1}{2}V_s + \frac{1}{2}V_s\cos\omega_A(t - t_{H6}) - \frac{1}{2}Z_A(I_{Lrm} - i_o)\sin\omega_A(t - t_{H6}) \tag{14}$$

$$v_{ds2}(t) = v_{ds3}(t) = \frac{1}{2}V_s - \frac{1}{2}V_s\cos\omega_A(t - t_{H6}) + \frac{1}{2}Z_A(I_{Lrm} - i_o)\sin\omega_A(t - t_{H6}) \tag{15}$$

where $\omega_A = \frac{1}{\sqrt{L_r C_r}}$, $Z_A = \sqrt{\frac{L_r}{C_r}}$, and I_{Lrm} is the initial resonant inductor current.

The pole voltage can be obtained as follows:

$$v_{ab}(t) = v_{ds3}(t) - v_{ds4}(t) = Z_A I_{boost1}\sin\omega_A(t - t_{H6}) - V_s\cos\omega_A(t - t_{H6}) \tag{16}$$

where I_{boost1} is the switch current at the initial resonant time $I_{boost1} = I_{Lrm1} - i_o$.

The ideal pole voltage, on the other hand, should be as follows:

$$v_{ab,id}(t) = V_s \tag{17}$$

The voltage error during the resonant stage t_{H6}–t_{H7} can be calculated as follows:

$$v_{err}(t) = v_{ab}(t) - v_{ab,id}(t) = Z_A I_{boost1}\sin\omega_A(t - t_{H6}) - V_s\cos\omega_A(t - t_{H6}) - V_s \tag{18}$$

For Equation (16) $v_{ab}(t) = V_s$, the resonant time can be obtained:

$$\Delta t_{H67} = t_{H7} - t_{H6} = \frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost1}^2}} \tag{19}$$

According to the analysis of dead-time effect in the heavy load condition, the voltage error in a switching cycle can be obtained from Equations (3) and (18):

$$v_{err} = \begin{cases} 2V_s - \frac{i_o}{C_r}(t - t_{H1}) & t_{H1} \le t \le t_{H2} \\ -V_s - V_s \cos\omega_A (t - t_{H6}) + Z_A I_{boost1} \sin\omega_A (t - t_{H6}) & t_{H6} \le t \le t_{H7} \\ 0 & t_{H0} \le t < t_{H1} \ \ or \ \ t_{H2} < t < t_{H6} \ \ or \ \ t_{H7} < t < t_{H10} \end{cases} \quad (20)$$

Thus, the average voltage error in a switching cycle can be calculated as follows:

$$V_{err} = \frac{1}{T_s}\int_{t_{H0}}^{t_{H10}} v_{err} dt = \frac{\Delta t_{H12} - \Delta t_{H67}}{T_s} V_s = \frac{V_s}{T_s}\left(\left| \frac{2C_r V_s}{i_o} \right| - \left| \frac{2}{\omega_A} \arcsin \frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost1}^2}} \right| \right) \quad (21)$$

where T_s is the switching period.

2.1.2. Light Load Condition

When the load current is low, the resonant capacitors cannot be discharged to zero-voltage during the dead-time. NZVS of S_2 and S_3 fails [22]. Therefore, the auxiliary circuit is operated to achieve AZVS of S_2 and S_3. One switching cycle of the operating waveforms in the LLM is shown in Figure 3.

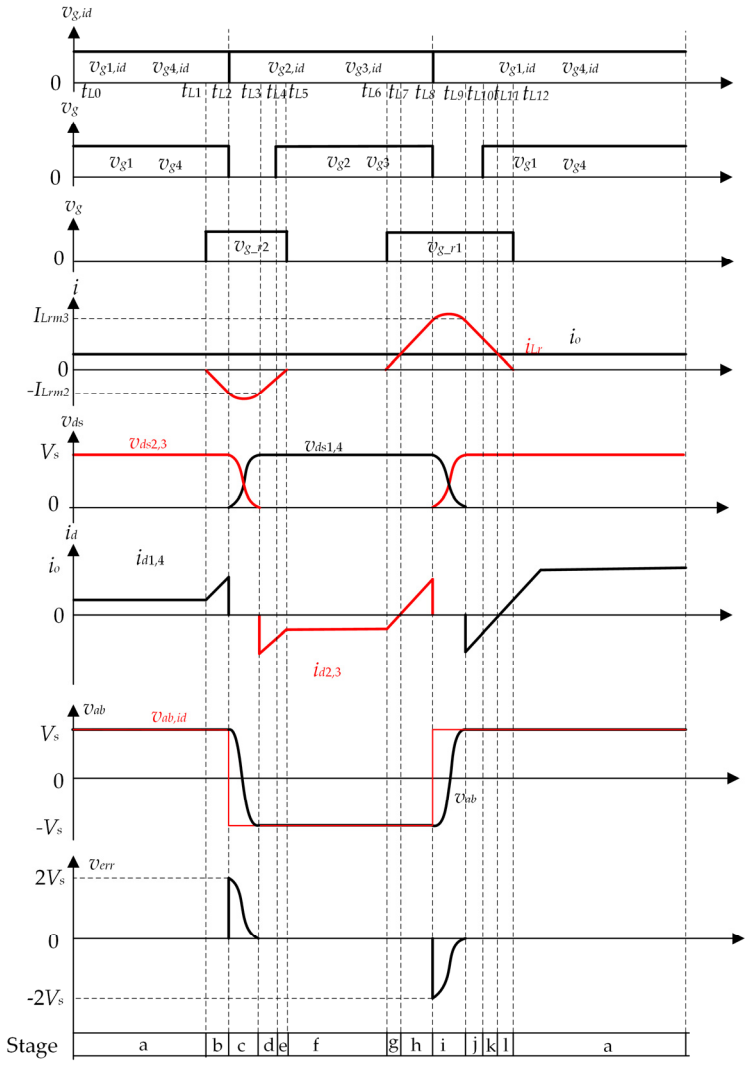


Figure 3. Key waveforms of the ARSI in the light load condition.

Before t_{L2}, S_{r2} is turned on to charge the resonant inductor L_r, thus increasing the switch current. After S_1 and S_4 are turned off at t_{L2}, the resonant capacitors resonate with the resonant inductor. Due to the higher switch current, C_{r2} and C_{r3} can be discharged to zero-voltage. Thus, S_2 and S_3 can be turned on at the ZVS condition. The voltage error also only occurs in the resonant stage t_{L2}–t_{L3}. This resonant stage is similar to the stage t_{H6}–t_{H7} in Figure 2. The same equations can be obtained as Equations (5)–(9). However, the initial resonant conditions are different as follows:

$$v_{ds1}(t_{L2}) = v_{ds4}(t_{L2}) = 0 \tag{22}$$

$$v_{ds2}(t_{L2}) = v_{ds3}(t_{L2}) = V_s \tag{23}$$

$$i_{Lr}(t_{L2}) = -I_{Lrm2} \tag{24}$$

Therefore, the inductor current and drain-source voltages of the main MOSFETs can be obtained as follows according to Equations (5)–(9) and (22)–(24):

$$v_{ds1}(t) = v_{ds4}(t) = \frac{1}{2}V_s - \frac{1}{2}V_s\cos\omega_A(t - t_{L2}) + \frac{1}{2}Z_A I_{boost2}\sin\omega_A(t - t_{L2}) \tag{25}$$

$$v_{ds2}(t) = v_{ds3}(t) = \frac{1}{2}V_s + \frac{1}{2}V_s\cos\omega_A(t - t_{L2}) - \frac{1}{2}Z_A I_{boost2}\sin\omega_A(t - t_{L2}) \tag{26}$$

$$i_{Lr}(t) = -I_{boost2}\cos\omega_A(t - t_{L2}) - \frac{V_s}{Z_A}\sin\omega_A(t - t_{L2}) + i_o \tag{27}$$

where I_{boost2} is the switch current at the initial resonant time $I_{boost2} = I_{Lrm2} + i_o$

Thus, the actual pole voltage can be calculated as follows,

$$v_{ab}(t) = v_{ds3}(t) - v_{ds4}(t) = V_s\cos\omega_A(t - t_{L2}) - Z_A I_{boost2}\sin\omega_A(t - t_{L2}) \tag{28}$$

whereas the ideal pole voltage is:

$$v_{ab,id}(t) = -V_s \tag{29}$$

The voltage error caused by the resonant stage can be calculated as follows:

$$v_{err}(t) = v_{ab}(t) - v_{ab,id}(t) = V_s\cos\omega_A(t - t_{L2}) - Z_A I_{boost2}\sin\omega_A(t - t_{L2}) + V_s \tag{30}$$

For Equation (28) $v_{ab}(t) = -V_s$, the resonant time can be obtained:

$$\Delta t_{L23} = t_{L3} - t_{L2} = \frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost2}^2}} \tag{31}$$

Regarding the dead-time t_{L8}–t_{L10}, the principle is the same as t_{H6}–t_{H8} in the heavy load condition, which is caused by the rise- and fall-times of the pole voltage. Therefore, the voltage error and the resonant time can be obtained:

$$v_{err}(t) = Z_A I_{boost3}\sin\omega_A(t - t_{L8}) - V_s\cos\omega_A(t - t_{L8}) - V_s \tag{32}$$

$$\Delta t_{L89} = t_{L9} - t_{L8} = \frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost3}^2}} \tag{33}$$

where I_{boost3} is the switch current at the initial resonant time $I_{boost3} = I_{Lrm3} - i_o$

The voltage error in a switching cycle can be obtained from Equations (30) and (32) in the light load condition:

$$v_{err} = \begin{cases} V_s \cos\omega_A (t - t_{L2}) - Z_A I_{boost2} \sin\omega_A (t - t_{L2}) + V_s & t_{L2} \le t \le t_{L3} \\ -V_s - V_s \cos\omega_A (t - t_{L8}) + Z_A I_{boost3} \sin\omega_A (t - t_{L8}) & t_{L8} \le t \le t_{L9} \\ 0 & t_{L0} \le t < t_{L2} \ \ or \ \ t_{L3} < t < t_{L8} \ \ or \ \ t_{L9} < t < t_{L12} \end{cases} \quad (34)$$

Thus, the average voltage error in a switching cycle can be calculated as follows:

$$V_{err} = \frac{1}{T_s}\int_{t_{L0}}^{t_{L12}} v_{err} dt = \frac{\Delta t_{L23} - \Delta t_{L89}}{T_s} V_s = \frac{V_s}{T_s}\left(\left| \frac{2}{\omega_A} \arcsin \frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost2}^2}} \right| - \left| \frac{2}{\omega_A} \arcsin \frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost3}^2}} \right| \right) \quad (35)$$

2.2. Compared with the Hard-Switching Inverter

According to the analysis in Section 2.1, the essential principle of ZVS both in the light and heavy load condition is that the resonant capacitors that are parallelly connected to the next turn-on switches are discharged to zero-voltage and then the body diodes conduct the current. Thus, the switches can be turned on with zero-voltage. The dead-time consists of the resonant stage and diode clamping stage. However, the dead-time effect only exists in the resonant stage, which is caused by the finite rise- and fall-times of the voltage. Figure 4 shows the dead-time effect of a single pole, S_1 and S_3, both in the HLM and LLM where v_a is the actual pole voltage and $v_{a,id}$ is the ideal pole voltage. In order to summarize the dead-time effect both in the HLM and LLM, all the rise- and fall-times are considered to be linearly changed in Figure 4.

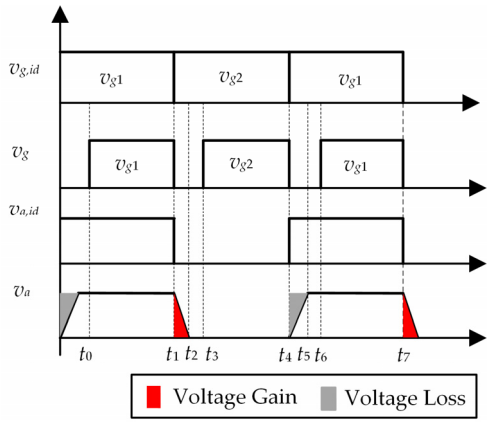


Figure 4. Dead-time effect of the ARSI.

As for the hard-switching inverter, the dead-time effect is different from that of the ARSI. To analyze the dead-time effect, the assumption is the same as that of the ARSI. Figure 5 shows the operating stages and key waveforms of the hard-switching inverter with a single pole.

Regarding the dead-time t_1–t_3, the body diode D_3 conducts the current after S_1 is turned off at t_1. The actual pole voltage is clamped to zero, which equals the ideal pole voltage. As for the dead-time t_4–t_6, the current is diverted from S_3 to its body diode D_3 rather than D_1 after the S_3 is turned off, because of the positive load current. The pole voltage is clamped to zero, whereas the ideal pole voltage is V_s. Therefore, the voltage loss occurs during the dead-time t_4–t_6. Only after S_1 is turned on can the current be diverted to S_1. The dead-time causes voltage loss when the output current is positive. However, when the output current is negative, the dead-time leads to voltage gain.

The dead-time effect of the hard-switching inverter is related to the output current polarity, which causes the blanking delay error, whereas the dead-time effect of the ARSI has no relation to the current polarity. Only the rise- and fall-error occurs in the ARSI, rather than the blanking delay error. Essentially, the voltage error caused by the finite commutation time of the voltage also occurs

in the hard-switching inverter due to the junction capacitances of the switches. However, compared with blanking delay error, this error can be neglected. Regarding the ARSI, the lower the resonant capacitances, the smaller the voltage error. The dead-time effect can be fully eliminated if the resonant capacitances are zero and the junction capacitances are not considered.

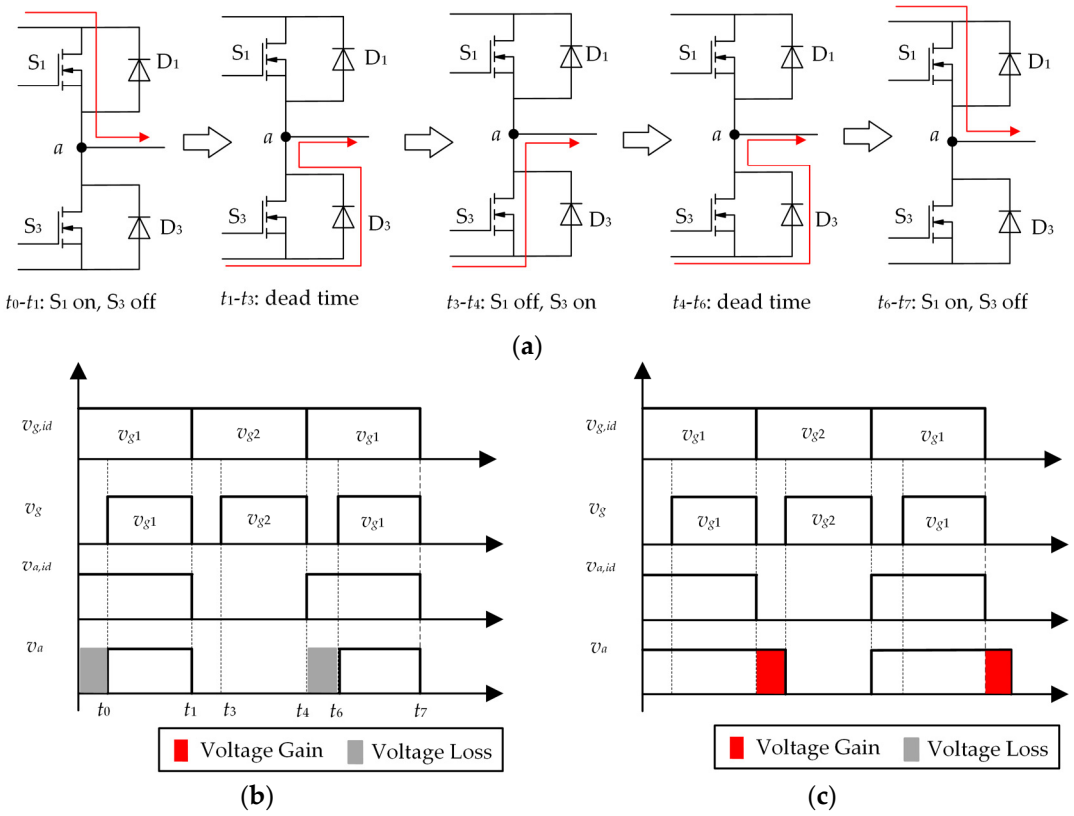


Figure 5. Dead-time effect of hard-switching inverter with single pole (**a**) the operating stages when $i_o > 0$; (**b**) the key waveforms when $i_o > 0$; (**c**) the key waveforms when $i_o < 0$.

3. Compensation Method

In the HLM, the ZVS realization of the main switches is "AZVS + NZVS." In the LLM, the ZVS realization is "AZVS + AZVS." To distinguish the HLM and LLM, the threshold current I_{th} is used, which is given as follows.

$$I_{th} = \frac{2C_r V_s}{t_{dead}} \tag{36}$$

When the magnitude of the load current is lower than I_{th}, the load current cannot discharge the resonant capacitors to zero-voltage. Thus, the ARSI operates in LLM. When the magnitude of the load current is higher than I_{th}, the HLM is adopted. Table 1 shows the realization type of ZVS from zero load to full load.

Table 1. Realization type of ZVS from zero load to full load.

Type	$i_o < -I_{th}$	$-I_{th} \leq i_o \leq I_{th}$	$i_o > I_{th}$
S_2 and S_3	AZVS (S_{r2})	AZVS (S_{r2})	NZVS
S_1 and S_4	NZVS	AZVS (S_{r1})	AZVS (S_{r1})
Load Condition	Heavy Load	Light Load	Heavy Load

The ARSI can reduce the switching loss, whereas the conduction loss is increased due to the auxiliary current. To maintain a low conduction loss, the auxiliary current should be as low as possible. Thus, the initial resonant current I_{boost} is controlled to be constant from zero load to full load as follows.

$$I_{boost1} = I_{boost2} = I_{boost3} = I_{boost} \tag{37}$$

The dead-time effect in the case of positive output current is introduced in Section 2.1. When the output current is negative, the dead-time effect is similar. Therefore, the voltage error caused by the dead-time can be obtained based on Equations (21), (35) and (37):

$$V_{err} = \begin{cases} \frac{V_s}{T_s}\left(\left|\frac{2C_rV_s}{i_o}\right| - \left|\frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2+Z_A^2I_{boost}^2}}\right|\right) & i_o > I_{th} \\ 0 & -I_{th} \le i_o \le I_{th} \\ \frac{V_s}{T_s}\left(\left|\frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2+Z_A^2I_{boost}^2}}\right| - \left|\frac{2C_rV_s}{i_o}\right|\right) & i_o < -I_{th} \end{cases} \tag{38}$$

The voltage error is related to the resonant time. Due to the same I_{boost}, the voltage error is zero in the LLM. As for the HLM, the voltage error occurs because the resonant time is adaptively related to the output current to achieve NZVS, whereas the commutation time to achieve AZVS is constant.

Due to the dead-time effect, a voltage error occurs between the actual pole voltage and ideal pole voltage. The ARSI can be modeled as a proportional gain K_{pwm} without consideration of delays. K_{pwm} is the ratio between the DC voltage and peak value of the carrier in the PWM modulator. The reference voltage v_c is amplified K_{pwm}, thus obtaining the ideal pole voltage $v_{ab,id}$. The actual pole voltage can be obtained by adding the voltage error v_{err}. Figure 6 shows the transfer function of the ARSI.

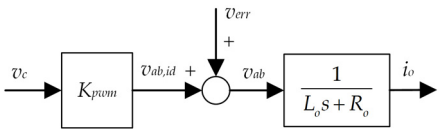


Figure 6. Transfer function of the ARSI.

The output current can be calculated as follows.

$$i_o = \frac{1}{L_os+R_o}v_{ab,id} + \frac{1}{L_os+R_o}v_{err} \tag{39}$$

where the actual voltage $v_{ab,id} = K_{pwm}v_c$.

The voltage error caused by the dead-time effect is considered as a disturbance in the ARSI. To compensate the voltage error, the feedforward method can be utilized, which is shown in Figure 7.

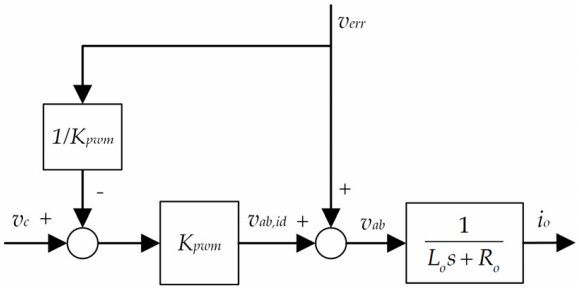


Figure 7. Transfer function of the ARSI with feedforward compensation.

After the feedforward compensation is utilized, the output current can be calculated as follows.

$$i_o = \frac{1}{L_o s + R_o}[(v_c - \frac{v_{err}}{K_{pwm}})K_{pwm} + v_{err}] = \frac{1}{L_o s + R_o} v_{ab,id} \tag{40}$$

According to Equations (39) and (40), the dead-time effect can be eliminated by using the proposed compensation method theoretically.

4. Simulation and Experiment

The proposed compensation method was implemented in the Altera Cyclone IV FPGA of a digitally controlled ARSI prototype using the parameters listed in Table 2. Figure 8 shows the photograph of the prototype, which consists of a FPGA (Altera Corporation EP4CE22E22C7N) control board, a switching power supply, a MOSFET driver and a power circuit. In addition, the method is also verified in the simulation using Saber.

Table 2. Parameters of the circuit.

Parameter	Value
DC voltage V_s	80 V
Switching frequency f_s	200 kHz
Dead-time t_{dead}	0.5 μs
Load	3.7 Ω, 4.87 mH
Resonant inductor L_r	4.4 μH
Resonant capacitor C_r	4.7 nF
Threshold current I_{th}	3 A
I_{boost}	4 A

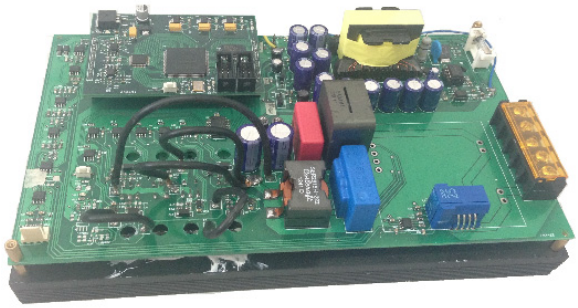


Figure 8. Photograph of the prototype.

Figure 9 shows the open-loop control diagram of the ARSI with proposed dead-time effect compensation. FPGA samples the output current in each switching cycle. Then the mode judgement is completed according to Table 1. The voltage error can be calculated from Equation (38). Therefore, the voltage error can be compensated in the reference voltage. As for the auxiliary current control, the on-time of the auxiliary switches can be calculated after the mode judgement. Finally, the gate signals of the switches can be generated from the compensated reference voltage and the on-time of the auxiliary switches.

The compensation method is based on the model of the voltage error. The more accurate the model, the more precise the compensation result. Figure 10 shows the calculated voltage error vs. output current according to Equation (38). The voltage error only occurs in the HLM. A voltage error about 1.2 V occurs at the threshold current 3A. As the output current increases, the voltage error decreases first before increasing.

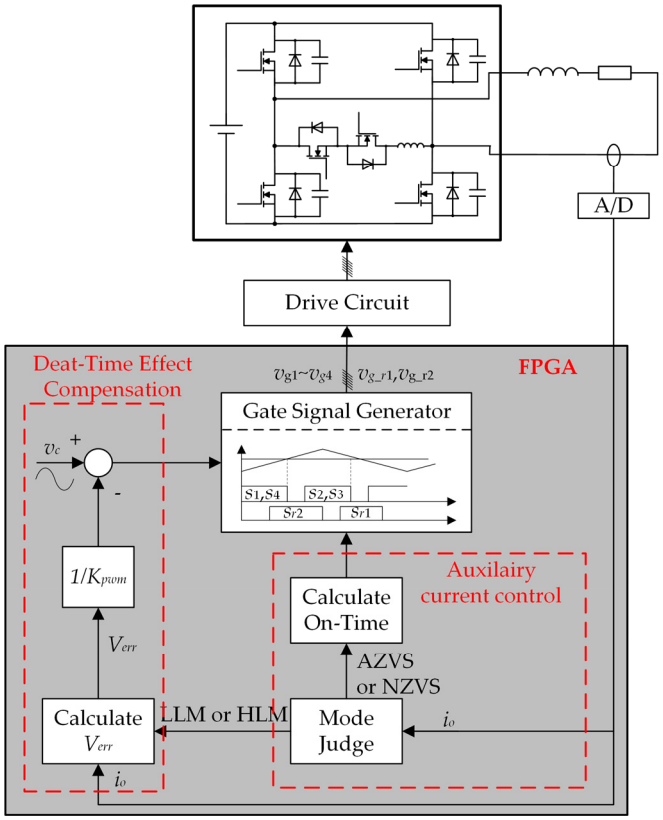


Figure 9. Open-loop control diagram of the ARSI with proposed dead-time effect compensation.

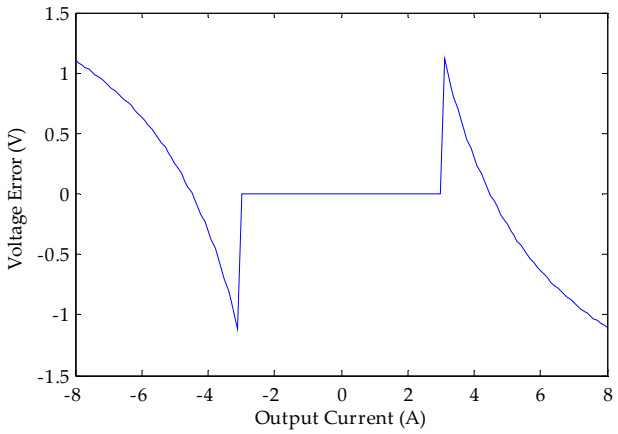


Figure 10. Average voltage error vs. output current in the calculation.

Figure 11 shows the resonant time vs. the switching current both in the calculation and simulation, where the switching current of AZVS is I_{boost} and the switching current of NZVS is i_o. The resonant time of AZVS is nonlinear related to the switching current. When the switching current is high enough, the resonant time of AZVS is close to that of NZVS. The calculation of the resonant time is in good agreement with the simulation results, which is related to the voltage error.

Figure 12 shows the output voltage and current of the hard-switching inverter when the modulation index is 0.4 in an open-loop configuration. To measure the output voltage v_o, a filter is added to attenuate the carrier harmonics of the pole voltage v_{ab}. A serious distortion occurs both in the output current and voltage due to the long dead-time of 0.5 µs.

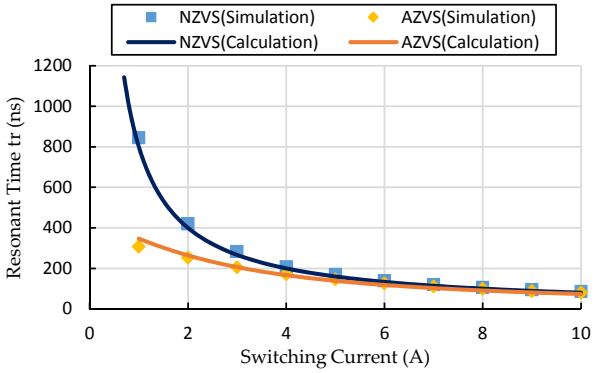
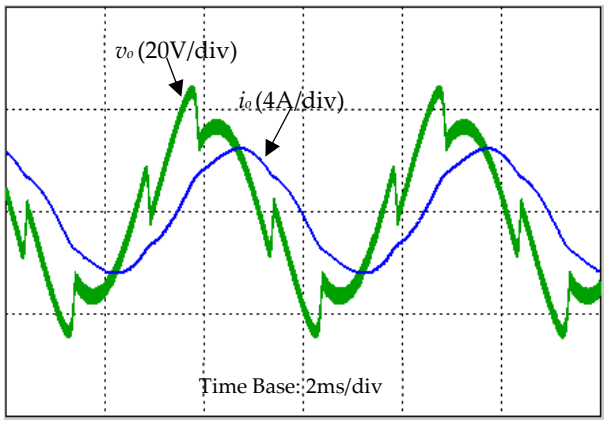
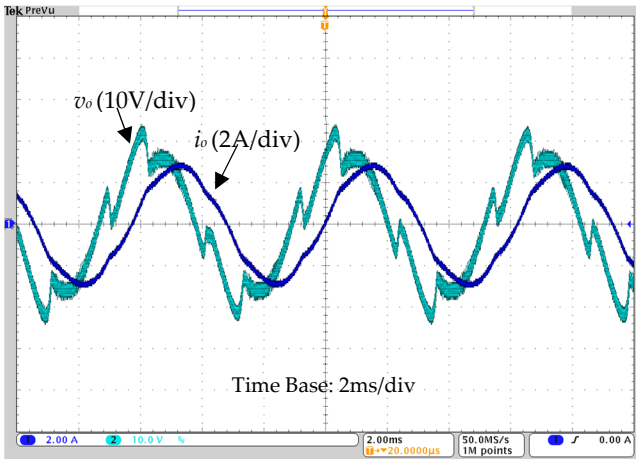


Figure 11. Resonant time vs. the switching current both in the calculation and simulation.



(**a**)



(**b**)

Figure 12. Output voltage and current of the hard-switching inverter when the modulation index is 0.4 in an open-loop configuration. (**a**) simulation results; (**b**) experimental results.

Figures 13 and 14 show the simulation and experimental results of ARSI without dead-time compensation, respectively, when the modulation index is 0.4 in an open-loop configuration. The auxiliary circuit is operated twice with bidirectional current in a switching cycle in the LLM. An obvious distortion occurs in the output voltage at the mode switching point. However, the distortion of the output current and voltage is less than that of the hard-switching inverter in Figure 12, owing to the absence of blanking delay error in the ARSI. Figure 13b shows the voltage error between the actual output voltage and ideal output voltage. The simulation results are in good agreement with

the calculation results in Figure 10 without consideration of the ripple. The maximum voltage error is about 2 V and occurs at the mode switching point.

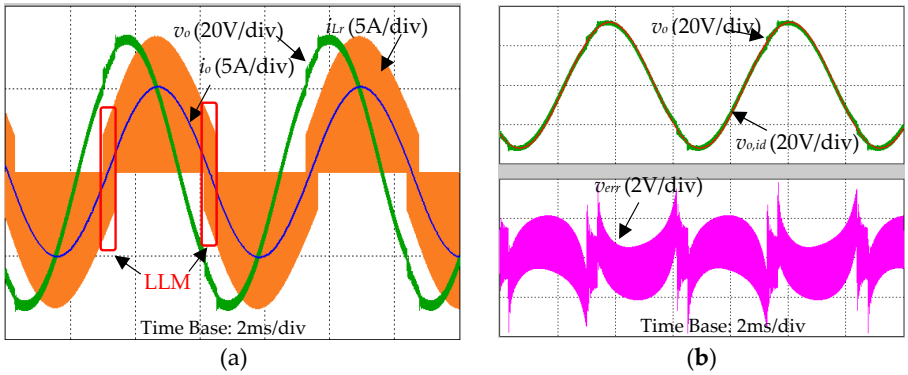


Figure 13. Simulation waveforms of ARSI without dead-time compensation when the modulation index is 0.4 in an open-loop configuration. (**a**) simulation results; (**b**) voltage error.

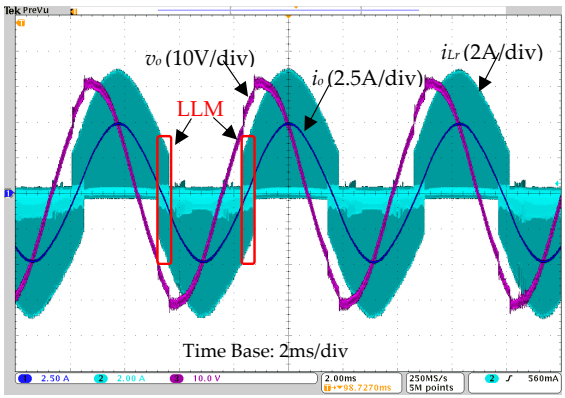


Figure 14. Experimental waveforms of ARSI without dead-time compensation when the modulation index is 0.4 in an open-loop configuration.

Figures 15 and 16 show the simulation and experimental results, respectively, when the proposed compensation method is used in the ARSI. The output voltage distortion is reduced in Figures 15a and 16 without increasing the auxiliary current i_{Lr}. Figure 15b demonstrates that the voltage error is reduced.

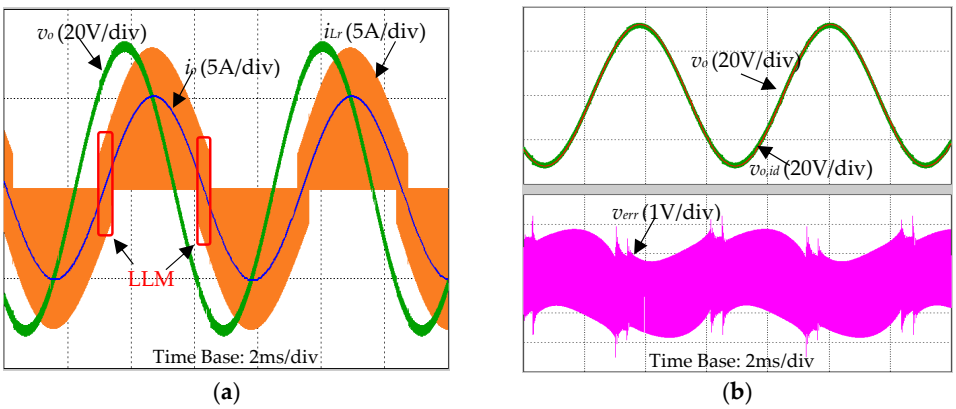


Figure 15. Simulation waveforms of ARSI with dead-time compensation when the modulation index is 0.4 in an open-loop configuration. (**a**) simulation results; (**b**) voltage error.

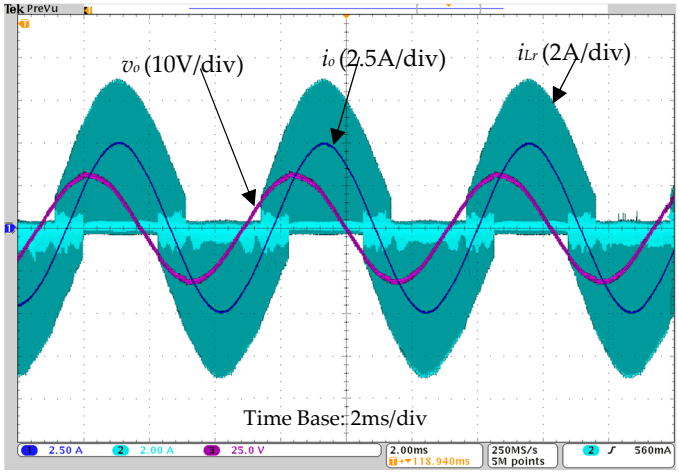


Figure 16. Experimental waveforms of ARSI with dead-time compensation when the modulation index is 0.4 in an open-loop configuration.

Figure 17 shows the magnitudes of the 2nd–10th harmonic components with respect to the fundamental component in the output voltage and current. The power analysis module DPO4PWR is used to analyze the total harmonic distortions (THDs) of the current and voltage. Figure 17a demonstrates that THD of the output voltage with the compensation method is 3.48% which is less than 6.29% than without dead-time effect compensation. The magnitudes of the 2nd–10th harmonics are reduced, except for the 8th harmonic. Figure 17b indicates that THD of the output current is reduced from 1.57% to 0.712% by using the proposed compensation method.

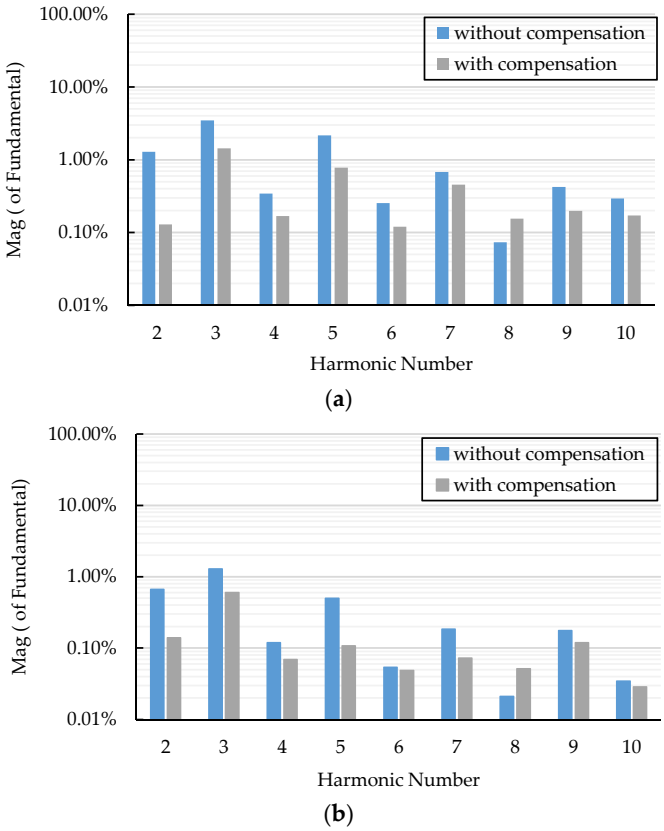


Figure 17. Magnitudes of the 2nd–10th harmonic components in respect to the fundamental component (**a**) output voltage; (**b**) output current.

Figure 18 shows the experimental voltage and current THDs under different load conditions. As the modulation index increases, the THDs of the output voltage and current both decrease. Through using the dead-time compensation strategy, the THDs of the output voltage and current are clearly reduced.

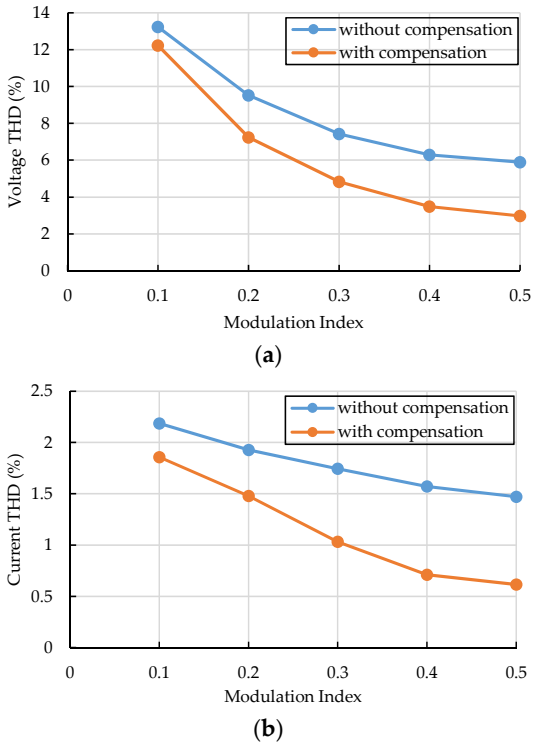


Figure 18. Experimental voltage and current THDs under different load condition (**a**) voltage THD; (**b**) current THD.

5. Conclusions

In this paper, the dead-time effect of a typical zero-voltage-switching (ZVT) inverter—the auxiliary resonant snubber inverter (ARSI)—is analyzed. The ARSI can fully eliminate the blanking delay error which is the main drawback of the hard-switching inverter. Only the rise- and fall-error caused by the resonant capacitors occurs in the ARSI, which is not considered in the hard-switching inverter. In the simulation and experiment, the quality of the output in the ARSI is significantly better than that in the hard-switching inverter, even if the dead-time compensation strategy is not used.

Furthermore, a feed-forward compensation method based on the voltage error estimation is proposed to compensate the rise- and fall-error of dead-time effect. Both the simulation and experimental results show that the compensation strategy can effectively reduce the THDs of the outputs.

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