

Article

# Digital Controller Design Based on Active Damping Method of Capacitor Current Feedback for Auxiliary Resonant Snubber Inverter with LC Filter

Hailin Zhang, Baoquan Kou \*, Lu Zhang and Yinxi Jin

Department of Electrical Engineering, Harbin Institute of Technology, Harbin 150080, China; zhanghailin0310@sina.com (H.Z.); zhanglu24@hit.edu.cn (L.Z.); jinyinxi2006@126.com (Y.J.)

\* Correspondence: koubq@hit.edu.cn; Tel.: +86-451-8640-3771

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**Abstract:** In some high-performance applications, an LC filter must be added to the auxiliary resonant snubber inverter (ARSI) to reduce the output current ripple. However, resonance occurs due to the additional LC filter, which makes the traditional closed-loop control not suitable to be used directly. Therefore, this paper presents a double-loop digital control based on the active damping method of capacitor current feedback to stabilize the system. Most of the studies on active damping methods are focused on the grid in consideration of zero resistance. However, the load resistance should not be neglected in the drive system. Therefore, the load resistance and digital control delays are considered in this paper. Moreover, an improved loading method is proposed to improve the duty ratio range. In order to verify the effectiveness of the controller, a prototype was developed. The simulation and experimental results demonstrate that soft-switching can be realized for the entire load range. The maximum duty ratio is improved by 0.01 by using the proposed loading method. The resonance can be eliminated by using the proposed control method.

**Keywords:** auxiliary resonant snubber inverter (ARSI); zero-voltage switching (ZVS); LC filter; active damping; delays

## 1. Introduction

In power electronic converters, high switching frequency is a highly desirable feature, which can not only reduce the volume and power density of converters, but also increase the dynamic response. However, high switching frequency brings about the problems of high switching loss and severe electromagnetic interference (EMI) [1,2]. The soft switching technique is one of the best options to address the problems above. To date, a variety of soft-switching DC-AC topologies have been proposed. Among them, the zero-voltage-transition (ZVT) pulse-width-modulation (PWM) inverter is a typical soft-switching inverter [3–11]. An auxiliary circuit connected parallel to the main power path is employed in the ZVT PWM inverter, which only operates for a short interval before and after the commutation period of the main switches. This makes the ZVT inverter closest to the PWM converter counterpart. Compared with other soft-switching inverters, the voltage and current stresses and conduction losses are much lower [3,4]. Contributing to these advantages, the ZVT PWM inverter is well accepted.

Several topologies of the ZVT PWM inverter have been proposed. The auxiliary resonant commutated pole inverter (ARCPI) has been proposed with two auxiliary switches per phase [5,6]. The ARCPI can meet the demand for high efficiency and low voltage and current stresses. However, the major drawback is the existence of the split capacitors, which cause the problems of capacitor charge unbalance. The auxiliary resonant snubber inverter (ARSI) has been proposed to eliminate the

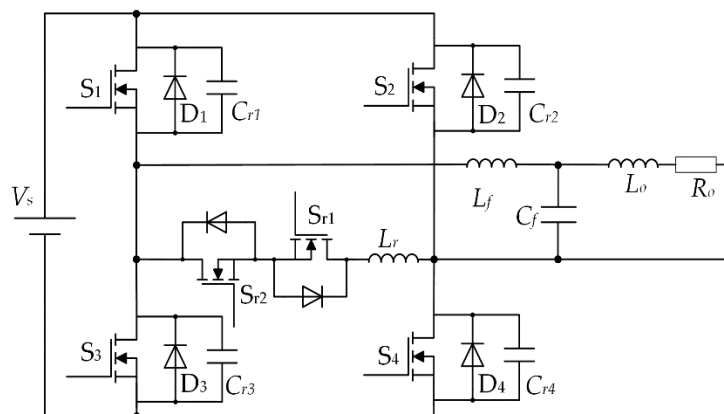
split capacitors, but the three-phase topology cannot utilize the conventional space-vector-pulse-width modulation (SVPWM) [7,8]. Thus, they are more suitable for permanent magnet brushless DC motors instead of all types of motors. The single-phase topology is very attractive with only two auxiliary switches and well fit to the conventional PWM. Meanwhile, the ZVT inverter using coupled magnetics has been proposed to eliminate the split capacitors [9–11]. However, these topologies need coupled inductors and a large number of auxiliary switches, which increases the cost and difficulty of the circuit realization. The ZVT PWM converter has been synthesized and summarized in [3,4].

In high-precision motor drive applications, an LC filter must be added in the ARSI to reduce the output current ripple. Moreover, the additional LC filter can solve problems of poor insulation that result from the overvoltage [12]. However, since the additional LC filter together with the inductor of the motor forms the LCL filter, a resonance peak occurs in the system, which makes the system unstable. Recently, the passive damping method has been used to stabilize the system [13,14]. The passive components of resistors, capacitors, and inductors are parallel or series-connected to the filter capacitor to damp out the resonance. The method is easy to implement; however, it reduces the efficiency of the system. The active damping method can be used to damp out the resonance at no expense of efficiency. The state variable feedback, such as filter capacitor voltage [15,16] or filter capacitor current [17,18], is introduced to provide virtual resistance. Among them, the capacitor current feedback is a typical and widely used method.

Most studies of the active damping method have focused on the grid with consideration of zero resistance. However, in the drive system, the load resistance should not be neglected. Until now, only a few researchers have studied the active damping in the motor drive system; however, they have not taken into consideration the digital control delays. In addition, previous studies on ARSI have focused on the circuit design and auxiliary current control but there has been a lack of research about the design of the closed-loop control. Thus, a step-by-step closed-loop controller design of the ARSI with LC filter is proposed in this paper, including the auxiliary current controller and the output current controller. A double-loop control based on active damping method of capacitor current feedback and PI regulator is introduced. The load resistance and digital control delays are considered. Moreover, an improved loading scheme of digital PWM (DPWM) is proposed to improve the duty ratio range of the ARSI. Finally, simulations and experiments are carried out to verify the effectiveness of the proposed method.

## 2. Control of the ARSI

Figure 1 depicts the single-phase ARSI topology analyzed in this paper, which consists of a standard H-bridge inverter, an auxiliary circuit, and an LC filter. The proper operation of the auxiliary switches  $S_{r1}$  and  $S_{r2}$  can create zero-voltage-switching (ZVS) conditions for the main switches  $S_1$ – $S_4$ . Meanwhile, the auxiliary switches can realize zero-current switching (ZCS).



**Figure 1.** Circuit of the single-phase auxiliary resonant snubber inverter (ARSI) with LC filter.

Figure 2 shows a control diagram of the ARSI. The ARSI controller consists of an output current controller and an auxiliary current controller. In the output current controller, the driving signals of the main switches are generated according to the output current. In order to dampen the resonance caused by the LC filter, a filter capacitor current feedback is introduced. The auxiliary current controller aims to control the auxiliary current to achieve ZVS of the main switches. Due to the large amount of calculations and the need for logic sequential control in the auxiliary current controller, a digital controller is required.

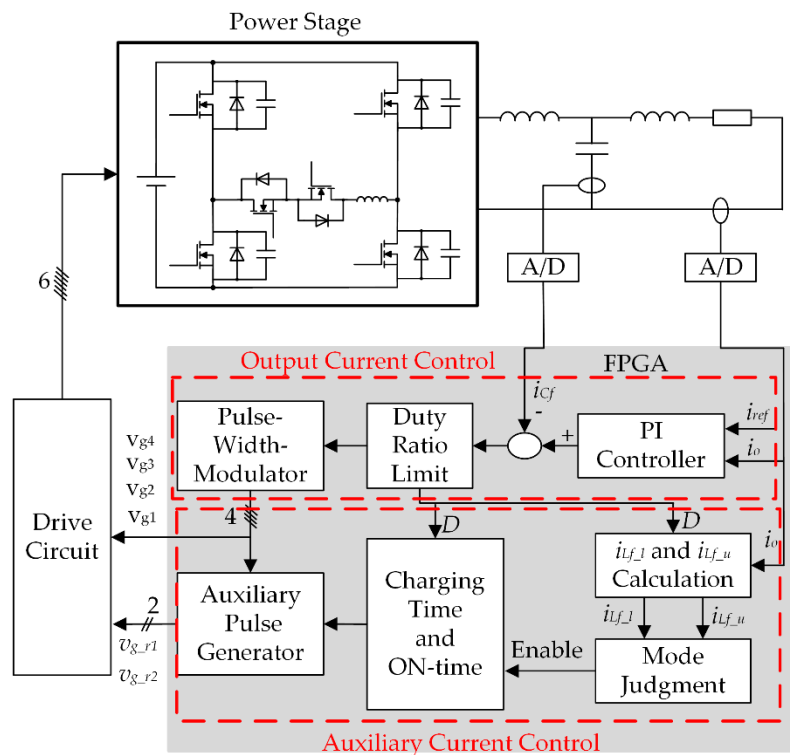


Figure 2. Control diagram of the ARSI.

The auxiliary current control involves two methods, fixed-timing control [19] and variable-timing control [20]. Owing to the advantages of lower conduction losses and achieving soft-switching for a wide load range, variable-time control methods are more widely used. By using the variable-timing control, the auxiliary current follows the magnitude of the load current adaptively. The auxiliary current controller in Figure 2 is realized based on the variable-timing control. The auxiliary controller is influenced by the output current controller, whereas the output current controller is independent of the auxiliary current controller.

### 3. The Load Adaptive Auxiliary Current Control

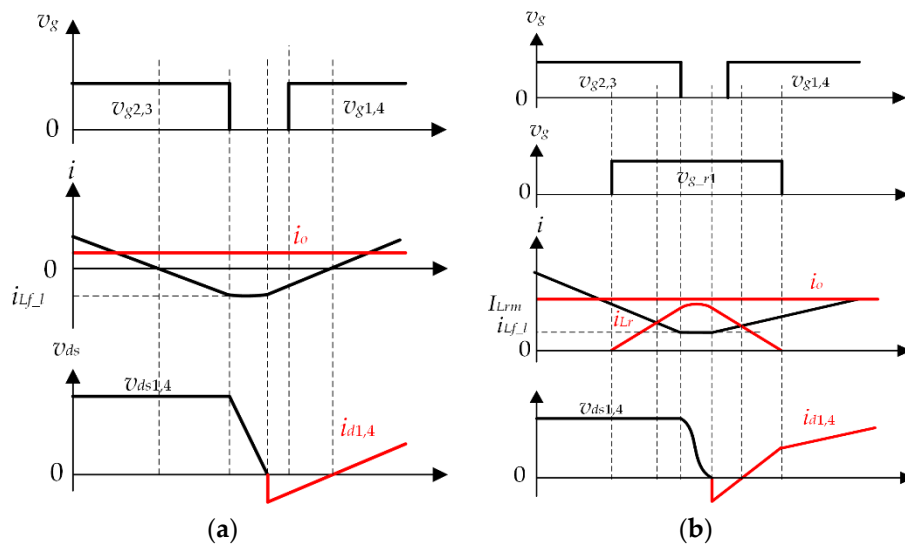
#### 3.1. Principle

Essentially, the ZVS realization of the main switches is to obtain a proper initial resonant current  $I_r$ , in order to discharge the resonant capacitors to zero voltage before the main switches are turned on. Figure 3 shows the key waveforms to realize ZVS of  $S_1$  and  $S_4$ , where  $v_{ds}$  is the drain-source voltage of a MOSFET,  $i_d$  is the drain current of a MOSFET,  $v_g$  is the gate signal,  $i_{L_f}$  is the filter inductor current,  $i_{L_f_l}$  is the lower envelope of  $i_{L_f}$ ,  $i_{L_f_u}$  is the upper envelope of  $i_{L_f}$ , and  $i_{L_r}$  is the auxiliary current. When  $i_{L_f_l} < -I_{r\_min}$ ,  $i_{L_f_l}$  can create natural ZVS (NZVS) conditions for  $S_1$  and  $S_4$  without the operation of auxiliary switches. When  $i_{L_f_l} > -I_{r\_min}$ ,  $S_{r1}$  is turned on before  $S_2$  and  $S_3$  are turned off. The resonant inductor  $L_r$  is charged, resulting in the linear increase of the auxiliary current. Therefore,

a proper  $I_r$  can be obtained with the operation of  $S_{r1}$ . The auxiliary ZVS (AZVS) of  $S_1$  and  $S_4$  is realized. In order to fully discharge the resonant capacitors, the minimum initial resonant current must meet the following requirement:

$$I_{r\_min} \geq \frac{2C_r V_s}{t_{dead}} \tag{1}$$

The principle of ARSI without LC filter was introduced in [21]. The initial resonant current is the difference between the auxiliary current and the output current. Namely, the required auxiliary current is the sum of the output current and initial resonant current. As for the ARSI with LC filter, the auxiliary current is the sum of the filter inductor envelope current and the initial resonant current, which is different from that of the ARSI without LC filter.



**Figure 3.** Key waveforms to realize the zero-voltage switching (ZVS) of  $S_1$  and  $S_4$  (a)  $i_{Lf\_l} < -I_{r\_min}$ ; (b)  $i_{Lf\_l} > -I_{r\_min}$ .

The filter current ripple can be calculated as follows:

$$\Delta i_{Lf} = \frac{V_s - v_o}{L_f} D T_s = \frac{(2 - 2D) D V_s T_s}{L_f} \tag{2}$$

where  $v_o$  is the output voltage,  $D$  is the duty ratio, and  $T_s$  is the switching period.

The upper and lower envelopes of the filter inductor current can be calculated as follows:

$$i_{Lf\_u} = i_o + \frac{1}{2} \Delta i_{Lf} = i_o + \frac{(1 - D) D V_s T_s}{L_f} \tag{3}$$

$$i_{Lf\_l} = i_o - \frac{1}{2} \Delta i_{Lf} = i_o - \frac{(1 - D) D V_s T_s}{L_f} \tag{4}$$

The ZVS realization of  $S_1$  and  $S_4$  is related to the lower envelope of the filter inductor current  $i_{Lf\_l}$  shown in Figure 3. Similarly, the ZVS realization of  $S_2$  and  $S_3$  is related to the upper envelope of the filter inductor current  $i_{Lf\_u}$ . Table 1 shows the ZVS types under different load conditions.

**Table 1.** Zero-voltage switching (ZVS) types of switches under different output currents.

Switch	$i_{Lf\_l} < -I_{r\_min}$	$i_{Lf\_l} > -I_{r\_min}$	Switch	$i_{Lf\_u} < I_{r\_min}$	$i_{Lf\_u} > I_{r\_min}$
$S_1$ & $S_4$	NZVS	AZVS ( $S_{r1}$ )	$S_2$ & $S_3$	AZVS ( $S_{r2}$ )	NZVS

The output current can be obtained through the current sensor. Therefore, the required auxiliary current can be calculated as follows:

$$I_{Lrm} = \begin{cases} I_r + i_{Lf\_l} & \text{for } S_{r1} \\ I_r - i_{Lf\_u} & \text{for } S_{r2} \end{cases} \quad (5)$$

The charging rate and the discharging rate of the resonant inductor are the same because of the same voltage  $V_s$ . Therefore, the charging time of the resonant inductor  $t_{ch}$  and the on-time of the auxiliary switch  $t_A$  can be calculated as follows:

$$t_{ch} = \frac{L_r I_{Lrm}}{V_s} \quad (6)$$

$$t_A = 2t_{ch} + t_{dead} \quad (7)$$

After generating the driving signals of the main switches, the gate signal of the auxiliary switches can be generated from Equations (6) and (7).

### 3.2. Limitation of the Duty Ratio

In the ARSI, to guarantee the ZVS of one set of switches, the auxiliary circuit must be turned on before the opposite set of switches is turned off. Subsequently, the resonant inductor can be charged to the required current. Therefore, the minimum on-time of the opposite set of switches must be longer than the maximum charging time of the resonant inductor. This requirement limits the maximum duty ratio  $D_{max}$ .

Figure 4 shows the DPWM diagram of the ARSI. The triangle carrier is adopted due to its lower harmonic compared to the sawtooth carrier [22]. Moreover, the current is synchronously sampled at twice the PWM carrier interval, which can eliminate the switching current ripple from the current samples without needing low-pass filtering or complex ripple elimination filters [23]. Then the calculated reference voltage  $v_c$  is loaded into a modulator at the point of upper limit and lower limit of the reference voltage  $V_{upperlimit}$  and  $V_{lowerlimit}$  instead of the conventional loading point  $V_{cmax}$  and  $V_{cmin}$ . The proposed loading method can improve the maximum duty ratio. The reason is given as follows:

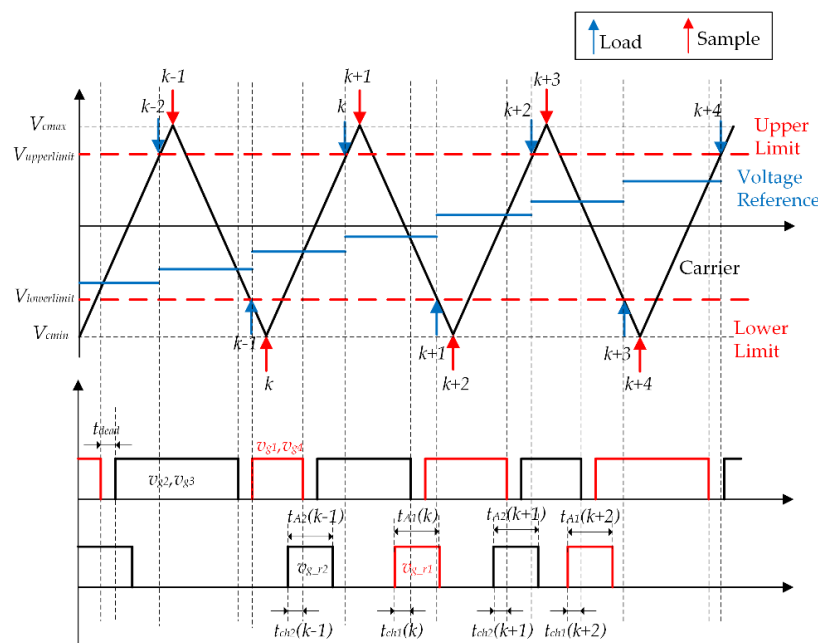


Figure 4. Digital pulse-width-modulation (DPWM) diagram of the ARSI.

In order to achieve ZVS from zero load to full load, the minimum on-time of the main switches must be longer than the maximum charging time of the resonant inductor:

$$t_{on\_min} \geq t_{ch\_max} \tag{8}$$

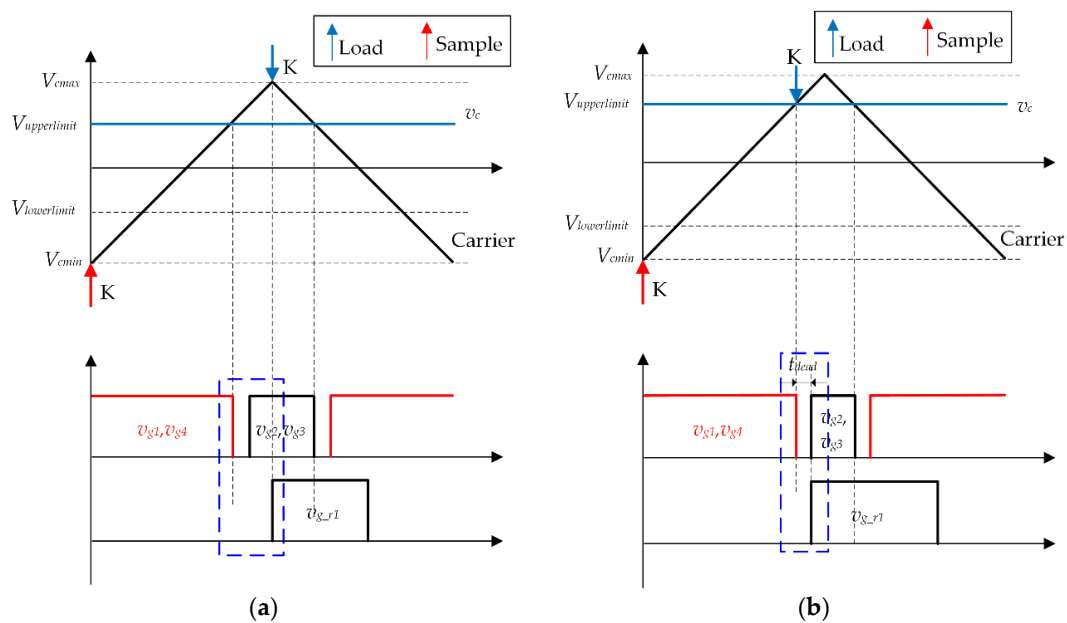
The maximum charging time occurs when the output current reaches its maximum value  $I_{o\_max}$ . The minimum on-time of the main switches occurs when the duty ratio reaches  $D_{max}$ . Figure 5 shows the DPWM diagram at the condition of  $I_{o\_max}$  and  $D_{max}$ . Figure 5a shows the conventional loading scheme, namely loading at  $V_{cmax}$  and  $V_{cmin}$ . The Kth current is sampled at the point  $V_{cmin}$ . Then the data are loaded at the next  $V_{cmax}$  after calculation. Subsequently,  $S_{r1}$  can be turned on to charge the resonant inductor. Therefore, the following requirement must be met based on Equation (8):

$$\frac{T_s}{2(V_{cmax} - V_{cmin})} (V_{cmax} - V_{upperlimit}) \geq t_{ch\_max} \tag{9}$$

The upper limit of the reference voltage can be obtained from Equation (9):

$$V_{upperlimit} \leq V_{cmax} - \frac{2(V_{cmax} - V_{cmin})t_{ch\_max}}{T_s} \tag{10}$$

The maximum duty ratio  $D_{max}$  occurs when  $t_{on\_min}$  equals  $t_{ch\_max}$ . However, Figure 5a shows that  $t_{on\_min}$  is still longer than  $t_{ch\_max}$  in this case. Only after the Kth data are loaded at  $V_{cmax}$ ,  $S_{r1}$  can be controlled. In this case, a short time cannot be utilized.



**Figure 5.** DPWM diagram at the condition of  $I_{o\_max}$  and  $D_{max}$ : (a) conventional loading scheme; (b) improved loading scheme.

In order to improve  $D_{max}$ , an improved loading scheme is adopted in which the data are loaded at  $V_{upperlimit}$  and  $V_{lowerlimit}$ . In this case,  $S_{r1}$  can be turned on in advance. Furthermore, this loading scheme will not influence the gate signal generation of the main switches because the reference voltage  $v_c$  is limited between  $V_{upperlimit}$  and  $V_{lowerlimit}$ . Figure 5b shows that  $t_{on\_min}$  equals  $t_{ch\_max}$  by using the improved loading scheme, which improves  $D_{max}$ .

In the improved loading scheme, the following requirement must be satisfied based on Equation (8):

$$\frac{T_s}{2(V_{cmax} - V_{cmin})} \cdot 2(V_{cmax} - V_{upperlimit}) - t_{dead} \geq t_{ch\_max} \tag{11}$$

The upper limit of the reference voltage can be obtained from Equation (11):

$$V_{upperlimit} \leq V_{cmax} - \frac{(V_{cmax} - V_{cmin})(t_{ch\_max} + t_{dead})}{T_s} \tag{12}$$

From Equations (10) and (12), the limit of the reference voltage  $v_c$  can be improved by adopting the improved loading scheme, resulting in larger  $D_{max}$ .

#### 4. Output Current Control

##### 4.1. The Model of the ARSI

Figure 6 shows the digital control model of the output current controller, where  $G_c(z)$  is the proportional integral (PI) regulator,  $G_{dc}(z)$  is the calculation and transport delay, the sampling switch stands for analog digital converter,  $K_{pwm}$  is the gain of the ARSI,  $K_{cf}$  is the filter capacitor current feedback coefficient, and  $G_1(s)$  and  $G_2(s)$  are the output impedance. In the digital controller, all the calculations and operations are discrete. Therefore, the digital controller is modeled on the z-domain.

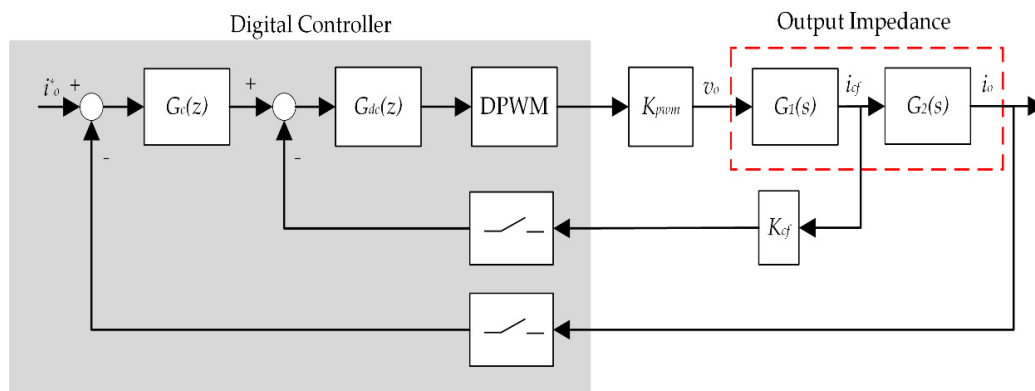


Figure 6. Digital control model of the output current controller.

##### 4.2. PI Controller Design

Commonly, the sample period is short and the time constant of the controlled plant is much larger than the sample period. Therefore, the digital PI controller can be designed in the s-domain. Figure 7 shows the output current controller model in the s-domain.

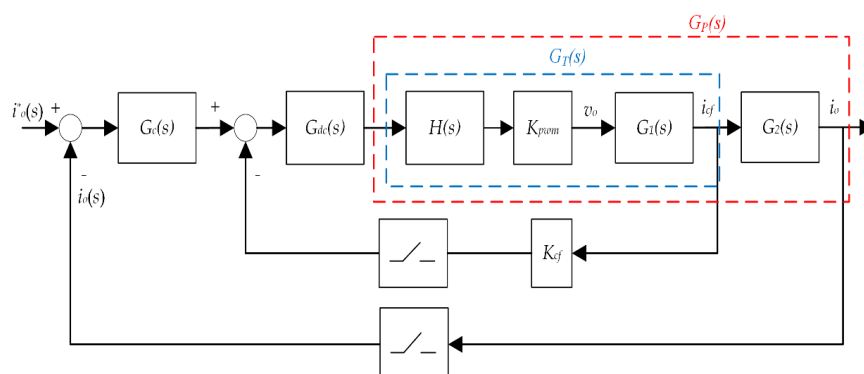


Figure 7. Output current controller model in the s-domain.

The PI regulator  $G_c(s)$  can be written as follows:

$$G_c(s) = K_p + \frac{K_i}{s} \tag{13}$$

After the current is sampled, a sampling period delay  $T_{sp}$  exists, which is shown in Figure 4. Therefore, the calculation and transport delay can be written as follows:

$$G_{dc}(s) = e^{-T_{sp}s}, \tag{14}$$

where the sampling period  $T_{sp} = T_s/2$ .

In the s-domain, the sampling switch can be modeled as  $1/T_{sp}$  [24]. The modulator can be modeled by zero-order holder (ZOH) [25], which can be expressed as:

$$H(s) = \frac{1 - e^{-T_{sp}s}}{s} \approx T_{sp}e^{-0.5T_{sp}s}. \tag{15}$$

Commonly, the cutoff frequency of the LC filter is larger than the bandwidth frequency of the ARSI. Therefore, the filter inductance is much lower than the load inductance, namely  $L_f \ll L_o$ . The output impedance can be written as follows:

$$G_1(s) = \frac{i_{cf}(s)}{v_o(s)} = \frac{s^2L_oC_f + sR_oC_f}{s^3L_fC_fL_o + s^2L_fC_fR_o + s(L_o + L_f) + R_o} \approx \frac{sC_f}{s^2L_fC_f + 1} \tag{16}$$

$$G_2(s) = \frac{i_o(s)}{i_{cf}(s)} = \frac{1}{s^2L_oC_f + sR_oC_f}. \tag{17}$$

The system open-loop transfer function can be calculated as follows:

$$G(s) = \frac{i_o(s)}{i_o^*(s) - i_o(s)} = (K_p + \frac{K_i}{s}) \cdot \frac{K_{pwm}e^{-1.5T_{sp}s}}{(s^2L_fC_f + 1)(sL_o + R_o) + sK_{pwm}K_{cf}e^{-1.5T_{sp}s}C_f(sL_o + R_o)}. \tag{18}$$

The closed-loop transfer function can be written as follows:

$$T(s) = \frac{i_o(s)}{i_o^*(s)} = \frac{G_{dc}(s)G_c(s)G_P(s)}{1 + K_{cf}G_{dc}(s)G_T(s) + G_{dc}(s)G_c(s)G_P(s)}. \tag{19}$$

In order not to reduce the bandwidth of the ARSI, the cutoff frequency of the LC filter is designed to be two times larger than the system bandwidth  $f_c$ . Therefore, the influence of the filter capacitor can be ignored when calculating the magnitude of the loop gain at  $f_c$  and frequencies lower than  $f_c$ . The low-frequency controller characteristics will still be dominated by the series filter inductance. Thus, the transfer Equation (18) can be approximated as follows:

$$G(s) \approx (K_p + \frac{K_i}{s}) \cdot \frac{K_{pwm}e^{-1.5T_{sp}s}}{sL_o + R_o}. \tag{20}$$

Figure 8 shows the Bode plots of the approximation model (20) and the precise model (18). It demonstrates that the cutoff frequency of the system will not be influenced by using the approximation model.



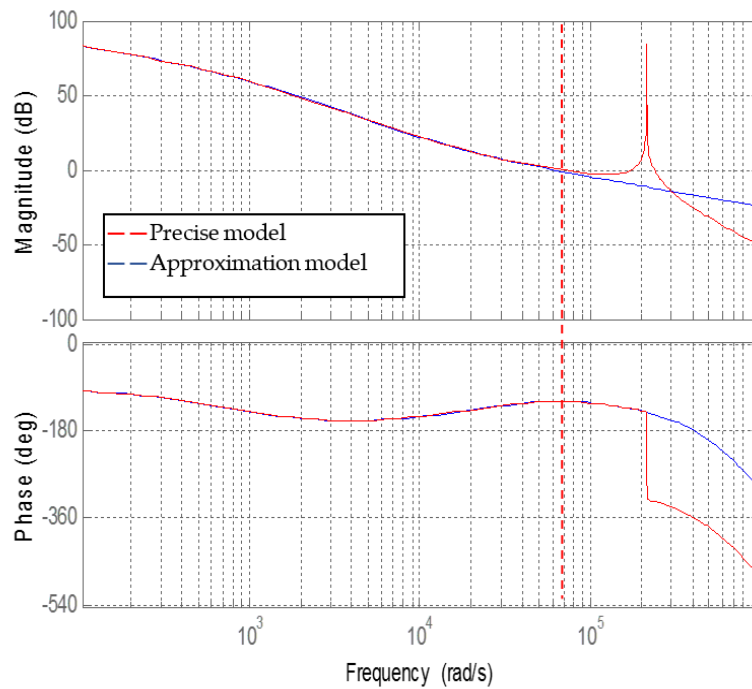


Figure 8. Bode plot of the approximated model and the precise model.

When the crossover frequency and phase margin are specified as  $\omega_c$  and  $\phi_m$  respectively, the parameters of the PI controller can be obtained:

$$\left\{ \begin{array}{l} K_p = \frac{\sqrt{(L_o\omega_c)^2 + R_o^2}}{K_{pwm} \sqrt{1 + \frac{1}{\tan^2(-\frac{\pi}{2} + 1.5\omega_c T_{sp} + \phi_m + \arctan \frac{\omega_c L_o}{R_o})}}} \\ K_i = \frac{\omega_c K_p}{\tan(-\frac{\pi}{2} + 1.5\omega_c T_{sp} + \phi_m + \arctan \frac{\omega_c L_o}{R_o})} \end{array} \right. \quad (21)$$

If  $K_p \gg K_i/\omega_c$ , Equation (21) can be approximated as:

$$\left\{ \begin{array}{l} K_p = \frac{\sqrt{(L_o\omega_c)^2 + R_o^2}}{K_{pwm}} \\ K_i = \frac{\omega_c K_p}{\tan(-\frac{\pi}{2} + 1.5\omega_c T_{sp} + \phi_m + \arctan \frac{\omega_c L_o}{R_o})} \end{array} \right. \quad (22)$$

Figure 9 shows the Bode plot of the ARSI with different PI parameters. The circuit parameters are listed in Table 2. When  $K_p \gg K_i/\omega_c$ , the crossover frequency  $\omega_c$  is determined by  $K_p$ . The larger  $K_p$ , the larger  $\omega_c$  and the faster the dynamic response. Regarding  $K_i$ , it will influence the low-frequency gain, which can influence the stable precision of the system. The larger  $K_i$ , the larger the low-frequency gain and the higher the stable precision.  $K_i$  has almost no influence on the frequency characteristic around  $\omega_c$  when  $K_p \gg K_i/\omega_c$ . However, when  $K_i/\omega_c$  is close to  $K_p$ ,  $K_i$  will influence the phase margin. The larger  $K_i$ , the smaller the phase margin.

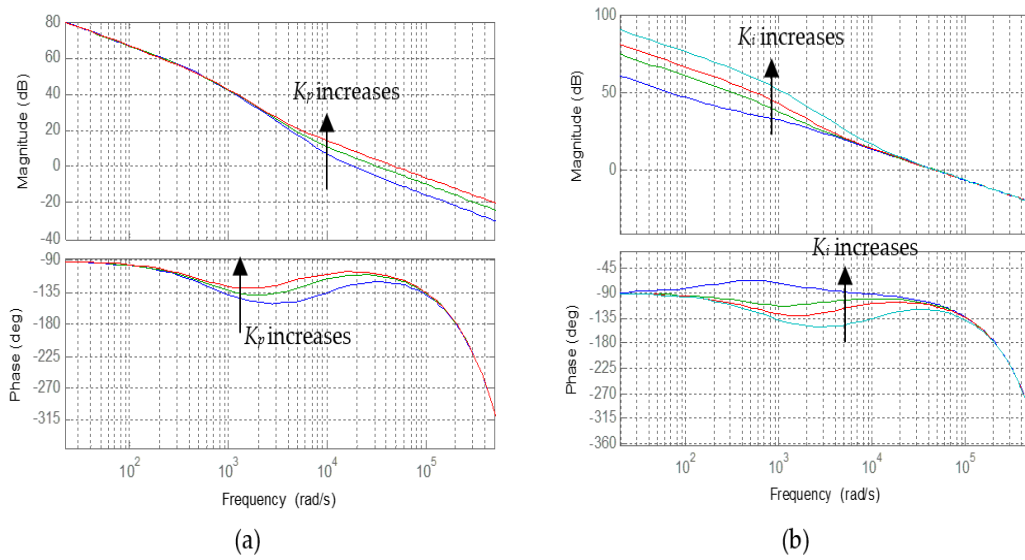


Figure 9. Bode plot of the ARSI with different PI parameters: (a) different  $K_p$ ; (b) different  $K_i$ .

Table 2. Parameters of the circuit.

Parameter	Value
DC voltage $V_s$	80 V
Switching frequency $f_s$	200 kHz
Dead time $t_{dead}$	0.2 $\mu$ s
Load	3.7 $\Omega$ , 4.87 mH
Resonant inductor $L_r$	2.2 $\mu$ H
Resonant capacitor $C_r$	2.7 nF
Filter inductor $L_f$	22 $\mu$ H
Filter capacitor $C_f$	1 $\mu$ F
Maximum output current $I_{o\_max}$	8 A

### 4.3. Capacitor Current Feedback Design

In Section 4.2, the influence of filter capacitor is neglected when the PI parameters are designed. However, the LC filter together with the load inductance forms the LCL filter, which leads to resonance. To analyze the stability of the ARSI, the influence of filter capacitor cannot be ignored. The filter capacitor current feedback is introduced to damp the resonance.

Because of the delay caused by the computation, the system is no longer a minimum phase system. To design the inner capacitor current loop, a discrete model must be built instead of a continuous model. Figure 10 shows the model of the inverter, which is obtained from Figure 6.

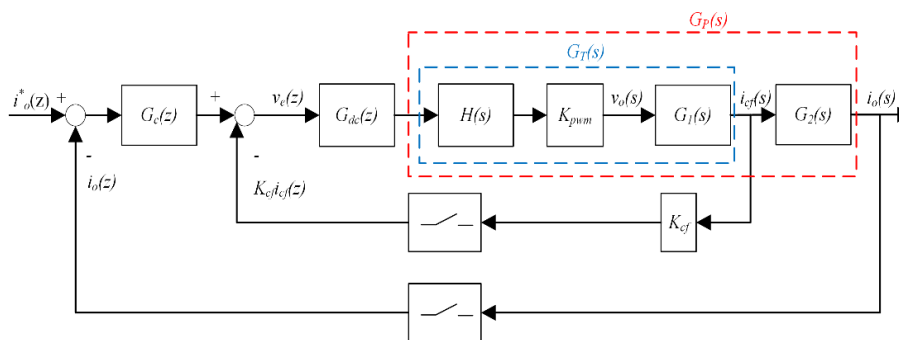


Figure 10. Model of ARSI in digital control.

The closed-loop and open-loop transfer functions can be obtained as follows. (The detailed proof is presented in Appendix A.)

$$T(z) = \frac{i_o(z)}{i_o^*(z)} = \frac{G_{dc}(z)G_c(z)G_P(z)}{1 + K_{cf}G_{dc}(z)G_T(z) + G_{dc}(z)G_c(z)G_P(z)} \tag{23}$$

$$G(z) = \frac{i_o(z)}{i_o^*(z) - i_o(z)} = \frac{G_{dc}(z)G_c(z)G_P(z)}{1 + K_{cf}G_{dc}(z)G_T(z)} \tag{24}$$

where

$$G_c(z) = K_p + \frac{K_i}{1 - z^{-1}}$$

$$G_{dc}(z) = z^{-1}$$

$$G_T(z) = K_{pwm} \sqrt{\frac{C_f}{L_f}} \frac{(z - 1)\sin\varphi}{z^2 - 2z\cos\varphi + 1}$$

$$G_P(z) = K_{pwm} \frac{-z(R_oF\cos\varphi + L_o\omega_{res}F\sin\varphi - R_oF) + R_oF - R_oF\cos\varphi + L_o\omega_{res}F\sin\varphi}{z^2 - 2z\cos\varphi + 1}$$

$$F = \frac{L_f C_f}{L_o^2 + L_f C_f R_o^2}$$

$$\varphi = \omega_{res} T_{sp}$$

$$\omega_{res} = \frac{1}{\sqrt{L_f C_f}}$$

In the z-domain, the root locus is used to analyze the stability of the system. The relevant expressions can be developed from Equation (23) as follows:

$$1 + K_{cf}G_{dc}(z)G_T(z) + G_{dc}(z)G_c(z)G_P(z) = 0. \tag{25}$$

Equation (19) can be transformed as follows:

$$1 + K_{cf} \frac{G_{dc}(z)G_c(z)}{1 + G_{dc}(z)G_c(z)G_P(z)} = 0. \tag{26}$$

From Equation (26), the root locus related to  $K_{cf}$  can be plotted in Figure 11. When the capacitor current feedback is not used, namely  $K_{cf} = 0$ , the closed-loop poles are outside the unit circle, which demonstrates that the system is unstable. As  $K_{cf}$  increases, the system becomes stable. However, if  $K_{cf}$  is too large, the system becomes unstable again.

Figure 12 shows the Bode plot with different  $K_{cf}$  which is obtained from Equation (24). In the magnitude-frequency characteristic,  $K_{cf}$  hardly influences the low-frequency characteristic. As  $K_{cf}$  increases, the open-loop gain decreases slightly around the crossover frequency  $\omega_c$ . Besides, the resonance peak is damped. In the phase-frequency characteristic, the phase margin decreases with the increase of  $K_{cf}$ . When  $K_{cf}$  is large enough, the phase-frequency curve crosses  $-180^\circ$  after it drops to  $-180^\circ$ . This makes the system unstable according to the stability criterion.

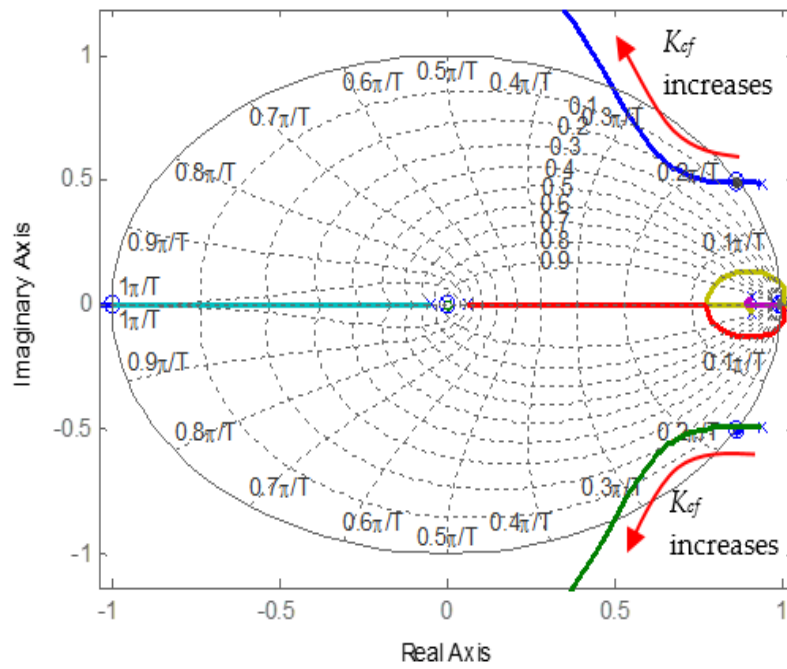


Figure 11. Root locus of variation in active damping gain  $K_{cf}$  using a dual-loop controller.

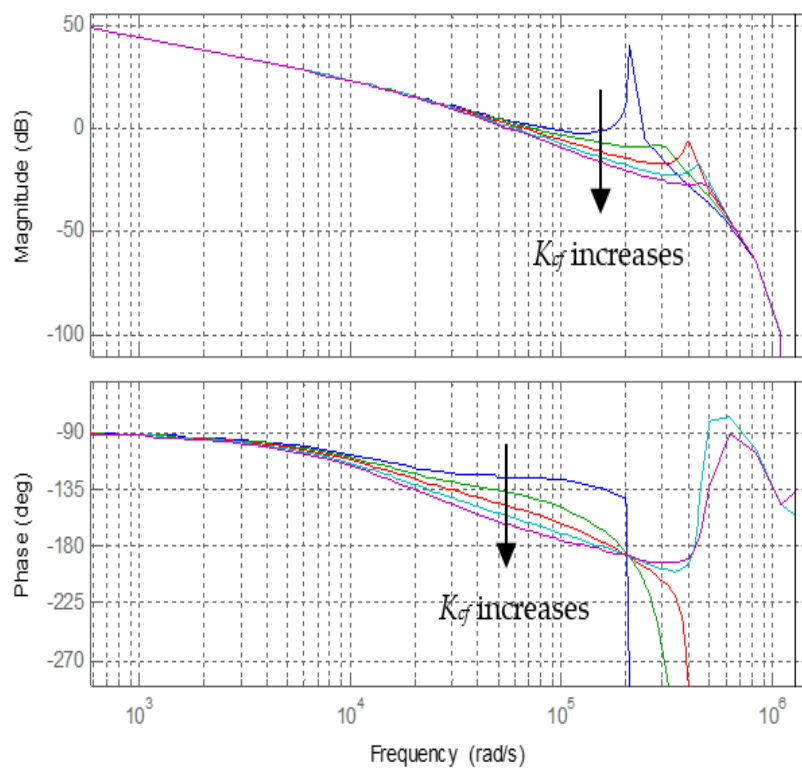


Figure 12. Open-loop Bode plot with different active damping gain  $K_{cf}$ .

In order to stabilize the system, the active damping gain  $K_{cf}$  must meet the requirements as follows. (The detailed proof is presented in Appendix B.)

$$K_{cfmin1} < K_{cf} < K_{cfmax1} \text{ and } K_{cfmin2} < K_{cf} < K_{cfmax2}, \tag{27}$$

where

$$K_{cfmin1} = \frac{-1 - \cos\varphi + K_{pwm}L_o\omega_{res}F\sin\varphi}{K_{pwm}\sqrt{\frac{C_f}{L_f}}\sin\varphi}$$

$$K_{cfmax1} = \frac{1 + \cos\varphi - K_pK_{pwm}F(R_o\cos\varphi - R_o - 2L_o\omega_{res}\sin\varphi)}{2K_{pwm}\sqrt{\frac{C_f}{L_f}}\sin\varphi}$$

$$K_{cfmin2} = -\frac{\frac{1 - 2\cos\varphi}{2} - K_pK_{pwm}F(R_o - R_o\cos\varphi + L_o\omega_{res}\sin\varphi) + \sqrt{\frac{(1 - 2\cos\varphi)^2}{4} + K_pK_{pwm}(2R_oF\cos\varphi - 2R_oF)}}{K_{pwm}\sqrt{\frac{C_f}{L_f}}\sin\varphi}$$

$$K_{cfmax2} = -\frac{\frac{1 - 2\cos\varphi}{2} - K_pK_{pwm}F(R_o - R_o\cos\varphi + L_o\omega_{res}\sin\varphi) - \sqrt{\frac{(1 - 2\cos\varphi)^2}{4} + K_pK_{pwm}(2R_oF\cos\varphi - 2R_oF)}}{K_{pwm}\sqrt{\frac{C_f}{L_f}}\sin\varphi}$$

### 5. Design Example

The circuit parameters are listed in Table 2. The specifications are given as the crossover frequency  $f_c \approx 10$  kHz and the phase margin  $\varphi_m > 45^\circ$ .

(1) Determination of the initial resonant current  $I_r$ :

According to Equation (1), the minimum initial resonant current is given as  $I_{r\_min} > 2.16$  A. The minimum initial resonant current and the initial resonant current for AZVS are selected as  $I_{r\_min} = 2.5$  A and  $I_{r\_A} = 5$  A, respectively. Therefore, when  $i_{L_f\_l} < -2.5$  A,  $S_{r1}$  is not operated, achieving NZVS of  $S_1$  and  $S_4$  according to Table 1. Otherwise,  $S_{r1}$  would be turned on properly to realize AZVS of  $S_1$  and  $S_4$ . Regarding  $S_2$  and  $S_3$ , when  $i_{L_f\_u} < 2.5$  A,  $S_{r2}$  must be turned on to create AZVS conditions. When  $i_{L_f\_u} > 2.5$  A,  $S_2$  and  $S_3$  can achieve NZVS.

(2) Determination of the upper limit and lower limit of the DPWM ( $V_{upperlimit}$  and  $V_{lowerlimit}$ )

The frequency of the DPWM clock is 120 MHz. Thus, the carriers are specified as  $V_{cmax} = 300$  and  $V_{cmin} = 0$  to achieve 200 kHz switching frequency. To simplify the calculation, the filter inductor current ripple is neglected. Therefore, the maximum required auxiliary current can be obtained from Equation (5) as  $I_{Lrm\_max} = I_{r\_A} + I_{o\_max} = 13$  A. The maximum charging time  $t_{ch\_max}$  can be calculated from Equation (6) as  $t_{ch\_max} = 357.5$  ns. The upper limit can be calculated from Equation (12) as  $V_{upperlimit} \approx 266$  by using the improved loading scheme. Thus, the lower limit  $V_{lowerlimit}$  and maximum duty ratio  $D_{max}$  are 34 and 0.867, respectively. Regarding the conventional loading scheme, the upper limit, lower limit, and maximum duty ratio are 257, 43, and 0.857, respectively. Table 3 shows a comparison of the parameters between the conventional and improved loading scheme. The range of the duty ratio is improved by utilizing the improved loading scheme.

**Table 3.** Comparison of the parameters between the conventional and improved loading scheme.

Parameter	Conventional Loading Scheme	Improved Loading Scheme
Maximum Duty Ratio $D_{max}$	0.857	0.867
Minimum Duty Ratio $D_{min}$	0.143	0.133
Upper Limit $V_{upperlimit}$	257	266
Lower Limit $V_{lowerlimit}$	43	34

(3) Determination of the PI regulator parameters and active damping gain  $K_{cf}$ 

The active damping gain  $K_{cf}$  will influence the stability of the system and the phase margin will decrease due to the increase of  $K_{cf}$  according to the analysis in Section 4.3. However, the influence of the filter capacitor is neglected to simplify the design of the PI regulator in Section 4.2. Therefore, in order to meet the requirement  $\varphi_m > 45^\circ$ , the phase margin is specified as  $60^\circ$  due to the capacitor current feedback. Thus, the parameters of the PI regulator can be calculated from Equation (21). The results are that  $K_p = 3.6522$  and  $K_i = 70,999$ . To ensure the system's stability, the capacitor current feedback gain  $K_{cf}$  must meet the requirement of  $0.0158 < K_{cf} < 0.119$  according to Equation (27). The feedback gain is selected as  $K_{cf} = 0.05$ .

Based on the above parameters, the Bode plots of the single loop and double loop can be obtained from Figure 13. The crossover frequency of the single loop is  $\sim 62,900$  rad/s and the phase margin is  $60^\circ$ . This is in agreement with the design specifications. However, the LC filter leads to resonance, which makes the phase–frequency curve cross  $-180^\circ$  after it drops to  $-180^\circ$ . According to the stability criterion, the single-loop system is unstable.

Regarding the double-loop control, the crossover frequency is  $\sim 61,000$  rad/s and the phase margin is  $46.4^\circ$ . Due to the capacitor current feedback, the crossover frequency and the phase margin decrease slightly. However, this outcome meets the requirement  $f_c \approx 10$  kHz and  $\varphi_m > 45^\circ$ . When  $20\log|G(j\omega)| \geq 0$ , the phase–frequency curve does not cross  $-180^\circ$ . According to the stability criterion, the double-loop system is stable.

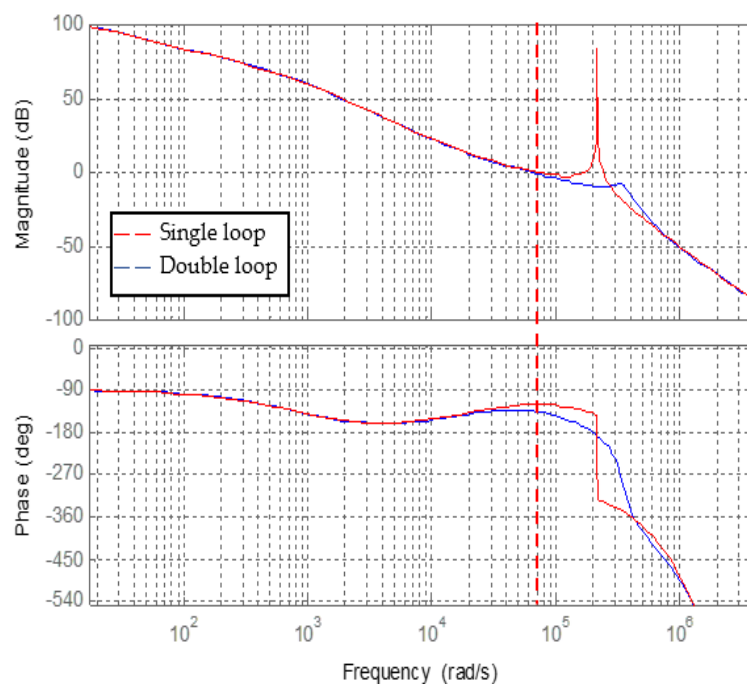


Figure 13. Bode plot of the single loop and double loop.

## 6. Simulations and Experiments

The method was implemented in the Altera Cyclone IV FPGA with the parameters given in Table 2. Figure 14 shows a photograph of the prototype. It consists of a FPGA (EP4CE22E22C7N, Altera Corporation, San Jose, CA, USA) control board, a switching power supply, a MOSFET driver, and a power circuit. The method is verified in the simulation using Saber.

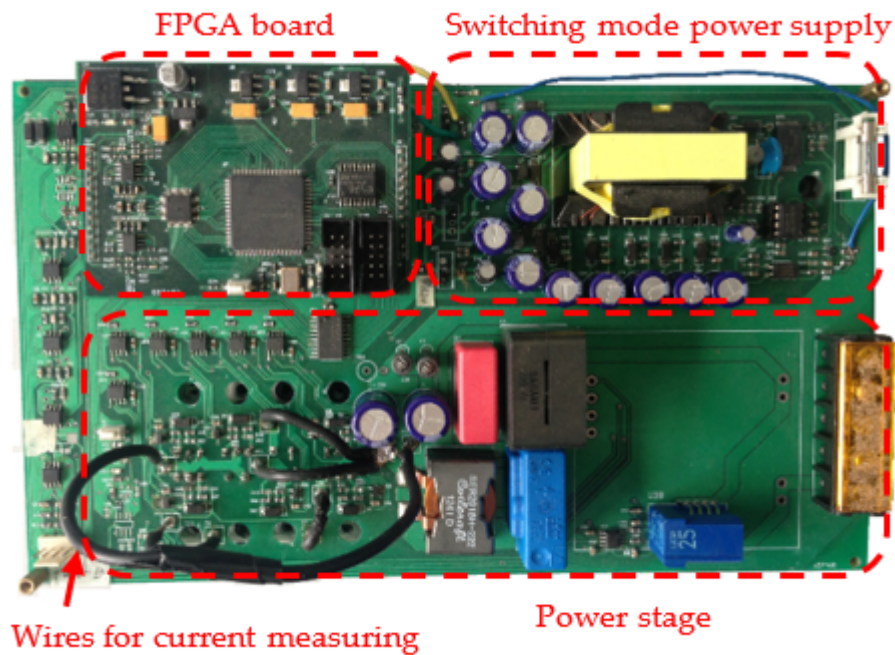


Figure 14. Photograph of the prototype.

Figures 15 and 16 show the simulation and experimental transitional waveforms of the main switches, respectively. During the turn-on commutation, the drain currents  $i_{d3}$  and  $i_{d4}$  begin increasing after the drain-source voltage  $v_{ds3}$  and  $v_{ds4}$  drop to zero. ZVS of  $S_4$  is achieved with the operation of  $S_{r1}$ , whereas the auxiliary switches are not turned on to achieve ZVS of  $S_3$ . Regarding the turn-off commutation, the drain current overlaps the drain-source voltage slightly because the resonant capacitance is not large enough. Due to the parasitic components, ringing occurs during the commutation in the experiment.

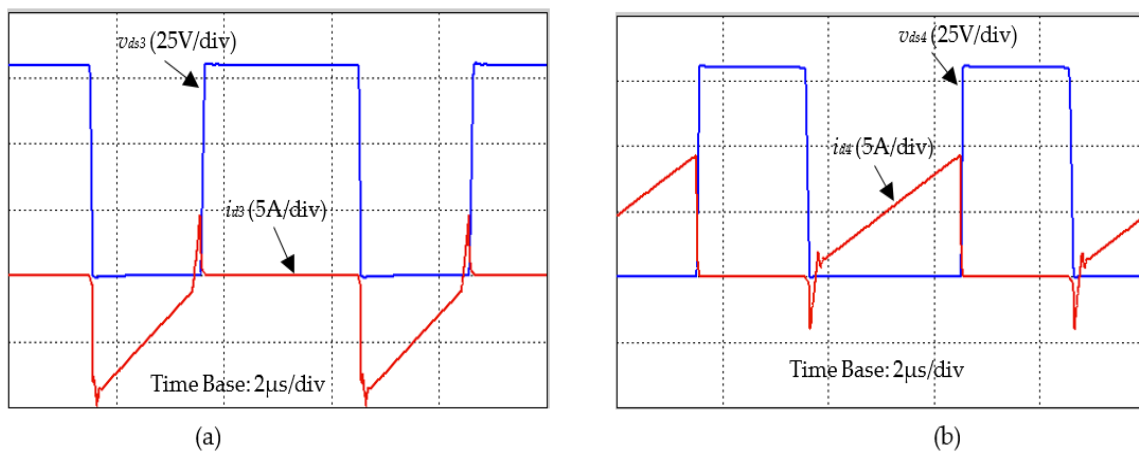
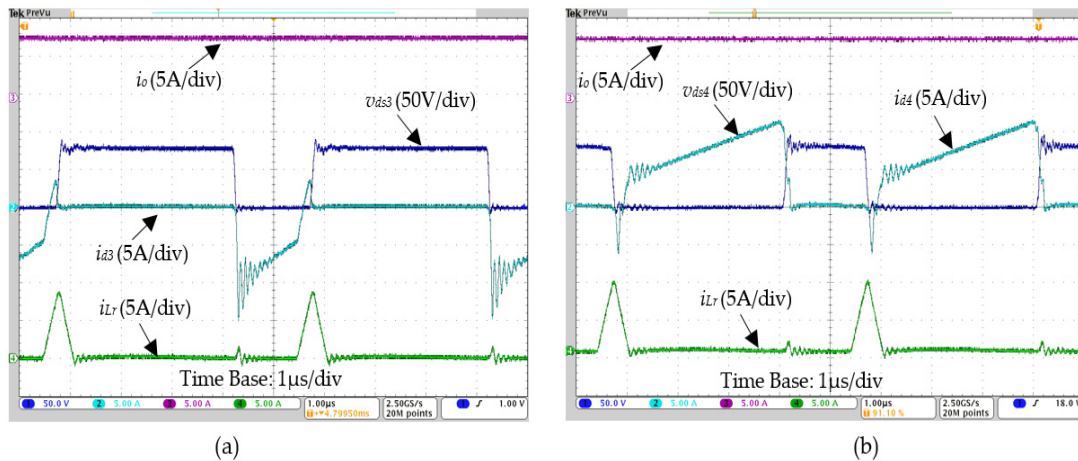
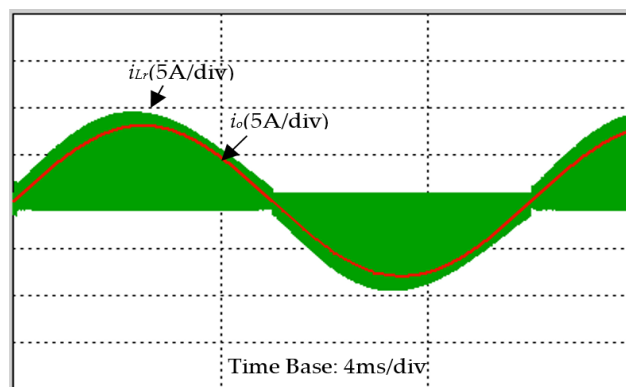


Figure 15. Simulation results of the current and voltage of the main switches when  $i_o = 8$  A. (a)  $S_3$ ; (b)  $S_4$ .

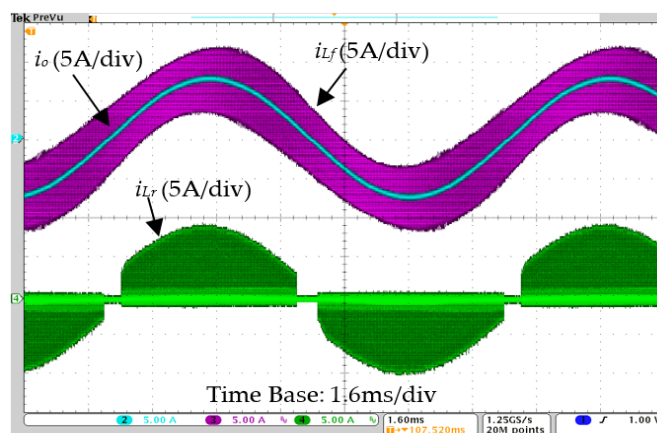


**Figure 16.** Experimental results of the current and voltage of the main switches when  $i_o = 8$  A. (a)  $S_3$ ; (b)  $S_4$ .

Figures 17 and 18 show the simulation and experimental waveforms of the auxiliary current with an 8 A, 100 Hz sinusoidal output current. The peak auxiliary switch current follows the load current with clear load adaptability. It can be seen that the lower the load current, the lower the auxiliary current.



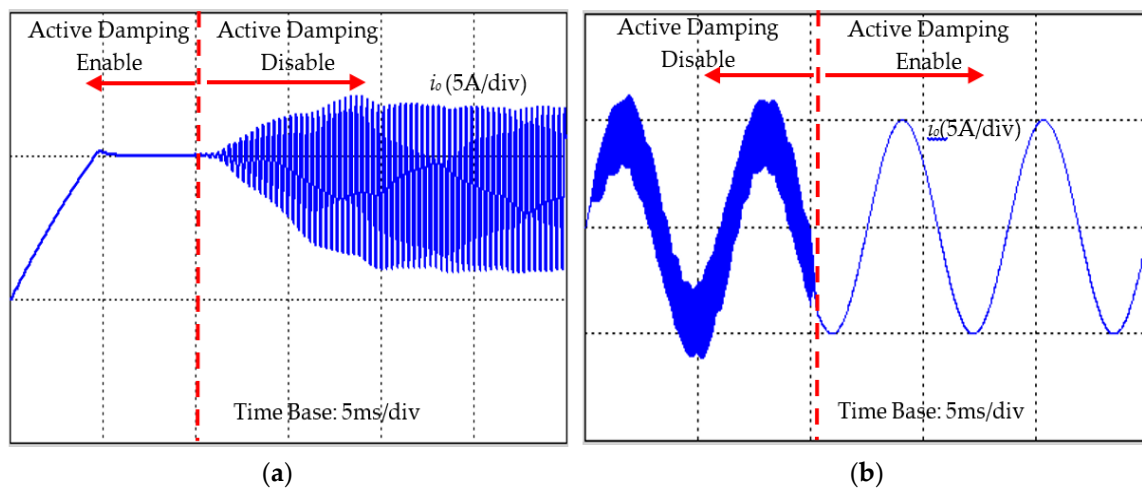
**Figure 17.** Simulation waveforms of the auxiliary current with an 8 A, 100 Hz sinusoidal output current.



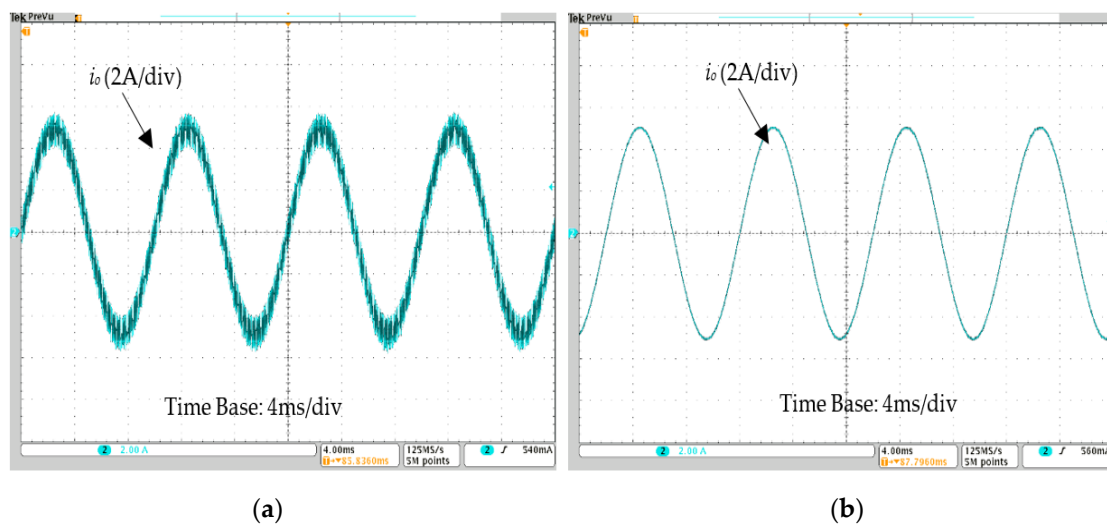
**Figure 18.** Experimental waveforms of the auxiliary current with an 8 A, 100 Hz sinusoidal output current.



Figures 19 and 20 show the simulation and experimental results of the output current with and without active damping method, respectively. Figure 19 demonstrates that strong resonance occurs in the output current without the active damping method, because closed-loop poles are outside the unit circle shown in Figure 11. After utilizing the capacitor current feedback, the poles can be moved into the unit circle. Therefore, the system can be stable both at the DC or sinusoidal output current conditions. Figure 20 also demonstrates that active damping is necessary to maintain stability and current quality.

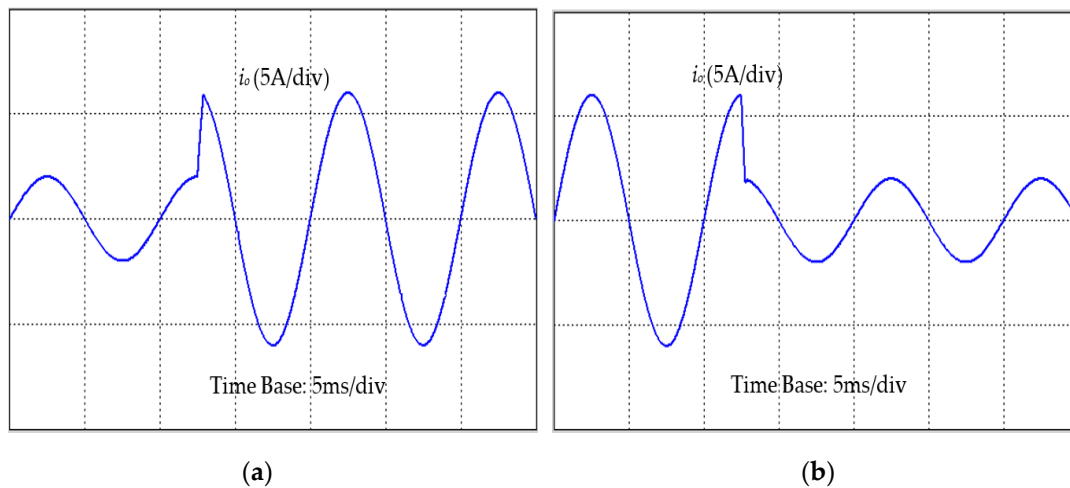


**Figure 19.** Simulation results of the output current with and without active damping method: (a) DC output current; (b) sinusoidal output current.

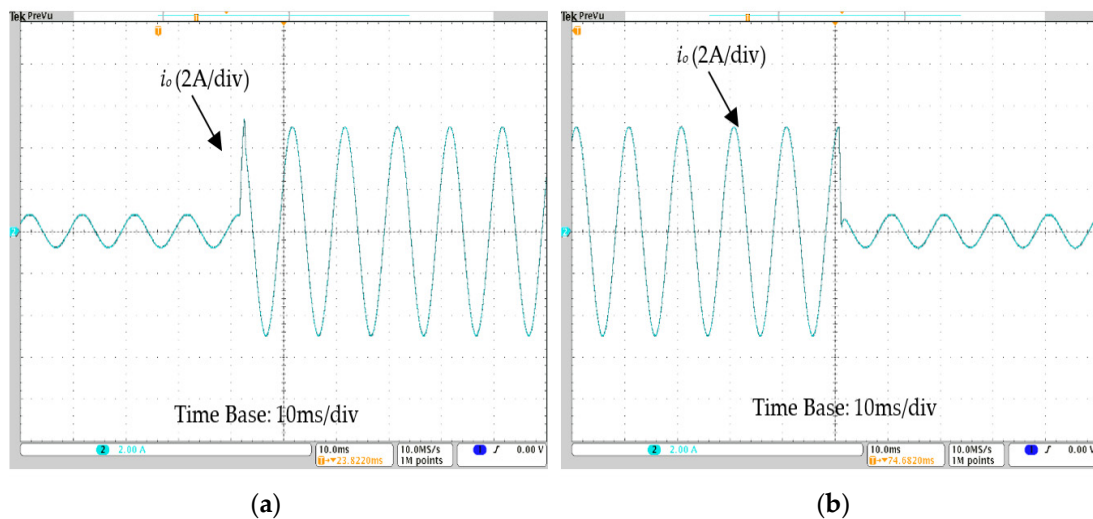


**Figure 20.** Experimental results of the output current (a) without and (b) with active damping method.

Figures 21 and 22 show the simulation and experimental results of the load dynamic response, respectively. The results demonstrate that the output current tracks the reference current quickly. However, a bit of overshoot exists in the transient response.



**Figure 21.** Simulation results of the load dynamic response: (a) a step change from 12.5% to 75% rated output power; (b) a step change from 75% to 12.5% rated output power.



**Figure 22.** Experimental results of the load dynamic response: (a) a step change from 12.5% to 62.5% rated output power; (b) a step change from 62.5% to 12.5% rated output power.

## 7. Conclusions

In some high-performance applications, an LC filter must be added to the auxiliary resonant snubber inverter (ARSI) to reduce the output current ripple. This makes the system quite different to the conventional ARSI without LC filter. This paper presents the modeling and the double-loop digital control of the ARSI with LC filter. The following points can be summarized to cover the paper:

- (1) An improved loading scheme that the data is updating at the upper limit and lower limit of the carrier is proposed to improve the maximum duty ratio.
- (2) The filter capacitor current feedback is introduced to damp the resonance caused by the LC filter.
- (3) A step-by-step digital controller design method, including the auxiliary current controller and the output PI controller, is proposed, in which the computation and transport delay is considered.

The control method has been verified by simulations and experiments. The maximum duty ratio is improved by 0.01 with the proposed loading method. In addition, soft-switching can be realized for the entire load range. Also, the resonance can be eliminated with the capacitor current feedback.

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**Author Contributions:** Hailin Zhang conceived the proposed method and wrote the paper; Baoquan Kou provided technical guidance and advice for the manuscript; Lu Zhang and Yinxi Jin performed the experiments and reviewed the manuscript.

**Conflicts of Interest:** The authors declare no conflict of interest.

### Appendix A

From Figure 10, the capacitor current feedback  $K_{cf}i_{cf}(z)$  and the output current  $i_o(z)$  to the voltage  $v_e(z)$  can be written as follows:

$$\frac{K_{cf}i_{cf}(z)}{v_e(z)} = K_{pwm}K_{cf}G_{dc}(z)G_T(z) \tag{A1}$$

$$\frac{i_o(z)}{v_e(z)} = K_{pwm}K_{cf}G_{dc}(z)G_P(z) \tag{A2}$$

$$v_e(z) = [i_o^*(z) - i_o(z)]G_c(z) - K_{cf}i_{cf}(z). \tag{A3}$$

From Equations (A1)–(A3), the closed-loop and open-loop transfer function, respectively, can be obtained as follows:

$$T(z) = \frac{i_o(z)}{i_o^*(z)} = \frac{G_{dc}(z)G_c(z)G_P(z)}{1 + K_{cf}G_{dc}(z)G_T(z) + G_{dc}(z)G_c(z)G_P(z)} \tag{A4}$$

$$G(z) = \frac{i_o(z)}{i_o^*(z) - i_o(z)} = \frac{G_{dc}(z)G_c(z)G_P(z)}{1 + K_{cf}G_{dc}(z)G_T(z)}. \tag{A5}$$

Applying z-transformation to  $G_T(s)$ ,  $G_T(z)$  can be obtained as follows:

$$G_T(z) = Z [K_{pwm}H(s)G_1(s)] = K_{pwm} \sqrt{\frac{C_f}{L_f}} \frac{(z - 1)\sin\varphi}{z^2 - 2z\cos\varphi + 1}, \tag{A6}$$

where

$$\varphi = \omega_{res}T_{sp} \text{ and } \omega_{res} = \frac{1}{\sqrt{L_f C_f}}.$$

Commonly, because  $T_{sp} \ll L_o/R_o$ ,  $e^{-\frac{R_o}{L_o}T_{sp}} \approx 1$ . Therefore, applying z-transformation to  $G_P(s)$ ,  $G_P(z)$  can be obtained as follows:

$$G_P(z) = Z [K_{pwm}H(s)G_1(s)G_2(s)] \approx K_{pwm} \frac{-z(R_o F \cos\varphi + L_o \omega_{res} F \sin\varphi - R_o F) + R_o F - R_o F \cos\varphi + L_o \omega_{res} F \sin\varphi}{z^2 - 2z\cos\varphi + 1}, \tag{A7}$$

where

$$F = \frac{L_f C_f}{L_o^2 + L_f C_f R_o^2}.$$

### Appendix B

Equation (25) can be simplified as follows:

$$z^3 - z \cdot 2\cos\varphi + az + b = 0, \tag{B1}$$

where

$$a = 1 + K_{cf}K_{pwm} \sqrt{\frac{C_f}{L_f}} \sin\varphi - K_p K_{pwm} F (R_o \cos\varphi + L_o \omega_{res} \sin\varphi - R_o)$$

$$b = -K_{cf}K_{pwm} \sqrt{\frac{C_f}{L_f}} \sin\varphi + K_p K_{pwm} F (R_o - R_o \cos\varphi + L_o \omega_{res} \sin\varphi).$$

In order to easily identify the quantity of the unstable poles,  $w$ -transform  $z = (1 + w)/(1 - w)$  is introduced. Therefore, Equation (B1) can be transformed as follows:

$$a_3 w^3 + a_2 w^2 + a_1 w + a_0 = 0, \tag{B2}$$

where

$$\begin{cases} a_3 = 1 + 2\cos\varphi + a - b \\ a_2 = 3 + 2\cos\varphi - a + 3b \\ a_1 = 3 - 2\cos\varphi - a - 3b \\ a_0 = 1 - 2\cos\varphi + a + b \end{cases}.$$

It can be obtained that  $a_0 > 0$ . Thus according to Routh’s Method, the following requirement must be satisfied to maintain the system’s stability:

$$\begin{cases} a_3 > 0 \\ a_2 > 0 \\ \frac{a_2 a_1 - a_3 a_0}{a_2} > 0 \\ a_0 > 0 \end{cases} . \tag{B3}$$

From Equation (B3), the filter capacitor current feedback gain  $K_{cf}$  must meet the following requirement:

$$K_{cfmin1} < K_{cf} < K_{cfmax1} \text{ and } K_{cfmin2} < K_{cf} < K_{cfmax2}, \tag{B4}$$

where

$$K_{cfmin1} = \frac{-1 - \cos\varphi + K_{pwm} L_o \omega_{res} F \sin\varphi}{K_{pwm} \sqrt{\frac{C_f}{L_f}} \sin\varphi}$$

$$K_{cfmax1} = \frac{1 + \cos\varphi - K_p K_{pwm} F (R_o \cos\varphi - R_o - 2L_o \omega_{res} \sin\varphi)}{2K_{pwm} \sqrt{\frac{C_f}{L_f}} \sin\varphi}$$

$$K_{cfmin2} = - \frac{\frac{1 - 2\cos\varphi}{2} - K_p K_{pwm} F (R_o - R_o \cos\varphi + L_o \omega_{res} \sin\varphi) + \sqrt{\frac{(1 - 2\cos\varphi)^2}{4} + K_p K_{pwm} (2R_o F \cos\varphi - 2R_o F)}}{K_{pwm} \sqrt{\frac{C_f}{L_f}} \sin\varphi}$$

$$K_{cfmax2} = - \frac{\frac{1 - 2\cos\varphi}{2} - K_p K_{pwm} F (R_o - R_o \cos\varphi + L_o \omega_{res} \sin\varphi) - \sqrt{\frac{(1 - 2\cos\varphi)^2}{4} + K_p K_{pwm} (2R_o F \cos\varphi - 2R_o F)}}{K_{pwm} \sqrt{\frac{C_f}{L_f}} \sin\varphi}$$

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