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Sharp Switching Characteristics of Single Electron Transistor with Discretized Charge Input

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Abstract: For the low-power consumption analog and digital circuit applications based on a single-electron transistor, enhancement of its switching performance is required. Our previous works analytically and numerically demonstrated that a discretized charge input device, which comprised a tunnel junction and two capacitors, improved the gain characteristics of single-electron devices. We report the design and fabrication of an aluminum-based single-electron transistor having the discretized charge input function. Flat-plate and interdigital geometries were employed for adjusting capacitances of grounded and the coupling capacitors. The sample exhibited clear switching on input-output characteristics at the finite temperature.

Keywords: input discretizer; Coulomb blockade

1. Introduction

Single-electron transistors (SETs) have unique characteristics based on a Coulomb blockade (CB) effect. In the past few decades, various applications were proposed such as an elemental charge sensor [1], low-power consumption analog and digital circuits [2–6], dc current standards by combination of superconductive island or electrodes [7,8] and a composite device utilizing ferromagnetic materials [9–11]. Since the shape of CB region of SETs is a rhombus with respect to axes of bias and gate voltages, threshold voltage is unwillingly changed by the bias voltage. This property is unfavourable from the viewpoint of the current switch application or applications for digital circuits. We proposed a single electron device, which we called input discretizer (ID), generates a discretized charge output from a continuous input voltage signal, and demonstrated that the ID improves the performance of capacitively-connected single electron devices [12]. In terms of providing discontinuous thresholds to the CB, the ID enhances their gain characteristics [13,14]. Nevertheless, those studies were based on analytically or numerically calculated results. Here we report an experimental result of the SET with the ID comprising aluminium by shadow evaporation technique. The device exhibited steep responses to the input signal compared to an SET without the ID.

2. Sample Design and Fabrication

Figure 1a,c show scanning electron microscope (SEM) images of the samples that we designed. The corresponding circuit diagrams are shown in Figure 1b,d. In Figure 1d, areas surrounded by a dotted and a dashed lines denote the ID and the SET, respectively. Input node of the SET is capacitively coupled to the ID with a coupling capacitance C_C. For the purpose of dividing electrical charge at the island n_1, two capacitors of C_C and a grounded capacitance C_B are connected to the island n_1. Red circles indicate tunnel junctions and the inset in Figure 1c shows a close-up picture of the tunnel junction J_1. The junction area of J_1 is approximately 180 nm $\times$ 40 nm.

When the island n_2 is connected to the ground, the electrical charge Q_C at C_C and the threshold voltages of the ID are expressed as follows [12]:

$$Q_C = \frac{C_C(C_{J_1}V_g + n_1 e)}{C_{J_1} + C_B + C_C}, \tag{1}$$

$$\left(n_1 - \frac{1}{2}\right)\frac{e}{C_B + C_C} \leq V_g \leq \left(n_1 + \frac{1}{2}\right)\frac{e}{C_B + C_C} \tag{2}$$

where C_{J_1} is the junction capacitance of J_1 and e is the elementary charge. When C_C is equal to C_B, the ID generates the discretized charge with a constant period of half of e/C_C to the input voltage V_g. In addition, from Equation (1), to obtain the clear discontinuity of Q_C, C_C is required as large as or larger than C_{J_1}. We used an interdigitized capacitor type [15,16] as C_C and the self-capacitor type [17] as C_B. A rectangular-like Al plate that roles the part of C_B is shown in Figure 1c. We deliberately enlarged n_2 in order to implement C_B as much as C_C. The size of the flat-plate structure was about 6.3 µm wide and 5.0 µm long. In order to adjust the ratio of capacitance values C_B/C_C, we designed geometories of the device utilizing the three dimensional capacitance extraction program (FFTCap) [18]. A back-gate voltage of V_{bg} and a capacitance C_{BG} were used for adjusting the offset charge on the island n_2. Another sample excluding J_1, which would work as a simple SET, was created simultaneously on the same substrate to be compared with the discontinuity of the electrical responses (see Figure 1a).

Samples were fabricated by using the electron beam lithography and the Al shadow evaporation technique [19] on a thermally oxidized silicon substrate. In this method, the oxidized Al layer that formed between the first and the second Al layer acts as tunnel barrier. The surface of the 1st-deposited Al layer was oxidized by adding 13 Pa of pure O_2 gas for 60 s into an evaporation chamber. At room temperature, the values of respective series resistance of the SETs with the ID and without the ID were 104 kΩ and 106 kΩ.

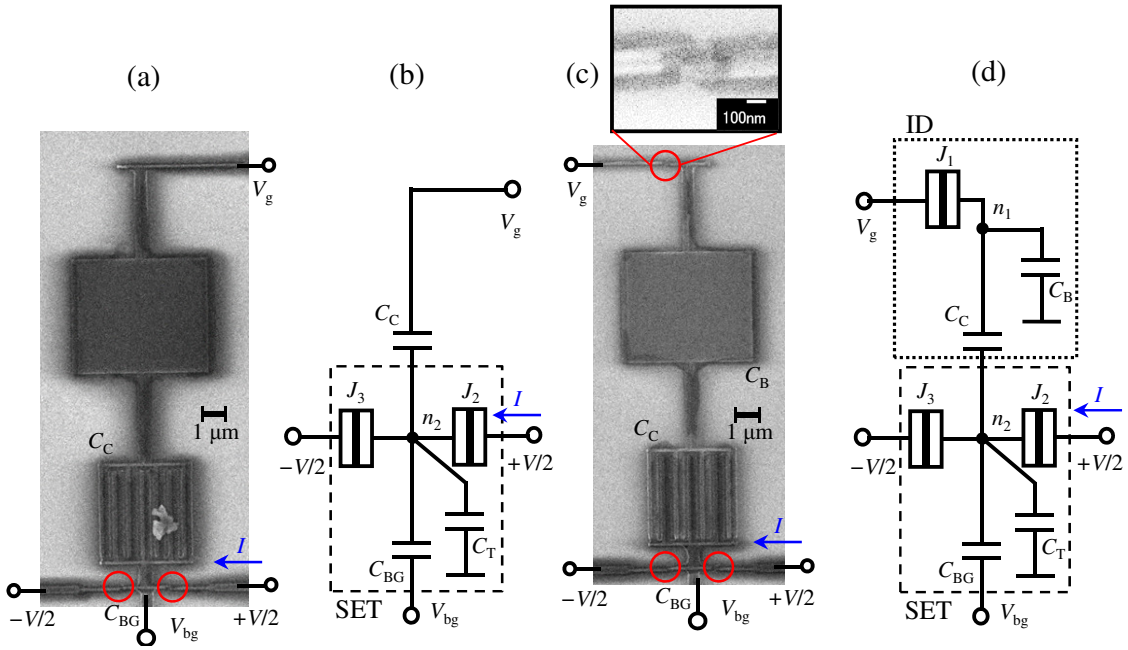

Figure 1. (**a**) Scanning electron microscope (SEM) image of a single electron transistor (SET) without an input discretizer (ID). Red circles indicate tunnel junctions; (**b**) The equivalent circuit of the SET without the ID; (**c**) The SEM image of the SET with the ID. The inset shows a close-up the tunnel junction of J_1; (**d**) The equivalent circuit of the SET with the ID.

3. Experimental Setup

Measurements were performed using a compact ^{3}He-^{4}He dilution refrigerator [20] with a base temperature of <80 mK in an electromagnetically shielded room. In order to avoid transmission of electrical noise to the sample, all measurement cables were equipped with an L-type filter at room temperature and with distributed low-pass filters placed between the 1 K stage and the mixing chamber. Superconductivity in the Al electrodes was suppressed by applying 10 kOe magnetic field from a superconductive magnet perpendicular to the substrate of the sample. While temperature was monitored with a 1010 Cernox^{TM} thermometer by Lake Shore Cryotronics (Westerville, OH, USA) which was placed in the mixing chamber during the measurement, it was difficult to tell the exact temperature under magnetic fields because it affected the accuracy of such resistance variable type sensors. A symmetrically voltage-biasing method was used for measuring electrical characteristics. The current I flowing from the junctions of J_2 to the J_3 and bias voltage V were measured by current and voltage pre-amplifiers (model SR570 from Stanford Research Systems, Sunnyvale, CA, USA; modified to apply external bias voltage to the sample, model INA116P from Texas Instruments, Dallas, TI, USA).

In order to extract the device parameters of the sample, we performed numerical calculation [21] and reproduce the measured electrical characteristics. For simplicity, we ignored parasitic capacitances and the cotunneling processes [22] in the simulation.

4. Results and Discussion

Initially we set V_{bg} to ground, and measured I versus V characteristics as a function of V_g for the SET with the ID. Colour plot of I versus V and V_g in steps of 0.2 mV were depicted in Figure 2. Contour lines of I except 0 A were drawn from −0.4 to 0.4 by 0.1 nA step. In this measurement, although thresholds are unclear to determine the the shape of the CB owing to insufficient numbers of step of V_g to the period of the Coulomb oscillation, several steep modulations of I to V_g shown by yellow arrows can be seen.

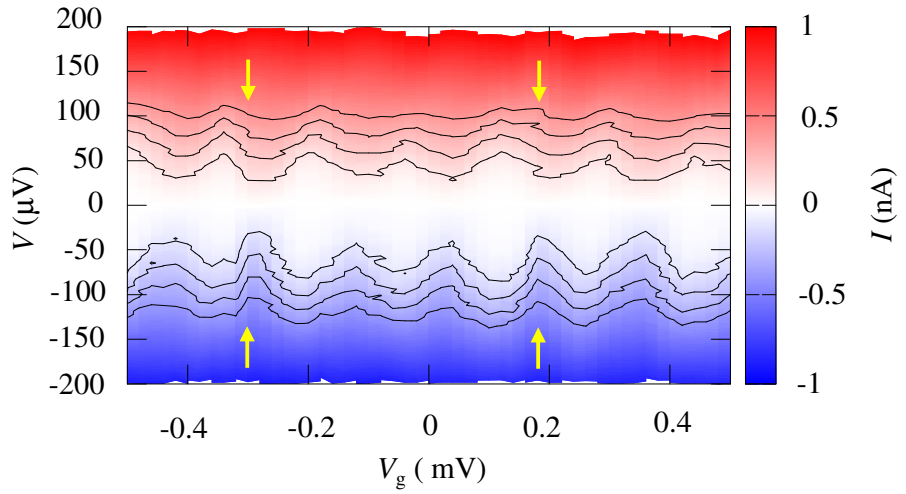

Figure 2. Current I characteristics of the SET with the ID as a function of V and V_g for V_{bg} = 0 V at T < 80 mK. Borders of contour lines are plotted of 0.1, 0.2, 0.3, 0.4, −0.1, −0.2, −0.3 and −0.4 nA. Abrupt modulation of I against V_g are indicated by yellow arrows.

Subsequently, on applying fixed V, we tuned V_{bg} of the SET with the ID in order to obtain the maximal modulation of I at V_g near to 0 V. Figure 3 shows I versus V_g as the input-output characteristics for the SETs without and with the ID at T < 80 mK. Crossed marks and open squares indicate the SET without the ID at V = 78 μV, the SET with the ID at V = 74 μV; and two solid lines indicate the best fits of both SETs without and with the ID using the numerical simulation

at T = 65 mK, respectively. In the simulation, the offset charge of the island was zero and V_{bg} was 780 mV for the SET without the ID, n_2 was 0.015 e and V_{bg} was 140 µV for the SET with the ID. The SET without the ID responded to a typical Coulomb oscillation. In contrast, sharp switching I clearly came against the V_g almost periodically in the SET with the ID. This result exhibited that the ID provides the quantized charge input, which was partially corresponded with the switching periodicity of the SET. Carrying out the simulation and examining the input-output characteristics, we listed the extracted capacitive and resistive parameters in Table 1. Both the values of C_C of SETs without and with the ID were identical of 872 aF. The value of C_B of the SET with the ID was estimated 1100 aF, that is 26 percent larger than the value of C_C yielding a shifted charge period from $e/2$.

Table 1. Typical parameter values for the SETs (single-electron transistors) with and without the ID (input discretizer).

Device	C_C (aF)	C_B (aF)	C_{J_1} (aF)	$C_{J_2} = C_{J_3}$ (aF)	C_T (aF)	C_{BG} (aF)	$R_{J_2} = R_{J_3}$ (kΩ)
SET without ID	872	-	120	160	900	96	60
SET with ID	872	1100	120	160	900	96	60

In this measurement, current spikes like random telegraph noise in the SET with the ID can be seen (for instance, at V_g = −0.68 mV, −0.62 mV, −0.16 mV). These current noise were prominent even compared to its the SET without the ID. We presume that the island n_1 enlarged with the metallic plate corresponding C_B is more sensitive to the dielectric charge traps in the substrate, or the natural oxdized layer of Al on the surface of the sample [23].

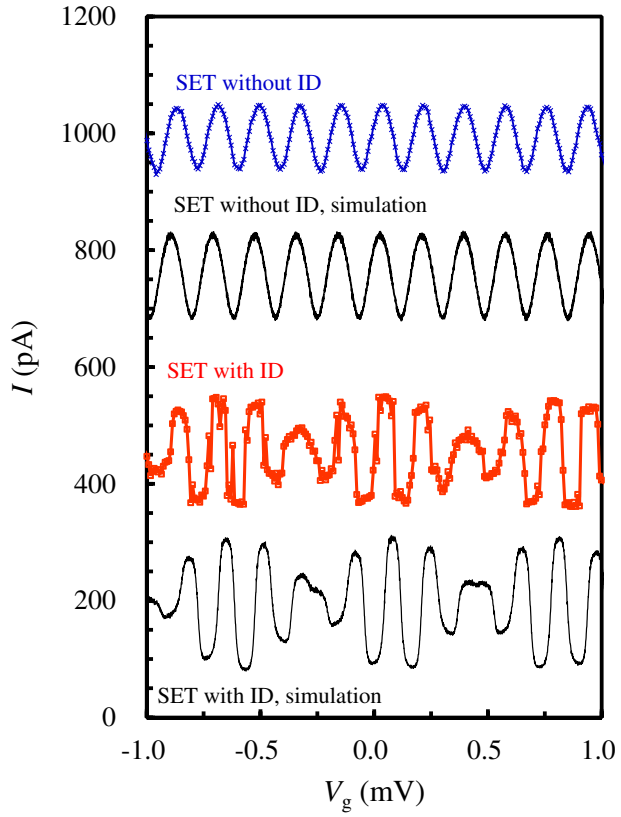

Figure 3. I-V_g for input-output characteristics. Crossed marks, open squares and two solid lines correspond the SET without the ID at V = 78 µV, the SET with the ID at V = 74 µV and the best fits using a numerical simulation, respectively. Curves are vertically shifted by 250 pA for clarity.

Several experimental studies reported that semiconductor-based SETs with tunable tunnel barriers to close to the quantum resistance enhanced the switching performance [24,25]. Applying our approach is also preferable to boost the switching characteristics of the semiconductor-based SETs.

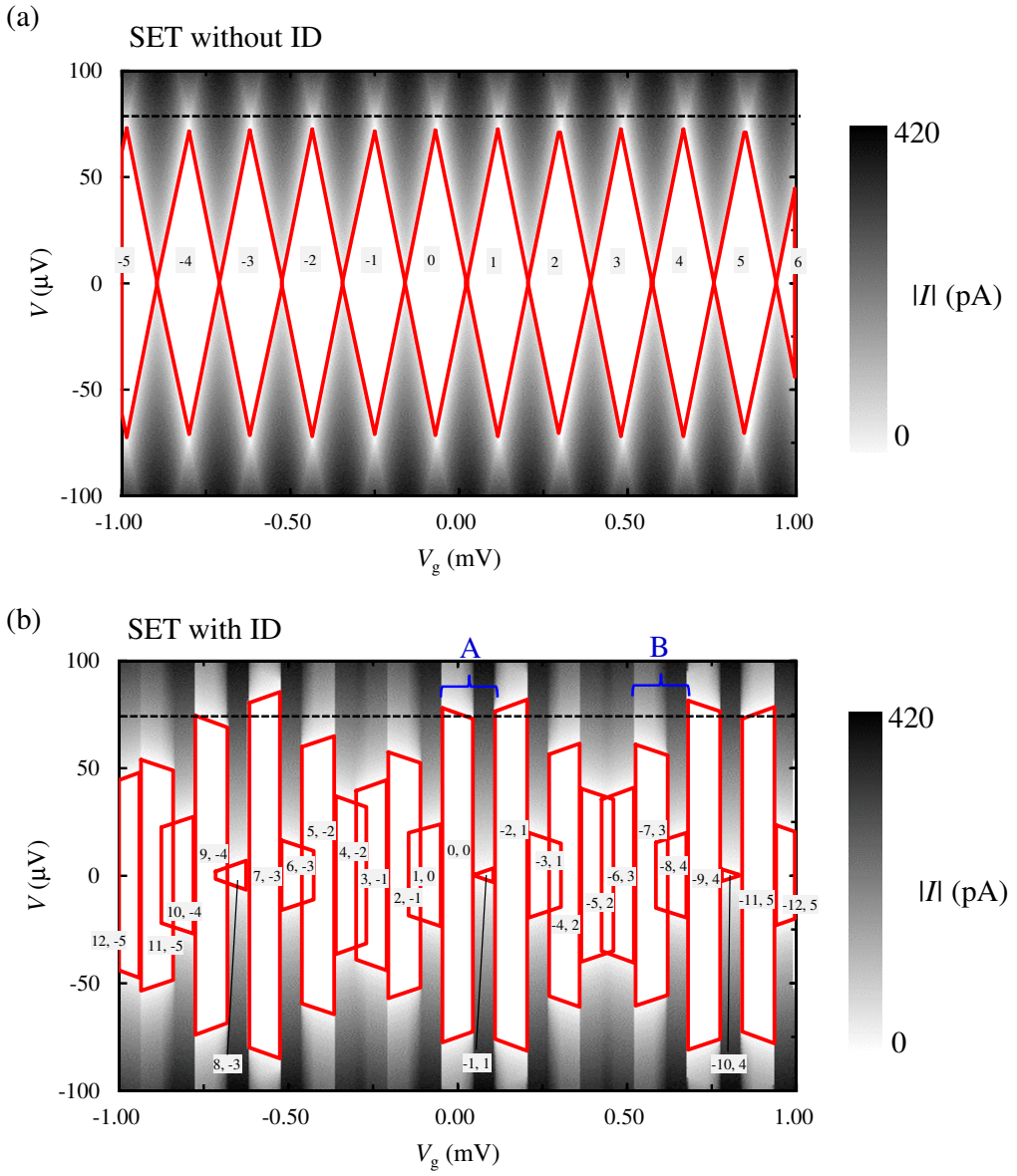

Figure 4. *I-V* characteristics as a function of V_g from numerical simulations at T = 0 K. Solid red lines denote thresholds of the Coulomb blockade region. (**a**) the SET without the ID; (**b**) the SET with the ID. The numbers indicate the charge state in n_2 for the SET without the ID; n_1 and n_2 for the SET with the ID. An area "A" indicates the steep current switching region, and an area "B" indicates bi-stability region. Horizontal dotted lines denote bias points of V = 78 μV and V = 74 μV corresponding to Figure 3.

Figure 4a,b shows CB diagrams extracted from stability diagrams of numerical calculations of the SETs without and with the ID, using the condition of Table 1 and symmetrically voltage biased condition at T = 0 K. The numbers in Figure 4a,b indicate the excessive charge state in n_2 for the SET without the ID; in n_1 and n_2 for the SET with the ID. We set the charge numbers to zero across V_g = 0 V. Horizontal dotted lines, which correspond to Figure 3, indicate bias voltages of V = 78 μV for the SET without the ID and V = 74 μV for the SET with the ID. Whereas conventional Coulomb

diamonds of an SET appear in the device of SET without the ID in Figure 4a, abrupt V changes of the CB thresholds are clearly seen in the SET with the ID in Figure 4b. Slopes of CB of the SET without the ID in the asymmetrical biased condition, which is maximum voltage gain in metal-based SET referred in Reference [12], was estimated $C_C/C_{J_2} \approx 5.5$ in our design. In Figure 4b, vertical and inclined threshold lines to V_g stem from the ID and the SET, respecitively [12]. Since the $C_C \neq C_B$ condition bears the shapes not only minimal and maximal regions but also intermediate regions of Coulomb diamonds of an SET, large and small steps of ΔV (typical region marked "A" in Figure 4b) appear against the V_g alternately, which correspond to the input-output characteristics of the SET with the ID in Figure 3. Partially overlapped regions (typical region marked "B" in Figure 4b) can be seen. When two electrons sequentially tunnel through J_1 and either J_2 or J_3, bi-stability regions appear inside the threshold of CB ($(n_1, n_2) \rightarrow (n_1 - 1, n_2 + 1)$ or $(n_1 + 1, n_2 - 1)$). According to the simulation result, I flows through the SET during an unstable condition of $(n_1 - 1, n_2)$ or $(n_1 + 1, n_2)$.

Moreover, we evaluated the differential conductance of the SETs with and without the ID via the absolute value of $\mathrm{d}I/\mathrm{d}V_g$. In Figure 5, simulated results of differential conductance of each samples were plotted as a function of temperature. From the measurement, $|\mathrm{d}I/\mathrm{d}V_g|$ of SET without the ID were also plotted as a blue crossed mark. In the SET with the ID, we picked six points on both sides of the slopes extracted from the top to third peaks of maximal I in Figure 3 and plotted a median value as a red open square. Note that both measurement results plotted at T = 65 mK were estimated from the fitting curve of the simulation. For comparison, values of $|\mathrm{d}I/\mathrm{d}V_g|$ are normalized by respective $R_{j_2} + R_{j_3}$. Under the low temperature, series junction resistances $R_{j_2} + R_{j_3}$ of the SETs with the ID and without the ID were 122 kΩ and 124 kΩ, respectively. The values of $|\mathrm{d}I/\mathrm{d}V_g|$ decrease accompanying a temperature rise, exhibiting a similar trend to the gain characteristics of a single-electron inverter with the ID [14].

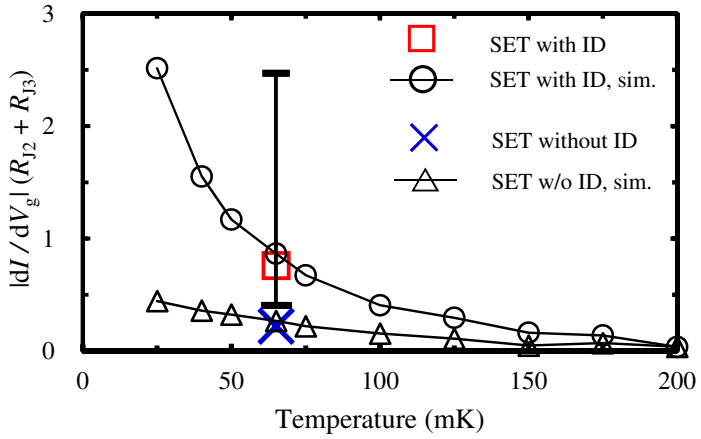

Figure 5. Absolute values of differential conductances plotted as a function of the temperature. In the SET with the ID, six $\mathrm{d}I/\mathrm{d}V_g$ values vicinity at top three high I were extracted from Figure 3. The median value is plotted as a red open square. Values are normalized by series resistance of $R_{j_2} + R_{j_3}$.

The temperature calculated by the thermal energy of the island n_1 in the SET with the ID is expressed with the charging energy E_{C1} [1]:

$$E_{C1}/k_B = e^2/2C_{\Sigma 1}k_B \sim 0.53\,\mathrm{K}, \tag{3}$$

where $C_{\Sigma 1}$ is the total capacitance from the perspective of n_1 and k_B is the Boltzmann constant. Thus, the estimation from Equation 3 that the device works by providing a higher gain value than its nominal SET under a finite temperature of $\ll$0.53 K agrees with the simulated results.

5. Conclusions

In conclusion, we implemented the SET having the discretized charge input function. The input-output characteristics of the fabricated sample had steep response to the input signal compared with the SET without the ID at the finite temperature of $T < 80$ mK. The experimental result demonstrated that the ID provided the quantized charge input resulting in the enhancement of the performance for the current switch application of the SET. However, the mismatch between the two values C_B and C_C, with a factor of 1.26 in the measured device, resulted in an alternating behaviour of discontinuous and continuous I-V_g characteristics at a modulated period. Numerical calculation indicated that the mismatch ratio of C_B/C_C was 1.26. Hence, the simulation result suggested that the further design of the ID having the optimized capacitance condition of $C_B = C_C$ would improve the steep switching characteristics throughout all the CB diamonds of the SET.

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Author Contributions: M.T. performed experiments, analyzed the results and prepared the manuscript. H.S. set up the complete experiment and revised the manuscript. Y.M. provided conceptual support and revised the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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