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A Self-Testing Platform with a Foreground Digital Calibration Technique for SAR ADCs

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Academic Editor: Teen-Hang Meen
Received: 29 May 2016; Accepted: 26 July 2016; Published: 29 July 2016

Abstract: This study presents a self-testing platform with a foreground digital calibration technique for successive approximation register (SAR) analog-to-digital converters (ADCs). A high-accuracy digital-to-analog converter (DAC) with digital control is used for the proposed self-testing platform to generate the sinusoidal test signal. This signal is then implemented using an Arduino board, and the clock signal is generated to test the ADCs. In addition, fast Fourier transform and recursive discrete Fourier transform (RDFT) processors are adopted for dynamic performance evaluation and calibration of the ADCs. The third harmonic distortion caused by the non-linearity of the track-and-hold circuit, the mismatch of the DAC capacitor array, and the direct current (DC) offset of the comparator can be calculated using the processors to improve the ADC performance. The advantages of the proposed platform include its low cost, high integration, and no need for an extra analogy compensation circuit to deal with calibration. In this work a 12 bit SAR ADC and an RDFT processor are used in the Taiwan Semiconductor Manufacturing Co., Ltd. (TSMC) 0.18 μm standard complementary metal–oxide–semiconductor (CMOS) process with a sampling rate of 18.75 kS/s to validate the proposed method. The measurement results show that the signal-to-noise and distortion ratio is 55.07 dB before calibration and 61.35 dB after calibration.

Keywords: analog-to-digital converters (ADCs); digital calibration method; self-testing; successive approximation register ADC (SAR)

1. Introduction

An analog-to-digital converter (ADC) is an important component in various areas, such as communication and biomedical systems, among others. The performance limitations of the ADCs are mainly dominated by the static and dynamic non-linearity effects, which cause the harmonic distortion in the output power spectrum. These non-linearities slightly deteriorate the overall system performance, and also increase the sensitivity to the process variation and system interface noise because of the technology scaling into the nano-scale region. A calibration method is thus essential to ensure system quality [1,2]. The successive approximation register (SAR) analog-to-digital converter (ADC) has the advantages of medium speed conversion and medium to high resolution. It is therefore very suitable for biomedical and communication systems. With regard to the implementation of most SAR ADCs, the performance should be maintained by the internal circuits, including the track-and-hold (T/H) circuit, the DAC capacitor array, and the comparator circuit. However, the non-linearity of

the internal circuits always limits the performance of the ADCs. This is the reason why a calibration method is required to overcome this problem. In this paper we focus on the digital calibration method. For example, the lookup table or the state-space technique is a common calibration method for ADC error correction [3]. The correction in this approach is based on a table that uses pre-calculated values or the slope of the input signal. However, the drawback of this method is the requirement of a large memory size, thus consuming more areas. An equalization-based digitally calibrated method is proposed in Reference [4]. The advantage of this is the reduction of both the ADC testing time and the convergence time. In addition, this paper utilizes the least mean squares (LMS) algorithm to correct and calibrate the ADC error, similar to that in Reference [5].

An internal redundancy dithering (IRD) technique is reported in Reference [6]. The IRD method based on bit-weight calibration employs a pseudorandom bit sequence to determine the threshold values. The method utilizes the LMS algorithm to calibrate the SAR ADC error. However, the main drawback of the approaches in References [5,6] is that a high resolution ADC is required, which is impractical in actual implementation. A fast-Fourier transform (FFT)-based calibration method for pipelined ADC is reported to calibrate the capacitor mismatch and non-linearity error of the operational amplifier (OPAMP) [7]. However, the shortcoming of the FFT process is the consumption of more power because all frequency bins should be computed during the operation mode. Juan et al. proposed an RDFT-based calibration algorithm to overcome this problem [8], because the RDFT processor has the advantages of variable transform length, lower complexity, and less hardware cost.

In this paper, we present a self-testing platform based on previous works [7,8] to measure the ADC performance using the proposed testing stimulus and compensate for the error using a simplified digital calibration algorithm. A 12 bit SAR ADC and an RDFT processor are implemented in the TSMC 0.18 μm to verify the proposed platform. The output is analyzed using MATLAB (version 7.6.0.324 (R2008a), The MathWorks, Natick, MA, USA, 2008), including the performance calculation and ADC calibration.

2. Proposed Self-Test Platform

2.1. Conventional SAR ADC Architecture

The basic block of the traditional SAR ADC includes a track-and-hold circuit (T/H), an N-bit DAC capacitor array, a comparator circuit, and a SAR controller (Figure 1). The SAR ADC generally uses a binary-weighted method to implement the circuit [9]. According to the results for the switching capacitor array, the digital output signal can be obtained as Logical High (“1”) or Logical Low (“0”). In addition, some biomedical applications require an adaptive resolution using a multi-switch operated in 8 bit or 12 bit mode [9]. However, the non-linearity of the multi-switch in the T/H circuit will limit the SAR ADC performance. The proposed calibration method also has the capability of eliminating the non-linearity and enhancing the performance of the multi-mode SAR ADC. Figure 2 depicts the multi-mode SAR ADC structure. In this, switch S2 is applied to control the two operation modes, namely the 8 bit and 12 bit modes. The bootstrapped switch is also adopted to provide a small on-resistance with a constant value and better linearity.

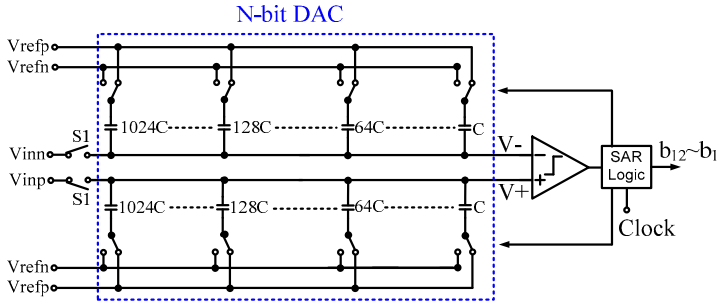

Figure 1. Traditional successive approximation register (SAR) Analog-to-Digital converter (ADC) structure.

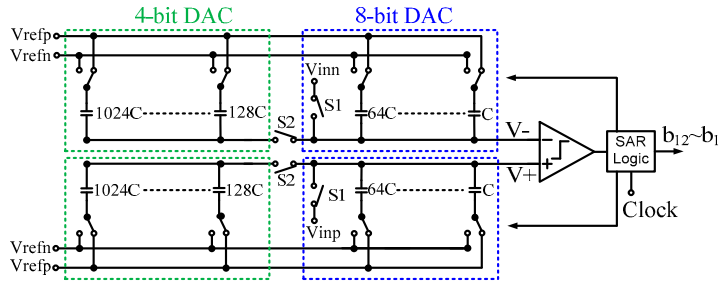

Figure 2. Multi-mode SAR ADC structure.

2.2. Proposed Calibration Method

A previous work [8] derived the proposed calibration formula using the FFT and a cosine wave input signal. The third harmonic distortion value a_3 can be detected by an RDFT processor. The error factor Δ_n can be further calculated for the calibration. In addition, the calibration code was only used for the first-time test to reduce the complexity. This calibration method can not only compensate for the error caused by the capacitor mismatch and DC offset in the traditional ADC but it can also be applied to calibrate the T/H circuit in the multi-mode SAR ADC (Figure 2).

The main calibration equation can be written as follows:

$$a_3 = 20\log\left(\frac{A \times \Delta_n \times 1.696 \times C_n}{2048} + 1.696 \times V_{os}\right), \quad (1)$$

where A is the amplitude of the cosine wave, C_n is the value of each capacitor ratio, Δ_n is the error factor of each capacitor mismatch, and V_{os} is the DC offset. The DC offset voltage of the comparator circuit can be expressed as:

$$V_{os} = \sqrt{\left(\frac{V_{ov}}{2}\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{V_{ov}}{2}\frac{\Delta\left(W/L\right)}{\left(W/L\right)}\right)^2 + \left(\Delta V_t\right)^2}, \quad (2)$$

where V_{ov}, W/L, and V_t are the overdrive voltage, transistor size, and threshold voltage of the differential pair, respectively. According to Equation (2), the threshold voltage is a static offset, which does not affect the dynamic performance of the ADC. Meanwhile, both the overdrive voltage and transistor size will degrade the ADC performance. Some approaches have been used to overcome this problem and improve the DC offset, such as reducing the overdrive voltage or increasing the comparator size. However, the drawbacks of these methods are the decrease in the comparison speed and higher power consumption, respectively. Therefore, the problem can be overcome using the RDFT processor in a system-on-a-chip to calibrate the ADC error [8]. Generally, if a DC offset value will be very small, it will not affect the performance of the ADC. However, if a DC offset is a bigger value,

the performance of the ADC will be decreased. Figure 3 shows the MATLAB simulation results with different DC offset variations.

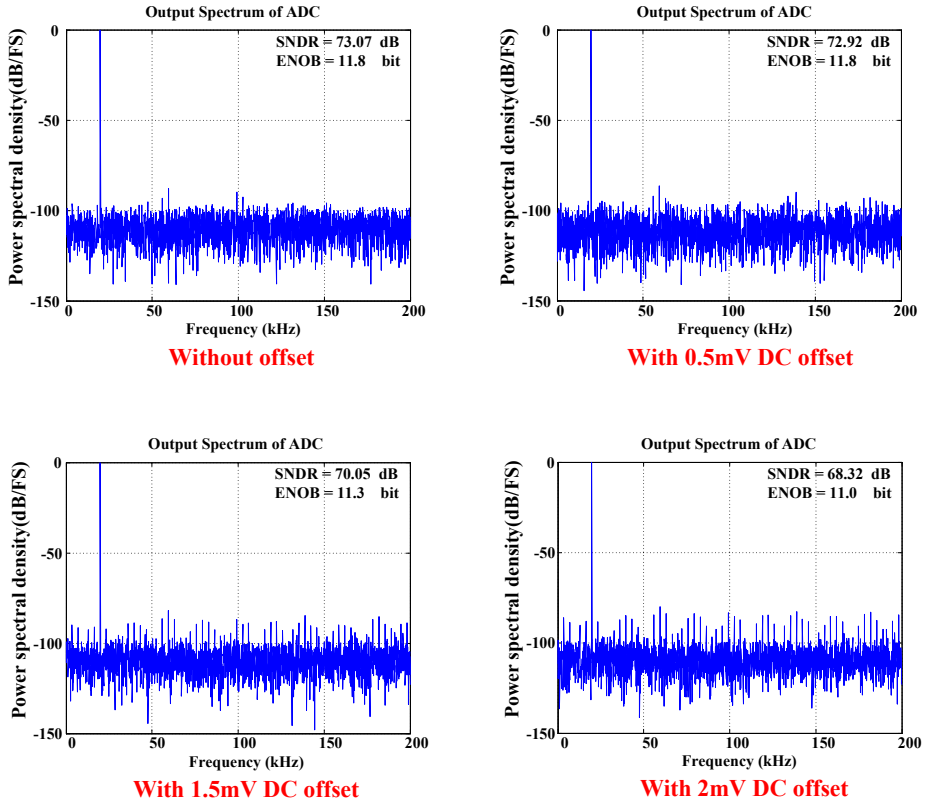

Figure 3. MATLAB simulation result with different direct current (DC) offset variation (The signal-to-noise and distortion ratio, SNDR; The effective number of bits, ENOB).

The calibration equation can be rewritten as (3). Here, we assume that A = 1 V, and the DC offset (V_{os}) is 2 mV:

$$\Delta_n = \frac{(10^{a_3} - 0.0033) \times 2048}{1 \times 1.696 \times C_n}, n = 11 \sim 0, \quad (3)$$

In addition, the input signal of the RDFT processor can be a sine or cosine wave signal. Therefore, the power spectra of the RDFT have real (Re) and imaginary (Im) part energies, respectively, in which a_3 is equal to:

$$20\log\sqrt{(\mathrm{Re})^2 + (\mathrm{Im})^2}, \quad (4)$$

The value of a_3 can be substituted as the real and imaginary parts. Therefore, Equation (3) can be further simplified as follows:

$$\Delta_n = \frac{\left(10^{\frac{1}{2}\log\sqrt{(\mathrm{Re})^2+(\mathrm{Im})^2}} - 0.0033\right) \times 2048}{1 \times 1.696 \times C_n}, n = 11 \sim 0, \quad (5)$$

where C_n is the value of each capacitor array. Equation (5) can be used to evaluate the error factor (Δ_n). The final correction code utilized to compensate for the error is further obtained as follows:

$$D_{new} = Bit_{12} \times 2^{11} \times (2 \pm \Delta_{12}) + Bit_{11} \times 2^{10} \times (2 \pm \Delta_{11}) + \cdots + Bit_1 \times 2^0, \quad (6)$$

The third harmonic distortion can be significantly reduced when the compensation is finished. The ADC performance can then be improved. In addition, the residue errors are not only compensated, but also corrected by fine-tuning.

2.3. MATLAB Verification

MATLAB is used to simulate and verify the proposed self-testing platform technique and calibration method and build the behavior model, which includes the 12 bit SAR ADC, RDFT computation, signal generator, and proposed calibration. In addition, a 1% capacitor mismatch, 2 mV DC offset, thermal noise, sampling jitter and switch nonlinearity are adopted in the 12 bit SAR ADC model to demonstrate the proposed calibration. Generally, the backgate effect of the switch transistor is the main source of its resistance nonlinearity. So, the input-dependent switch transistor can be defined as:

$$R = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)[V_{DD} - V_{th}]}, \tag{7}$$

In this work, the parameters of the sampling switch are determined by the virtual process, so the backgate effect value of this switch transistor is:

$$R_p = \frac{1}{86 \times 10^{-6}\,(0.18)\,[1.8 - (-0.5)]} \approx 0.911k, \tag{8}$$

$$R_n = \frac{1}{387 \times 0^{-6}\,(0.18)\,[1.8 - 0.5]} \approx 0.358k, \tag{9}$$

It is worthily noted that the body effect problem is not considered in this issue. In this work, the switch model given by using the MATLAB Simulink tool is the transmission gate (pmos and nmos) architectures, and then we further determine the switch nonlinearity error according to the virtual CMOS process parameter. After putting these parameters into Equation (7), we can process the performance analysis of the SAR ADC under the conditions of a 1% capacitor mismatch, 2 mV DC offset, thermal noise, sampling jitter and switch nonlinearity error.

Figure 4a shows the simulation result. It can be easily observed that the distortion deteriorates the ADC performance in the simulation result with a 5 Hz input frequency at a sampling rate of 126.26 Hz. Furthermore, the third harmonic distortion tone is −55.29 dB without calibration and −80.97 dB with calibration (Figure 4b). The signal-to-noise and distortion (SNDR) can be improved from 48.32 dB to 65.65 dB, while the effective number of bits (ENOB) is improved from 7.73 bits to 10.61 bits. However, the proposed calibration method cannot compensate for the error of the thermal noise, sampling jitter and sampling switch nonlinearity, which generated the harmonic distortion at the output power spectrum, so the ADC such as SNDR and spurious-free dynamic range (SFDR) cannot achieve the ideal ADC performance. Figure 5 shows the time domain result, and it is clear that the signal can be improved when the proposed calibration method is applied.

Figure 6 shows the simulation result with capacitor mismatch only and analyzes the performance of the ADC before/after calibration. According to the simulation result, the third harmonic distortion tone is −65.59 dB without calibration and −90.81 dB with calibration. The ENOB can be improved from 9.92 bits to 11.11 bits. In addition, Figure 7 shows the simulation result with 2 mV DC offset only and analyzes the performance of the ADC before/after calibration. According to the simulation, the proposed calibration method can reduce the DC offset error and enhance the performance of the ADC.

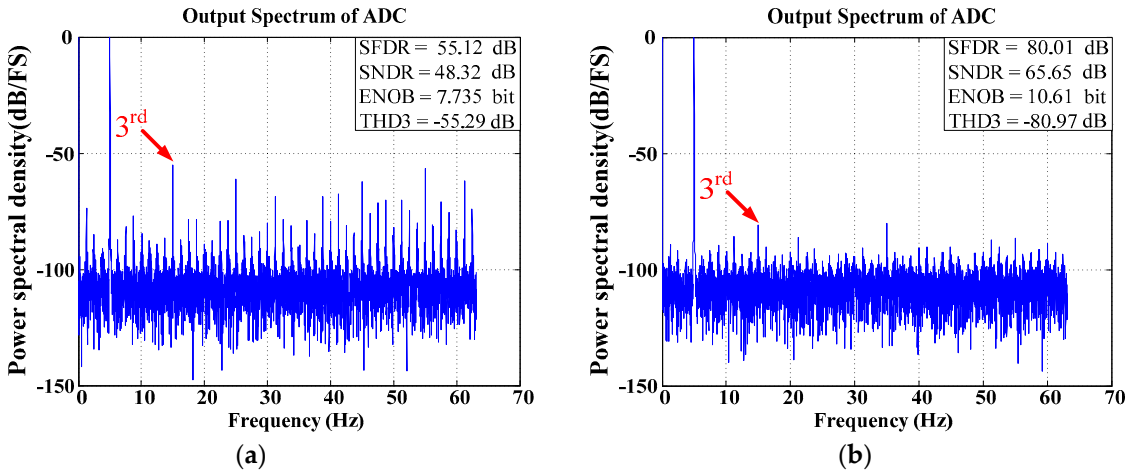

Figure 4. Simulation result from the MATLAB tool (**a**) without and (**b**) with calibration. (Total third harmonic distortion, THD3; Spurious-free dynamic range, SFDR).

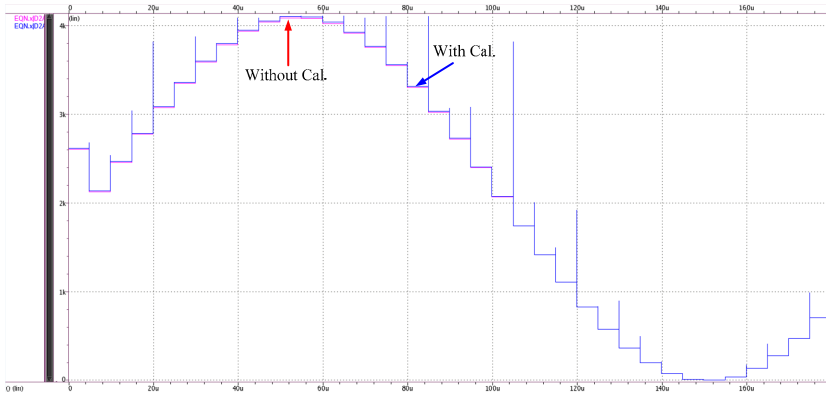

Figure 5. Time domain result with/without calibration.

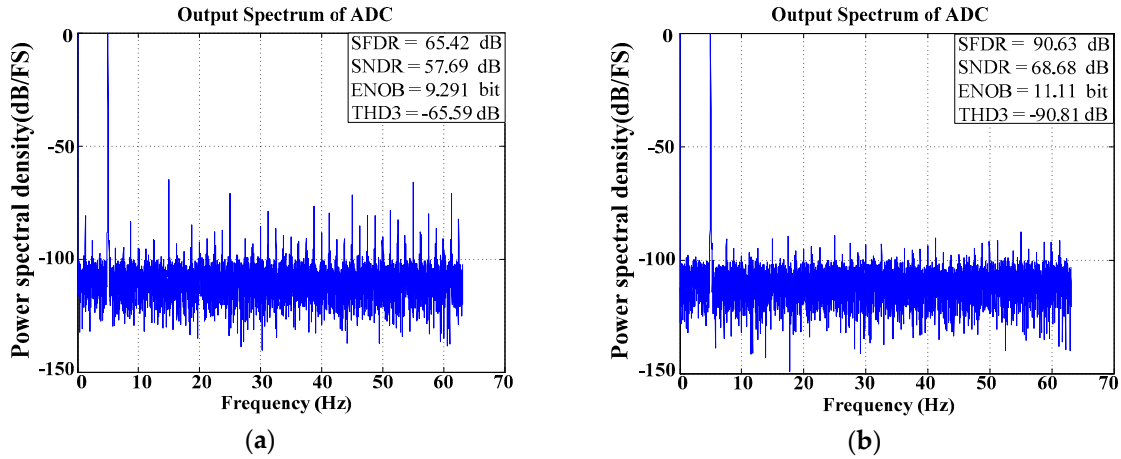

Figure 6. Simulation result from the MATLAB tool with capacitor mismatch only (**a**) before and (**b**) after calibration.

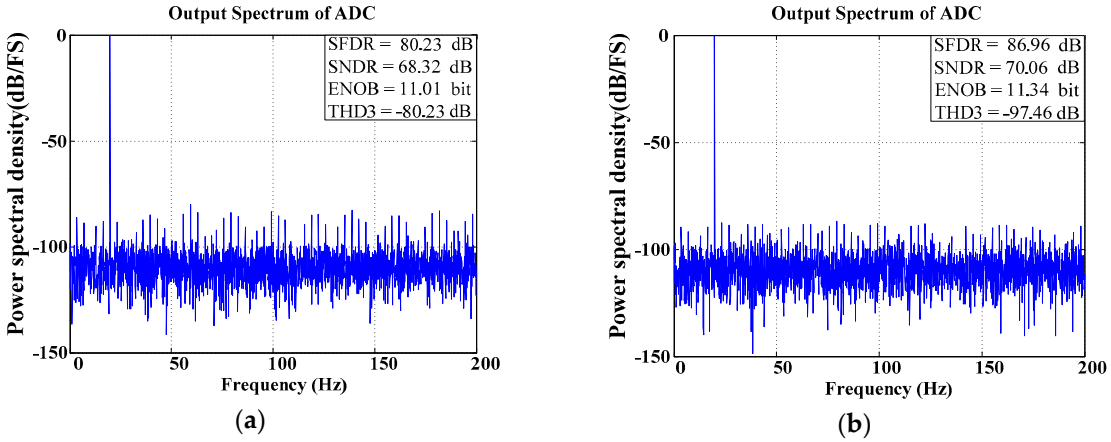

Figure 7. Simulation result from the MATLAB tool with 2 mV DC offset only (**a**) before and (**b**) after calibration.

2.4. Testing Stimulus Signal

Generally, the dynamic performance of the ADC, including the total harmonic distortion, signal-to-noise ratio, signal-to-noise and distortion ratio (SNDR), and effective number of bits (ENOB), is evaluated by stimulation using the input signal of a sinusoidal waveform and analysis using a digital signal processor [10]. Therefore, a high-accuracy DAC controlled by a digital code in the Arduino board is used to implement the sinusoidal testing signal. Figure 8 shows the basic block of the signal generator. A gain stage and a level shift are employed to adjust the signal amplitude and the required DC level. In addition, a low-pass filter is used to reduce the noise, eliminate the error, and enhance the signal performance. Figure 9 shows the experimental results, which reveal that this signal generator has a spurious dynamic range (SFDR) of 52 dB.

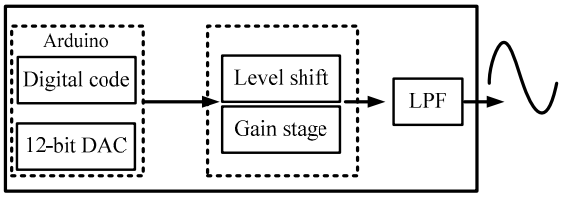

Figure 8. Block diagram of the sinusoidal signal generator.

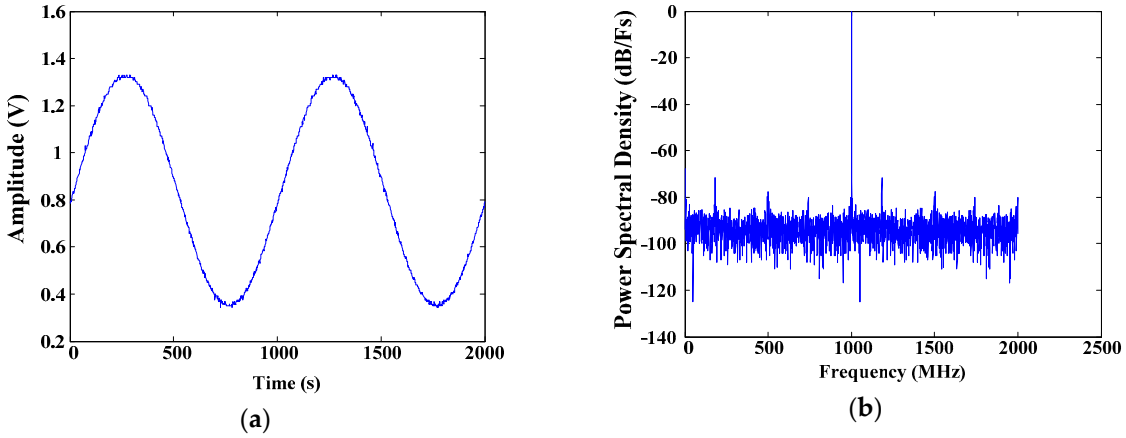

Figure 9. (**a**) Output signal waveform of the signal generator. (**b**) Output power spectrum of the signal generator.

The clock signal is required to control the ADC for most of the ADC testing platform. Figure 10 shows the experimental results of the clock signal, and the root mean square of the jitter is 0.808 ns.

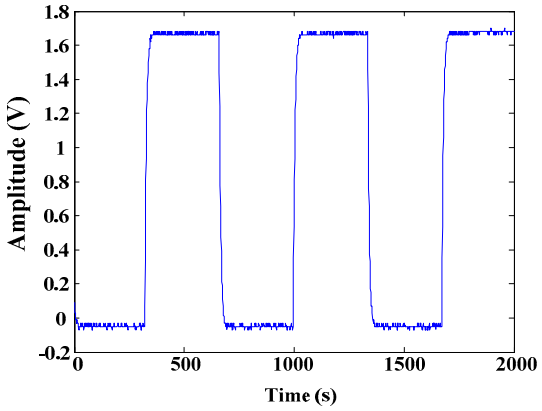

Figure 10. Output signal waveform of the clock generator.

2.5. RDFT Design

Figure 11 shows an RDFT processor structure used to efficiently compute the desired power spectrum density of the signals, including fundamental and third harmonic tones [11]. According to Reference [11], we found that the z-transform formula of the N-point RDFT computation can be defined as follows:

$$H(z) = \frac{W_N^k - z^{-1}}{1 - 2\cos\left(2\pi k/N\right) \times z^{-1} + z^{-2}}, \tag{10}$$

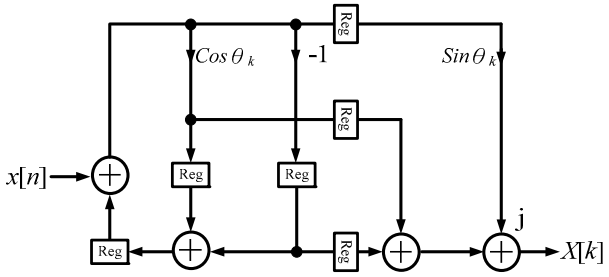

Figure 11. The recursive discrete Fourier transform (RDFT) structure.

The coefficients of $\cos(\theta_k)$ and $2\cos(\theta_k)$ can be shared to reduce the multiplication of $\cos(\theta_k)$ using the same computation; hence, Equation (4) can be written as follows:

$$H(z) = \frac{j\sin\left(\theta_k\right) + \left(\cos\left(\theta_k\right) - z^{-1}\right)}{1 - z^{-1}\left(2\cos\left(\theta_k\right) - z^{-1}\right)}, \tag{11}$$

In the targeted application, the RDFT processor calibration method would have a better performance than the FFT processor because only two frequency bins (i.e., the main and third harmonic tones) should be calculated. Therefore, the computational complexity can be lower than in the FFT processor. In this work, an RDFT processor is implemented in the TSMC 0.18 μm standard CMOS process to execute the calibration under the transform length of 4096 and the world length of 24 bits. Moreover, the computational complexity includes a total of (2N + 2) multiplications and (4N + 2) additions.

2.6. Processing Flow of the Proposed Self-Testing Platform

Figure 12 shows the processing flow of the self-testing platform method. According to the block diagram, it starts from a sine wave generator with a frequency condition setting, and then a 12 bit DAC output signal is fed into the target SAR ADC. Next, the RDFT processor is used to detect the third harmonic tone and the proposed calibration formula is employed to calculate the error factor. Finally, we can use this error factor to compensate for the ADC error using the re-coding method.

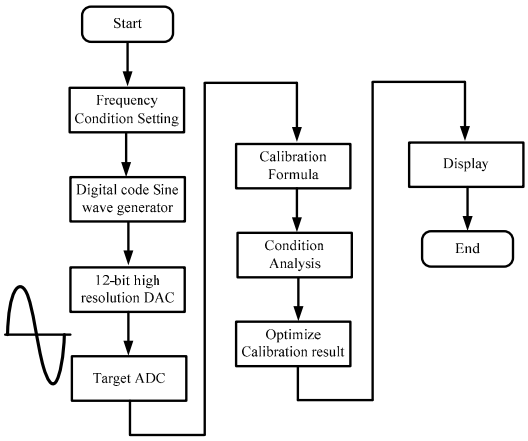

Figure 12. The processing flow of the proposed self-testing platform.

2.7. Proposed Platform Design

The proposed self-testing platform architecture is illustrated in Figure 13. This platform includes a power board, clock generator, sinusoidal waveform generator, and testing chip. In the power board design, the LM317 device is adopted to provide a stable and high-performance supply voltage for the testing platform. We can utilize the logic analyzer or the Arduino board to catch the output data. Finally, the MATLAB tool is adopted to analyze the output signal.

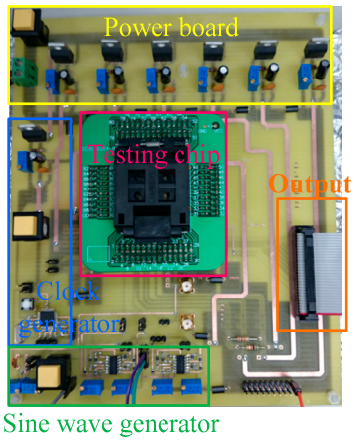

Figure 13. The self-testing platform architecture.

3. Measurement Results

3.1. Multi-Mode SAR ADC

A 12 bit multi-mode SAR ADC is implemented in the 0.18 μm standard CMOS process to demonstrate the proposed idea. The chip microphotograph is shown in Figure 14, in which the core circuits have an area of 1.219 mm × 0.938 mm. Figure 15a,b show the output power spectrum

before/after calibration under a 3 kHz and 1 $V_{p\text{-}p}$ input signal with a 125 kHz sampling rate. The third harmonic distortions without and with calibration are −65.53 dB and −78.95 dB, respectively. The SFDR here is 65.39 dB before calibration. The SFDR of 78.80 dB can be achieved after calibration. However, the improvement in SNDR and ENOB is not that significant because the SAR ADC performances are dominated by system noise and tones caused by supply noise and cross-talk, which should be overcome by careful layout.

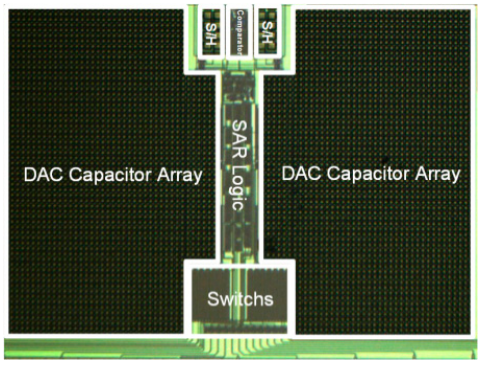

Figure 14. Chip micrograph of the multi-mode SAR ADC.

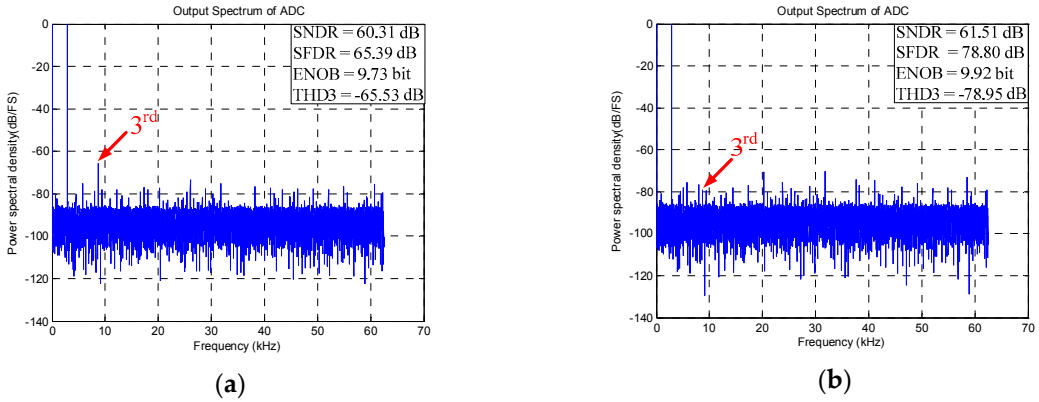

Figure 15. Measurements (**a**) without and (**b**) with calibration.

3.2. Proposed Self-Testing Platform

The 12 bit SAR ADC and RDFT processor is implemented in the 0.18 µm standard CMOS process to demonstrate the proposed method. The chip microphotograph is shown in Figure 16, in which the core area is 1.118 mm × 2.13 mm.

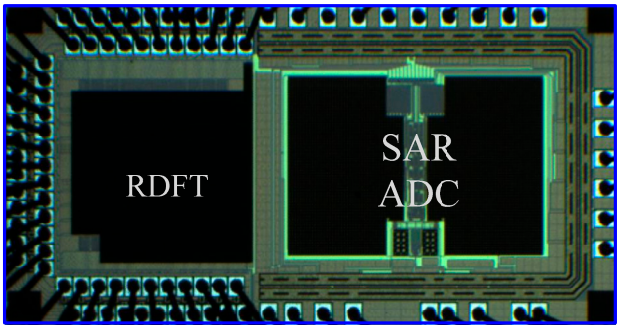

Figure 16. Chip micrograph of SAR ADC and RDFT.

Figure 17a,b show the output power spectrum with and without calibration under a 1 kHz and 1 V_{p-p} input signal with an 18.75 kHz sampling rate. According to the measurement results, the third harmonic distortions without and with calibration are −57.23 dB and −74.15 dB, respectively. The SNDR can be improved from 55.07 dB to 61.35 dB. Figure 18 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) measurement results for this work. The INL is improved from +8.3/−7.2 least significant bit (LSB) to +4/−2.9 LSB. This calibration method enhances INL but not DNL because this method is only adopted using the RDFT processor to evaluate the real radixes, and thus the DNL has no significant change. The calibration procedure is also tested with different testing chips (Figure 19). It is easy to observe that the performance of the ENOB can be enhanced to about 1 bit for different testing chips.

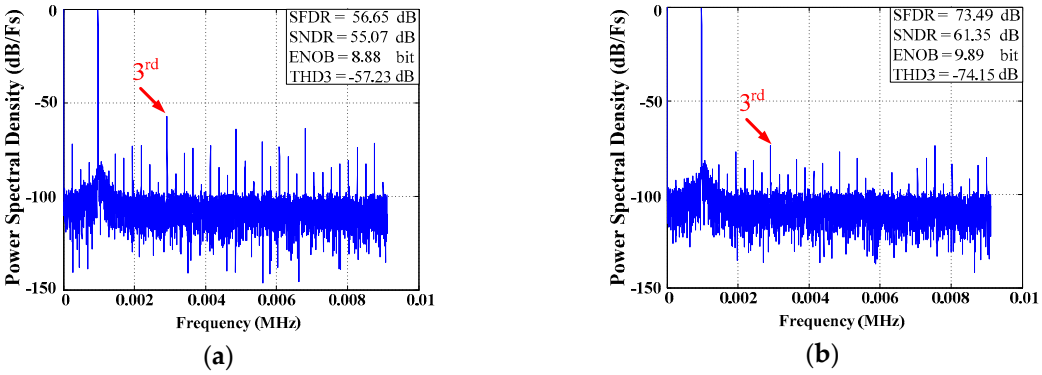

Figure 17. Measured output power spectra (**a**) without and (**b**) with calibration.

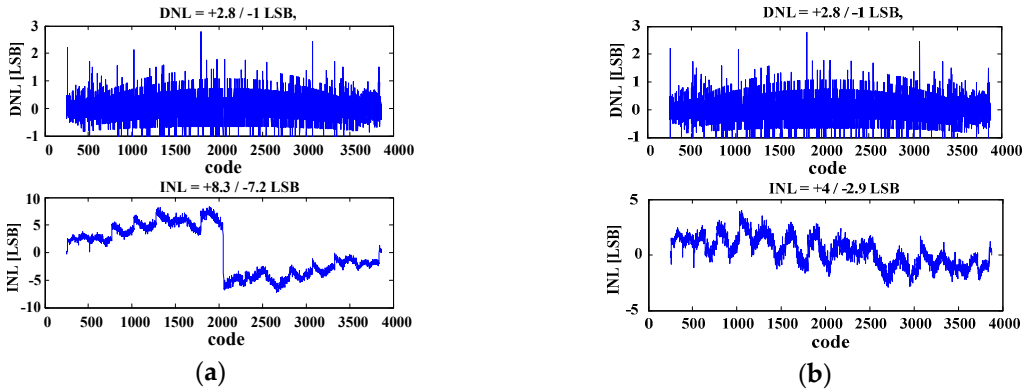

Figure 18. Measured differential nonlinearity (DNL) / integral nonlinearity (INL) (**a**) without and (**b**) with calibration.

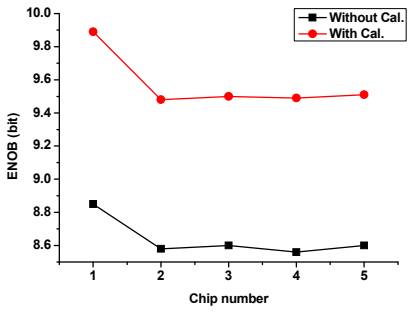

Figure 19. Measured performance of ENOB with different testing chips.

Table 1 compares the proposed method and other state-of-the-art ADCs. Although the proposed method does not have a better performance than that in Reference [12], it still exhibits better power consumption and area improvement. In addition, the performance of the split-capacitive digital-to-analog converter (CDAC) method with 0.9 bit improvement is not as good as that of our proposed method.

Table 1. Comparison of Analog-to-Digital Converters (ADCs) with different calibration methods.

	JSSCC'12 [13]	TCASI,13 [14]	TVLSI,15 [12]	This work
Technology	0.18 μm	0.13 μm	0.6 μm	0.18 μm
Method	Dither	Split-CDAC	CDAC	RDFT
Supply voltage	3.3 V (analog) 1.8 V (digital)	0.5 V	15 V	3.3 V (digital) 1.8 V (analog)
Resolution	10 bit	11 bit	14 bit	12 bit
Sampling rate	768 kS/s	10 kS/s	400 kS/s	18.75 kS/s
SNDR (dB) (Wo/Wi)	49.7/60.9	56.5/61.6	61.2/73.3	55.0/61.35
ENOB (bit) (Wo/Wi)	7.96/9.83	9.09/9.93	9.88/11.9	8.88/9.89
Power (analog)	58 μW	0.56 μW	90 mW	41.5 μW
Area	10.6 mm^2	0.58 mm^2	9.76 mm^2 (only ADC)	2.38 mm^2

4. Conclusion and Discussion

In this paper, a self-testing platform with a digital calibration method for SAR ADC is presented to overcome the non-linearity error of the T/H circuit, the capacitor mismatch of the DAC capacitor array, and the DC offset of the comparator. The proposed platform has the advantages of low cost and high integration without requiring extra analogue circuits or a complex digital calibration algorithm. The testing chip is implemented in the 0.18 μm standard CMOS process. The background signal is analyzed by the MATLAB tool to demonstrate the calibration algorithm and measured performance. According to the measurement results, the ENOB can be improved by 1 bit.

Acknowledgments: The authors would like to thank the Chip Implementation Center of Taiwan and the Ministry of Science and Technology (MOST) of Taiwan under Grants MOST 104-2218-E-006-022 for their support in this study, as well as the CBIC Lab, APSIC Lab, and Hui-Wen Chang in the CWMI Lab.

Author Contributions: Yi-Hsiang Juan, Hong-Yi Huang, Shuenn-Yuh Lee and Ching-Hsing Luo conceived and designed the analog circuit, the proposed calibration method, and the experiments. Shin-Chi Lai and Wen-Ho Juang provided the digital circuit design and analyzed the data. Yi-Hsing Juan and Shuenn-Yun Lee wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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